High Performance Regulators for PCs

2ch Switching Regulator for Desktop PC

BD9536FV

No.10030EAT35

●Description

BD9536FV is a 2ch switching regulator controller that can generate low output voltages (0.7V to 5.5V) from a wide input voltage range (7.5V to 15V). High efficiency for the switching regulator can be achieved due to its internal N-MOSFET power transistor. The IC also incorporates a new technology called H^3Reg^{TM}, a Rohm proprietary control method which facilitates ultra-high transient response against changes in load. For protection and ease of use, the IC also incorporates soft start, variable frequency, and short circuit protection with timer latch functions. This switching regulator is specially designed for DRAM and power supplies for graphics chips.

●Features

1) 2ch H^3Reg^{TM} DC/DC converter controller
2) Thermal Shut down (TSD), Under-Voltage Lock-Out (UVLO),
   Adjustable Over Current Protection (OCP): detected FET Ron,
   Over Voltage Protection (OVP), Short Circuit Protection (SCP) built-in
3) Soft start function to minimize rush current during startup
4) Adjustable switching frequency (f = 200 kHz – 600 kHz)
5) SSOP-B28 Package
6) Built-in 5V power supply for FET driver
7) Integrated bootstrap diode

●Applications

LCD, Game Consoles, Desktop PCs

●Maximum Absolute Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input Voltage	VIN	16 *1	V
BOOT Voltage	BOOT1/2	23 *1	V
BOOT-SW Voltage	BOOT1-SW1, BOOT2-SW2	7 *1	V
HG-SW Voltage	HG1-SW1, HG2-SW2	7 *1	V
LG Voltage	LG1/2	5VReg	V
Output Voltage	V_{OUT}1/2	7 *1	V
Output Feedback Voltage	FB1/2	5VReg	V
FS Voltage	FS1/2	5VReg	V
5VReg Voltage	5VReg	7 *1	V
Current Limit Setting Voltage	ILIM1/2	5VReg	V
Logic Input Voltage	EN1/2, CTL1/2	7 *1	V
Power dissipation 1	Pd1	0.8 *2	W
Power dissipation 2	Pd2	1.06 *3	W
Operating Temperature Range	Topr	-20～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Reduced by 6.4mW for each increase in Ta of 1℃ over 25℃ (when not mounted on a heat radiation board)
*3 Reduced by 8.5mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB.)

●Operating Conditions (Ta=25℃)

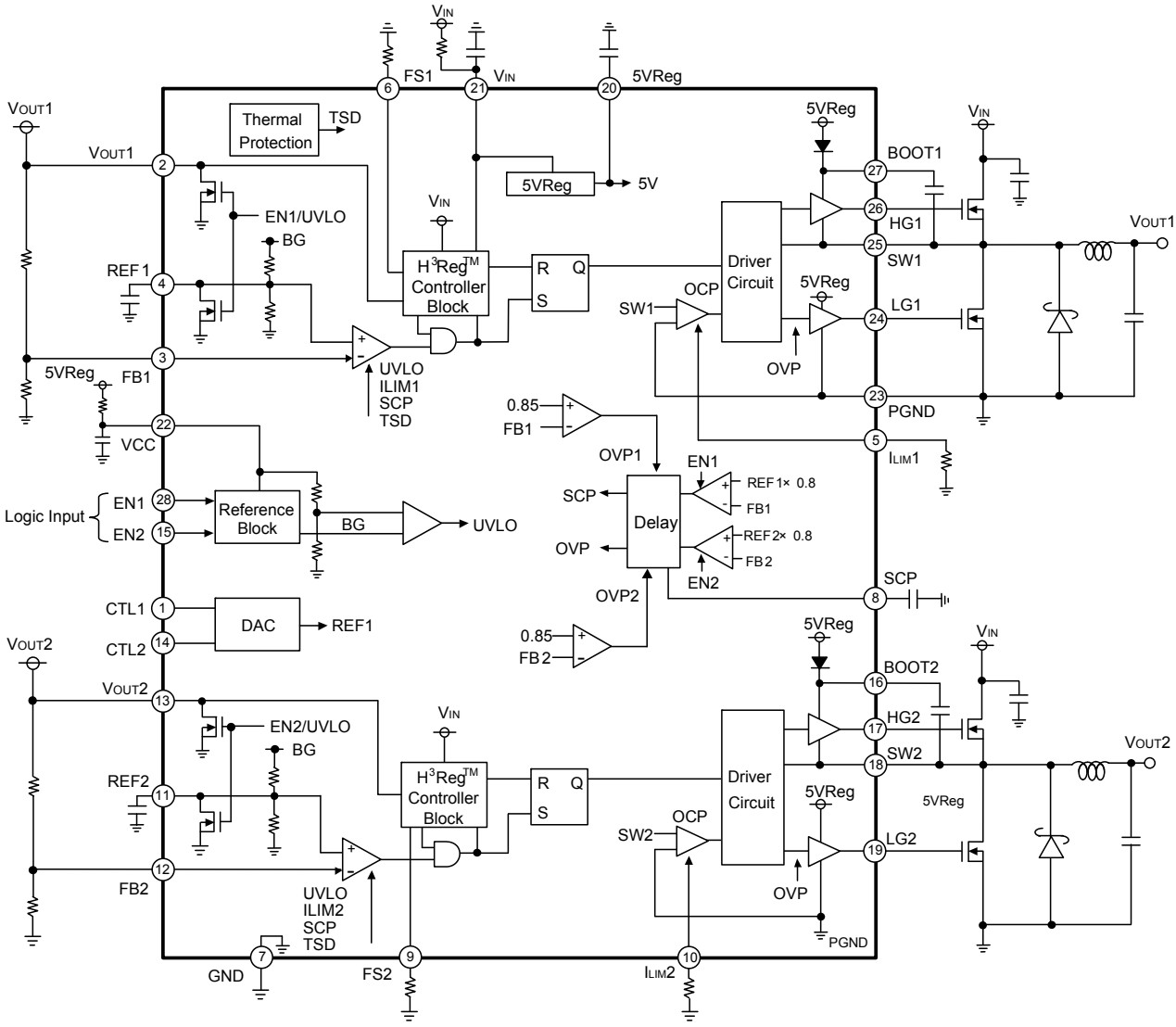
Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Input voltage	VIN	7.5	15	V
BOOT voltage	BOOT1/2	4.5	20	V
SW Voltage	SW1/2	-0.7	15	V
BOOT-SW voltage	BOOT1-SW1, BOOT2-SW2	4.5	5.5	V
Logic Input Voltage	EN1/2, CTL1/2	0	5.5	V
Output Voltage	V_{OUT}1/2	0.7	5.5	V
MIN ON Time	tonmin	-	100	ns

★ This product should not be used in a radioactive environment.

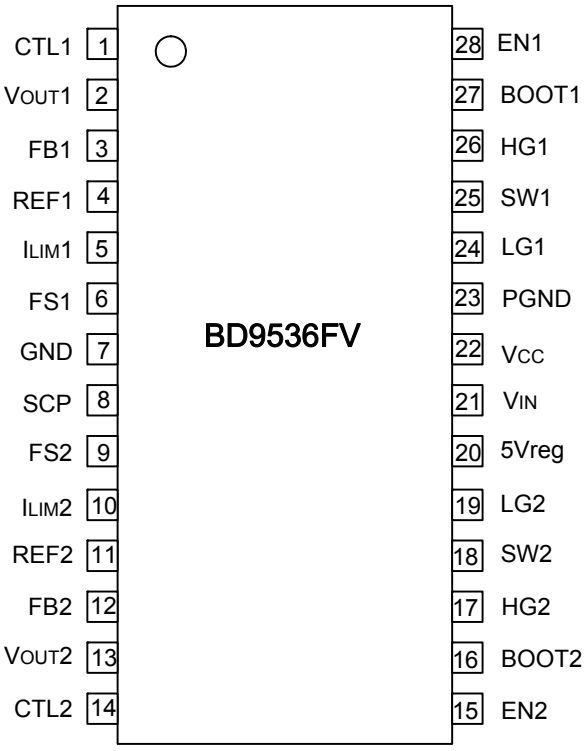
●**Electrical Characteristics** (Unless otherwise noted, Ta=25℃, V_{CC}=5V, V_{IN}=12V, V_{EN1}=V_{EN2}=3V, V_{OUT1}=V_{OUT2}=1.8V, R_{FS}=75kΩ)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
[General]						
VIN Bias Current	I_{IN}	-	1.6	2.5	mA	
VIN Standby Current	I_{IN}_stb	-	0	10	μA	V_{EN1}=V_{EN2}=0V
EN Low Voltage 1,2	V_{EN}_low$_{1,2}$	GND	-	0.3	V	
EN High Voltage 1,2	V_{EN}_high$_{1,2}$	2.2	-	5.5	V	
EN Bias Current 1,2	$I_{EN1,2}$	-	14	20	μA	
[5V Linear Regulator]						
5VReg Standby Voltage	5Vreg_stb	-	-	0.1	V	V_{EN1}=V_{EN2}=0V
5VReg Output Voltage	5VReg	4.8	5.0	5.2	V	V_{IN}=7.5V to 15V Ireg=0mA to 10mA
Maximum Current	IReg	50	-	-	mA	
[Under-Voltage Lock-Out]						
5VReg Threshold Voltage	5VReg$_{UVLO}$	3.75	4.20	4.65	V	5VReg:Sweep up
5VReg Hysteresis Voltage	d5VReg$_{UVLO}$	100	160	220	mV	5VReg:Sweep down
[OVP Block]						
FB Threshold Voltage 1,2	FB$_{OVP1,2}$	0.75	0.85	0.95	V	
[H^3REG^{TM} Control Block]						
ON Time1	ton_1	480	600	720	ns	R_{FS1}=75kΩ
MAX ON Time 1	$Tonmax_1$	3.0	4.0	5.0	μs	
MIN OFF Time 1	$Toffmin_1$	600	900	-	ns	
ON Time 2	Ton_2	480	600	720	ns	R_{FS2}=75kΩ
MAX ON Time 2	$Tonmax_2$	3.0	4.0	5.0	μs	
MIN OFF Time 2	$Toffmin_2$	600	900	-	ns	
[FET Block]						
HG High side ON Resistance 1,2	$R_{HGhon1,2}$	-	3.0	6.0	Ω	
HG Low side ON Resistance 1,2	$R_{HGlon1,2}$	-	2.0	4.0	Ω	
LG High side ON Resistance 1,2	$R_{LGhon1,2}$	-	2.0	4.0	Ω	
LG Low side ON Resistance 1,2	$R_{LGlon1,2}$	-	0.5	1.0	Ω	
[Over Current Protection Block]						
Current Limit Threshold Voltage1_1,2	$V_{ilim11,2}$	80	100	120	mV	R_{ILIM}=100k
Reverse Current Limit Threshold Voltage 1_1,2	$V_{Rellim11,2}$	80	100	120	mV	R_{ILIM}=100k
[Output Voltage Detection Block]						
FB1 threshold Voltage 1	FB1-1	0.615	0.625	0.635	V	CTL1/2=0V or 3V
FB1 threshold Voltage 2	FB1-2	0.640	0.650	0.660	V	CTL1=0V, CTL2=3V
FB1 threshold Voltage 3	FB1-3	0.590	0.600	0.610	V	CTL1=3V, CTL2=0V
FB2 threshold Voltage	FB2	0.640	0.650	0.660	V	
CTL Low Voltage 1,2	$V_{CTL\_low1,2}$	GND	-	0.5	V	
CTL High Voltage 1,2	$V_{CTL\_high1,2}$	VCC-0.5	-	VCC	V	
FB1/2 Input Current	I_{FB}	-1	-	1	μA	
VOUT Discharge Current	I_{VOUT}	5	10	-	mA	V_{OUT}=1V, EN=0V
[SCP Block]						
Threshold Voltage 1,2	$V_{thscp1,2}$	REF1/2 × 0.70	REF1/2 × 0.80	REF1/2 × 0.90	V	
Charge Current (SCP)	I_{SCP}	1	2	3	μA	
Charge Current (OVP)	I_{OVP}	4	8	12	μA	
Delay Setting Voltage	V_{SCP}	1.05	1.2	1.35	V	

●Block Diagram



●Pin Configuration



●Pin Function

PIN No.	PIN name	PIN Function
1	CTL1	1ch Output Voltage Setting Control Pin 1 :See P13/17
2	VOUT1	Output Voltage Sence Pin 1
3	FB1	Output Voltage Feedback Pin 1
4	REF1	Reference Voltage Pin 1 / Soft Start Time Setting Pin 1 (0.625V±25mV select) :See P13/17
5	ILIM1	1ch OCP Setting Pin
6	FS1	Switching Frequency Adjustable Pin 1
7	GND	Sense GND
8	SCP	Timer Latch Delay time Setting Pin for short circuit protection
9	FS2	Switching Frequency Adjustable Pin 2
10	ILIM2	2ch OCP Setting Pin
11	REF2	Reference Voltage Pin 2 / Soft Start Time Setting Pin 2(0.65V)
12	FB2	Output Voltage Feedback Pin 2
13	VOUT2	Output Voltage Sense Pin 2
14	CTL2	1ch Output Voltage Setting Control Pin 2 :See P13/17

PIN No.	PIN name	PIN Function
15	EN2	Enable Input Pin 2 (0～0.3V:OFF, 2.2～5.5V:ON)
16	BOOT2	HG Driver Power Supply Pin 2
17	HG2	High side FET Gate Driver Pin 2
18	SW2	High side FET Source Pin 2
19	LG2	Low side FET Gate Driver Pin 2
20	5VReg	Reference Voltage Inside IC (5V Voltage / always ON)
21	VIN	Battery Voltage Sense Pin
22	VCC	Power Supply Input Pin
23	PGND	Power GND
24	LG1	Low side FET Gate Driver Pin 1
25	SW1	High side FET Source Pin 1
26	HG1	High side FET Gate Driver Pin 1
27	BOOT1	HG Driver Power Supply Pin 1
28	EN1	Enable Input Pin 1 (0～0.3V:OFF, 2.2～5.5V:ON)

●Reference Data

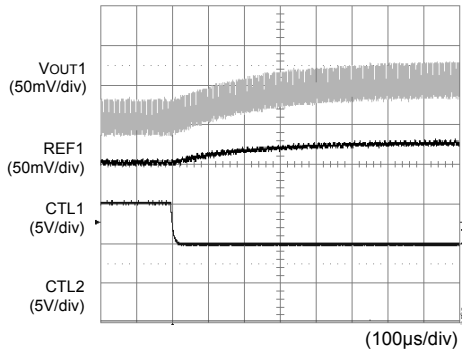


Fig.1 DAC switch1

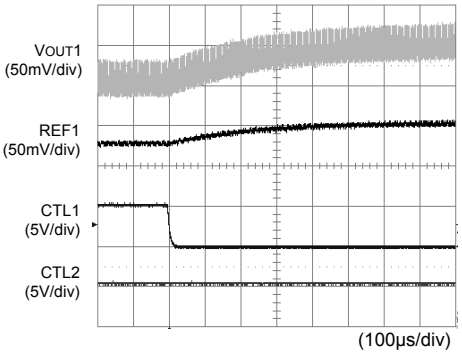


Fig.2 DAC switch 2

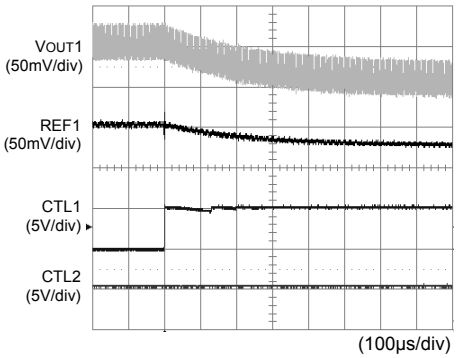


Fig.3 DAC switch 3

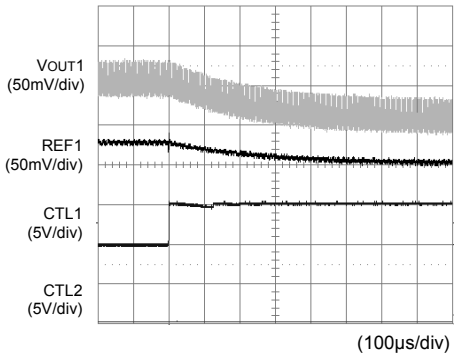


Fig.4 DAC switch 4

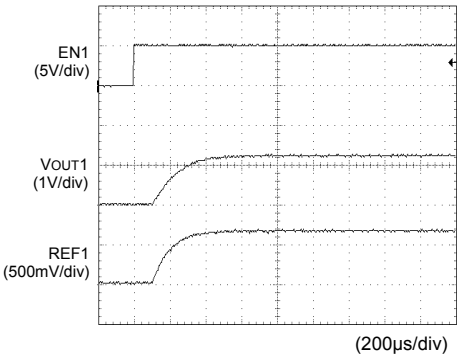


Fig.5 EN startup (REF1)

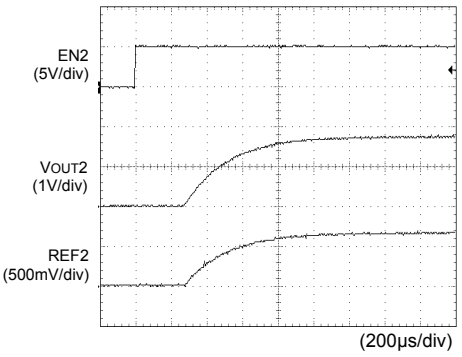


Fig.6 EN startup (REF2)

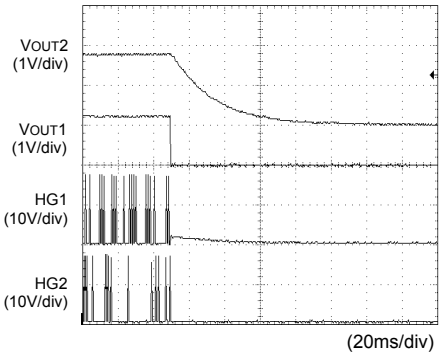


Fig.7 VOUT1 SCP function

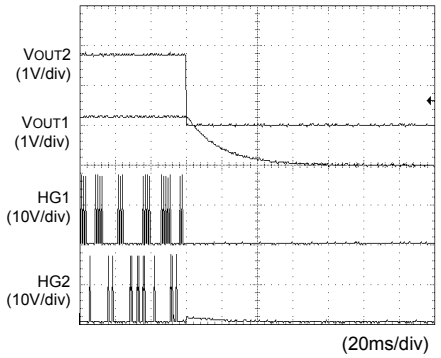


Fig.8 VOUT2 SCP function

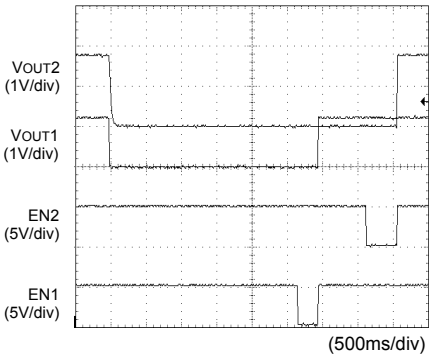


Fig.9 VOUT1 VOUT2 SCP function

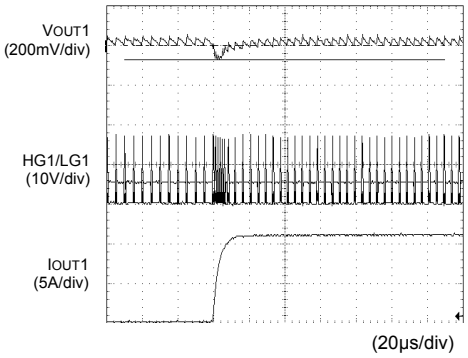


Fig.10 VOUT1transient response

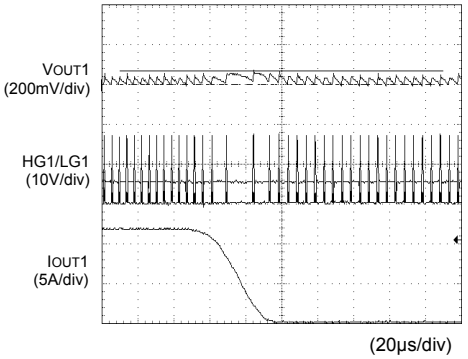


Fig.11 VOUT1 transient response

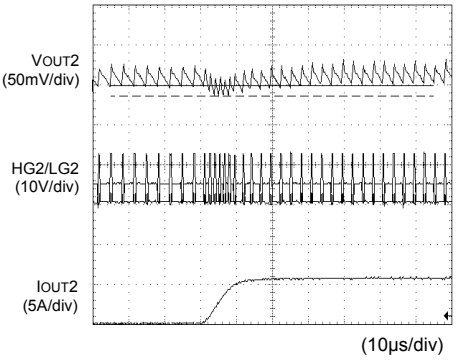


Fig.12 VOUT2 transient response

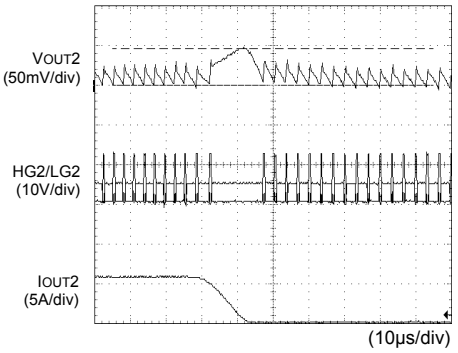


Fig.13 VOUT2 transient response

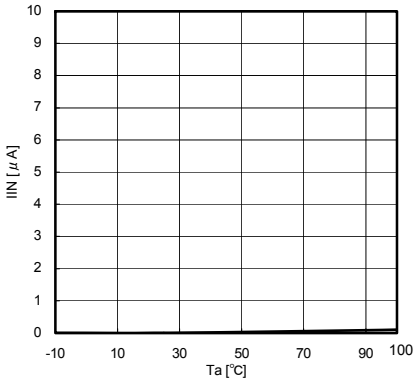


Fig.14 Ta vs IIN (standby)

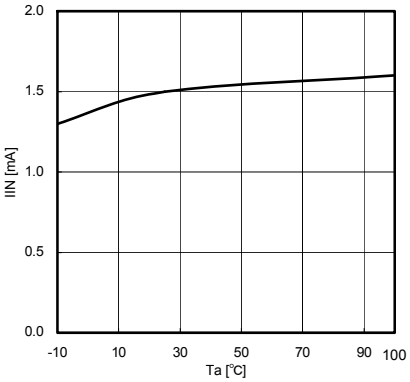


Fig.15 Ta vs IIN (active)

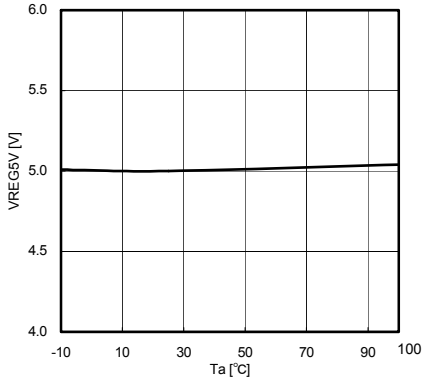


Fig.16 Ta vs VREG5V

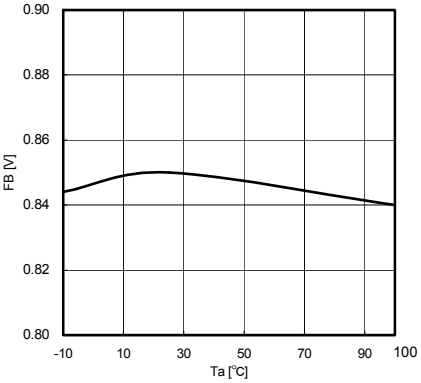


Fig.17 Ta vs OVP threshold

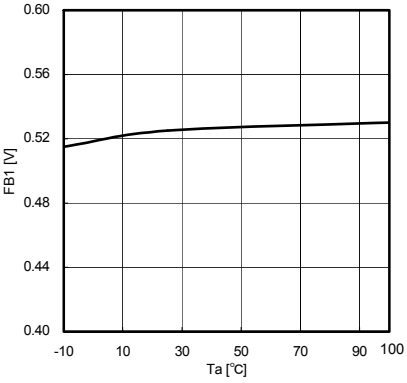


Fig.18 Ta vs SCP threshold (1ch)

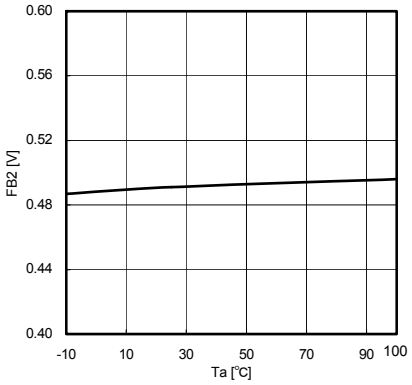


Fig.19 Ta vs SCP threshold (2ch)

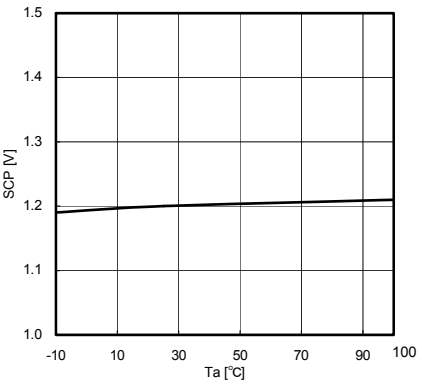


Fig.20 Ta vs delay setting voltage

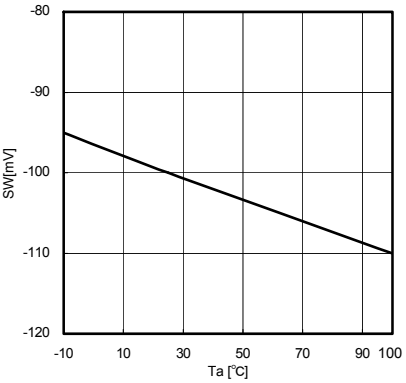


Fig.21 Ta vs OCP threshold

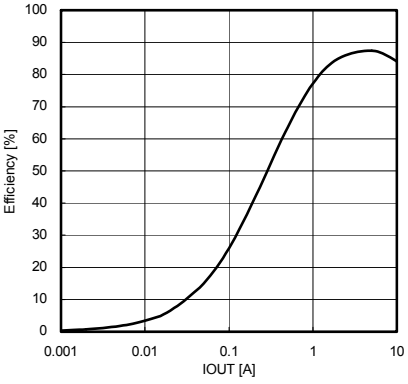


Fig.22 efficiency (1ch)

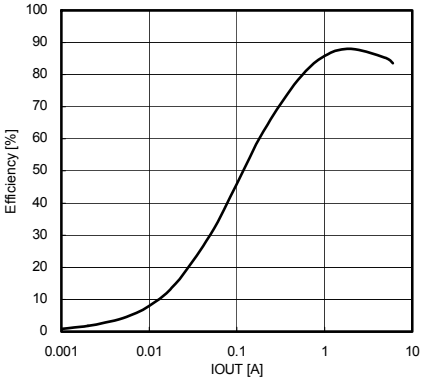


Fig.23 efficiency (2ch)

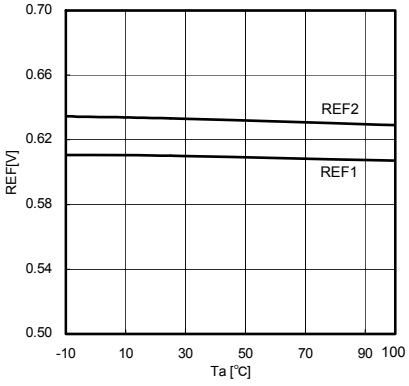
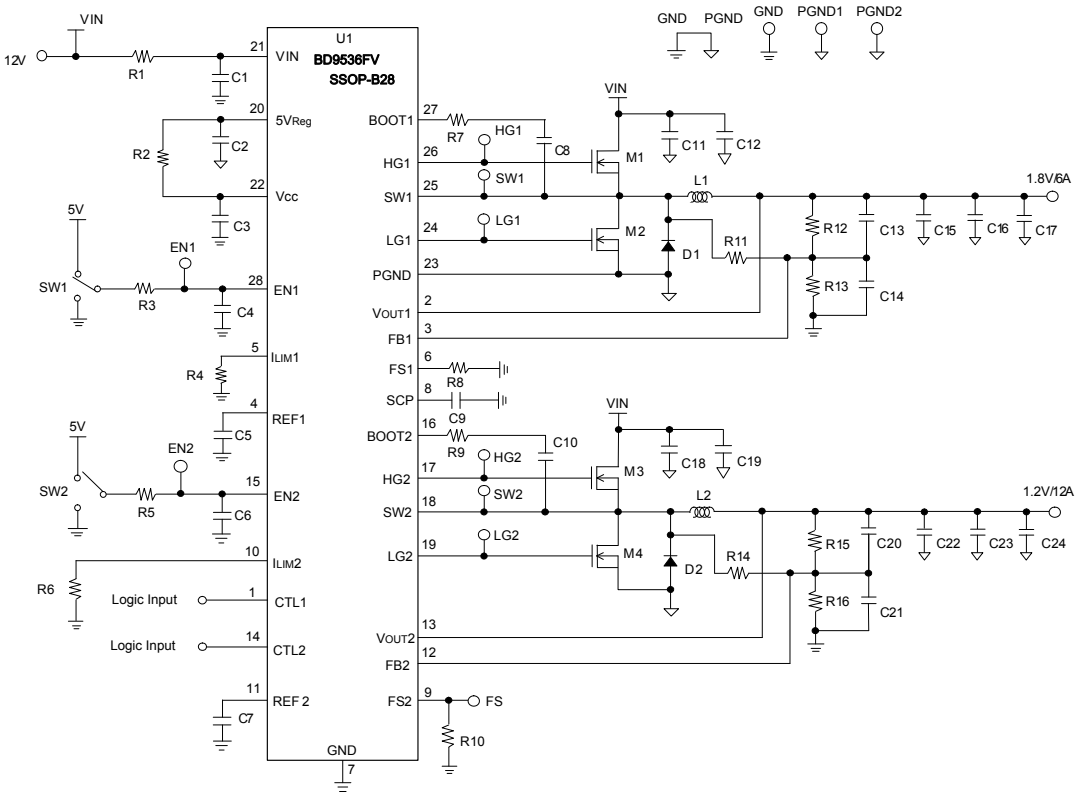


Fig.24 Ta vs REF

●Evaluation Board Circuit



●Evaluation Board Parts List

Designation	Value	Part No.	Company
R1	0Ω	MCR03 series	ROHM
R2	10Ω	MCR03 series	ROHM
R3	1kΩ	MCR03 series	ROHM
R4	100kΩ	MCR03 series	ROHM
R5	1kΩ	MCR03 series	ROHM
R6	100kΩ	MCR03 series	ROHM
R7	0Ω	MCR03 series	ROHM
R8	68kΩ	MCR03 series	ROHM
R9	0Ω	MCR03 series	ROHM
R10	58kΩ	MCR03 series	ROHM
R11	-	MCR03 series	ROHM
R12	11.5kΩ	MCR03 series	ROHM
R13	6.5kΩ	MCR03 series	ROHM
R14	-	MCR03 series	ROHM
R15	6.5kΩ	MCR03 series	ROHM
R16	6.5kΩ	MCR03 series	ROHM
C1	1μF		KYOCERA
C2	10μF		KYOCERA
C3	0.1μF		KYOCERA
C4	33pF		KYOCERA
C5	0.01μF		KYOCERA
C6	33pF		KYOCERA
C7	0.01μF		KYOCERA
C8	0.1μF		KYOCERA
C9	0.01μF		KYOCERA

Designation	Value	Part No.	Company
C10	0.1μF		KYOCERA
C11	0.1μF		KYOCERA
C12	10μF		KYOCERA
C13	330pF		KYOCERA
C14	100pF		KYOCERA
C15	330μF	OS-CON	SANYO
C16	0.1μF		KYOCERA
C17	-		KYOCERA
C18	10μF		KYOCERA
C19	10μF		KYOCERA
C20	330pF		KYOCERA
C21	100pF		KYOCERA
C22	330μF	SPCAP	Panasonic
C23	0.1μF		KYOCERA
C24	-		KYOCERA
D1		RB083L-20	ROHM
D2		RB083L-20	ROHM
L1	3.9μH	B966AS	TOKO
L2	1.6μH	962BS	TOKO
M1		SH8K4 (Q1)	ROHM
M2		SH8K4 (Q2)	ROHM
M3		RSS100N03	ROHM
M4		RSS100N03	ROHM
U1	-	BD9536FV	ROHM

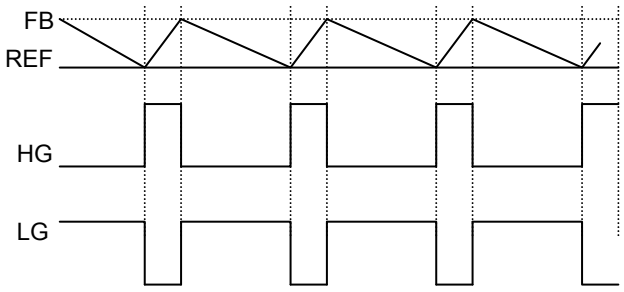
●Pin Descriptions

- EN1 (28 Pin) / EN2 (15 Pin)
  When the input voltage on the EN pin reaches at least 2.2 V, the switching regulator becomes active. At voltages less than 0.3 V, the switching regulator becomes inactive, and the input current drops to 10 μA or less. Thus the IC can be controlled from 2.5 V, 3.3 V or 5 V power supplies.
- 5VReg (20 Pin)
  5.0 V reference voltage output pin. If at least 2.2 V is supplied to either the EN1 or EN2 pin, the reference output is switched on. This pin supplies 5.0 V at up to 50 mA. Inserting a 10 μF capacitor (with a X5R or X7R rating) between the 5VReg and GND pins is recommended.
- $I_{LIM}1$ (5 Pin) / $I_{LIM}2$ (10 Pin)
  The IC monitors the voltage between the SW pin and PGND pin as a control for the output current protection (OCP) mechanism. The voltage at which OCP engages is determined by the resistance value connected to the ILIM pin. This also allows for compatibility with FETs of various R_{ON} values.
- V_{IN} (21 pin)
  The IC determines the duty cycles internally based upon the input voltage on this pin. Therefore, variations in voltage on this pin can lead to highly unstable operation. This pin also acts as the voltage input to the internal switching regulator block, and is sensitive to the impedance of the power supply. Attaching a bypass capacitor or RC filter on this pin as appropriate for the application is recommended.
- FS1 (6 Pin) / FS2 (9 Pin)
  This pin is used to adjust the switching frequency via an external resistor. The frequency range is from 200 kHz to 600 kHz.
- BOOT1 (27 pin) / BOOT2 (16 pin)
  This pin supplies voltage used for driving the high-side FET. Maximum absolute ratings are 23V from GND and 5.5V from SW. BOOT voltage swings between VIN + 5VReg and 5VReg during active operation.
- HG1 (26 pin) / HG2 (17 pin)
  This pin supplies voltage used for driving the gate of the high-side FET. This voltage swings between BOOT and SW. High-speed gate driving for the high side FET can be achieved due to its low on-resistance (3 Ω when HG = high, 2 Ω when HG = low) of the driver.
- SW1 (25 pin) / SW2 (18 pin)
  This pin acts as the source connection to the high-side FET. Maximum absolute rating is 16V from GND. SW voltage swings between VIN and GND.
- LG1 (24 pin) / LG2 (19 pin)
  This pin supplies voltage used for driving the gate of the low-side FET. This voltage swings between VDD and PGND. High-speed gate driving for the low-side FET can be achieved due to its low on-resistance (2 Ω when LG = high, 0.5 Ω when LG = low) of the driver.
- PGND (23 pin)
  This pin acts as the ground connection to the source of the low-side FET.
- GND (7 pin)
  This is the ground pin for all internal analog and digital power supplies.
- SCP (8 pin)
  This pin allows for adjustment of the latch timer used for short circuit protection. When voltage on this pin drops lower than 80% of REF, the output will switch off and remain latched after the specified time interval. When the UVLO circuit becomes active, or when EN is pulled low, the timer-latching function is disabled.
- $V_{OUT}1$ (2 pin) / $V_{OUT}2$ (13 pin)
  This is the output voltage sense pin; this pin features an integrated discharge FET used to discharge the output capacitor when status is set to OFF.
- FB1 (3 pin) / FB2 (12 pin)
  This is the output feedback pin. While channel 2 internal reference voltages is fixed at 0.650V, channel 1 internal reference voltage is adjustable depending on the input conditions of the CTL1 and CTL2 pins.
- REF1 (4 pin) / REF2 (11 pin)
  This is the reference/adjustment pin for soft start time. Output rise time is determined by the RC time constant of the IC's internal resistance (50kΩ typ.) and an external capacitor.
- Vcc (22 pin)
  This is the power supply pin for all internal circuitry. This pin can be supplied directly by a 5V source, or via an RC filter (10 Ω, 0.01 μF) from the 5VReg pin.
- CTL1 (1 pin) / CTL2 (14 pin)
  These pins allow for the adjustment of the internal voltage reference (REF1) for channel 1. The pins recognize a logic HI at VCC-0.5 V or above and logic LO at 0.5 V or below. Refer to the voltage adjustment table for REF1 on page 13.

●Explanation of Operation

The BD9536FV is a 2ch switching regulator controller incorporating ROHM's proprietary H^3Reg CONTROLLA control system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the TON time interval.

H^3Reg^{TM} control
(Normal operation)

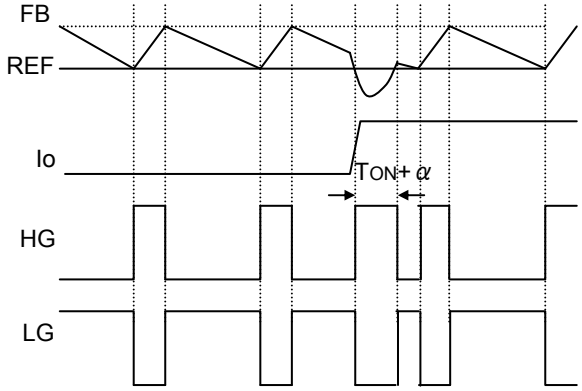


When FB falls below the threshold voltage (REF), a drop is detected, activating the H^3REG CONTROLLA system.

$$t_{ON} = \frac{REF}{VIN} \times \frac{1}{f} \text{ [sec]} \cdot \cdot \cdot (1)$$

HG output is determined by the formula above.

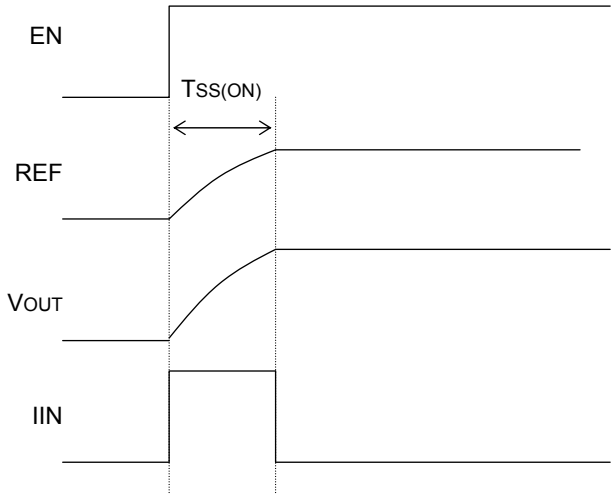
(VOUT drops due to a rapid load change)



When FB (V_{OUT}) drops due to a rapid load change, and the voltage remains below REF after the programmed t_{ON} time interval has elapsed, the system quickly restores V_{OUT} by extending the t_{ON} time, improving transient response.

●Timing Chart

・Soft Start Function



Soft start is utilized when the EN pin is set high. Current control takes effect at startup, enabling a moderate "ramping start" on the output voltage. Soft start timing and input current are determined via formula (2) and (3) below.

Soft start time:

$$T_{SS(ON)} = 50k\Omega \times Css \text{ [sec]} \cdot \cdot \cdot (2)$$

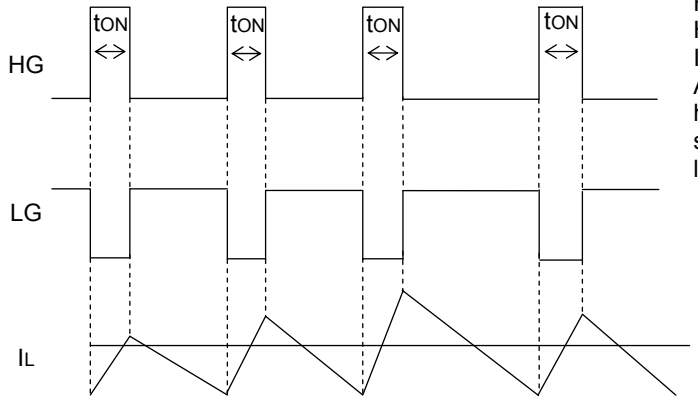
Rush current:

$$IIN = \frac{Co \times VOUT}{Tss} \text{ [A]} \cdot \cdot \cdot (3)$$

(Css: Soft start capacitor; Co: Output capacitor)

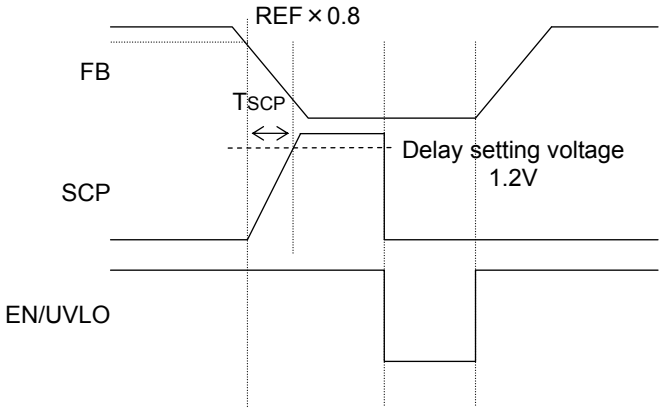
●Timing Chart

・Over current protection circuit



During normal operation, when VOUT falls below REF, HG switches high during for the period of time t_{ON} (P8). However, if the current through the inductor exceeds the I_{LIMIT} threshold, HG will switch off.
After the MAX ON TIME period elapses, HG switches high again if the output voltage is lower than the specified voltage level, and if I_L is lower than the I_{LIMIT} level.

・Timer Latch Type Short Circuit Protection

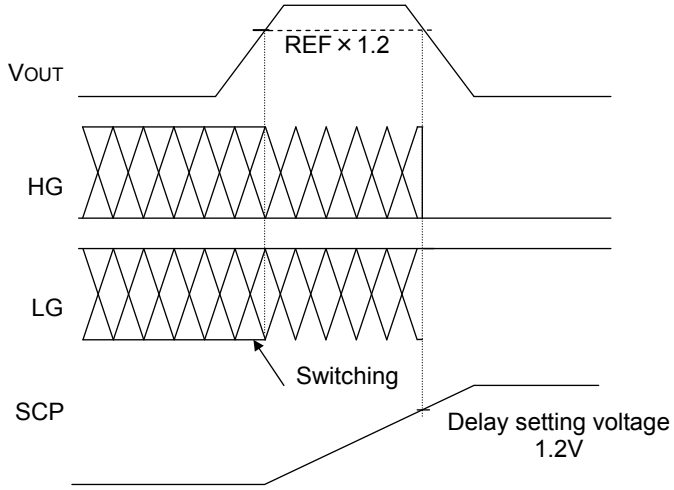


Short protection engages when output falls to or below REF x 0.8. When the programmed time period elapses, output is latched off to prevent damage to the IC. Output voltage can be restored either by reconnecting the EN pin or disabling UVLO. Short circuit protection time is determined via formula (4) below.

Short protection time setting

$$Tscp = \frac{1.2(V) \times C_{SCP}}{2\ \mu A(typ)} \quad [sec] \quad \cdots (4)$$

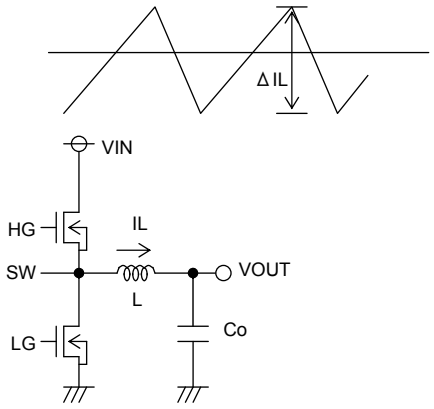
・Output Over Voltage Protection



When output voltage rises to or above REF x 1.2, output over-voltage protection engages after the set time $T_{SCP}/8$ has elapsed. During this protection period, the low-side FET opens completely for maximum reduction of output voltage (LG = high, HG = low). Output voltage can be restored either by reconnecting the EN pin or disabling UVLO.

●External Component Selection

1. Inductor (L) selection



Output Ripple Current

The inductance value has a major influence on output ripple current. As formula (5) below indicates, the greater the inductance or switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \text{ [A]} \cdot \cdot \cdot (5)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}\text{max. [A]} \cdot \cdot \cdot (6)$$

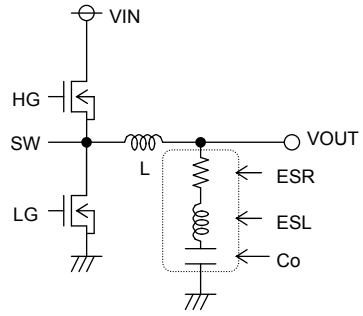
$$L = \frac{(VIN-VOUT) \times VOUT}{\Delta I_L \times VIN \times f} \text{ [H]} \cdot \cdot \cdot (7)$$

(ΔI_L: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. When selecting an inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor's rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2. Output Capacitor (C_O) Selection



Output Capacitor

When determining a proper output capacitor, be sure to factor in the equivalent series resistance and equivalent series inductance required to set the output ripple voltage to 20mV or more. Also, make sure the capacitor's voltage rating is high enough for the set output voltage (including ripple).
Output ripple voltage is determined as in formula (8) below.

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L / T_{ON} \cdot \cdot \cdot (8)$$

(ΔI_L: Output ripple current; ESR: C_O equivalent series resistance, ESL: equivalent series inductance)

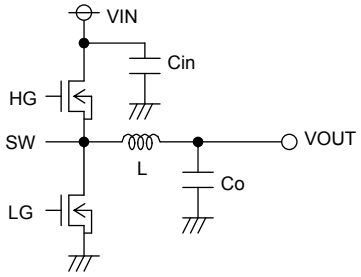
Also, give due consideration to the conditions in formula (9) below for output capacitance, bearing in mind that output rise time must be established within the soft start time frame:

$$Co \leqq \frac{TSS \times (Limit-I_{OUT})}{V_{OUT}} \cdot \cdot \cdot (9)$$

Tss: Soft start time
Limit: Over current detection
I_{OUT} : Output current

Note: an improper output capacitor may cause startup malfunctions.

3. Input Capacitor (Cin) Selection



Input Capacitor

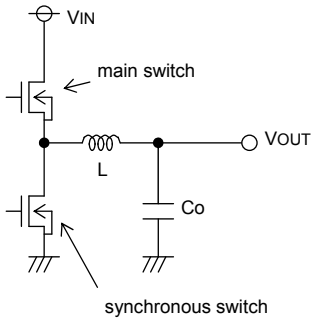
In order to prevent transient spikes in voltage, the input capacitor selected must have a low enough ESR resistance to fully support a large ripple current on the output. The formula for ripple current IRMS is given in equation (10) below:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}} \text{ [A]} \cdot \cdot \cdot (10)$$

Where $V_{IN}=2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low-ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. MOSFET Selection



Main MOSFET power dissipation is computed as follows:

$$Pmain = P_{RON} + P_{GATE} + P_{TRAN}$$

$$= \frac{V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + Qg(Hi) \times f \times 5VReg + \frac{V_{IN}^2 \times Crss \times I_{OUT} \times f}{I_{DRIVE}} \quad \cdot\cdot\cdot (11)$$

(Ron: On-resistance of FET; Qg: FET gate capacitance;
f: Switching frequency; Crss: FET inverse transfers function;
I_{DRIVE}: Gate peak current)

Synchronous MOSFET power dissipation is computed as follows:

$$Psyn = P_{RON} + P_{GATE}$$

$$= \frac{V_{IN}-V_{OUT}}{V_{IN}} \times R_{ON} \times I_{OUT}^2 + 5VReg \times f \times V_{DD} \quad \cdot\cdot\cdot (12)$$

Qg loss is also incurred as internal power dissipation in the IC:

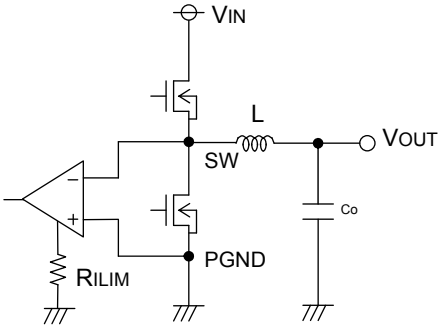
$$= P_{IC(DRIVE)} = \left\{ Qg(Hi) \times f + Qg(Low) \times f \right\} \times (VIN - 5VReg) \quad \cdot\cdot\cdot (13)$$

For example:
If Qg(Hi) = 20nq, Qg(Low) = 50nq, f = 300kHz,

$$P_{IC(DRIVE)} = \left\{ 20n \times 300k + 50n \times 300k \right\} \times (12-5)$$

= 0.147W

5. Determining Detection Resistance



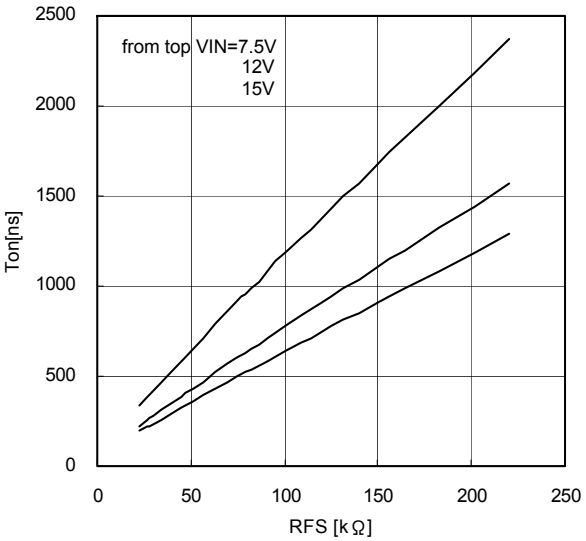
The over-current protection function is controlled via the voltage detected between the SW and PGND pins – i.e., the ON-resistance of the synchronous FET. The current limit value is determined by formula (14) below:

$$I_{LIM} = \frac{10k}{R_{ILIM} \times R_{ON}} \text{ [A]} \cdot\cdot\cdot (14)$$

(R_{ILIM}: Resistance for setting over-current protection limit,
R_{ON}: Low side FET on-resistance)

6. Setting frequency

【1,2ch】



The on-time (TON) at steady state is determined by the resistance value connected to the FS pin. However, the actual SW rise/fall time is influenced by the gate capacitance and switching speed of the external MOSFET, thereby increasing TON. The frequency is determined by the following formula after TON, input current and the REF voltage are fixed.

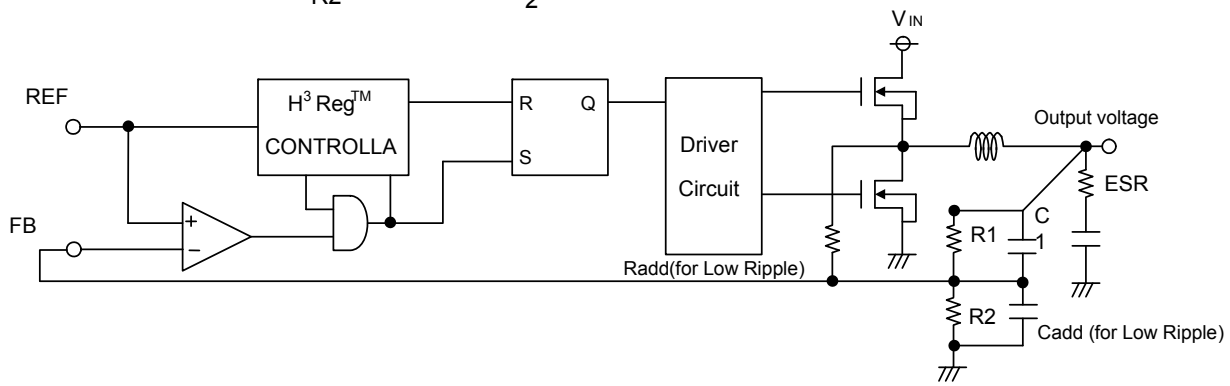
$$Freq = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad \cdot \cdot \cdot (15)$$

Consequently, the actual overall frequency becomes lower than the value obtained by the formula above.
TON is also influenced by “dead time,” which occurs when the output current approaches the 0A range in continuous mode; frequency in this output range will also be lower than the set oscillation frequency.
It is recommended to check the steady-state frequency while pulling a large current (but without saturating the output inductor).

7. Output Voltage Setting

The IC will try to maintain output voltage such that $V_{REF} \fallingdotseq V_{FB}$.
However, the actual output voltage will also reflect the average ripple voltage value.
The output voltage is set via a resistive voltage divider between the output and the FB pin. The formula for output voltage is given in (16) below:

$$\text{Output voltage} = \frac{R1+R2}{R2} \times REF + \frac{1}{2} \times \Delta I_L \times ESR \quad \cdot \cdot \cdot (16)$$



It is recommended that R1 and C1 be connected in parallel to the FB pin.
In low output ripple applications (ΔV < 20 mV), add R_{add} and C_{add} as shown in the above application circuit.
For value settings, refer to the tool provided separately.

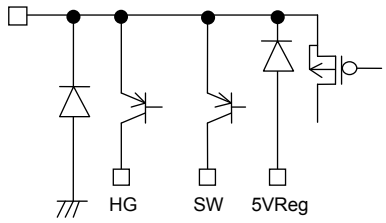
REF2 voltage is fixed at 0.65 V; however, REF1 voltage can be adjusted via the CTL1 and CTL2 pins.

REF1 voltage setting table

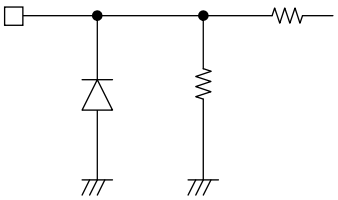
CTL1	CTL2	REF1
L	L	0.625V
H	L	0.600V
L	H	0.650V
H	H	0.625V

●I/O Equivalent Circuits

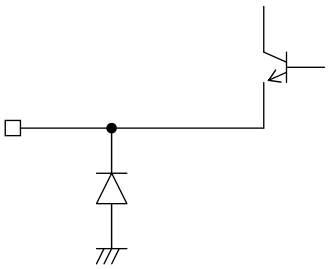
16pin, 27pin (BOOT1/2)



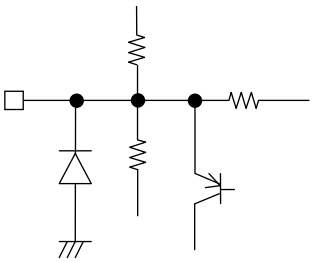
15pin, 28pin (EN1/2)



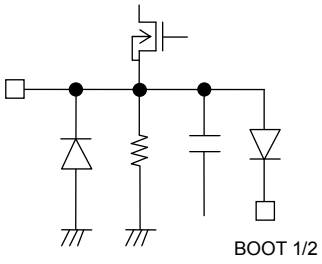
6pin, 9pin (FS1/2)



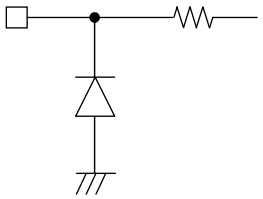
4pin, 11pin (REF 1/2)



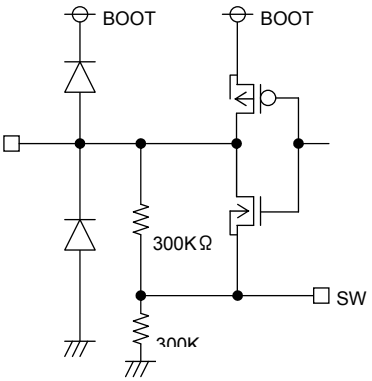
20pin (5VReg)



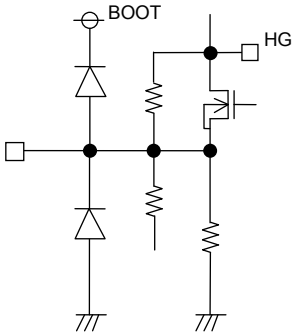
1pin 14pin(CTL 1/2)



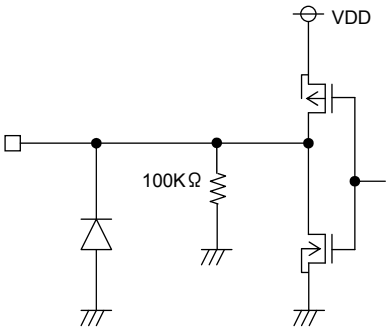
26pin, 17pin (HG1/2)



25pin, 18pin (SW1/2)



24pin, 19pin (LG1/2)



●Operation Notes

1) Absolute Maximum Ratings
Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2) Power Supply Polarity
Connecting the power supply in reverse polarity can cause damage to the IC. Take precautions when connecting the power supply lines. An external power diode can be added.

3) Power Supply Lines
In order to minimize noise, PCB layout should be designed such that separate, low-impedance power lines are routed to the digital and analog blocks. Additionally, a coupling capacitor should be inserted between all power input pins and the ground terminal. If electrolytic capacitors are used, keep in mind that their capacitance characteristics are reduced at low temperatures.

4) GND voltage
The potential of the GND pin must be the minimum potential in the system in all operating conditions.

5) Thermal design
Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

6) Inter-pin Shorts and Mounting Errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

7) Operation in Strong Electromagnetic Fields
Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

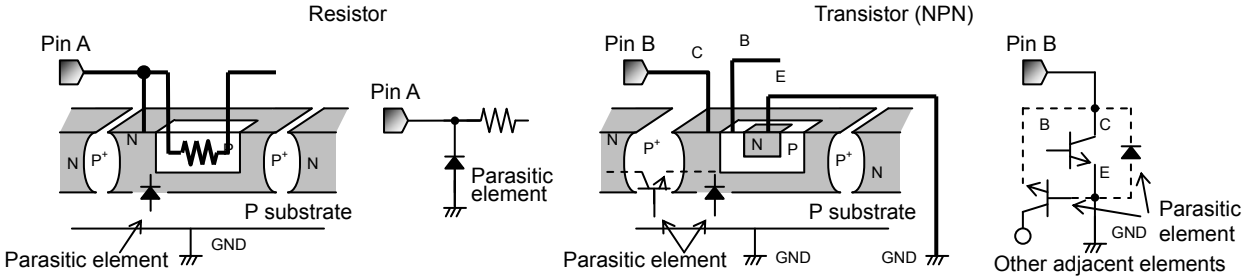
8) ASO - Area of Safe Operation
When using the IC, ensure that operating conditions do not exceed absolute maximum ratings or ASO of the output transistors.

9) Thermal shutdown (TSD) circuit
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

	TSD ON Temp. [°C] (typ.)	Hysteresis Temp. [°C] (typ.)
BD9536FV	175	15

10) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

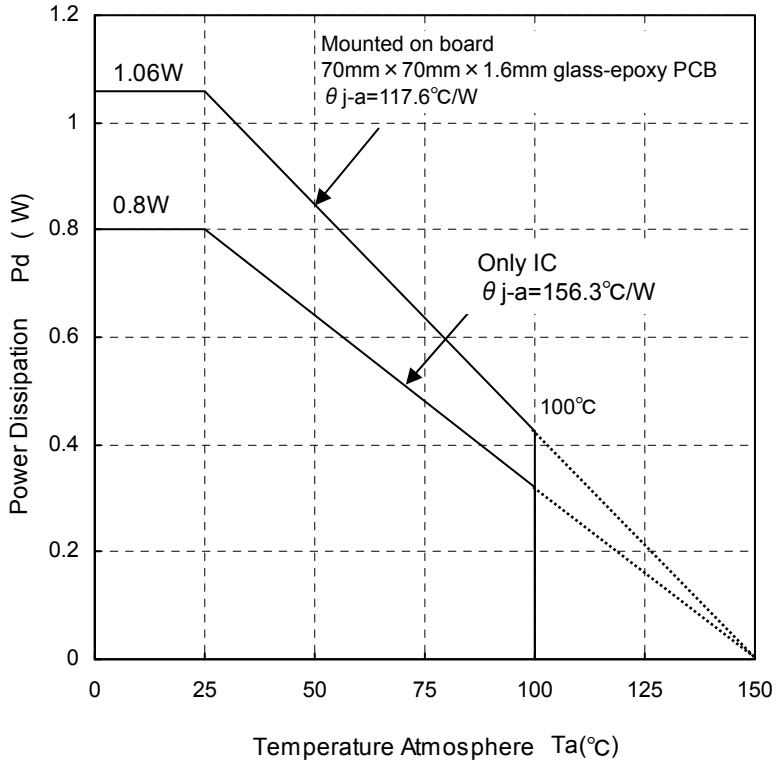
11) Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):
・When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
・When GND > Pin B, the PN junction operates as a parasitic transistor
Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of IC structure

12) Ground Wiring Pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

●Power Dissipation



●Ordering part number

B	D	9	5	3	6	F	V	-	E	2

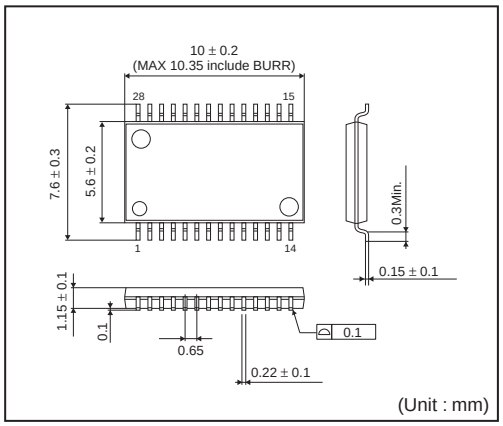
Part No. (BD)

Part No. (9536)

Package
F: SSSOP-B28

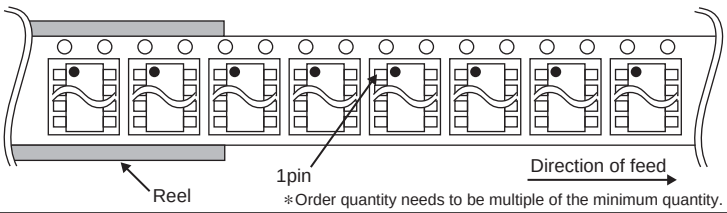
Packaging and forming specification
E2: Embossed tape and reel

SSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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