

# Field Programmable Blank Oscillator

Series **CPPFX**

- Programmed with the PG-3000 field oscillator programming instrument within seconds
- Can be programmed twice
- Provides a sealed finished custom oscillator
- Standard Package Options

**Part Numbering Example: CPPFX C 1 L Z - A5 BR - XX.XXXX TS**

CPPFX	C	1	L	Z	A7	BR	XX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CPPFX	C = CMOS T = TTL	1 = Full Size 4 = Half Size 7 = 5X7 Ceramic 8 = PLASTIC SMD	Blank = 5V L = 3.3 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A7 = -40°C +85°C	BD = ±20 ppm BR = ±25 ppm BP = ±50 ppm	1.000~133.000 MHz	TS = Tri-State PD=PowerDwn

## Specifications:

	Min	Typ	Max	Unit
<b>Frequency Range:</b> Programmable to Any Discrete Frequency	1.000		133.000	MHz
<b>Available Stability Options:</b>	-20 -25		20 25	ppm ppm
<b>Programmable Input Voltage:</b> (1–133 MHz)	+4.5	5.0	5.5	VDC
(1–133 MHz)	+3.0	3.3	3.6	VDC
<b>Operating Temperature Range Options:</b>	0 -40		+70 +85	°C °C
<b>Storage Temperature:</b>	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=5/3.3V			±5	
<b>Programmable Output Level:</b>	TTL/CMOS			
<b>Packaging:</b>	Tape and Reel (1K per Reel) Tube			

## Operating Conditions:

	Description	Min	Max	Unit
V <sub>DD</sub>	Digital Supply Voltage	3.0	5.5	V
C <sub>TTL</sub>	Max Capacitive Load on outputs for TTL levels 4.5V–5.5V V <sub>DD</sub> ≤ 40 MHz 4.5V–5.5V V <sub>DD</sub> > 40–133 MHz		50 25	pF pF
C <sub>CMOS</sub>	Max Capacitive Load on outputs for CMOS levels 4.5V–5.5V V <sub>DD</sub> , ≤ 66 MHz 4.5V–5.5V V <sub>DD</sub> , >66–133 MHz 3.0V–3.6V V <sub>DD</sub> , ≤ 40 MHz 3.0V–3.6V V <sub>DD</sub> , >40–100 MHz		50 25 30 15	pF pF pF pF



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## Electrical Characteristics

	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Input Characteristics (Pin 1):</b>					
V <sub>IL</sub> , Low-Level Input Voltage TO DISABLE OUTPUT	4.5–5.5V V <sub>dd</sub> 3.0–3.6V V <sub>dd</sub>			0.8 0.2V <sub>dd</sub>	V V
V <sub>IH</sub> , High-Level Input Voltage TO ENABLE OUTPUT OR NO CONNECT	4.5–5.5V V <sub>dd</sub> 3.0–3.6V V <sub>dd</sub>	2.0 0.7V <sub>dd</sub>			V V
I <sub>IL</sub> , Input Low Current I <sub>IH</sub> , Input High Current	V <sub>IN</sub> = 0V V <sub>IN</sub> = V <sub>dd</sub>			10 5	μA μA
<b>Output Characteristics:</b>					
V <sub>OL</sub> , Low-Level Output Voltage	4.5V–5.5V V <sub>dd</sub> , 16 mA I <sub>oL</sub> 3.0V–3.6V V <sub>dd</sub> , 8 mA I <sub>oL</sub>			0.40 0.40	V V
V <sub>OHTTL</sub> , High-level Output Voltage TTL	4.5V–5.5V V <sub>dd</sub> , -16 mA I <sub>oL</sub>	2.40			V
V <sub>OHCMS</sub> , High-level CMOS Voltage	4.5V–5.5V V <sub>dd</sub> , -16 mA I <sub>oL</sub> 3.0V–3.6V V <sub>dd</sub> , -8 mA I <sub>oL</sub>	V <sub>dd</sub> -0.4 V <sub>dd</sub> -0.4			V V
<b>Power Supply Current: (unloaded)</b>	4.5–5.5 V <sub>dd</sub> , OUTPUT FREQ ≤ 133 MHz 3.0–3.6 V <sub>dd</sub> , OUTPUT FREQ ≤ 100 MHz			45 25	mA mA
<b>Standby Current:</b>			10	50	μA
<b>Input Pull-Up Resistor</b>	4.5–5.5 V <sub>dd</sub> , V <sub>IN</sub> = 0V 4.5–5.5 V <sub>dd</sub> , V <sub>IN</sub> = 0.7V	1.1 50	3.0 100	8.0 200	MΩ KΩ
<b>CLKOUT Pull-Down Current</b>	5.0 V <sub>dd</sub>		20		μA
<b>Output Enable Mode:</b>	Output is Tri-Stated				
<b>Power Down Mode:</b>	Output is Tri-Stated.				



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## Output Clock Switching Characteristics

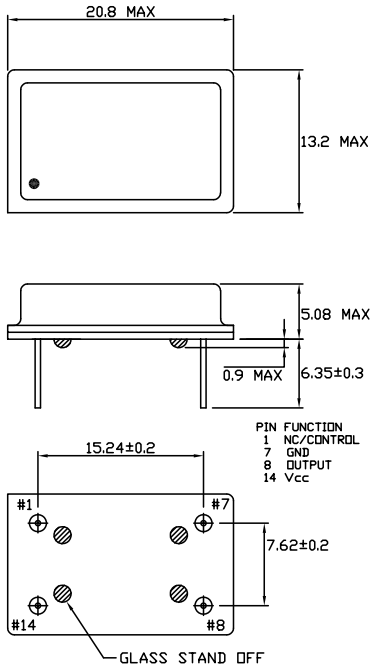
	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Duty Cycle:</b> TTL @ 1.4 V, 4.5–5.5 Vdd	≤ 50 MHz, C <sub>L</sub> = 50 pF	45		55	%
	50–66 MHz, C <sub>L</sub> = 15 pF	45		55	%
	66–125 MHz, C <sub>L</sub> = 25 pF	40		60	%
	125–133 MHz, C <sub>L</sub> = 15 pF	40		60	%
CMOS @ Vdd/2, 4.5–5.5 Vdd  3.0–3.6 Vdd	≤ 66 MHz, C <sub>L</sub> ≤ 25 pF	45		55	%
	66–125 MHz, C <sub>L</sub> ≤ 25 pF	40		60	%
	125–133 MHz, C <sub>L</sub> ≤ 15 pF	40		60	%
	≤ 40 MHz, C <sub>L</sub> ≤ 30 pF	45		55	%
	40–100 MHz, C <sub>L</sub> ≤ 15 pF	40		60	%
<b>Output Clock Rise/Fall</b>	0.8V–2.0V, 4.5-5.5 Vdd, C <sub>L</sub> = 50			1.8	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C <sub>L</sub> = 25			1.2	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C <sub>L</sub> = 15			0.9	ns
	0.2–0.8Vdd, 4.5-5.5 Vdd, C <sub>L</sub> = 50			3.4	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd, C <sub>L</sub> = 30			4.0	ns
	0.2–0.8Vdd, 3.0–3.6 Vdd, C <sub>L</sub> = 15			2.4	ns
<b>Start Up Time</b>	From power on			10	ms
<b>Power Down Delay Time</b> Synchronous Asynchronous	PWR_DWN pin LOW to output Hi-Z		T/2	T+10	ns
			10	15	ns
<b>Output Disable Time</b> Synchronous Asynchronous	OE pin LOW to output Hi-Z T = Frequency oscillator period		T/2	T+10	ns
			10	15	ns
<b>Output Enable Time</b>				100	ns
<b>Period Jitter: Σ</b>	≤ 33.000 MHz		11	13	ps
	> 33.000, MHz		11	17	ps
Peak to Peak	≤ 33.000 MHz		83	100	ps
	> 33.000 Mhz		82	110	ps



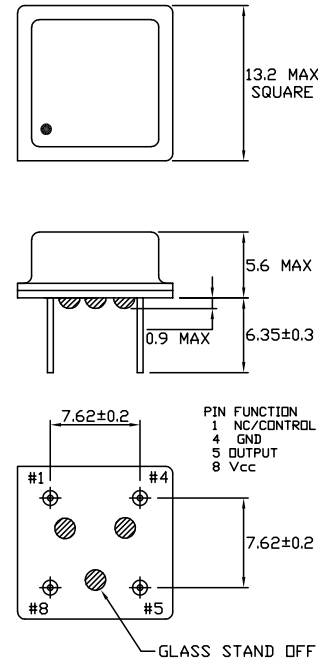
# Field Programmable Blank Oscillator Package Styles

*Note: Bypass Vdd to GND with a 0.01 μF capacitor*

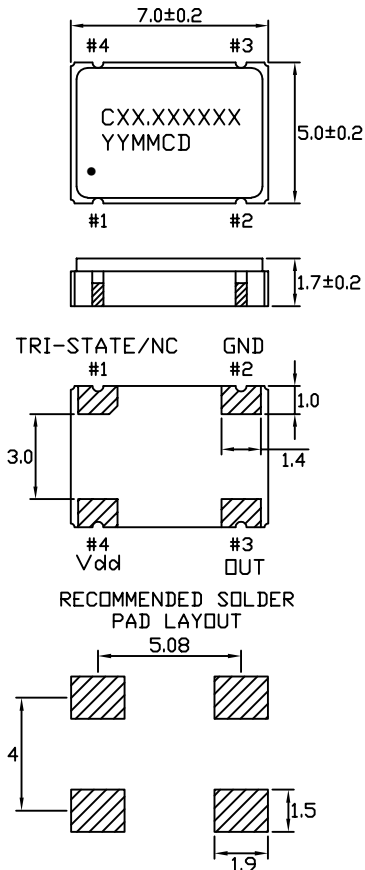
## Style 1 Full Size 14 Pin Dip



## Style 4 Half Size 8 Pin Dip



## Style 7 5x7 Ceramic SMD



## Style 8 Plastic SMD

