

# 256 Megabit Synchronous DRAM

## DPDSD16MX16TKY5

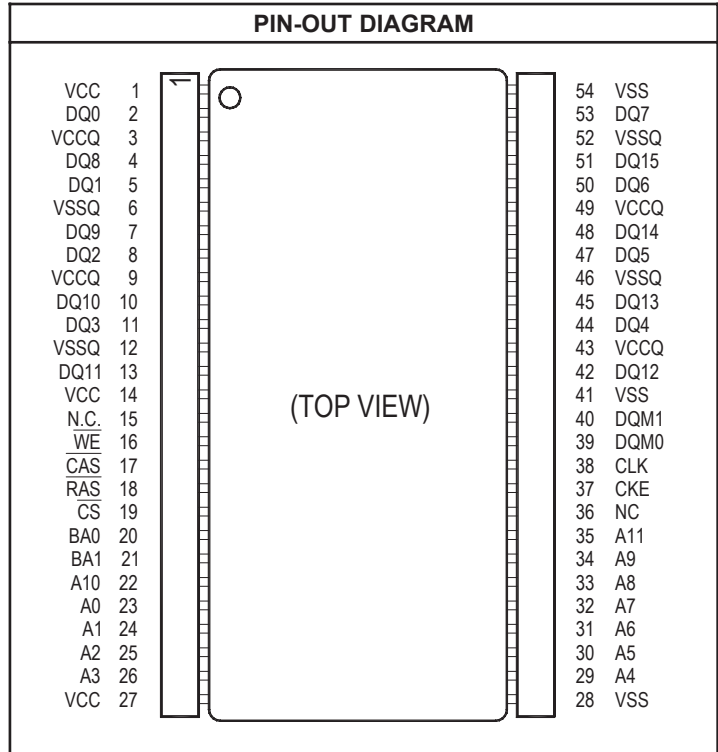
**DESCRIPTION:**

The Memory Stack™ series is a family of interchangeable memory devices. The 256 Megabit SDRAM assembly utilizes the space saving LP-Stack™ technology to increase memory density. This stack is constructed with two 128Mb (16M x 8) SDRAMs.

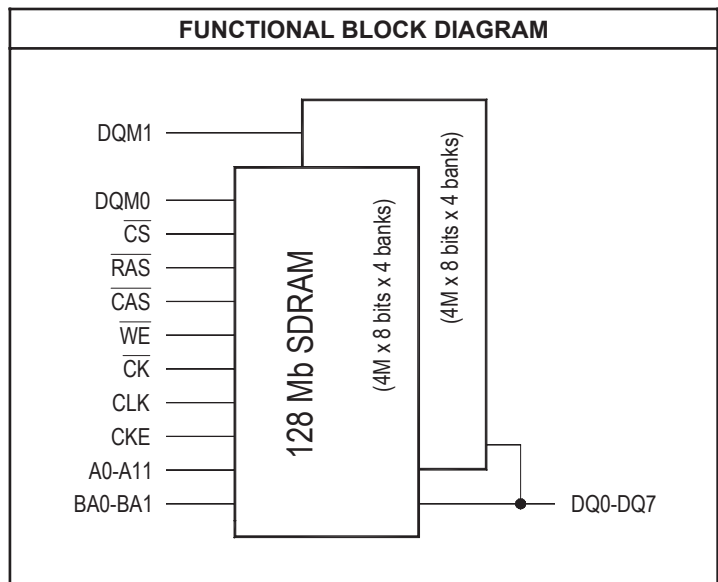
This 256Mb LP-Stack™ has been designed to fit in the same footprint as the 128Mb (16M x 8) SDRAM TSOPII monolithic. This stack allows for system upgrade without electrical or mechanical redesign, providing an alternative low cost memory solution.

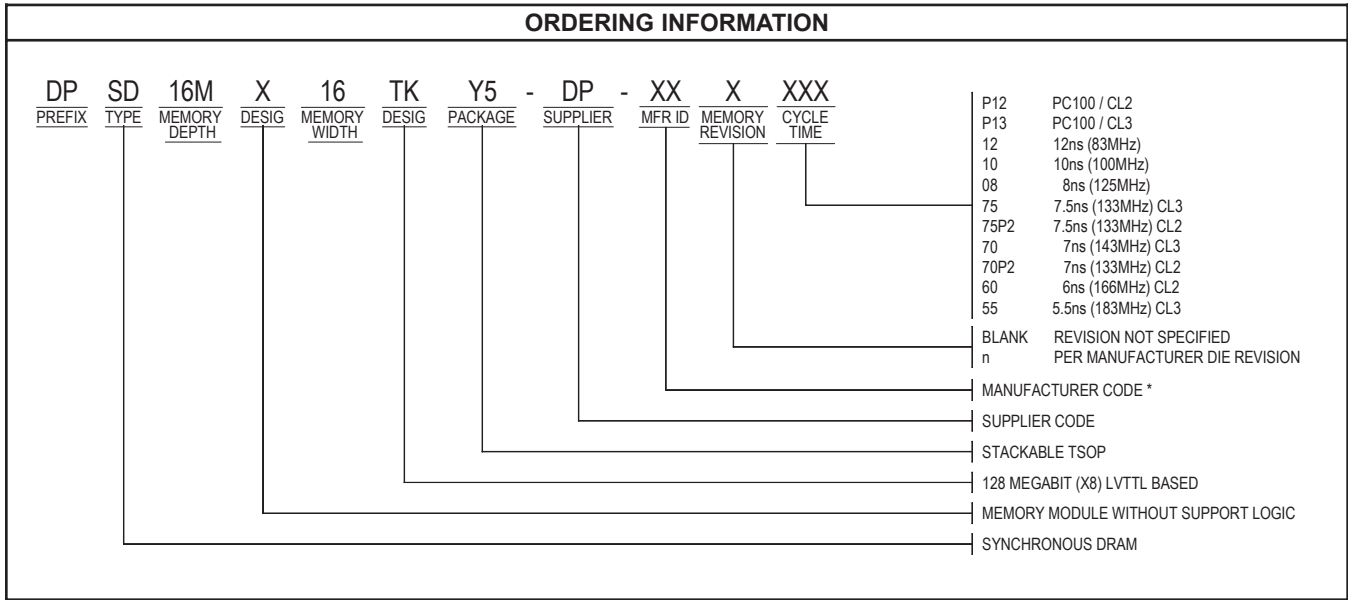
**FEATURES:**

- Electrical characteristics meet semiconductor manufacturers' datasheets
- Memory organization:  
(2) 128Mb memory devices. Each device arranged as 16M x 8 bits (4M x 8 bits x 4 banks)
- Memory stack organization:  
16M x 16 bits (4M x 16 bits x 4 banks)
- JEDEC approved TSOPII footprint / non JEDEC pin assignment  
(with 1 CS, 1 CE, 2 DQMs and DQ0-DQ15)
- Optimized for RDIMMs
- IPC-A-610, class 2, manufacturing standards
- Lead free manufacturing process
- Package: 54-Pin TSOPII stack



PIN NAMES	
A0-A11	Row Address: A0-A11 Column Address: A0-A9
BA0, BA1	Bank Select Address
DQ0-DQ15	Data In/Data Out
CAS	Column Address Strobe
RAS	Row Address Strobe
WE	Data Write Enable
DQM0, DQM1	Data Input/Output Masks
CKE	Clock Enable
CLK	System Clock
CS	Chip Select
Vcc/Vss	Power Supply/Ground
Vccq/Vssq	Data Output Power/Ground
NC	No Connect





\* Contact your sales representative for supplier and manufacturer codes.

**NOTE:**

1. AC Parameters of base memory are unchanged from device manufacturers' specifications.
2. DC Parameters may be affected by stacking. Please refer to application note 53A004-00 for further information.
3. For assembly and inspection procedures, refer to application note 53A001-00.
4. Maximum reflow temperature recommendation is 215°C.

