16-bit Proprietary Microcontroller

CMOS

F²MC-16FX MB96330 Series

MB96336/338*1
MB96F338*1

■ **DESCRIPTION**

MB96330 series is based on Fujitsu's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 48MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 20.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

*1: These devices are under development. All information in this datasheet is preliminary for the devices under development.

FUJITSU

2008-2-7

■ **FEATURES**

Feature	Description
Technology	• 0.18μm CMOS
CPU	• F2MC-16FX CPU • Up to 48 MHz internal, 20.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1..25, x1 when PLL stop) • 3-16 MHz external quartz clock • Up to 48 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
CAN	• Supports CAN protocol version 2.0 part A and B • ISO16845 certified • Bit rates up to 1 Mbit/s • 32 message objects • Each message object has its own identifier mask • Programmable FIFO mode (concatenation of message objects) • Maskable interrupt • Disabled Automatic Retransmission mode for Time Triggered CAN applications • Programmable loop-back mode for self-test operation
USART	• Full duplex USARTs (SCI/LIN) • Wide range of baud rate settings using a dedicated reload timer • Special synchronous options for adapting to different synchronous serial protocols • LIN functionality working either as master or slave LIN device
I2C	• Up to 400 kbit/s • Master and Slave functionality, 8-bit and 10-bit addressing
A/D converter	• SAR-type • 10-bit resolution • Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
Reload Timers	• 16-bit wide • Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency • Event count function
Free Running Timers	• Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
Input Capture Units	• 16-bit wide • Signals an interrupt upon external event • Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	• 16-bit wide • Signals an interrupt when a match with 16-bit I/O Timer occurs • A pair of compare registers can be used to generate an output signal.
Programmable Pulse Generator	• 16-bit down counter, cycle and duty setting registers • Interrupt at trigger, counter borrow and/or duty match • PWM operation and one-shot operation • Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input • Can be triggered by software or reload timer

Feature	Description
Real Time Clock	• Can be clocked either from sub oscillator (devices with part number suffix "W"), main oscillator or from the RC oscillator • Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) • Read/write accessible second/minute/hour registers • Can signal interrupts every half second/second/minute/hour/day • Internal clock divider and prescaler provide exact 1s clock
External Interrupts	• Edge sensitive or level sensitive • Interrupt mask and pending bit per channel • Each available CAN channel RX has an external interrupt for wake-up • Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
External bus interface	• 8-bit or 16-bit bidirectional data • Up to 24-bit addresses • 6 chip select signals • Multiplexed address/data lines • Non-multiplexed address/data lines • Wait state request • External bus master possible • Timing programmable
Alarm comparators	• Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds • Threshold voltages defined externally or generated internally • Status is readable, interrupts can be masked separately
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels (Automotive / CMOS-Schmitt trigger / TTL) • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Package	• 144-pin plastic LQFP M08

Feature	Description
Flash Memory	• Supports automatic programming, Embedded Algorithm™*1 • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase
USB	• USB function (corresponds to USB Full Speed) • USB Mini-HOST function • Supports up to 6 endpoints

*1: Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP

Features		MB96V300	MB9633xY/R / MB96F33xY/R	MB96F33xU
Product type		Evaluation sample	Flash product: MB96F33x Mask ROM product: MB9633x	
YS		NA	LVD persistently on / Single clock devices	
RS			LVD can be disabled / Single clock devices	
YW			LVD persistently on / Dual clock devices	
RW			LVD can be disabled / Dual clock devices	
US			USB / LVD can be disabled / Single clock devices	
UW			USB / LVD can be disabled / Dual clock devices	
Flash/ ROM	RAM			
288kB	16kB	ROM/Flash memory emulation by external RAM, 92kB internal RAM	MB96336Y [1], MB96336R[1]	
544kB	32kB		MB96F338Y [1], MB96F338R[1] MB96338Y [1], MB96338R[1]	MB96F338U [1]
Package		BGA416	FPT-144P-M08	
DMA		16 channels	10 channels	
USART		10 channels	8 channels	
I2C		2 channels		
A/D Converter		40 channels	40 channels	36 channels
A/D Converter Reference Voltage switch		yes	No	
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)	
16-bit Free-Running Timer		4 channels		
16-bit Output Compare		12 channels		
16-bit Input Capture		10 channels		
16-bit Programmable Pulse Generator		20 channels		
CAN Interface		5 channels	3 channels	
USB		No	No	1 channel
External Interrupts		16 channels		
Non-Maskable Interrupt		1 channel		
Real Time Clock		1		

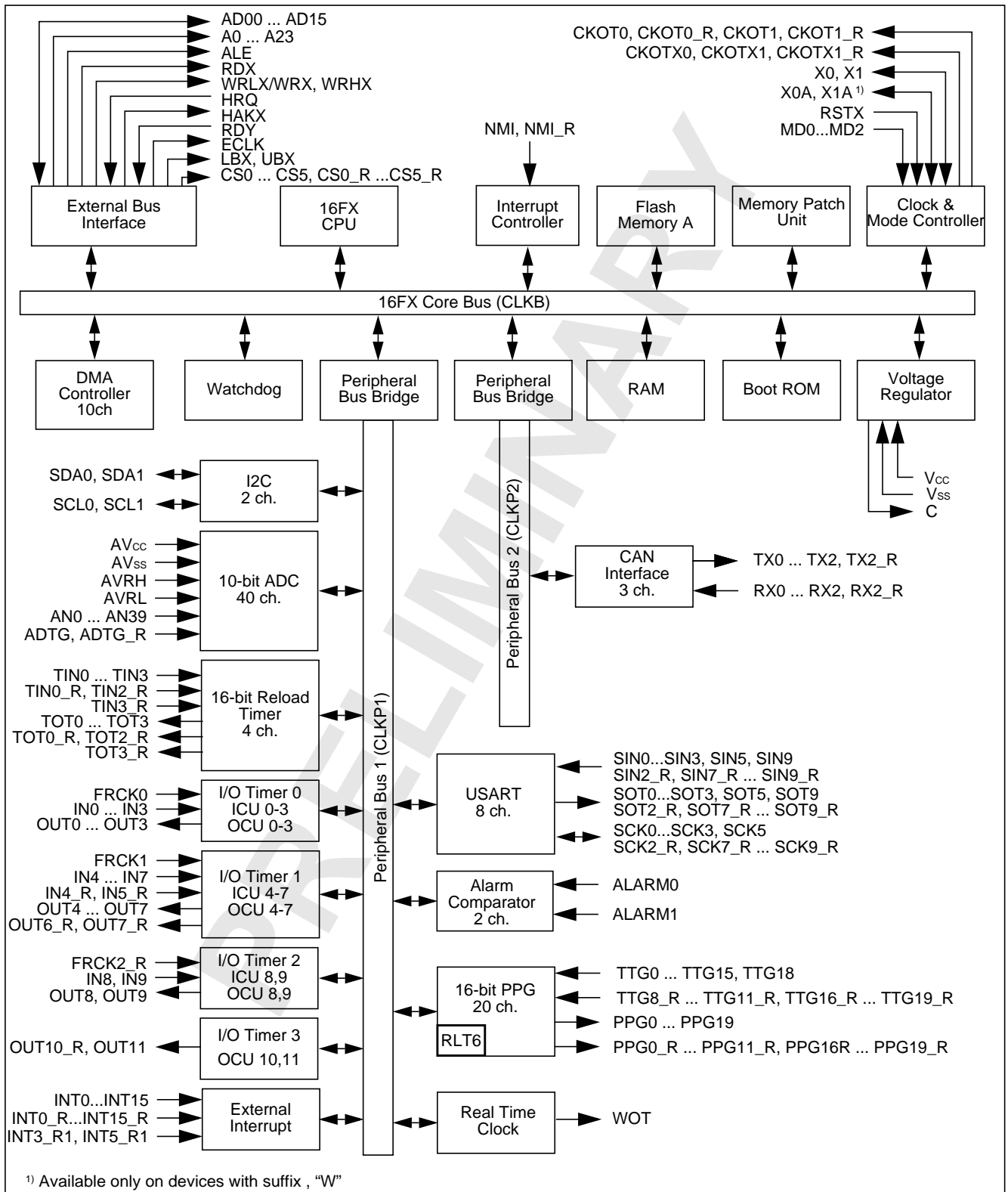| Features	MB96V300	MB9633xY/R / MB96F33xY/R	MB96F33xU
I/O Ports	136	122 for part number with suffix "W", 124 for part number with suffix "S"	118 for part number with suffix "W", 120 for part number with suffix "S"
Alarm comparator	2 channels		
External bus interface	Yes		
Chip select	6 signals		
Clock output function	2 channels		
Low voltage reset	Yes		
On-chip RC-oscillator	Yes		

*1: These devices are under development. All information in this datasheet is preliminary for the devices under development.
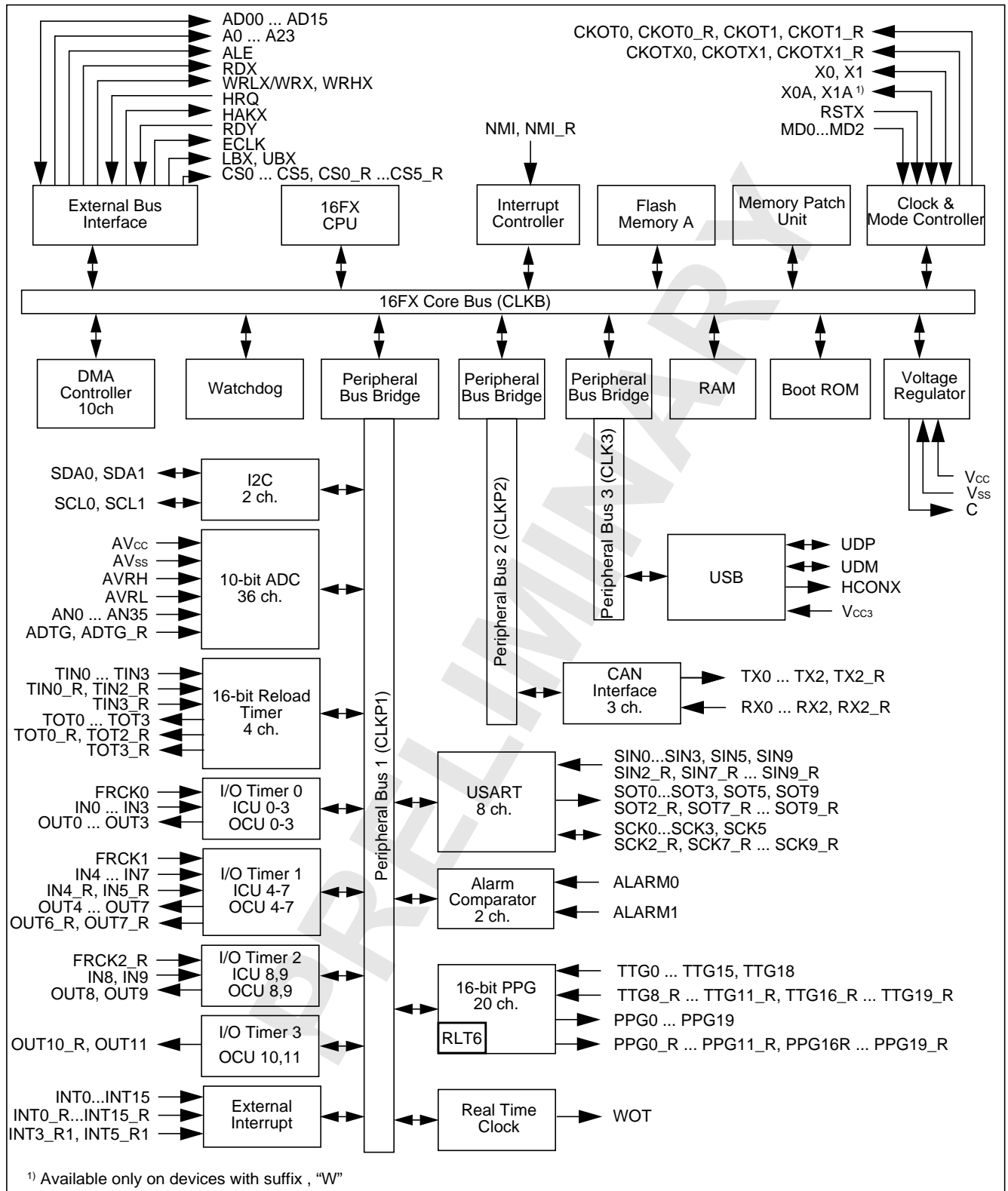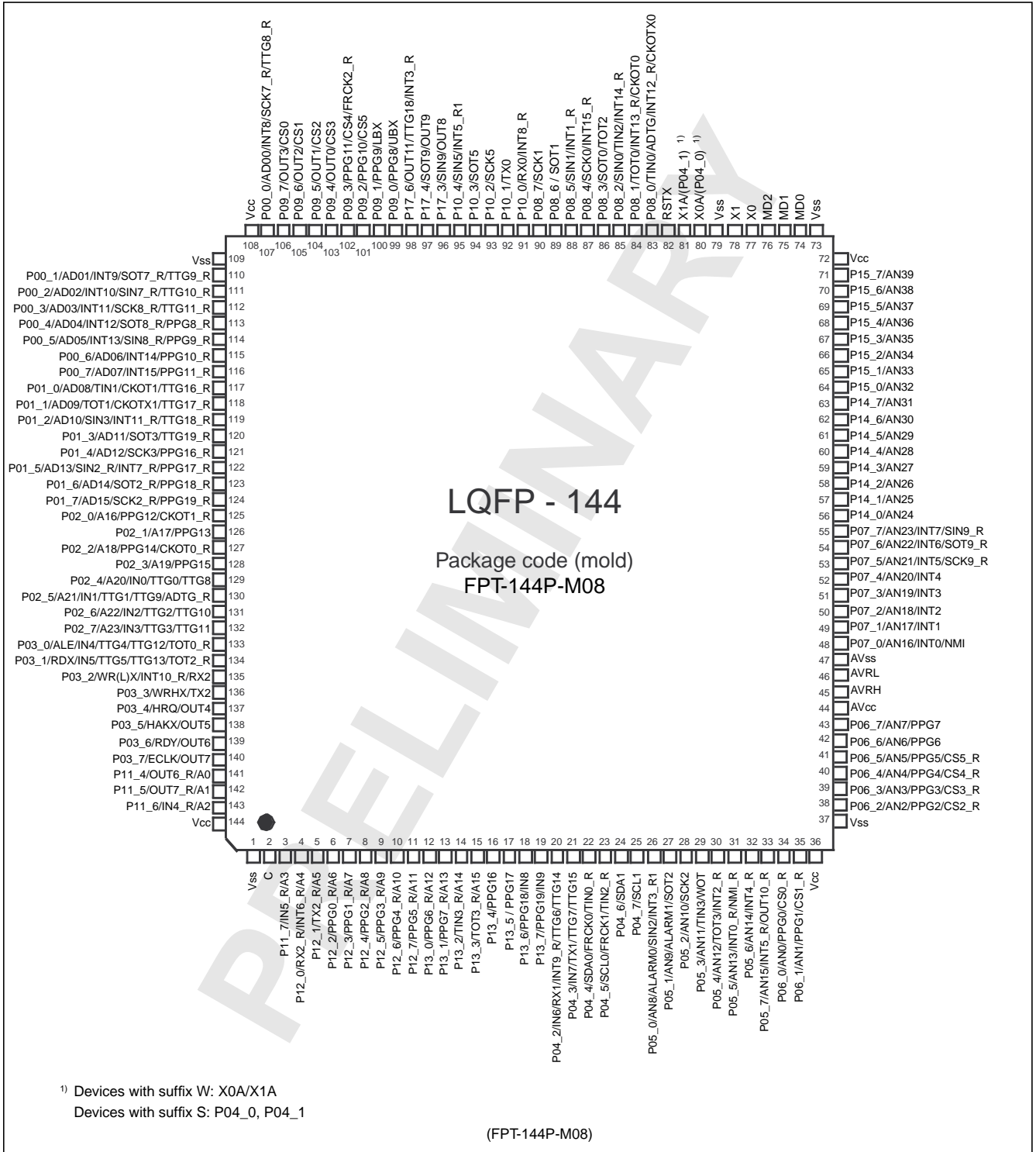
■ BLOCK DIAGRAM

Block diagram of MB96(F)33xY/R

1) Available only on devices with suffix , "W"

Block diagram of MB96(F)33xU

1) Available only on devices with suffix , "W"

■ PIN ASSIGNMENTS

Pin assignment of M96F338Y/R (FPT-144P-M08)

LQFP - 144

Package code (mold)
FPT-144P-M08

(FPT-144P-M08)

Top-side pins (108–73):

Vcc, P00_0/AD00/INT8/SCK7_R/TTG8_R, P09_7/OUT3/CS0, P09_6/OUT2/CS1, P09_5/OUT1/CS2, P09_4/OUT0/CS3, P09_3/PPG11/CS4/FRCK2_R, P09_2/PPG10/CS5, P09_1/PPG9/LBX, P09_0/PPG8/UBX, P17_6/OUT11/TTG18/INT3_R, P17_4/SOT9/OUT9, P17_3/SIN9/OUT8, P10_4/SIN5/INT5_R1, P10_3/SOT5, P10_2/SCK5, P10_1/TX0, P10_0/RX0/INT8_R, P08_7/SCK1, P08_6/SOT1, P08_5/SIN1/INT1_R, P08_4/SCK0/INT15_R, P08_3/SOT0/TOT2, P08_2/SIN0/TIN2/INT14_R, P08_1/TOT0/INT13_R/CKOT0, P08_0/TIN0/ADTG/INT12_R/CKOTX0, RSTX, X1A/(P04_1) [1], X0A/(P04_0) [1], Vss, X1, X0, MD2, MD1, MD0, Vss

Left-side pins (109–144):

Pin	Label
109	Vss
110	P00_1/AD01/INT9/SOT7_R/TTG9_R
111	P00_2/AD02/INT10/SIN7_R/TTG10_R
112	P00_3/AD03/INT11/SCK8_R/TTG11_R
113	P00_4/AD04/INT12/SOT8_R/PPG8_R
114	P00_5/AD05/INT13/SIN8_R/PPG9_R
115	P00_6/AD06/INT14/PPG10_R
116	P00_7/AD07/INT15/PPG11_R
117	P01_0/AD08/TIN1/CKOT1/TTG16_R
118	P01_1/AD09/TOT1/CKOTX1/TTG17_R
119	P01_2/AD10/SIN3/INT11_R/TTG18_R
120	P01_3/AD11/SOT3/TTG19_R
121	P01_4/AD12/SCK3/PPG16_R
122	P01_5/AD13/SIN2_R/INT7_R/PPG17_R
123	P01_6/AD14/SOT2_R/PPG18_R
124	P01_7/AD15/SCK2_R/PPG19_R
125	P02_0/A16/PPG12/CKOT1_R
126	P02_1/A17/PPG13
127	P02_2/A18/PPG14/CKOT0_R
128	P02_3/A19/PPG15
129	P02_4/A20/IN0/TTG0/TTG8
130	P02_5/A21/IN1/TTG1/TTG9/ADTG_R
131	P02_6/A22/IN2/TTG2/TTG10
132	P02_7/A23/IN3/TTG3/TTG11
133	P03_0/ALE/IN4/TTG4/TTG12/TOT0_R
134	P03_1/RDX/IN5/TTG5/TTG13/TOT2_R
135	P03_2/WR(L)X/INT10_R/RX2
136	P03_3/WRHX/TX2
137	P03_4/HRQ/OUT4
138	P03_5/HAKX/OUT5
139	P03_6/RDY/OUT6
140	P03_7/ECLK/OUT7
141	P11_4/OUT6_R/A0
142	P11_5/OUT7_R/A1
143	P11_6/IN4_R/A2
144	Vcc

Right-side pins (72–37):

Pin	Label
72	Vcc
71	P15_7/AN39
70	P15_6/AN38
69	P15_5/AN37
68	P15_4/AN36
67	P15_3/AN35
66	P15_2/AN34
65	P15_1/AN33
64	P15_0/AN32
63	P14_7/AN31
62	P14_6/AN30
61	P14_5/AN29
60	P14_4/AN28
59	P14_3/AN27
58	P14_2/AN26
57	P14_1/AN25
56	P14_0/AN24
55	P07_7/AN23/INT7/SIN9_R
54	P07_6/AN22/INT6/SOT9_R
53	P07_5/AN21/INT5/SCK9_R
52	P07_4/AN20/INT4
51	P07_3/AN19/INT3
50	P07_2/AN18/INT2
49	P07_1/AN17/INT1
48	P07_0/AN16/INT0/NMI
47	AVss
46	AVRL
45	AVRH
44	AVcc
43	P06_7/AN7/PPG7
42	P06_6/AN6/PPG6
41	P06_5/AN5/PPG5/CS5_R
40	P06_4/AN4/PPG4/CS4_R
39	P06_3/AN3/PPG3/CS3_R
38	P06_2/AN2/PPG2/CS2_R
37	Vss

Bottom-side pins (1–36):

Vss, C, P11_7/IN5_R/A3, P12_0/RX2_R/INT6_R/A4, P12_1/TX2_R/A5, P12_2/PPG0_R/A6, P12_3/PPG1_R/A7, P12_4/PPG2_R/A8, P12_5/PPG3_R/A9, P12_6/PPG4_R/A10, P12_7/PPG5_R/A11, P13_0/PPG6_R/A12, P13_1/PPG7_R/A13, P13_2/TIN3_R/A14, P13_3/TOT3_R/A15, P13_4/PPG16, P13_5 / PPG17, P13_6/PPG18/IN8, P13_7/PPG19/IN9, P04_2/IN6/RX1/INT9_R/TTG6/TTG14, P04_3/IN7/TX1/TTG7/TTG15, P04_4/SDA0/FRCK0/TIN0_R, P04_5/SCL0/FRCK1/TIN2_R, P04_6/SDA1, P04_7/SCL1, P05_0/AN8/ALARM0/SIN2/INT3_R1, P05_1/AN9/ALARM1/SOT2, P05_2/AN10/SCK2, P05_3/AN11/TIN3/WOT, P05_4/AN12/TOT3/INT2_R, P05_5/AN13/INT0_R/NMI_R, P05_6/AN14/INT4_R, P05_7/AN15/INT5_R/OUT10_R, P06_0/AN0/PPG0/CS0_R, P06_1/AN1/PPG1/CS1_R, Vcc

[1] Devices with suffix W: X0A/X1A
Devices with suffix S: P04_0, P04_1

Pin assignment of MB96F338U (FPT-144P-M08) USB device

Top pins (108–73):
Vcc, P00_0/AD00/INT8/SCK7_R/TTG8_R, P09_7/OUT3/CS0, P09_6/OUT2/CS1, P09_5/OUT1/CS2, P09_4/OUT0/CS3, P09_3/PPG11/CS4/FRCK2_R, P09_2/PPG10/CS5, P09_1/PPG9/LBX, P09_0/PPG8/UBX, P17_6/OUT11/TTG18/INT3_R, P17_4/SOT9/OUT9, P17_3/SIN9/OUT8, P10_4/SIN5/INT5_R1, P10_3/SOT5, P10_2/SCK5, P10_0/RX0/INT8_R, P08_7/SCK1, P08_6 / SOT1, P08_5/SIN1/INT1_R, P08_4/SCK0/INT15_R, P08_3/SOT0/TOT2, P08_2/SIN0/TIN2/INT14_R, P08_1/TOT0/INT13_R/CKOT0, P08_0/TIN0/ADTG/INT12_R/CKOTX0, RSTX, X1A/(P04_1) 1), X0A/(P04_0) 1), Vss, X1, X0, MD2, MD1, MD0, Vss

Left side (109–144):
- 109 Vss
- 110 P00_1/AD01/INT9/SOT7_R/TTG9_R
- 111 P00_2/AD02/INT10/SIN7_R/TTG10_R
- 112 P00_3/AD03/INT11/SCK8_R/TTG11_R
- 113 P00_4/AD04/INT12/SOT8_R/PPG8_R
- 114 P00_5/AD05/INT13/SIN8_R/PPG9_R
- 115 P00_6/AD06/INT14/PPG10_R
- 116 P00_7/AD07/INT15/PPG11_R
- 117 P01_0/AD08/TIN1/CKOT1/TTG16_R
- 118 P01_1/AD09/TOT1/CKOTX1/TTG17_R
- 119 P01_2/AD10/SIN3/INT11_R/TTG18_R
- 120 P01_3/AD11/SOT3/TTG19_R
- 121 P01_4/AD12/SCK3/PPG16_R
- 122 P01_5/AD13/SIN2_R/INT7_R/PPG17_R
- 123 P01_6/AD14/SOT2_R/PPG18_R
- 124 P01_7/AD15/SCK2_R/PPG19_R
- 125 P02_0/A16/PPG12/CKOT1_R
- 126 P02_1/A17/PPG13
- 127 P02_2/A18/PPG14/CKOT0_R
- 128 P02_3/A19/PPG15
- 129 P02_4/A20/IN0/TTG0/TTG8
- 130 P02_5/A21/IN1/TTG1/TTG9/ADTG_R
- 131 P02_6/A22/IN2/TTG2/TTG10
- 132 P02_7/A23/IN3/TTG3/TTG11
- 133 P03_0/ALE/IN4/TTG4/TTG12/TOT0_R
- 134 P03_1/RDX/IN5/TTG5/TTG13/TOT2_R
- 135 P03_2/WR(L)X/INT10_R/RX2
- 136 P03_3/WRHX/TX2
- 137 P03_4/HRQ/OUT4
- 138 P03_5/HAKX/OUT5
- 139 P03_6/RDY/OUT6
- 140 P03_7/ECLK/OUT7
- 141 P11_4/OUT6_R/A0
- 142 P11_5/OUT7_R/A1
- 143 P11_6/IN4_R/A2
- 144 Vcc

LQFP - 144

Package code (mold)
FPT-144P-M08

Right side (72–37):
- 72 Vcc
- 71 UDM
- 70 UDP
- 69 Vcc3
- 68 HCONX
- 67 P15_3/AN35
- 66 P15_2/AN34
- 65 P15_1/AN33
- 64 P15_0/AN32
- 63 P14_7/AN31
- 62 P14_6/AN30
- 61 P14_5/AN29
- 60 P14_4/AN28
- 59 P14_3/AN27
- 58 P14_2/AN26
- 57 P14_1/AN25
- 56 P14_0/AN24
- 55 P07_7/AN23/INT7/SIN9_R
- 54 P07_6/AN22/INT6/SOT9_R
- 53 P07_5/AN21/INT5/SCK9_R
- 52 P07_4/AN20/INT4
- 51 P07_3/AN19/INT3
- 50 P07_2/AN18/INT2
- 49 P07_1/AN17/INT1
- 48 P07_0/AN16/INT0/NMI
- 47 AVss
- 46 AVRL
- 45 AVRH
- 44 AVcc
- 43 P06_7/AN7/PPG7
- 42 P06_6/AN6/PPG6
- 41 P06_5/AN5/PPG5/CS5_R
- 40 P06_4/AN4/PPG4/CS4_R
- 39 P06_3/AN3/PPG3/CS3_R
- 38 P06_2/AN2/PPG2/CS2_R
- 37 Vss

Bottom pins (1–36):
Vss, C, P11_7/IN5_R/A3, P12_0/RX2_R/INT6_R/A4, P12_1/TX2_R/A5, P12_2/PPG0_R/A6, P12_3/PPG1_R/A7, P12_4/PPG2_R/A8, P12_5/PPG3_R/A9, P12_6/PPG4_R/A10, P12_7/PPG5_R/A11, P13_0/PPG6_R/A12, P13_1/PPG7_R/A13, P13_2/TIN3_R/A14, P13_3/TOT3_R/A15, P13_4/PPG16, P13_5 /PPG17, P13_6/PPG18/IN8, P13_7/PPG19/IN9, P04_2/IN6/RX1/INT9_R/TTG6/TTG14, P04_3/INT7/TX1/TTG7/TTG15, P04_4/SDA0/FRCK0/TIN0_R, P04_5/SCL0/FRCK1/TIN2_R, P04_6/SDA1, P04_7/SCL1, P05_0/AN8/ALARM0/SIN2/INT3_R1, P05_1/AN9/ALARM1/SOT2, P05_2/AN10/SCK2, P05_3/AN11/TIN3/WOT, P05_4/AN12/TOT3/INT2_R, P05_5/AN13/INT0_R/NMI_R, P05_6/AN14/INT4_R, P05_7/AN15/INT5_R/OUT10_R, P06_0/AN0/PPG0/CS0_R, P06_1/AN1/PPG1/CS1_R, Vcc

1) Devices with suffix W: X0A/X1A
   Devices with suffix S: P04_0, P04_1

(FPT-144P-M08)

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 / 3)

Pin name	Feature	Description
ADn	External bus	External bus interface (non multiplexed mode) data input/output. External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus non-multiplexed address output
ANn	ADC	A/D converter channel n input
AV$_{CC}$	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV$_{SS}$	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
CSn_R	External bus	Relocated External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HCONX	USB	USB connection to host or hub
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input

Pin Function description (2 / 3)

Pin name	Feature	Description
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
OUTn_R	OCU	Relocated Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
RXn_R	CAN	Relocated CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
TXn_R	CAN	Relocated CAN interface n TX output

Pin Function description (3 / 3)

Pin name	Feature	Description
UBX	External bus	External Bus Interface Upper Byte select strobe output
UDM	USB	USB minus
UDP	USB	USB plus
V_{CC}	Supply	Power supply
V_{CC3}	Supply	USB Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

PRELIMINARY

■ **PIN CIRCUIT TYPE**

Pin no.	FPT-144P-M08	
	Circuit type[1]	
	MB96(F)33xY/R	MB96(F)33xU (USB device)
1	Supply	
2	F	
3 to 21	H	
22 to 25	N	
26 to 35	I	
36, 37	Supply	
38 to 43	I	
44	Supply	
45	G	
46 to 47	Supply	
48 to 67	I	
68	I	O
69	I	Supply (3.3V)
70, 71	I	P
72, 73	Supply	
74 to 76	C	
77, 78	A	
79	Supply	
80, 81	B[2]	
80, 81	H[3]	
82	E	
83 to 107	H	
108, 109	Supply	
110 to 143	H	
144	Supply	
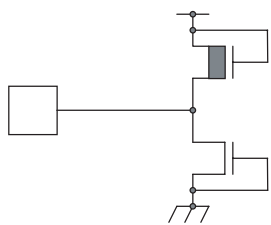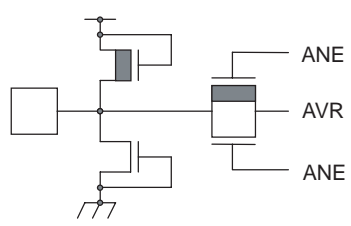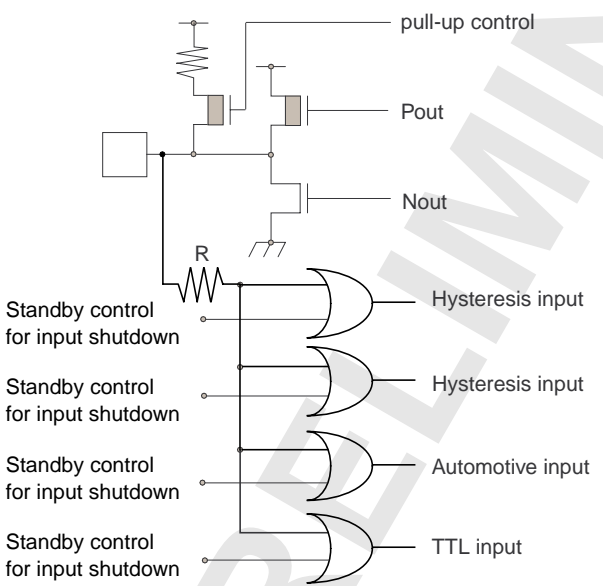
[1] About each circuit type, please refer to IO circuit type below
[2] Devices with suffix "W"
[3] Devices without suffix "W"
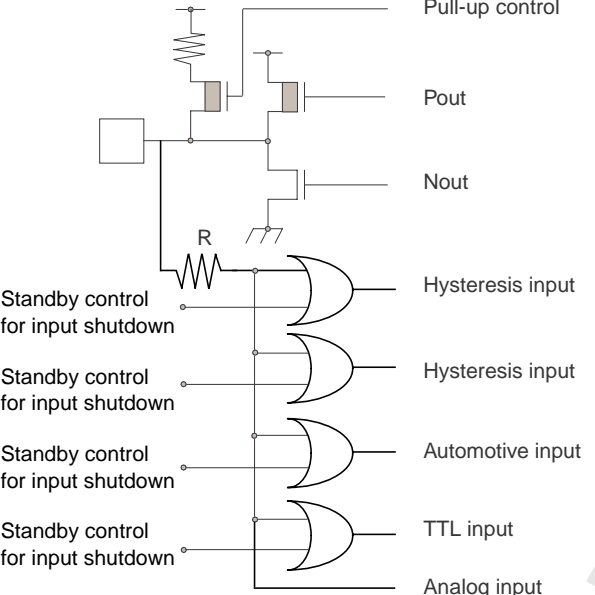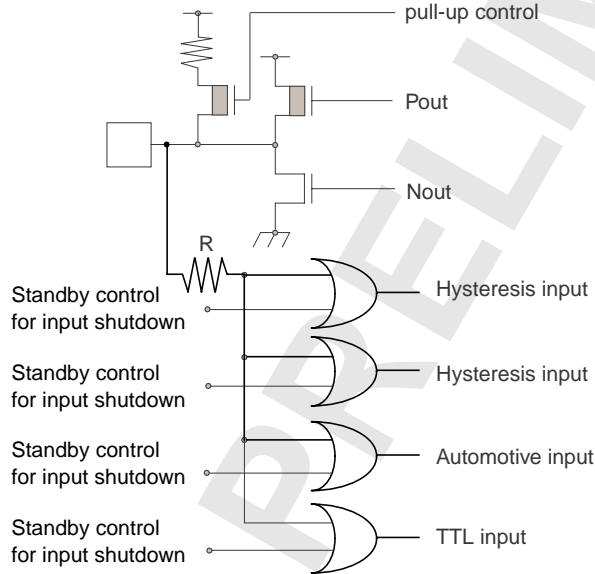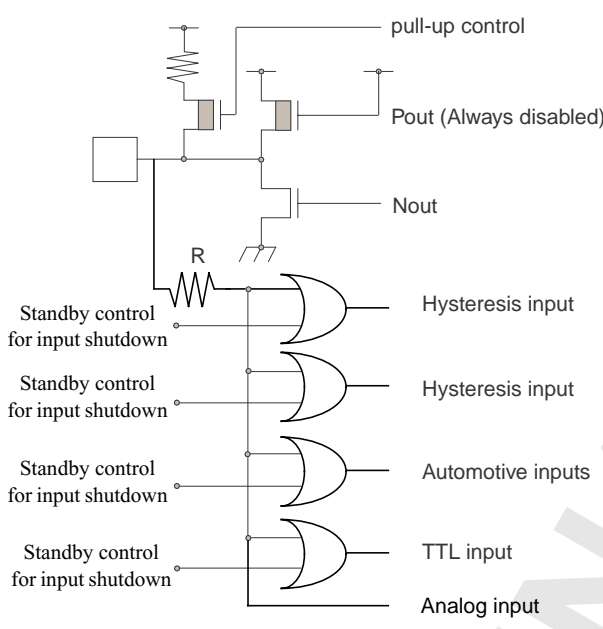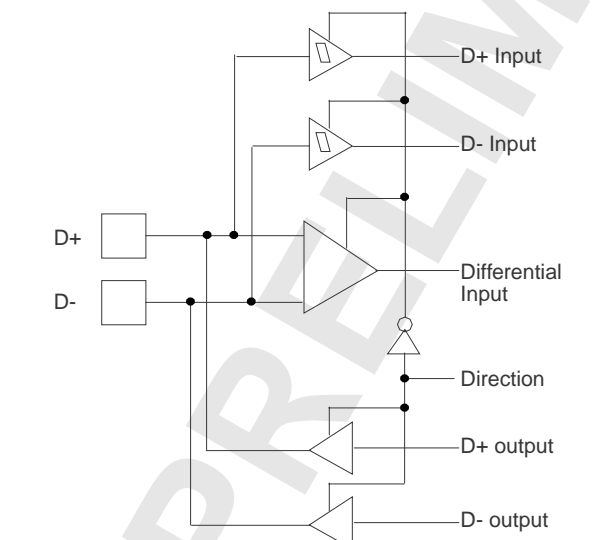
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pins AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
I	Pull-up control / Pout / Nout / R / Standby control for input shutdown / Hysteresis input / Standby control for input shutdown / Hysteresis input / Standby control for input shutdown / Automotive input / Standby control for input shutdown / TTL input / Analog input	• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input
N	pull-up control / Pout / Nout / R / Standby control for input shutdown / Hysteresis input / Standby control for input shutdown / Hysteresis input / Standby control for input shutdown / Automotive input / Standby control for input shutdown / TTL input	• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.

Type	Circuit	Remarks
O	pull-up control Pout (Always disabled) Nout R Standby control for input shutdown — Hysteresis input Standby control for input shutdown — Hysteresis input Standby control for input shutdown — Automotive inputs Standby control for input shutdown — TTL input Analog input	HCONX • Available only for device with suffix "U"
P	D+ Input D- Input D+ D- Differential Input Direction D+ output D- output	USB IO cell: UDP and UDM • Available only for device with suffix "U"

PRELIMINARY

■ MEMORY MAP

	MB96V300B		**MB96(F)3xx**	
FF:FFFF$_H$	Emulation ROM		USER ROM / External Bus^{*4}	
DE:0000$_H$				
	External Bus		External Bus	
10:0000$_H$				
0F:E000$_H$	Boot-ROM		Boot-ROM	
	Reserved			
0E:0000$_H$			Reserved	
	External RAM			
02:0000$_H$			Reserved	
	Internal RAM bank 1	RAMEND1^{*2} RAMSTART1^{*2}	Internal RAM bank 1	RAM availability depending on the device
01:0000$_H$			Reserved	
	ROM/RAM MIRROR		ROM/RAM MIRROR	
00:8000$_H$				
	Internal RAM bank 0	RAMSTART0^{*2}	Internal RAM bank 0	
			Reserved	
RAMSTART0^{*3}			External Bus	External Bus end address^{*2}
00:0C00$_H$	External Bus			
	Peripherals		Peripherals	
00:0380$_H$				
00:0180$_H$	GPR^{*1}		GPR^{*1}	
	DMA		DMA	
00:0100$_H$				
00:00F0$_H$	External Bus		External Bus	
00:0000$_H$	Peripheral		Peripheral	

*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the USER ROM MEMORY MAP on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ **RAMSTART/END AND EXTERNAL BUS END ADDRESSES**

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96336	16kB	-	00:11FF$_H$	00:4240$_H$	-	-
MB96F338, MB96338	28kB	4kB	00:11FF$_H$	00:1240$_H$	01:8000$_H$	01:8FFF$_H$

■ USER ROM MEMORY MAP FOR FLASH DEVICES

Alternative mode CPU address	Flash memory mode address	Flash size 544kByte (MB96F338Y / MB96F338R / MB96F338U)	
FF:FFFFH / FF:0000H	3F:FFFFH / 3F:0000H	S39 - 64K	
FE:FFFFH / FE:0000H	3E:FFFFH / 3E:0000H	S38 - 64K	
FD:FFFFH / FD:0000H	3D:FFFFH / 3D:0000H	S37 - 64K	
FC:FFFFH / FC:0000H	3C:FFFFH / 3C:0000H	S36 - 64K	Flash A
FB:FFFFH / FB:0000H	3B:FFFFH / 3B:0000H	S35 - 64K	
FA:FFFFH / FA:0000H	3A:FFFFH / 3A:0000H	S34 - 64K	
F9:FFFFH / F9:0000H	39:FFFFH / 39:0000H	S33 - 64K	
F8:FFFFH / F8:0000H	38:FFFFH / 38:0000H	S32 - 64K	
F7:FFFFH / F7:0000H	37:FFFFH / 37:0000H		
F6:FFFFH / F6:0000H	36:FFFFH / 36:0000H		
F5:FFFFH / F5:0000H	35:FFFFH / 35:0000H		
F4:FFFFH / F4:0000H	34:FFFFH / 34:0000H		
F3:FFFFH / F3:0000H	33:FFFFH / 33:0000H	External bus	
F2:FFFFH / F2:0000H	32:FFFFH / 32:0000H		
F1:FFFFH / F1:0000H	31:FFFFH / 31:0000H		
F0:FFFFH / F0:0000H	30:FFFFH / 30:0000H		
E0:FFFFH / E0:0000H			
DF:FFFFH / DF:8000H		Reserved	
DF:7FFFH / DF:6000H	1F:7FFFH / 1F:6000H	SA3 - 8K	
DF:5FFFH / DF:4000H	1F:5FFFH / 1F:4000H	SA2 - 8K	Flash A
DF:3FFFH / DF:2000H	1F:3FFFH / 1F:2000H	SA1 - 8K	
DF:1FFFH / DF:0000H	1F:1FFFH / 1F:0000H	SA0 - 8K *1	
DE:FFFFH / DE:0000H		Reserved	

*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

■ USER ROM MEMORY MAP FOR MASK ROM DEVICES

CPU address	MB96336Y MB96336R ROM size 288kByte	MB96338Y MB96338R ROM size 544kByte
FF:FFFFH		
FF:0000H	256K ROM	512K ROM
FE:FFFFH		
FE:0000H		
FD:FFFFH		
FD:0000H		
FC:FFFFH		
FC:0000H		
FB:FFFFH	Reserved	
FB:0000H		
FA:FFFFH		
FA:0000H		
F9:FFFFH		
F9:0000H		
F8:FFFFH		
F8:0000H		
F7:FFFFH	External bus	External bus
E0:0000H		
DF:FFFFH	Reserved	Reserved
DF:8000H		
DF:7FFFH	32K ROM	32K ROM
DF:0080H		
DF:007FH	ROM configuration block RCB	ROM configuration block RCB
DF:0000H		
DE:FFFFH	Reserved	Reserved
DE:0000H		

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F33x		
Pin number	USART Number	Normal function
LQFP-144		
85	USART0	SIN0
86		SOT0
87		SCK0
88	USART1	SIN1
89		SOT1
90		SCK1
26	USART2	SIN2
27		SOT2
28		SCK2

Note: For handshaking pin, please use for this device the default port P00_1 on pin 110. If any other pin is required, please contact the Flash programmer device vendor.

■ **I/O MAP**

I/O map MB96(F)33x (1 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000H	I/O Port P00 - Port Data Register	PDR00		RW
000001H	I/O Port P01 - Port Data Register	PDR01		RW
000002H	I/O Port P02 - Port Data Register	PDR02		RW
000003H	I/O Port P03 - Port Data Register	PDR03		RW
000004H	I/O Port P04 - Port Data Register	PDR04		RW
000005H	I/O Port P05 - Port Data Register	PDR05		RW
000006H	I/O Port P06 - Port Data Register	PDR06		RW
000007H	I/O Port P07 - Port Data Register	PDR07		RW
000008H	I/O Port P08 - Port Data Register	PDR08		RW
000009H	I/O Port P09 - Port Data Register	PDR09		RW
00000AH	I/O Port P10 - Port Data Register	PDR10		RW
00000BH	I/O Port P11 - Port Data Register	PDR11		RW
00000CH	I/O Port P12 - Port Data Register	PDR12		RW
00000DH	I/O Port P13 - Port Data Register	PDR13		RW
00000EH	I/O Port P14 - Port Data Register	PDR14		RW
00000FH	I/O Port P15 - Port Data Register	PDR15		RW
000010H	Reserved			-
000011H	I/O Port P17 - Port Data Register	PDR17		RW
000012H-000017H	Reserved			-
000018H	ADC0 - Control Status register Low	ADCSL	ADCS	RW
000019H	ADC0 - Control Status register High	ADCSH		RW
00001AH	ADC0 - Data Register Low	ADCRL	ADCR	R
00001BH	ADC0 - Data Register High	ADCRH		R
00001CH	ADC0 - Setting Register		ADSR	RW
00001DH	ADC0 - Setting Register			RW
00001EH	ADC0 - Extended Configuration Register	ADECR		RW
00001FH	Reserved			-
000020H	FRT0 - Data register of free-running timer		TCDT0	RW

I/O map MB96(F)33x (2 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000021H	FRT0 - Data register of free-running timer			RW
000022H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	RW
000023H	FRT0 - Control status register of free-running timer High	TCCSH0		RW
000024H	FRT1 - Data register of free-running timer		TCDT1	RW
000025H	FRT1 - Data register of free-running timer			RW
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	RW
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		RW
000028H	OCU0 - Output Compare Control Status	OCS0		RW
000029H	OCU1 - Output Compare Control Status	OCS1		RW
00002AH	OCU0 - Compare Register		OCCP0	RW
00002BH	OCU0 - Compare Register			RW
00002CH	OCU1 - Compare Register		OCCP1	RW
00002DH	OCU1 - Compare Register			RW
00002EH	OCU2 - Output Compare Control Status	OCS2		RW
00002FH	OCU3 - Output Compare Control Status	OCS3		RW
000030H	OCU2 - Compare Register		OCCP2	RW
000031H	OCU2 - Compare Register			RW
000032H	OCU3 - Compare Register		OCCP3	RW
000033H	OCU3 - Compare Register			RW
000034H	OCU4 - Output Compare Control Status	OCS4		RW
000035H	OCU5 - Output Compare Control Status	OCS5		RW
000036H	OCU4 - Compare Register		OCCP4	RW
000037H	OCU4 - Compare Register			RW
000038H	OCU5 - Compare Register		OCCP5	RW
000039H	OCU5 - Compare Register			RW
00003AH	OCU6 - Output Compare Control Status	OCS6		RW
00003BH	OCU7 - Output Compare Control Status	OCS7		RW

I/O map MB96(F)33x (3 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00003CH	OCU6 - Compare Register		OCCP6	RW
00003DH	OCU6 - Compare Register			RW
00003EH	OCU7 - Compare Register		OCCP7	RW
00003FH	OCU7 - Compare Register			RW
000040H	ICU0/ICU1 - Control Status Register	ICS01		RW
000041H	ICU0/ICU1 - Edge register	ICE01		RW
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043H	ICU0 - Capture Register High	IPCPH0		R
000044H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045H	ICU1 - Capture Register High	IPCPH1		R
000046H	ICU2/ICU3 - Control Status Register	ICS23		RW
000047H	ICU2/ICU3 - Edge register	ICE23		RW
000048H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049H	ICU2 - Capture Register High	IPCPH2		R
00004AH	ICU3 - Capture Register Low	IPCPL3	IPCP3	R
00004BH	ICU3 - Capture Register High	IPCPH3		R
00004CH	ICU4/ICU5 - Control Status Register	ICS45		RW
00004DH	ICU4/ICU5 - Edge register	ICE45		RW
00004EH	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004FH	ICU4 - Capture Register High	IPCPH4		R
000050H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051H	ICU5 - Capture Register High	IPCPH5		R
000052H	ICU6/ICU7 - Control Status Register	ICS67		RW
000053H	ICU6/ICU7 - Edge register	ICE67		RW
000054H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055H	ICU6 - Capture Register High	IPCPH6		R
000056H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057H	ICU7 - Capture Register High	IPCPH7		R
000058H	EXTINT0 - External Interrupt Enable Register	ENIR0		RW

I/O map MB96(F)33x (4 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000059H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		RW
00005AH	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	RW
00005BH	EXTINT0 - External Interrupt Level Select High	ELVRH0		RW
00005CH	EXTINT1 - External Interrupt Enable Register	ENIR1		RW
00005DH	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		RW
00005EH	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	RW
00005FH	EXTINT1 - External Interrupt Level Select High	ELVRH1		RW
000060H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	RW
000061H	RLT0 - Timer Control Status Register High	TMCSRH0		RW
000062H	RLT0 - Reload Register - for writing		TMRLR0	W
000062H	RLT0 - Reload Register - for reading		TMR0	R
000063H	RLT0 - Reload Register - for writing			W
000063H	RLT0 - Reload Register - for reading			R
000064H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	RW
000065H	RLT1 - Timer Control Status Register High	TMCSRH1		RW
000066H	RLT1 - Reload Register - for writing		TMRLR1	W
000066H	RLT1 - Reload Register - for reading		TMR1	R
000067H	RLT1 - Reload Register - for writing			W
000067H	RLT1 - Reload Register - for reading			R
000068H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	RW
000069H	RLT2 - Timer Control Status Register High	TMCSRH2		RW
00006AH	RLT2 - Reload Register - for writing		TMRLR2	W
00006AH	RLT2 - Reload Register - for reading		TMR2	R
00006BH	RLT2 - Reload Register - for writing			W
00006BH	RLT2 - Reload Register - for reading			R
00006CH	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	RW
00006DH	RLT3 - Timer Control Status Register High	TMCSRH3		RW
00006EH	RLT3 - Reload Register - for writing		TMRLR3	W
00006EH	RLT3 - Reload Register - for reading		TMR3	R

I/O map MB96(F)33x (5 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00006FH	RLT3 - Reload Register - for writing			W
00006FH	RLT3 - Reload Register - for reading			R
000070H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	RW
000071H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		RW
000072H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	RW
000075H	PPG3-PPG0 - General Control register 1 High	GCN1H0		RW
000076H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	RW
000077H	PPG3-PPG0 - General Control register 2 High	GCN2H0		RW
000078H	PPG0 - Timer register		PTMR0	R
000079H	PPG0 - Timer register			R
00007AH	PPG0 - Period setting register		PCSR0	W
00007BH	PPG0 - Period setting register			W
00007CH	PPG0 - Duty cycle register		PDUT0	W
00007DH	PPG0 - Duty cycle register			W
00007EH	PPG0 - Control status register Low	PCNL0	PCN0	RW
00007FH	PPG0 - Control status register High	PCNH0		RW
000080H	PPG1 - Timer register		PTMR1	R
000081H	PPG1 - Timer register			R
000082H	PPG1 - Period setting register		PCSR1	W
000083H	PPG1 - Period setting register			W
000084H	PPG1 - Duty cycle register		PDUT1	W
000085H	PPG1 - Duty cycle register			W

I/O map MB96(F)33x (6 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000086H	PPG1 - Control status register Low	PCNL1	PCN1	RW
000087H	PPG1 - Control status register High	PCNH1		RW
000088H	PPG2 - Timer register		PTMR2	R
000089H	PPG2 - Timer register			R
00008AH	PPG2 - Period setting register		PCSR2	W
00008BH	PPG2 - Period setting register			W
00008CH	PPG2 - Duty cycle register		PDUT2	W
00008DH	PPG2 - Duty cycle register			W
00008EH	PPG2 - Control status register Low	PCNL2	PCN2	RW
00008FH	PPG2 - Control status register High	PCNH2		RW
000090H	PPG3 - Timer register		PTMR3	R
000091H	PPG3 - Timer register			R
000092H	PPG3 - Period setting register		PCSR3	W
000093H	PPG3 - Period setting register			W
000094H	PPG3 - Duty cycle register		PDUT3	W
000095H	PPG3 - Duty cycle register			W
000096H	PPG3 - Control status register Low	PCNL3	PCN3	RW
000097H	PPG3 - Control status register High	PCNH3		RW
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	RW
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1		RW
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	RW
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1		RW
00009CH	PPG4 - Timer register		PTMR4	R
00009DH	PPG4 - Timer register			R
00009EH	PPG4 - Period setting register		PCSR4	W
00009FH	PPG4 - Period setting register			W
0000A0H	PPG4 - Duty cycle register		PDUT4	W
0000A1H	PPG4 - Duty cycle register			W
0000A2H	PPG4 - Control status register Low	PCNL4	PCN4	RW
0000A3H	PPG4 - Control status register High	PCNH4		RW

I/O map MB96(F)33x (7 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000A4H	PPG5 - Timer register		PTMR5	R
0000A5H	PPG5 - Timer register			R
0000A6H	PPG5 - Period setting register		PCSR5	W
0000A7H	PPG5 - Period setting register			W
0000A8H	PPG5 - Duty cycle register		PDUT5	W
0000A9H	PPG5 - Duty cycle register			W
0000AAH	PPG5 - Control status register Low	PCNL5	PCN5	RW
0000ABH	PPG5 - Control status register High	PCNH5		RW
0000ACH	I2C0 - Bus Status Register	IBSR0		R
0000ADH	I2C0 - Bus Control Register	IBCR0		RW
0000AEH	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	RW
0000AFH	I2C0 - Ten bit Slave address Register High	ITBAH0		RW
0000B0H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	RW
0000B1H	I2C0 - Ten bit Address mask Register High	ITMKH0		RW
0000B2H	I2C0 - Seven bit Slave address Register	ISBA0		RW
0000B3H	I2C0 - Seven bit Address mask Register	ISMK0		RW
0000B4H	I2C0 - Data Register	IDAR0		RW
0000B5H	I2C0 - Clock Control Register	ICCR0		RW
0000B6H	I2C1 - Bus Status Register	IBSR1		R
0000B7H	I2C1 - Bus Control Register	IBCR1		RW
0000B8H	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	RW
0000B9H	I2C1 - Ten bit Slave address Register High	ITBAH1		RW
0000BAH	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	RW
0000BBH	I2C1 - Ten bit Address mask Register High	ITMKH1		RW
0000BCH	I2C1 - Seven bit Slave address Register	ISBA1		RW
0000BDH	I2C1 - Seven bit Address mask Register	ISMK1		RW
0000BEH	I2C1 - Data Register	IDAR1		RW
0000BFH	I2C1 - Clock Control Register	ICCR1		RW
0000C0H	USART0 - Serial Mode Register	SMR0		RW
0000C1H	USART0 - Serial Control Register	SCR0		RW

I/O map MB96(F)33x (8 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000C2H	USART0 - TX Register	TDR0		W
0000C2H	USART0 - RX Register	RDR0		R
0000C3H	USART0 - Serial Status	SSR0		RW
0000C4H	USART0 - Control/Com. Register	ECCR0		RW
0000C5H	USART0 - Ext. Status Register	ESCR0		RW
0000C6H	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	RW
0000C7H	USART0 - Baud Rate Generator Register High	BGRH0		RW
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0		RW
0000C9H	Reserved			-
0000CAH	USART1 - Serial Mode Register	SMR1		RW
0000CBH	USART1 - Serial Control Register	SCR1		RW
0000CCH	USART1 - TX Register	TDR1		W
0000CCH	USART1 - RX Register	RDR1		R
0000CDH	USART1 - Serial Status	SSR1		RW
0000CEH	USART1 - Control/Com. Register	ECCR1		RW
0000CFH	USART1 - Ext. Status Register	ESCR1		RW
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	RW
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1		RW
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1		RW
0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		RW
0000D5H	USART2 - Serial Control Register	SCR2		RW
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		RW
0000D8H	USART2 - Control/Com. Register	ECCR2		RW
0000D9H	USART2 - Ext. Status Register	ESCR2		RW
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	RW
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		RW
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		RW

I/O map MB96(F)33x (9 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000DDH	Reserved			-
0000DEH	USART3 - Serial Mode Register	SMR3		RW
0000DFH	USART3 - Serial Control Register	SCR3		RW
0000E0H	USART3 - TX Register	TDR3		W
0000E0H	USART3 - RX Register	RDR3		R
0000E1H	USART3 - Serial Status	SSR3		RW
0000E2H	USART3 - Control/Com. Register	ECCR3		RW
0000E3H	USART3 - Ext. Status Register	ESCR3		RW
0000E4H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	RW
0000E5H	USART3 - Baud Rate Generator Register High	BGRH3		RW
0000E6H	USART3 - Extended Serial Interrupt Register	ESIR3		RW
0000E7H-0000EFH	Reserved			-
0000F0H-0000FFH	External Bus area	EXTBUS0		RW
000100H	DMA0 - Buffer address pointer low byte	BAPL0		RW
000101H	DMA0 - Buffer address pointer middle byte	BAPM0		RW
000102H	DMA0 - Buffer address pointer high byte	BAPH0		RW
000103H	DMA0 - DMA control register	DMACS0		RW
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	RW
000105H	DMA0 - I/O register address pointer high byte	IOAH0		RW
000106H	DMA0 - Data counter low byte	DCTL0	DCT0	RW
000107H	DMA0 - Data counter high byte	DCTH0		RW
000108H	DMA1 - Buffer address pointer low byte	BAPL1		RW
000109H	DMA1 - Buffer address pointer middle byte	BAPM1		RW
00010AH	DMA1 - Buffer address pointer high byte	BAPH1		RW
00010BH	DMA1 - DMA control register	DMACS1		RW
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	RW
00010DH	DMA1 - I/O register address pointer high byte	IOAH1		RW
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1	RW
00010FH	DMA1 - Data counter high byte	DCTH1		RW

I/O map MB96(F)33x (10 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000110H	DMA2 - Buffer address pointer low byte	BAPL2		RW
000111H	DMA2 - Buffer address pointer middle byte	BAPM2		RW
000112H	DMA2 - Buffer address pointer high byte	BAPH2		RW
000113H	DMA2 - DMA control register	DMACS2		RW
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	RW
000115H	DMA2 - I/O register address pointer high byte	IOAH2		RW
000116H	DMA2 - Data counter low byte	DCTL2	DCT2	RW
000117H	DMA2 - Data counter high byte	DCTH2		RW
000118H	DMA3 - Buffer address pointer low byte	BAPL3		RW
000119H	DMA3 - Buffer address pointer middle byte	BAPM3		RW
00011AH	DMA3 - Buffer address pointer high byte	BAPH3		RW
00011BH	DMA3 - DMA control register	DMACS3		RW
00011CH	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	RW
00011DH	DMA3 - I/O register address pointer high byte	IOAH3		RW
00011EH	DMA3 - Data counter low byte	DCTL3	DCT3	RW
00011FH	DMA3 - Data counter high byte	DCTH3		RW
000120H	DMA4 - Buffer address pointer low byte	BAPL4		RW
000121H	DMA4 - Buffer address pointer middle byte	BAPM4		RW
000122H	DMA4 - Buffer address pointer high byte	BAPH4		RW
000123H	DMA4 - DMA control register	DMACS4		RW
000124H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	RW
000125H	DMA4 - I/O register address pointer high byte	IOAH4		RW
000126H	DMA4 - Data counter low byte	DCTL4	DCT4	RW
000127H	DMA4 - Data counter high byte	DCTH4		RW
000128H	DMA5 - Buffer address pointer low byte	BAPL5		RW
000129H	DMA5 - Buffer address pointer middle byte	BAPM5		RW
00012AH	DMA5 - Buffer address pointer high byte	BAPH5		RW
00012BH	DMA5 - DMA control register	DMACS5		RW
00012CH	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	RW
00012DH	DMA5 - I/O register address pointer high byte	IOAH5		RW

I/O map MB96(F)33x (11 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00012EH	DMA5 - Data counter low byte	DCTL5	DCT5	RW
00012FH	DMA5 - Data counter high byte	DCTH5		RW
000130H	DMA6 - Buffer address pointer low byte	BAPL6		RW
000131H	DMA6 - Buffer address pointer middle byte	BAPM6		RW
000132H	DMA6 - Buffer address pointer high byte	BAPH6		RW
000133H	DMA6 - DMA control register	DMACS6		RW
000134H	DMA6 - I/O register address pointer low byte	IOAL6	IOA6	RW
000135H	DMA6 - I/O register address pointer high byte	IOAH6		RW
000136H	DMA6 - Data counter low byte	DCTL6	DCT6	RW
000137H	DMA6 - Data counter high byte	DCTH6		RW
000138H	DMA7 - Buffer address pointer low byte	BAPL7		RW
000139H	DMA7 - Buffer address pointer middle byte	BAPM7		RW
00013AH	DMA7 - Buffer address pointer high byte	BAPH7		RW
00013BH	DMA7 - DMA control register	DMACS7		RW
00013CH	DMA7 - I/O register address pointer low byte	IOAL7	IOA7	RW
00013DH	DMA7 - I/O register address pointer high byte	IOAH7		RW
00013EH	DMA7 - Data counter low byte	DCTL7	DCT7	RW
00013FH	DMA7 - Data counter high byte	DCTH7		RW
000140H	DMA8 - Buffer address pointer low byte	BAPL8		RW
000141H	DMA8 - Buffer address pointer middle byte	BAPM8		RW
000142H	DMA8 - Buffer address pointer high byte	BAPH8		RW
000143H	DMA8 - DMA control register	DMACS8		RW
000144H	DMA8 - I/O register address pointer low byte	IOAL8	IOA8	RW
000145H	DMA8 - I/O register address pointer high byte	IOAH8		RW
000146H	DMA8 - Data counter low byte	DCTL8	DCT8	RW
000147H	DMA8 - Data counter high byte	DCTH8		RW
000148H	DMA9 - Buffer address pointer low byte	BAPL9		RW
000149H	DMA9 - Buffer address pointer middle byte	BAPM9		RW
00014AH	DMA9 - Buffer address pointer high byte	BAPH9		RW
00014BH	DMA9 - DMA control register	DMACS9		RW

I/O map MB96(F)33x (12 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00014CH	DMA9 - I/O register address pointer low byte	IOAL9	IOA9	RW
00014DH	DMA9 - I/O register address pointer high byte	IOAH9		RW
00014EH	DMA9 - Data counter low byte	DCTL9	DCT9	RW
00014FH	DMA9 - Data counter high byte	DCTH9		RW
000150H-00017FH	Reserved			-
000180H-00037FH	CPU - General Purpose registers (RAM access)	GPR_RAM		RW
000380H	DMA0 - Interrupt select	DISEL0		RW
000381H	DMA1 - Interrupt select	DISEL1		RW
000382H	DMA2 - Interrupt select	DISEL2		RW
000383H	DMA3 - Interrupt select	DISEL3		RW
000384H	DMA4 - Interrupt select	DISEL4		RW
000385H	DMA5 - Interrupt select	DISEL5		RW
000386H	DMA6 - Interrupt select	DISEL6		RW
000387H	DMA7 - Interrupt select	DISEL7		RW
000388H	DMA8 - Interrupt select	DISEL8		RW
000389H	DMA9 - Interrupt select	DISEL9		RW
00038AH-00038FH	Reserved			-
000390H	DMA - Status register low byte	DSRL	DSR	RW
000391H	DMA - Status register high byte	DSRH		RW
000392H	DMA - Stop status register low byte	DSSRL	DSSR	RW
000393H	DMA - Stop status register high byte	DSSRH		RW
000394H	DMA - Enable register low byte	DERL	DER	RW
000395H	DMA - Enable register high byte	DERH		RW
000396H-00039FH	Reserved			-
0003A0H	Interrupt level register	ILR	ICR	RW
0003A1H	Interrupt index register	IDX		RW
0003A2H	Interrupt vector table base register Low	TBRL	TBR	RW

I/O map MB96(F)33x (13 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003A3H	Interrupt vector table base register High	TBRH		RW
0003A4H	Delayed Interrupt register	DIRR		RW
0003A5H	Non Maskable Interrupt register	NMI		RW
0003A6H-0003ABH	Reserved			-
0003ACH	EDSU communication interrupt selection Low	EDSU2L	EDSU2	RW
0003ADH	EDSU communication interrupt selection High	EDSU2H		RW
0003AEH	ROM mirror control register	ROMM		RW
0003AFH	EDSU configuration register	EDSU		RW
0003B0H	Memory patch control/status register ch 0/1		PFCS0	RW
0003B1H	Memory patch control/status register ch 0/1			RW
0003B2H	Memory patch control/status register ch 2/3		PFCS1	RW
0003B3H	Memory patch control/status register ch 2/3			RW
0003B4H	Memory patch control/status register ch 4/5		PFCS2	RW
0003B5H	Memory patch control/status register ch 4/5			RW
0003B6H	Memory patch control/status register ch 6/7		PFCS3	RW
0003B7H	Memory patch control/status register ch 6/7			RW
0003B8H	Memory Patch function - Patch address 0 low	PFAL0		RW
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0		RW
0003BAH	Memory Patch function - Patch address 0 high	PFAH0		RW
0003BBH	Memory Patch function - Patch address 1 low	PFAL1		RW
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1		RW
0003BDH	Memory Patch function - Patch address 1 high	PFAH1		RW
0003BEH	Memory Patch function - Patch address 2 low	PFAL2		RW
0003BFH	Memory Patch function - Patch address 2 middle	PFAM2		RW
0003C0H	Memory Patch function - Patch address 2 high	PFAH2		RW
0003C1H	Memory Patch function - Patch address 3 low	PFAL3		RW
0003C2H	Memory Patch function - Patch address 3 middle	PFAM3		RW
0003C3H	Memory Patch function - Patch address 3 high	PFAH3		RW
0003C4H	Memory Patch function - Patch address 4 low	PFAL4		RW

I/O map MB96(F)33x (14 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003C5H	Memory Patch function - Patch address 4 middle	PFAM4		RW
0003C6H	Memory Patch function - Patch address 4 high	PFAH4		RW
0003C7H	Memory Patch function - Patch address 5 low	PFAL5		RW
0003C8H	Memory Patch function - Patch address 5 middle	PFAM5		RW
0003C9H	Memory Patch function - Patch address 5 high	PFAH5		RW
0003CAH	Memory Patch function - Patch address 6 low	PFAL6		RW
0003CBH	Memory Patch function - Patch address 6 middle	PFAM6		RW
0003CCH	Memory Patch function - Patch address 6 high	PFAH6		RW
0003CDH	Memory Patch function - Patch address 7 low	PFAL7		RW
0003CEH	Memory Patch function - Patch address 7 middle	PFAM7		RW
0003CFH	Memory Patch function - Patch address 7 high	PFAH7		RW
0003D0H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	RW
0003D1H	Memory Patch function - Patch data 0 High	PFDH0		RW
0003D2H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	RW
0003D3H	Memory Patch function - Patch data 1 High	PFDH1		RW
0003D4H	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	RW
0003D5H	Memory Patch function - Patch data 2 High	PFDH2		RW
0003D6H	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	RW
0003D7H	Memory Patch function - Patch data 3 High	PFDH3		RW
0003D8H	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	RW
0003D9H	Memory Patch function - Patch data 4 High	PFDH4		RW
0003DAH	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	RW
0003DBH	Memory Patch function - Patch data 5 High	PFDH5		RW
0003DCH	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	RW
0003DDH	Memory Patch function - Patch data 6 High	PFDH6		RW
0003DEH	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	RW
0003DFH	Memory Patch function - Patch data 7 High	PFDH7		RW
0003E0H-0003F0H	Reserved			-
0003F1H	Memory Control Status Register A	MCSRA		RW

I/O map MB96(F)33x (15 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003F2H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	RW
0003F3H	Memory Timing Configuration Register A High	MTCRAH		RW
0003F4H-0003F8H	Reserved			-
0003F9H	Flash Memory Write Control register 1	FMWC1		RW
0003FAH	Flash Memory Write Control register 2	FMWC2		RW
0003FBH	Flash Memory Write Control register 3	FMWC3		RW
0003FCH	Flash Memory Write Control register 4	FMWC4		RW
0003FDH	Flash Memory Write Control register 5	FMWC5		RW
0003FEH-0003FFH	Reserved			-
000400H	Standby Mode control register	SMCR		RW
000401H	Clock select register	CKSR		RW
000402H	Clock Stabilisation select register	CKSSR		RW
000403H	Clock monitor register	CKMR		R
000404H	Clock Frequency control register Low	CKFCRL	CKFCR	RW
000405H	Clock Frequency control register High	CKFCRH		RW
000406H	PLL Control register Low	PLLCRL	PLLCR	RW
000407H	PLL Control register High	PLLCRH		RW
000408H	RC clock timer control register	RCTCR		RW
000409H	Main clock timer control register	MCTCR		RW
00040AH	Sub clock timer control register	SCTCR		RW
00040BH	Reset cause and clock status register with clear function	RCCSRC		R
00040CH	Reset configuration register	RCR		RW
00040DH	Reset cause and clock status register	RCCSR		R
00040EH	Watch dog timer configuration register	WDTC		RW
00040FH	Watch dog timer clear pattern register	WDTCP		W
000410H-000414H	Reserved			-
000415H	Clock output activation register	COAR		RW

I/O map MB96(F)33x (16 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000416H	Clock output configuration register 0	COCR0		RW
000417H	Clock output configuration register 1	COCR1		RW
000418H	Clock Modulator control register	CMCR		RW
000419H	Reserved			-
00041AH	Clock Modulator Parameter register Low	CMPRL	CMPR	RW
00041BH	Clock Modulator Parameter register High	CMPRH		RW
00041CH-00042BH	Reserved			-
00042CH	Voltage Regulator Control register	VRCR		RW
00042DH	Clock Input and LVD Control Register	CILCR		RW
00042EH-00042FH	Reserved			-
000430H	I/O Port P00 - Data Direction Register	DDR00		RW
000431H	I/O Port P01 - Data Direction Register	DDR01		RW
000432H	I/O Port P02 - Data Direction Register	DDR02		RW
000433H	I/O Port P03 - Data Direction Register	DDR03		RW
000434H	I/O Port P04 - Data Direction Register	DDR04		RW
000435H	I/O Port P05 - Data Direction Register	DDR05		RW
000436H	I/O Port P06 - Data Direction Register	DDR06		RW
000437H	I/O Port P07 - Data Direction Register	DDR07		RW
000438H	I/O Port P08 - Data Direction Register	DDR08		RW
000439H	I/O Port P09 - Data Direction Register	DDR09		RW
00043AH	I/O Port P10 - Data Direction Register	DDR10		RW
00043BH	I/O Port P11 - Data Direction Register	DDR11		RW
00043CH	I/O Port P12 - Data Direction Register	DDR12		RW
00043DH	I/O Port P13 - Data Direction Register	DDR13		RW
00043EH	I/O Port P14 - Data Direction Register	DDR14		RW
00043FH	I/O Port P15 - Data Direction Register	DDR15		RW
000440H	Reserved			-
000441H	I/O Port P17 - Data Direction Register	DDR17		RW

I/O map MB96(F)33x (17 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000442H-000443H	Reserved			-
000444H	I/O Port P00 - Port Input Enable Register	PIER00		RW
000445H	I/O Port P01 - Port Input Enable Register	PIER01		RW
000446H	I/O Port P02 - Port Input Enable Register	PIER02		RW
000447H	I/O Port P03 - Port Input Enable Register	PIER03		RW
000448H	I/O Port P04 - Port Input Enable Register	PIER04		RW
000449H	I/O Port P05 - Port Input Enable Register	PIER05		RW
00044AH	I/O Port P06 - Port Input Enable Register	PIER06		RW
00044BH	I/O Port P07 - Port Input Enable Register	PIER07		RW
00044CH	I/O Port P08 - Port Input Enable Register	PIER08		RW
00044DH	I/O Port P09 - Port Input Enable Register	PIER09		RW
00044EH	I/O Port P10 - Port Input Enable Register	PIER10		RW
00044FH	I/O Port P11 - Port Input Enable Register	PIER11		RW
000450H	I/O Port P12 - Port Input Enable Register	PIER12		RW
000451H	I/O Port P13 - Port Input Enable Register	PIER13		RW
000452H	I/O Port P14 - Port Input Enable Register	PIER14		RW
000453H	I/O Port P15 - Port Input Enable Register	PIER15		RW
000454H	Reserved			-
000455H	I/O Port P17 - Port Input Enable Register	PIER17		RW
000456H-000457H	Reserved			-
000458H	I/O Port P00 - Port Input Level Register	PILR00		RW
000459H	I/O Port P01 - Port Input Level Register	PILR01		RW
00045AH	I/O Port P02 - Port Input Level Register	PILR02		RW
00045BH	I/O Port P03 - Port Input Level Register	PILR03		RW
00045CH	I/O Port P04 - Port Input Level Register	PILR04		RW
00045DH	I/O Port P05 - Port Input Level Register	PILR05		RW
00045EH	I/O Port P06 - Port Input Level Register	PILR06		RW
00045FH	I/O Port P07 - Port Input Level Register	PILR07		RW
000460H	I/O Port P08 - Port Input Level Register	PILR08		RW

I/O map MB96(F)33x (18 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000461H	I/O Port P09 - Port Input Level Register	PILR09		RW
000462H	I/O Port P10 - Port Input Level Register	PILR10		RW
000463H	I/O Port P11 - Port Input Level Register	PILR11		RW
000464H	I/O Port P12 - Port Input Level Register	PILR12		RW
000465H	I/O Port P13 - Port Input Level Register	PILR13		RW
000466H	I/O Port P14 - Port Input Level Register	PILR14		RW
000467H	I/O Port P15 - Port Input Level Register	PILR15		RW
000468H	Reserved			-
000469H	I/O Port P17 - Port Input Level Register	PILR17		RW
00046AH-00046BH	Reserved			-
00046CH	I/O Port P00 - Extended Port Input Level Register	EPILR00		RW
00046DH	I/O Port P01 - Extended Port Input Level Register	EPILR01		RW
00046EH	I/O Port P02 - Extended Port Input Level Register	EPILR02		RW
00046FH	I/O Port P03 - Extended Port Input Level Register	EPILR03		RW
000470H	I/O Port P04 - Extended Port Input Level Register	EPILR04		RW
000471H	I/O Port P05 - Extended Port Input Level Register	EPILR05		RW
000472H	I/O Port P06 - Extended Port Input Level Register	EPILR06		RW
000473H	I/O Port P07 - Extended Port Input Level Register	EPILR07		RW
000474H	I/O Port P08 - Extended Port Input Level Register	EPILR08		RW
000475H	I/O Port P09 - Extended Port Input Level Register	EPILR09		RW
000476H	I/O Port P10 - Extended Port Input Level Register	EPILR10		RW
000477H	I/O Port P11 - Extended Port Input Level Register	EPILR11		RW
000478H	I/O Port P12 - Extended Port Input Level Register	EPILR12		RW
000479H	I/O Port P13 - Extended Port Input Level Register	EPILR13		RW
00047AH	I/O Port P14 - Extended Port Input Level Register	EPILR14		RW
00047BH	I/O Port P15 - Extended Port Input Level Register	EPILR15		RW
00047CH	Reserved			-
00047DH	I/O Port P17 - Extended Port Input Level Register	EPILR17		RW
00047EH-00047FH	Reserved			-

I/O map MB96(F)33x (19 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000480H	I/O Port P00 - Port Output Drive Register	PODR00		RW
000481H	I/O Port P01 - Port Output Drive Register	PODR01		RW
000482H	I/O Port P02 - Port Output Drive Register	PODR02		RW
000483H	I/O Port P03 - Port Output Drive Register	PODR03		RW
000484H	I/O Port P04 - Port Output Drive Register	PODR04		RW
000485H	I/O Port P05 - Port Output Drive Register	PODR05		RW
000486H	I/O Port P06 - Port Output Drive Register	PODR06		RW
000487H	I/O Port P07 - Port Output Drive Register	PODR07		RW
000488H	I/O Port P08 - Port Output Drive Register	PODR08		RW
000489H	I/O Port P09 - Port Output Drive Register	PODR09		RW
00048AH	I/O Port P10 - Port Output Drive Register	PODR10		RW
00048BH	I/O Port P11 - Port Output Drive Register	PODR11		RW
00048CH	I/O Port P12 - Port Output Drive Register	PODR12		RW
00048DH	I/O Port P13 - Port Output Drive Register	PODR13		RW
00048EH	I/O Port P14 - Port Output Drive Register	PODR14		RW
00048FH	I/O Port P15 - Port Output Drive Register	PODR15		RW
000490H	Reserved			-
000491H	I/O Port P17 - Port Output Drive Register	PODR17		RW
000492H-00049BH	Reserved			-
00049CH	I/O Port P08 - Port High Drive Register	PHDR08		RW
00049DH	I/O Port P09 - Port High Drive Register	PHDR09		RW
00049EH	I/O Port P10 - Port High Drive Register	PHDR10		RW
00049FH-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		RW
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		RW
0004AAH	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		RW
0004ABH	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		RW
0004ACH	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		RW
0004ADH	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		RW

I/O map MB96(F)33x (20 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004AEH	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		RW
0004AFH	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		RW
0004B0H	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		RW
0004B1H	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		RW
0004B2H	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		RW
0004B3H	I/O Port P11 - Pull-Up resistor Control Register	PUCR11		RW
0004B4H	I/O Port P12 - Pull-Up resistor Control Register	PUCR12		RW
0004B5H	I/O Port P13 - Pull-Up resistor Control Register	PUCR13		RW
0004B6H	I/O Port P14 - Pull-Up resistor Control Register	PUCR14		RW
0004B7H	I/O Port P15 - Pull-Up resistor Control Register	PUCR15		RW
0004B8H	Reserved			-
0004B9H	I/O Port P17 - Pull-Up resistor Control Register	PUCR17		RW
0004BAH-0004BBH	Reserved			-
0004BCH	I/O Port P00 - External Pin State Register	EPSR00		R
0004BDH	I/O Port P01 - External Pin State Register	EPSR01		R
0004BEH	I/O Port P02 - External Pin State Register	EPSR02		R
0004BFH	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3H	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4H	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5H	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6H	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7H	I/O Port P11 - External Pin State Register	EPSR11		R
0004C8H	I/O Port P12 - External Pin State Register	EPSR12		R
0004C9H	I/O Port P13 - External Pin State Register	EPSR13		R
0004CAH	I/O Port P14 - External Pin State Register	EPSR14		R
0004CBH	I/O Port P15 - External Pin State Register	EPSR15		R

I/O map MB96(F)33x (21 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004CCH	Reserved			-
0004CDH	I/O Port P17 - External Pin State Register	EPSR17		R
0004CEH-0004CFH	Reserved			-
0004D0H	ADC analog input enable register 0	ADER0		RW
0004D1H	ADC analog input enable register 1	ADER1		RW
0004D2H	ADC analog input enable register 2	ADER2		RW
0004D3H	ADC analog input enable register 3	ADER3		RW
0004D4H	ADC analog input enable register 4	ADER4		RW
0004D5H	Reserved			-
0004D6H	Peripheral Resource Relocation Register 0	PRRR0		RW
0004D7H	Peripheral Resource Relocation Register 1	PRRR1		RW
0004D8H	Peripheral Resource Relocation Register 2	PRRR2		RW
0004D9H	Peripheral Resource Relocation Register 3	PRRR3		RW
0004DAH	Peripheral Resource Relocation Register 4	PRRR4		RW
0004DBH	Peripheral Resource Relocation Register 5	PRRR5		RW
0004DCH	Peripheral Resource Relocation Register 6	PRRR6		RW
0004DDH	Peripheral Resource Relocation Register 7	PRRR7		RW
0004DEH	Peripheral Resource Relocation Register 8	PRRR8		RW
0004DFH	Peripheral Resource Relocation Register 9	PRRR9		RW
0004E0H	RTC - Sub Second Register L	WTBRL0	WTBR0	RW
0004E1H	RTC - Sub Second Register M	WTBRH0		RW
0004E2H	RTC - Sub-Second Register H	WTBR1		RW
0004E3H	RTC - Second Register	WTSR		RW
0004E4H	RTC - Minutes	WTMR		RW
0004E5H	RTC - Hour	WTHR		RW
0004E6H	RTC - Timer Control Extended Register	WTCER		RW
0004E7H	RTC - Clock select register	WTCKSR		RW
0004E8H	RTC - Timer Control Register Low	WTCRL	WTCR	RW
0004E9H	RTC - Timer Control Register High	WTCRH		RW

I/O map MB96(F)33x (22 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004EAH	CAL - Calibration unit Control register	CUCR		RW
0004EBH	Reserved			-
0004ECH	CAL - Duration Timer Data Register Low	CUTDL	CUTD	RW
0004EDH	CAL - Duration Timer Data Register High	CUTDH		RW
0004EEH	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EFH	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2H-0004F9H	Reserved			-
0004FAH	RLT - Timer input select (for Cascading)	TMISR		RW
0004FBH-0004FFH	Reserved			-
000500H	FRT2 - Data register of free-running timer		TCDT2	RW
000501H	FRT2 - Data register of free-running timer			RW
000502H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	RW
000503H	FRT2 - Control status register of free-running timer High	TCCSH2		RW
000504H	FRT3 - Data register of free-running timer		TCDT3	RW
000505H	FRT3 - Data register of free-running timer			RW
000506H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	RW
000507H	FRT3 - Control status register of free-running timer High	TCCSH3		RW
000508H	OCU8 - Output Compare Control Status	OCS8		RW
000509H	OCU9 - Output Compare Control Status	OCS9		RW
00050AH	OCU8 - Compare Register		OCCP8	RW
00050BH	OCU8 - Compare Register			RW
00050CH	OCU9 - Compare Register		OCCP9	RW
00050DH	OCU9 - Compare Register			RW
00050EH	OCU10 - Output Compare Control Status	OCS10		RW

I/O map MB96(F)33x (23 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00050FH	OCU11 - Output Compare Control Status	OCS11		RW
000510H	OCU10 - Compare Register		OCCP10	RW
000511H	OCU10 - Compare Register			RW
000512H	OCU11 - Compare Register		OCCP11	RW
000513H	OCU11 - Compare Register			RW
000514H	ICU8/ICU9 - Control Status Register	ICS89		RW
000515H	ICU8/ICU9 - Edge Register	ICE89		RW
000516H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517H	ICU8 - Capture Register High	IPCPH8		R
000518H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519H	ICU9 - Capture Register High	IPCPH9		R
00051AH-000529H	Reserved			-
00052AH	USART5 - Serial Mode Register	SMR5		RW
00052BH	USART5 - Serial Control Register	SCR5		RW
00052CH	USART5 - RX Register	TDR5		W
00052CH	USART5 - TX Register	RDR5		R
00052DH	USART5 - Serial Status	SSR5		RW
00052EH	USART5 - Control/Com. Register	ECCR5		RW
00052FH	USART5 - Ext. Status Register	ESCR5		RW
000530H	USART5 - Baud Rate Generator Register Low	BGRL5	BGR5	RW
000531H	USART5 - Baud Rate Generator Register High	BGRH5		RW
000532H	USART5 - Extended Serial Interrupt Register	ESIR5		RW
000533H-00053DH	Reserved			-
00053EH	USART7 - Serial Mode Register	SMR7		RW
00053FH	USART7 - Serial Control Register	SCR7		RW
000540H	USART7 - Serial TX Register	TDR7		W
000540H	USART7 - Serial RX Register	RDR7		R
000541H	USART7 - Serial Status Register	SSR7		RW
000542H	USART7 - Ext. Control/Com. Register	ECCR7		RW

I/O map MB96(F)33x (24 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000543H	USART7 - Ext. Status Com. Register	ESCR7		RW
000544H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	RW
000545H	USART7 - Baud Rate Generator Register High	BGRH7		RW
000546H	USART7 - Extended Serial Interrupt Register	ESIR7		RW
000547H	Reserved			-
000548H	USART8 - Serial Mode Register	SMR8		RW
000549H	USART8 - Serial Control Register	SCR8		RW
00054AH	USART8 - Serial TX Register	TDR8		W
00054AH	USART8 - Serial RX Register	RDR8		R
00054BH	USART8 - Serial Status Register	SSR8		RW
00054CH	USART8 - Ext. Control/Com. Register	ECCR8		RW
00054DH	USART8 - Ext. Status Com. Register	ESCR8		RW
00054EH	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	RW
00054FH	USART8 - Baud Rate Generator Register High	BGRH8		RW
000550H	USART8 - Extended Serial Interrupt Register	ESIR8		RW
000551H	Reserved			-
000552H	USART9 - Serial Mode Register	SMR9		RW
000553H	USART9 - Serial Control Register	SCR9		RW
000554H	USART9 - Serial TX Register	TDR9		W
000554H	USART9 - Serial RX Register	RDR9		R
000555H	USART9 - Serial Status Register	SSR9		RW
000556H	USART9 - Ext. Control/Com. Register	ECCR9		RW
000557H	USART9 - Ext. Status Com. Register	ESCR9		RW
000558H	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	RW
000559H	USART9 - Baud Rate Generator Register High	BGRH9		RW
00055AH	USART9 - Extended Serial Interrupt Register	ESIR9		RW
00055BH-00055FH	Reserved			-
000560H	ALARM0 - Control Status Register	ACSR0		RW
000561H	ALARM0 - Extended Control Status Register	AECSR0		RW

I/O map MB96(F)33x (25 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000562H	ALARM1 - Control Status Register	ACSR1		RW
000563H	ALARM1 - Extended Control Status Register	AECSR1		RW
000564H	PPG6 - Timer register		PTMR6	R
000565H	PPG6 - Timer register			R
000566H	PPG6 - Period setting register		PCSR6	W
000567H	PPG6 - Period setting register			W
000568H	PPG6 - Duty cycle register		PDUT6	W
000569H	PPG6 - Duty cycle register			W
00056AH	PPG6 - Control status register Low	PCNL6	PCN6	RW
00056BH	PPG6 - Control status register High	PCNH6		RW
00056CH	PPG7 - Timer register		PTMR7	R
00056DH	PPG7 - Timer register			R
00056EH	PPG7 - Period setting register		PCSR7	W
00056FH	PPG7 - Period setting register			W
000570H	PPG7 - Duty cycle register		PDUT7	W
000571H	PPG7 - Duty cycle register			W
000572H	PPG7 - Control status register Low	PCNL7	PCN7	RW
000573H	PPG7 - Control status register High	PCNH7		RW
000574H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	RW
000575H	PPG11-PPG8 - General Control register 1 High	GCN1H2		RW
000576H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	RW
000577H	PPG11-PPG8 - General Control register 2 High	GCN2H2		RW
000578H	PPG8 - Timer register		PTMR8	R
000579H	PPG8 - Timer register			R
00057AH	PPG8 - Period setting register		PCSR8	W
00057BH	PPG8 - Period setting register			W
00057CH	PPG8 - Duty cycle register		PDUT8	W
00057DH	PPG8 - Duty cycle register			W
00057EH	PPG8 - Control status register Low	PCNL8	PCN8	RW
00057FH	PPG8 - Control status register High	PCNH8		RW

I/O map MB96(F)33x (26 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000580H	PPG9 - Timer register		PTMR9	R
000581H	PPG9 - Timer register			R
000582H	PPG9 - Period setting register		PCSR9	W
000583H	PPG9 - Period setting register			W
000584H	PPG9 - Duty cycle register		PDUT9	W
000585H	PPG9 - Duty cycle register			W
000586H	PPG9 - Control status register Low	PCNL9	PCN9	RW
000587H	PPG9 - Control status register High	PCNH9		RW
000588H	PPG10 - Timer register		PTMR10	R
000589H	PPG10 - Timer register			R
00058AH	PPG10 - Period setting register		PCSR10	W
00058BH	PPG10 - Period setting register			W
00058CH	PPG10 - Duty cycle register		PDUT10	W
00058DH	PPG10 - Duty cycle register			W
00058EH	PPG10 - Control status register Low	PCNL10	PCN10	RW
00058FH	PPG10 - Control status register High	PCNH10		RW
000590H	PPG11 - Timer register		PTMR11	R
000591H	PPG11 - Timer register			R
000592H	PPG11 - Period setting register		PCSR11	W
000593H	PPG11 - Period setting register			W
000594H	PPG11 - Duty cycle register		PDUT11	W
000595H	PPG11 - Duty cycle register			W
000596H	PPG11 - Control status register Low	PCNL11	PCN11	RW
000597H	PPG11 - Control status register High	PCNH11		RW
000598H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	RW
000599H	PPG15-PPG12 - General Control register 1 High	GCN1H3		RW
00059AH	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	RW
00059BH	PPG15-PPG12 - General Control register 2 High	GCN2H3		RW
00059CH	PPG12 - Timer register		PTMR12	R
00059DH	PPG12 - Timer register			R

I/O map MB96(F)33x (27 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00059EH	PPG12 - Period setting register		PCSR12	W
00059FH	PPG12 - Period setting register			W
0005A0H	PPG12 - Duty cycle register		PDUT12	W
0005A1H	PPG12 - Duty cycle register			W
0005A2H	PPG12 - Control status register Low	PCNL12	PCN12	RW
0005A3H	PPG12 - Control status register High	PCNH12		RW
0005A4H	PPG13 - Timer register		PTMR13	R
0005A5H	PPG13 - Timer register			R
0005A6H	PPG13 - Period setting register		PCSR13	W
0005A7H	PPG13 - Period setting register			W
0005A8H	PPG13 - Duty cycle register		PDUT13	W
0005A9H	PPG13 - Duty cycle register			W
0005AAH	PPG13 - Control status register Low	PCNL13	PCN13	RW
0005ABH	PPG13 - Control status register High	PCNH13		RW
0005ACH	PPG14 - Timer register		PTMR14	R
0005ADH	PPG14 - Timer register			R
0005AEH	PPG14 - Period setting register		PCSR14	W
0005AFH	PPG14 - Period setting register			W
0005B0H	PPG14 - Duty cycle register		PDUT14	W
0005B1H	PPG14 - Duty cycle register			W
0005B2H	PPG14 - Control status register Low	PCNL14	PCN14	RW
0005B3H	PPG14 - Control status register High	PCNH14		RW
0005B4H	PPG15 - Timer register		PTMR15	R
0005B5H	PPG15 - Timer register			R
0005B6H	PPG15 - Period setting register		PCSR15	W
0005B7H	PPG15 - Period setting register			W
0005B8H	PPG15 - Duty cycle register		PDUT15	W
0005B9H	PPG15 - Duty cycle register			W
0005BAH	PPG15 - Control status register Low	PCNL15	PCN15	RW
0005BBH	PPG15 - Control status register High	PCNH15		RW

I/O map MB96(F)33x (28 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005BCH	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	RW
0005BDH	PPG19-PPG16 - General Control register 1 High	GCN1H4		RW
0005BEH	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	RW
0005BFH	PPG19-PPG16 - General Control register 2 High	GCN2H4		RW
0005C0H	PPG16 - Timer register		PTMR16	R
0005C1H	PPG16 - Timer register			R
0005C2H	PPG16 - Period setting register		PCSR16	W
0005C3H	PPG16 - Period setting register			W
0005C4H	PPG16 - Duty cycle register		PDUT16	W
0005C5H	PPG16 - Duty cycle register			W
0005C6H	PPG16 - Control status register Low	PCNL16	PCN16	RW
0005C7H	PPG16 - Control status register High	PCNH16		RW
0005C8H	PPG17 - Timer register		PTMR17	R
0005C9H	PPG17 - Timer register			R
0005CAH	PPG17 - Period setting register		PCSR17	W
0005CBH	PPG17 - Period setting register			W
0005CCH	PPG17 - Duty cycle register		PDUT17	W
0005CDH	PPG17 - Duty cycle register			W
0005CEH	PPG17 - Control status register Low	PCNL17	PCN17	RW
0005CFH	PPG17 - Control status register High	PCNH17		RW
0005D0H	PPG18 - Timer register		PTMR18	R
0005D1H	PPG18 - Timer register			R
0005D2H	PPG18 - Period setting register		PCSR18	W
0005D3H	PPG18 - Period setting register			W
0005D4H	PPG18 - Duty cycle register		PDUT18	W
0005D5H	PPG18 - Duty cycle register			W
0005D6H	PPG18 - Control status register Low	PCNL18	PCN18	RW
0005D7H	PPG18 - Control status register High	PCNH18		RW
0005D8H	PPG19 - Timer register		PTMR19	R
0005D9H	PPG19 - Timer register			R

I/O map MB96(F)33x (29 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005DAH	PPG19 - Period setting register		PCSR19	W
0005DBH	PPG19 - Period setting register			W
0005DCH	PPG19 - Duty cycle register		PDUT19	W
0005DDH	PPG19 - Duty cycle register			W
0005DEH	PPG19 - Control status register Low	PCNL19	PCN19	RW
0005DFH	PPG19 - Control status register High	PCNH19		RW
0005E0H-00065FH	Reserved			-
000660H	Peripheral Resource Relocation Register 10	PRRR10		RW
000661H	Peripheral Resource Relocation Register 11	PRRR11		RW
000662H	Peripheral Resource Relocation Register 12	PRRR12		RW
000663H	Peripheral Resource Relocation Register 13	PRRR13		W
000664H-00069FH	Reserved			-
0006A0H	USB - Host Control register Low	HCNTL0	HCNT0	RW
0006A1H	USB - Host Control register High	HCNTH0		RW
0006A2H	USB - Host Interrupt Register	HIRQ0		RW
0006A3H	USB - Host Error Status Register	HERR0		RW
0006A4H	USB - Host State Status Register	HSTATE0		RW
0006A5H	USB - Host SOF Int. Frame Compare Register	HFCOMP0		RW
0006A6H	USB - Host Retry Timer Setting Register Low	HRTIMERL0		RW
0006A7H	USB - Host Retry Timer Setting Register Middle	HRTIMERM0		RW
0006A8H	USB - Host Retry Timer Setting Register High	HRTIMERH0		RW
0006A9H	USB - Host Address Register	HADR0		RW
0006AAH	USB - Host EOF Setting Register Low	HEOFL0	HEOF0	RW
0006ABH	USB - Host EOF Setting Register High	HEOFH0		RW
0006ACH	USB - Host Frame Register Low	HFRAMEL0	HFRAME0	RW
0006ADH	USB - Host Frame Register High	HFRAMEH0		RW
0006AEH	USB - Host Token End Point Register	HTOKEN0		RW
0006AFH	Reserved			-
0006B0H	USB - UDC Control Register	UDCC0		RW

I/O map MB96(F)33x (30 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006B1H	Reserved			-
0006B2H	USB - EP0 Control Register Low	EP0CL0	EP0C0	RW
0006B3H	USB - EP0 Control Register High	EP0CH0		RW
0006B4H	USB - EP1 Control Register Low	EP1CL0	EP1C0	RW
0006B5H	USB - EP1 Control Register High - non public	EP1CH0		RW
0006B6H	USB - EP2 Control Register Low	EP2CL0	EP2C0	RW
0006B7H	USB - EP2 Control Register High	EP2CH0		RW
0006B8H	USB - EP3 Control Register Low	EP3CL0	EP3C0	RW
0006B9H	USB - EP3 Control Register High	EP3CH0		RW
0006BAH	USB - EP4 Control Register Low	EP4CL0	EP4C0	RW
0006BBH	USB - EP4 Control Register High	EP4CH0		RW
0006BCH	USB - EP5 Control Register Low	EP5CL0	EP5C0	RW
0006BDH	USB - EP5 Control Register High	EP5CH0		RW
0006BEH	USB - Timer Stamp Register Low	TMSPL0	TMSP0	RW
0006BFH	USB - Timer Stamp Register High	TMSPH0		RW
0006C0H	USB - UDC Status Register	UDCS0		RW
0006C1H	USB - UDC Interrupt Enable Register	UDCIE0		RW
0006C2H	USB - EP0I Status Register Low	EP0ISL0	EP0IS0	W
0006C3H	USB - EP0I Status Register High	EP0ISH0		RW
0006C4H	USB - EP0O Status Register Low	EP0OSL0	EP0OS0	RW
0006C5H	USB - EP0O Status Register High	EP0OSH0		RW
0006C6H	USB - EP1 Status Register Low	EP1SL0	EP1S0	RW
0006C7H	USB - EP1 Status Register High	EP1SH0		RW
0006C8H	USB - EP2 Status Register Low	EP2SL0	EP2S0	RW
0006C9H	USB - EP2 Status Register High	EP2SH0		RW
0006CAH	USB - EP3 Status Register Low	EP3SL0	EP3S0	RW
0006CBH	USB - EP3 Status Register High	EP3SH0		RW
0006CCH	USB - EP4 Status Register Low	EP4SL0	EP4S0	RW
0006CDH	USB - EP4 Status Register High	EP4SH0		RW
0006CEH	USB - EP5 Status Register Low	EP5SL0	EP5S0	RW

I/O map MB96(F)33x (31 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006CFH	USB - EP5 Status Register High	EP5SH0		RW
0006D0H	USB - EP0 Data register Low	EP0DTL0	EP0DT0	RW
0006D1H	USB - EP0 Data register High	EP0DTH0		RW
0006D2H	USB - EP1 Data register Low	EP1DTL0	EP1DT0	RW
0006D3H	USB - EP1 Data register High	EP1DTH0		RW
0006D4H	USB - EP2 Data register Low	EP2DTL0	EP2DT0	RW
0006D5H	USB - EP2 Data register High	EP2DTH0		RW
0006D6H	USB - EP3 Data register Low	EP3DTL0	EP3DT0	RW
0006D7H	USB - EP3 Data register High	EP3DTH0		RW
0006D8H	USB - EP4 Data register Low	EP4DTL0	EP4DT0	RW
0006D9H	USB - EP4 Data register High	EP4DTH0		RW
0006DAH	USB - EP5 Data register Low	EP5DTL0	EP5DT0	RW
0006DBH	USB - EP5 Data register High	EP5DTH0		RW
0006DCH-0006DFH	Reserved			-
0006E0H	External Bus - Area configuration register 0 Low	EACL0	EAC0	RW
0006E1H	External Bus - Area configuration register 0 High	EACH0		RW
0006E2H	External Bus - Area configuration register 1 Low	EACL1	EAC1	RW
0006E3H	External Bus - Area configuration register 1 High	EACH1		RW
0006E4H	External Bus - Area configuration register 2 Low	EACL2	EAC2	RW
0006E5H	External Bus - Area configuration register 2 High	EACH2		RW
0006E6H	External Bus - Area configuration register 3 Low	EACL3	EAC3	RW
0006E7H	External Bus - Area configuration register 3 High	EACH3		RW
0006E8H	External Bus - Area configuration register 4 Low	EACL4	EAC4	RW
0006E9H	External Bus - Area configuration register 4 High	EACH4		RW
0006EAH	External Bus - Area configuration register 5 Low	EACL5	EAC5	RW
0006EBH	External Bus - Area configuration register 5 High	EACH5		RW
0006ECH	External Bus - Area select register 2	EAS2		RW
0006EDH	External Bus - Area select register 3	EAS3		RW
0006EEH	External Bus - Area select register 4	EAS4		RW

I/O map MB96(F)33x (32 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006EFH	External Bus - Area select register 5	EAS5		RW
0006F0H	External Bus - Mode register	EBM		RW
0006F1H	External Bus - Clock and Function register	EBCF		RW
0006F2H	External Bus - Address output enable register 0	EBAE0		RW
0006F3H	External Bus - Address output enable register 1	EBAE1		RW
0006F4H	External Bus - Address output enable register 2	EBAE2		RW
0006F5H	External Bus - Control signal register	EBCS		RW
0006F6H-0006FFH	Reserved			-
000700H	CAN0 - Control register Low	CTRLRL0	CTRLR0	RW
000701H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702H	CAN0 - Status register Low	STATRL0	STATR0	RW
000703H	CAN0 - Status register High (reserved)	STATRH0		R
000704H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	RW
000707H	CAN0 - Bit Timing Register High	BTRH0		RW
000708H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709H	CAN0 - Interrupt Register High	INTRH0		R
00070AH	CAN0 - Test Register Low	TESTRL0	TESTR0	RW
00070BH	CAN0 - Test Register High (reserved)	TESTRH0		R
00070CH	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	RW
00070DH	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070EH-00070FH	Reserved			-
000710H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	RW
000711H	CAN0 - IF1 Command request register High	IF1CREQH0		RW
000712H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	RW
000713H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	RW

I/O map MB96(F)33x (33 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000715H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		RW
000716H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	RW
000717H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		RW
000718H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	RW
000719H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		RW
00071AH	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	RW
00071BH	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		RW
00071CH	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	RW
00071DH	CAN0 - IF1 Message Control Register High	IF1MCTRH0		RW
00071EH	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	RW
00071FH	CAN0 - IF1 Data A1 High	IF1DTA1H0		RW
000720H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	RW
000721H	CAN0 - IF1 Data A2 High	IF1DTA2H0		RW
000722H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	RW
000723H	CAN0 - IF1 Data B1 High	IF1DTB1H0		RW
000724H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	RW
000725H	CAN0 - IF1 Data B2 High	IF1DTB2H0		RW
000726H-00073FH	Reserved			-
000740H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	RW
000741H	CAN0 - IF2 Command request register High	IF2CREQH0		RW
000742H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	RW
000743H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	RW
000745H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		RW
000746H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	RW
000747H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		RW
000748H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	RW
000749H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		RW
00074AH	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	RW

I/O map MB96(F)33x (34 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00074BH	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		RW
00074CH	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	RW
00074DH	CAN0 - IF2 Message Control Register High	IF2MCTRH0		RW
00074EH	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	RW
00074FH	CAN0 - IF2 Data A1 High	IF2DTA1H0		RW
000750H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	RW
000751H	CAN0 - IF2 Data A2 High	IF2DTA2H0		RW
000752H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	RW
000753H	CAN0 - IF2 Data B1 High	IF2DTB1H0		RW
000754H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	RW
000755H	CAN0 - IF2 Data B2 High	IF2DTB2H0		RW
000756H-00077FH	Reserved			-
000780H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784H-00078FH	Reserved			-
000790H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794H-00079FH	Reserved			-
0007A0H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
0007A4H-0007AFH	Reserved			-

I/O map MB96(F)33x (35 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0007B0H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1H	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
0007B2H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3H	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
0007B4H-0007CDH	Reserved			-
0007CEH	CAN0 - Output enable register	COER0		RW
0007CFH-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	RW
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	RW
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	RW
000807H	CAN1 - Bit Timing Register High	BTRH1		RW
000808H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809H	CAN1 - Interrupt Register High	INTRH1		R
00080AH	CAN1 - Test Register Low	TESTRL1	TESTR1	RW
00080BH	CAN1 - Test Register High (reserved)	TESTRH1		R
00080CH	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	RW
00080DH	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080EH-00080FH	Reserved			-
000810H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	RW
000811H	CAN1 - IF1 Command request register High	IF1CREQH1		RW
000812H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	RW
000813H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	RW

I/O map MB96(F)33x (36 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000815H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		RW
000816H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	RW
000817H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		RW
000818H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	RW
000819H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		RW
00081AH	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	RW
00081BH	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		RW
00081CH	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	RW
00081DH	CAN1 - IF1 Message Control Register High	IF1MCTRH1		RW
00081EH	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	RW
00081FH	CAN1 - IF1 Data A1 High	IF1DTA1H1		RW
000820H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	RW
000821H	CAN1 - IF1 Data A2 High	IF1DTA2H1		RW
000822H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	RW
000823H	CAN1 - IF1 Data B1 High	IF1DTB1H1		RW
000824H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	RW
000825H	CAN1 - IF1 Data B2 High	IF1DTB2H1		RW
000826H-00083FH	Reserved			-
000840H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	RW
000841H	CAN1 - IF2 Command request register High	IF2CREQH1		RW
000842H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	RW
000843H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	RW
000845H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		RW
000846H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	RW
000847H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		RW
000848H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	RW
000849H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		RW
00084AH	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	RW

I/O map MB96(F)33x (37 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00084BH	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		RW
00084CH	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	RW
00084DH	CAN1 - IF2 Message Control Register High	IF2MCTRH1		RW
00084EH	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	RW
00084FH	CAN1 - IF2 Data A1 High	IF2DTA1H1		RW
000850H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	RW
000851H	CAN1 - IF2 Data A2 High	IF2DTA2H1		RW
000852H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	RW
000853H	CAN1 - IF2 Data B1 High	IF2DTB1H1		RW
000854H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	RW
000855H	CAN1 - IF2 Data B2 High	IF2DTB2H1		RW
000856H-00087FH	Reserved			-
000880H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884H-00088FH	Reserved			-
000890H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894H-00089FH	Reserved			-
0008A0H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4H-0008AFH	Reserved			-

I/O map MB96(F)33x (38 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0008B0H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4H-0008CDH	Reserved			-
0008CEH	CAN1 - Output enable register	COER1		RW
0008CFH-0008FFH	Reserved			-
000900H	CAN2 - Control register Low	CTRLRL2	CTRLR2	RW
000901H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902H	CAN2 - Status register Low	STATRL2	STATR2	RW
000903H	CAN2 - Status register High (reserved)	STATRH2		R
000904H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	RW
000907H	CAN2 - Bit Timing Register High	BTRH2		RW
000908H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909H	CAN2 - Interrupt Register High	INTRH2		R
00090AH	CAN2 - Test Register Low	TESTRL2	TESTR2	RW
00090BH	CAN2 - Test Register High (reserved)	TESTRH2		R
00090CH	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	RW
00090DH	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090EH-00090FH	Reserved			-
000910H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	RW
000911H	CAN2 - IF1 Command request register High	IF1CREQH2		RW
000912H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	RW
000913H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	RW

I/O map MB96(F)33x (39 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000915H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		RW
000916H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	RW
000917H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		RW
000918H	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	RW
000919H	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		RW
00091AH	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	RW
00091BH	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		RW
00091CH	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	RW
00091DH	CAN2 - IF1 Message Control Register High	IF1MCTRH2		RW
00091EH	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	RW
00091FH	CAN2 - IF1 Data A1 High	IF1DTA1H2		RW
000920H	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	RW
000921H	CAN2 - IF1 Data A2 High	IF1DTA2H2		RW
000922H	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	RW
000923H	CAN2 - IF1 Data B1 High	IF1DTB1H2		RW
000924H	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	RW
000925H	CAN2 - IF1 Data B2 High	IF1DTB2H2		RW
000926H-00093FH	Reserved			-
000940H	CAN2 - IF2 Command request register Low	IF2CREQL2	IF2CREQ2	RW
000941H	CAN2 - IF2 Command request register High	IF2CREQH2		RW
000942H	CAN2 - IF2 Command Mask register Low	IF2CMSKL2	IF2CMSK2	RW
000943H	CAN2 - IF2 Command Mask register High (reserved)	IF2CMSKH2		R
000944H	CAN2 - IF2 Mask 1 Register Low	IF2MSK1L2	IF2MSK12	RW
000945H	CAN2 - IF2 Mask 1 Register High	IF2MSK1H2		RW
000946H	CAN2 - IF2 Mask 2 Register Low	IF2MSK2L2	IF2MSK22	RW
000947H	CAN2 - IF2 Mask 2 Register High	IF2MSK2H2		RW
000948H	CAN2 - IF2 Arbitration 1 Register Low	IF2ARB1L2	IF2ARB12	RW
000949H	CAN2 - IF2 Arbitration 1 Register High	IF2ARB1H2		RW
00094AH	CAN2 - IF2 Arbitration 2 Register Low	IF2ARB2L2	IF2ARB22	RW

I/O map MB96(F)33x (40 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00094BH	CAN2 - IF2 Arbitration 2 Register High	IF2ARB2H2		RW
00094CH	CAN2 - IF2 Message Control Register Low	IF2MCTRL2	IF2MCTR2	RW
00094DH	CAN2 - IF2 Message Control Register High	IF2MCTRH2		RW
00094EH	CAN2 - IF2 Data A1 Low	IF2DTA1L2	IF2DTA12	RW
00094FH	CAN2 - IF2 Data A1 High	IF2DTA1H2		RW
000950H	CAN2 - IF2 Data A2 Low	IF2DTA2L2	IF2DTA22	RW
000951H	CAN2 - IF2 Data A2 High	IF2DTA2H2		RW
000952H	CAN2 - IF2 Data B1 Low	IF2DTB1L2	IF2DTB12	RW
000953H	CAN2 - IF2 Data B1 High	IF2DTB1H2		RW
000954H	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	RW
000955H	CAN2 - IF2 Data B2 High	IF2DTB2H2		RW
000956H-00097FH	Reserved			-
000980H	CAN2 - Transmission Request 1 Register Low	TREQR1L2	TREQR12	R
000981H	CAN2 - Transmission Request 1 Register High	TREQR1H2		R
000982H	CAN2 - Transmission Request 2 Register Low	TREQR2L2	TREQR22	R
000983H	CAN2 - Transmission Request 2 Register High	TREQR2H2		R
000984H-00098FH	Reserved			-
000990H	CAN2 - New Data 1 Register Low	NEWDT1L2	NEWDT12	R
000991H	CAN2 - New Data 1 Register High	NEWDT1H2		R
000992H	CAN2 - New Data 2 Register Low	NEWDT2L2	NEWDT22	R
000993H	CAN2 - New Data 2 Register High	NEWDT2H2		R
000994H-00099FH	Reserved			-
0009A0H	CAN2 - Interrupt Pending 1 Register Low	INTPND1L2	INTPND12	R
0009A1H	CAN2 - Interrupt Pending 1 Register High	INTPND1H2		R
0009A2H	CAN2 - Interrupt Pending 2 Register Low	INTPND2L2	INTPND22	R
0009A3H	CAN2 - Interrupt Pending 2 Register High	INTPND2H2		R
0009A4H-0009AFH	Reserved			-

I/O map MB96(F)33x (41 / 41)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0009B0H	CAN2 - Message Valid 1 Register Low	MSGVAL1L2	MSGVAL12	R
0009B1H	CAN2 - Message Valid 1 Register High	MSGVAL1H2		R
0009B2H	CAN2 - Message Valid 2 Register Low	MSGVAL2L2	MSGVAL22	R
0009B3H	CAN2 - Message Valid 2 Register High	MSGVAL2H2		R
0009B4H-0009CDH	Reserved			-
0009CEH	CAN2 - Output enable register	COER2		RW
0009CFH-000BFFH	Reserved			-

■ INTERRUPT VECTOR TABLE

▐ Interrupt vector table MB96(F)33x (1 / 5)

Vector number	Offset in vector ta-ble	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC	CALLV0	No	-	
1	3F8	CALLV1	No	-	
2	3F4	CALLV2	No	-	
3	3F0	CALLV3	No	-	
4	3EC	CALLV4	No	-	
5	3E8	CALLV5	No	-	
6	3E4	CALLV6	No	-	
7	3E0	CALLV7	No	-	
8	3DC	RESET	No	-	
9	3D8	INT9	No	-	
10	3D4	EXCEPTION	No	-	
11	3D0	NMI	No	-	Non-Maskable Interrupt
12	3CC	DLY	No	12	Delayed Interrupt
13	3C8	RC_TIMER	No	13	RC Timer
14	3C4	MC_TIMER	No	14	Main Clock Timer
15	3C0	SC_TIMER	No	15	Sub Clock Timer
16	3BC	PLL_UNLOCK	No	16	Reserved
17	3B8	EXTINT0	Yes	17	External Interrupt 0
18	3B4	EXTINT1	Yes	18	External Interrupt 1
19	3B0	EXTINT2	Yes	19	External Interrupt 2
20	3AC	EXTINT3	Yes	20	External Interrupt 3
21	3A8	EXTINT4	Yes	21	External Interrupt 4
22	3A4	EXTINT5	Yes	22	External Interrupt 5
23	3A0	EXTINT6	Yes	23	External Interrupt 6
24	39C	EXTINT7	Yes	24	External Interrupt 7
25	398	EXTINT8	Yes	25	External Interrupt 8
26	394	EXTINT9	Yes	26	External Interrupt 9
27	390	EXTINT10	Yes	27	External Interrupt 10

Interrupt vector table MB96(F)33x (2 / 5)

Vector number	Offset in vector ta- ble	Vector name	Cleared by DMA	Index in ICR to program	Description
28	38C	EXTINT11	Yes	28	External Interrupt 11
29	388	EXTINT12	Yes	29	External Interrupt 12
30	384	EXTINT13	Yes	30	External Interrupt 13
31	380	EXTINT14	Yes	31	External Interrupt 14
32	37C	EXTINT15	Yes	32	External Interrupt 15
33	378	CAN0	No	33	CAN Controller 0
34	374	CAN1	No	34	CAN Controller 1
35	370	CAN2	No	35	CAN Controller 2
36	36C	PPG0	Yes	36	Programmable Pulse Generator 0
37	368	PPG1	Yes	37	Programmable Pulse Generator 1
38	364	PPG2	Yes	38	Programmable Pulse Generator 2
39	360	PPG3	Yes	39	Programmable Pulse Generator 3
40	35C	PPG4	Yes	40	Programmable Pulse Generator 4
41	358	PPG5	Yes	41	Programmable Pulse Generator 5
42	354	PPG6	Yes	42	Programmable Pulse Generator 6
43	350	PPG7	Yes	43	Programmable Pulse Generator 7
44	34C	PPG8	Yes	44	Programmable Pulse Generator 8
45	348	PPG9	Yes	45	Programmable Pulse Generator 9
46	344	PPG10	Yes	46	Programmable Pulse Generator 10
47	340	PPG11	Yes	47	Programmable Pulse Generator 11
48	33C	PPG12	Yes	48	Programmable Pulse Generator 12
49	338	PPG13	Yes	49	Programmable Pulse Generator 13
50	334	PPG14	Yes	50	Programmable Pulse Generator 14
51	330	PPG15	Yes	51	Programmable Pulse Generator 15
52	32C	PPG16	Yes	52	Programmable Pulse Generator 16
53	328	PPG17	Yes	53	Programmable Pulse Generator 17
54	324	PPG18	Yes	54	Programmable Pulse Generator 18
55	320	PPG19	Yes	55	Programmable Pulse Generator 19
56	31C	RLT0	Yes	56	Reload Timer 0

Interrupt vector table MB96(F)33x (3 / 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
57	318	RLT1	Yes	57	Reload Timer 1
58	314	RLT2	Yes	58	Reload Timer 2
59	310	RLT3	Yes	59	Reload Timer 3
60	30C	PPGRLT	Yes	60	Reload Timer 6 - dedicated for PPG
61	308	ICU0	Yes	61	Input Capture Unit 0
62	304	ICU1	Yes	62	Input Capture Unit 1
63	300	ICU2	Yes	63	Input Capture Unit 2
64	2FC	ICU3	Yes	64	Input Capture Unit 3
65	2F8	ICU4	Yes	65	Input Capture Unit 4
66	2F4	ICU5	Yes	66	Input Capture Unit 5
67	2F0	ICU6	Yes	67	Input Capture Unit 6
68	2EC	ICU7	Yes	68	Input Capture Unit 7
69	2E8	ICU8	Yes	69	Input Capture Unit 8
70	2E4	ICU9	Yes	70	Input Capture Unit 9
71	2E0	OCU0	Yes	71	Output Compare Unit 0
72	2DC	OCU1	Yes	72	Output Compare Unit 1
73	2D8	OCU2	Yes	73	Output Compare Unit 2
74	2D4	OCU3	Yes	74	Output Compare Unit 3
75	2D0	OCU4	Yes	75	Output Compare Unit 4
76	2CC	OCU5	Yes	76	Output Compare Unit 5
77	2C8	OCU6	Yes	77	Output Compare Unit 6
78	2C4	OCU7	Yes	78	Output Compare Unit 7
79	2C0	OCU8	Yes	79	Output Compare Unit 8
80	2BC	OCU9	Yes	80	Output Compare Unit 9
81	2B8	OCU10	Yes	81	Output Compare Unit 10
82	2B4	OCU11	Yes	82	Output Compare Unit 11
83	2B0	FRT0	Yes	83	Free Running Timer 0
84	2AC	FRT1	Yes	84	Free Running Timer 1
85	2A8	FRT2	Yes	85	Free Running Timer 2

Interrupt vector table MB96(F)33x (4 / 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
86	2A4	FRT3	Yes	86	Free Running Timer 3
87	2A0	RTC0	No	87	Real Timer Clock
88	29C	CAL0	No	88	Clock Calibration Unit
89	298	IIC0	Yes	89	I2C interface
90	294	IIC1	Yes	90	I2C interface
91	290	ADC0	Yes	91	A/D Converter
92	28C	ALARM0	No	92	Alarm Comparator 0
93	288	ALARM1	No	93	Alarm Comparator 1
94	284	LINR0	Yes	94	LIN USART 0 RX
95	280	LINT0	Yes	95	LIN USART 0 TX
96	27C	LINR1	Yes	96	LIN USART 1 RX
97	278	LINT1	Yes	97	LIN USART 1 TX
98	274	LINR2	Yes	98	LIN USART 2 RX
99	270	LINT2	Yes	99	LIN USART 2 TX
100	26C	LINR3	Yes	100	LIN USART 3 RX
101	268	LINT3	Yes	101	LIN USART 3 TX
102	264	LINR5	Yes	102	LIN USART 5 RX
103	260	LINT5	Yes	103	LIN USART 5 TX
104	25C	LINR7	Yes	104	LIN USART 7 RX
105	258	LINT7	Yes	105	LIN USART 7 TX
106	254	LINR8	Yes	106	LIN USART 8 RX
107	250	LINT8	Yes	107	LIN USART 8 TX
108	24C	LINR9	Yes	108	LIN USART 9 RX
109	248	LINT9	Yes	109	LIN USART 9 TX
110	244	FLASH_A	No	110	Main Flash memory interrupt (only Flash devices)
111	240	reserved	-	-	reserved
112	23C	USB_EP0IN0	Yes	112	USB End point 0 IN
113	238	USB_EP0OUT0	Yes	113	USB End point 0 OUT
114	234	USB_EP10	Yes	114	USB End point 1

Interrupt vector table MB96(F)33x (5 / 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
115	230	USB_EP20	Yes	115	USB End point 2
116	22C	USB_EP30	Yes	116	USB End point 3
117	228	USB_EP40	Yes	117	USB End point 4
118	224	USB_EP50	Yes	118	USB End point 5
119	220	USB_F10	No	119	USB function Flags 1 (SUSP SOF BRST WKUP CONF)
120	21C	USB_F20	No	120	USB function Flags 2 (SPK)
121	218	USB_H10	No	121	USB MiniHost 1 (DIRQ CNNIRQ URIRQ RWKIRQ)
122	214	USB_H20	No	122	USB MiniHost 2 (SOFIRQ CMPIRQ)

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage

1. Latch-up prevention

- CMOS IC chips may suffer latch-up under the following conditions:

  - A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
  - A voltage higher than the rated voltage is applied between V_{CC} and V_{SS}.
  - The AV_{CC} power supply is applied before the V_{CC} voltage.

- Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

- For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Unused pins handling

- Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

- Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

- Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

- The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

  #### 1. Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.
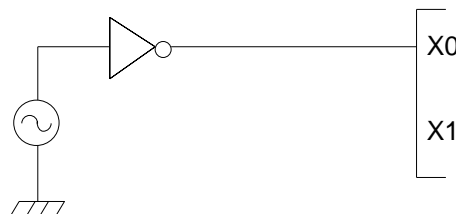
  #### 2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.
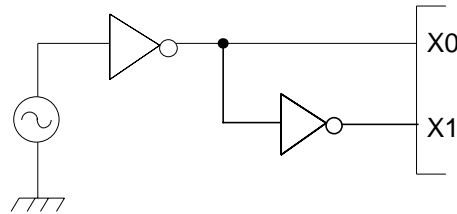
4. Unused sub clock signal
- If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation
- If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V$_{CC}$/V$_{SS}$)
- It is required that all V$_{CC}$-level as well as all V$_{SS}$-level power supply pins are at the same potential. If there is more than one V$_{CC}$ or V$_{SS}$ level, the device may operate incorrectly or be damaged even within the guaranteed operating range.
- V$_{CC}$ and V$_{SS}$ must be connected to the device from the power supply with lowest possible impedance.
- As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V$_{CC}$ and V$_{SS}$ as close as possible to V$_{CC}$ and V$_{SS}$ pins.

7. Crystal oscillator circuit
- Noise at X0 or X1 pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.
- It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.
- It is highly recommended to evaluate the quartz/MCU system at the quartz manufacturer.

8. Turn on sequence of power supply to A/D converter and analog inputs
- It is required to turn the A/D converter power supply (AV$_{CC}$, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V$_{CC}$) on.
- It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV$_{CC}$ (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter
- It is required to connect the unused pins of the A/D converter as AV$_{CC}$ = V$_{CC}$, AV$_{SS}$ = AVRH = AVRL = V$_{SS}$.

10. Notes on energization
- To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50μs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

• If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/μs or less in instantaneous fluctuation for power supply switching.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Parameter	Symbol	Rating Min	Rating Max	Unit	Remarks
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ [*1]
USB power supply voltage	V_{CC3}	V_{SS} - 0.3	V_{SS} + 4.0		USB device only
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC} + 0.3V$ [*2]
USB Input voltage	V_{IUSB}	V_{SS} - 0.3	V_{CC3} + 0.5, 4.0	V	USB pins UDP, UDM
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC} + 0.3V$ [*2]
USB output voltage	V_{OUSB}	V_{SS} - 0.3	V_{CC3} + 0.5, 4.0	V	USB pins UDP, UDM
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins [*3]
Total Maximum Clamp Current	$\Sigma |I_{CLAMP}|$	-	40	mA	Applicable to general purpose I/O pins [*3]
"L" level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
	I_{OLUSB}	-	36	mA	USB pins UDP, UDM
"L" level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
	$I_{OLAVUSB}$	-	15	mA	USB pins UDP, UDM
"L" level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
"L" level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
"H" level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
	I_{OHUSB}	-	-36	mA	USB pins UDP, UDM
"H" level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
	$I_{OHAVUSB}$	-	-15	mA	USB pins UDP, UDM
"H" level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
"H" level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation [*4]	P_D	-	TBD[*5]	mW	

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Operating ambient temperature	T_A	0	+70	°C	MB96V300B
		-40	+105		MB96(F)338
		-40	+125		MB96(F)338Y/R[*6]
Storage temperature	T_{STG}	-55	+150	°C	

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3: • Applicable to all general purpose I/O pins (Pnn_m)
   • Use within recommended operating conditions.
   • Use at DC voltage (current)
   • The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
   • The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
   • Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
   • Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
   • Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

   • Sample recommended circuits:
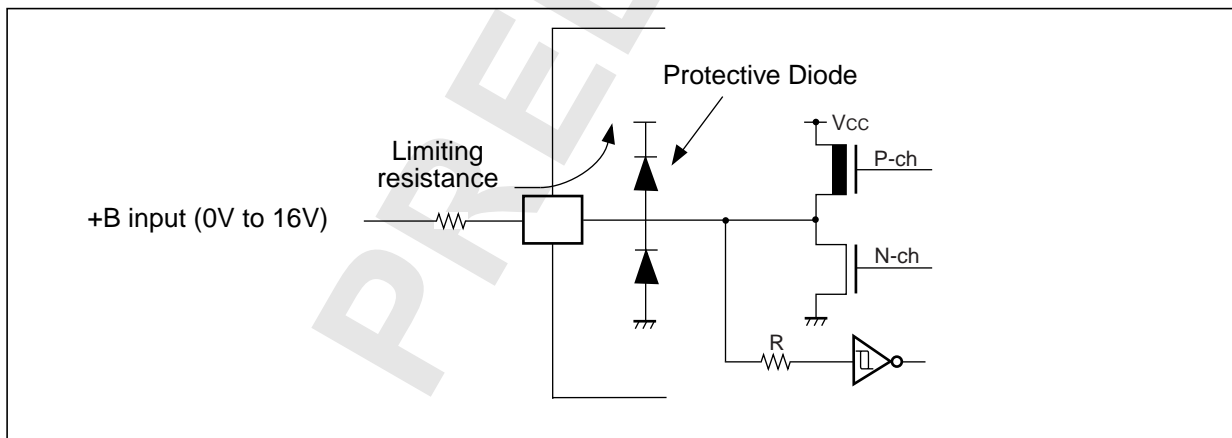
*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
   The actual power dissipation depends on the customer application and can be calculated as follows:
   $P_D = P_{IO} + P_{INT}$
   $P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
   $P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.

I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Fujitsu for reliability limitations when using under these conditions.

2. Recommended Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	4.7	-	10	µF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are guaranteed when the device is operated within these ranges.

Semiconductor devices must always be operated within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC characteristics

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Min	Typ	Max	Unit	Remarks
				Value				
Input "H" voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHUSB}	UDP, UDM	-	2.0	-	V_{CC3} + 0.3	V	USB pins
	V_{IHX0F}	X0	External clock in "Fast Clock Input mode"	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "L" voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILUSB}	UDP, UDM	-	-0.3	-	0.8	V	USB pins
	V_{ILX0F}	X0	External clock in "Fast Clock Input mode"	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	V_{SS} - 0.3	-	0.5	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output "H" voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
			$3.0V \leq V_{CC} < 4.5V$ I_{OH} = -1.6mA					
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -5mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
			$3.0V \leq V_{CC} < 4.5V$ I_{OH} = -3mA					
	V_{OH3}	I²C outputs	$4.5V \leq V_{CC} \leq 5.5V$ I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	
			$3.0V \leq V_{CC} < 4.5V$ I_{OH} = -2mA					
	V_{OHUSB}	UDP, UDM	$3.0V \leq V_{CC3} < 3.6V$ I_{OH} = -100μA	V_{CC3} - 0.2	-	-	V	USB pins

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output "L" voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +2mA / 3.0V ≤ V_{CC} < 4.5V I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +5mA / 3.0V ≤ V_{CC} < 4.5V I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA
	V_{OL3}	I²C outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +3mA / 3.0V ≤ V_{CC} < 4.5V I_{OL} = +2mA	-	-	0.4	V	
	V_{OLUSB}	UDP, UDM	3.0V ≤ V_{CC3} < 3.6V I_{OL} = 100µA	-	-	0.3	V	USB pins
Input leak current	I_{IL}	Pnn_m	V_{CC} = 5.5V V_{SS} < V_I < V_{CC}	-1	-	+1	µA	
		UDP, UDM	V_{CC3} = 3.6V V_{SS} < V_I < V_{CC3}	-5	-	+5	µA	USB pins
Pull-up resistance	R_{UP}	Pnn_m, RSTX	-	25	50	100	kΩ	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2/3 = 24MHz	35	44	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 0 Flash/ROM wait states
			36	47		125˚C	
		PLL Run mode with CLKS1/2 = CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	44	57	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 2 Flash/ROM wait states
			45	60		125˚C	
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	49	62	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V 1 Flash/ROM wait state
			50	65		125˚C	
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 4MHz	4.5	5.5	mA	25˚C	CLKPLL, CLKSC and CLKRC stopped 1 Flash/ROM wait state
			5.1	8.5		125˚C	
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 2MHz	2.9	4	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped 1 Flash/ROM wait state
			3.5	6.5		125˚C	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 0	0.4	0.6	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode 1 Flash/ROM wait state
			0.9	3.5		125˚C	
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 1	0.15	0.25	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			0.65	3.2		125˚C	
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 32kHz	0.1	0.2	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			0.6	3		125˚C	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2/3 = 24MHz	9	10.5	mA	25°C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			9.7	13		125°C	
		PLL Sleep mode with CLKS1/2 = CLKP1/3 = 48MHz, CLKP2 = 24MHz	14	15.5	mA	25°C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			14.8	18		125°C	
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1 = 48MHz, CLKP2 = 24MHz	14	15.5	mA	25°C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			14.8	18		125°C	
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2/3 = 4MHz	1.5	1.8	mA	25°C	CLKPLL, CLKSC and CLKRC stopped
			2	4.5		125°C	
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2/3 = 2MHz	0.8	1.3	mA	25°C	CLKMC, CLKPLL and CLKSC stopped
			1.4	4		125°C	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2/3 = 100kHz, SMCR:LPMSS = 0	0.3	0.5	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.4		125˚C	
		RC Sleep mode with CLKS1/2 = CLKP1/2/3 = 100kHz, SMCR:LPMSS = 1	0.06	0.15	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.56	3		125˚C	
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2/3 = 32kHz	0.04	0.12	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped
			0.54	2.9		125˚C	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = MHz	1.6	2	mA	25°C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			2.1	4.8		125°C	
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0	0.35	0.5	mA	25°C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125°C	
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1	0.1	0.15	mA	25°C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125°C	
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0	0.35	0.5	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125°C	
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1	0.1	0.15	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125°C	
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0	0.3	0.45	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.2		125°C	
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1	0.05	0.1	mA	25°C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.55	2.8		125°C	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz	0.03	0.1	mA	25°C	CLKMC, CLKPLL and CLKRC stopped
			0.53	2.8		125°C	
Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = "110"	0.02	0.08	mA	25°C	Core voltage at 1.8V
			0.52	2.8		125°C	
		VRCR:LPMB[2:0] = "000"	0.015	0.06	mA	25°C	Core voltage at 1.2V
			0.4	2.3		125°C	
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE='1')	90	140	µA	25°C	This current must be added to all Power supply currents above
			100	150		125°C	
Clock modulator current	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = '1')	3	4.5	mA	-	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	15	40	mA	-	Must be added to all current above
Input capacitance	C_{IN}	-	5	15	pF		Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}

* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.

4. AC Characteristics

Source Clock timing
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using an oscillation circuit, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using an oscillation circuit or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	48	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			3.5	-	48	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
Clock frequency	f_{CLKVCO}	-	-	50	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	
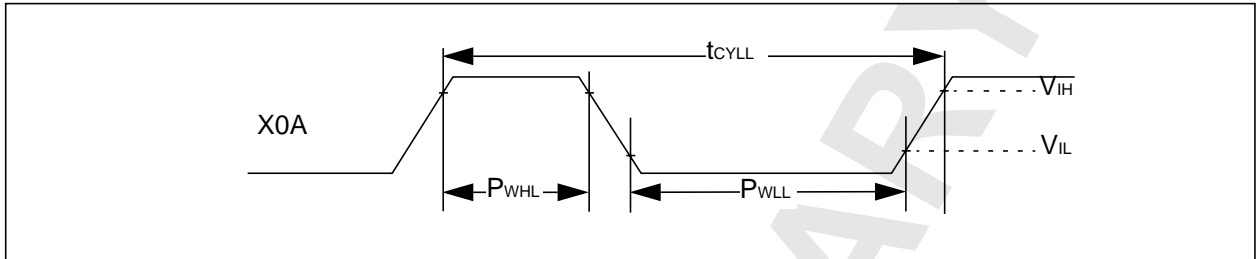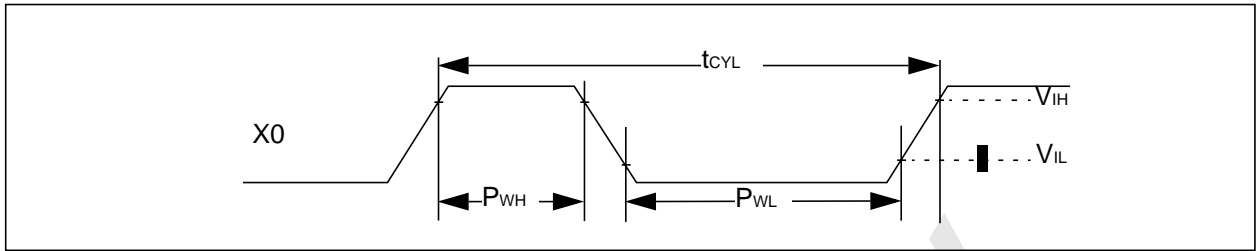
Internal Clock timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	90	0	96	MHz	MB96F338
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	43.5	0	48	MHz	MB96F338
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	
Internal peripheral clock frequency (Clock CLKP3)	f_{CLKP3}	0	43.5	0	48	MHz	MB96F338

WARNING: For USB usage, it is important to change the voltage regulator setting to output 1.9V. Please refer to the chapter Standby Mode and Voltage Regulator control circuit of the hardware manual to perform such setting.

External Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	
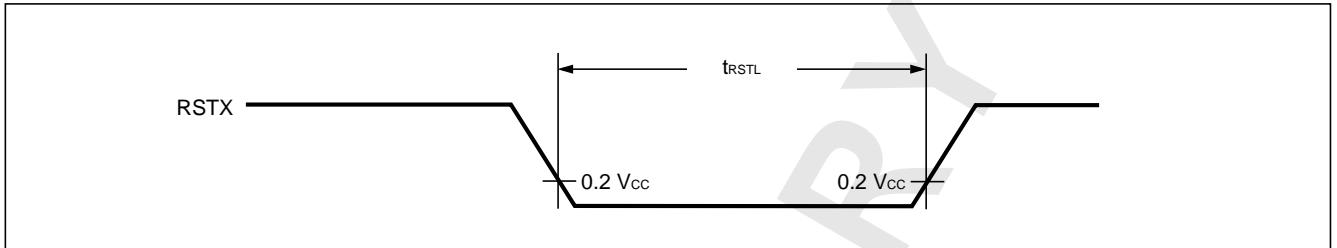
Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	

If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

Rising edge of 50 mV/ms maximum is allowed
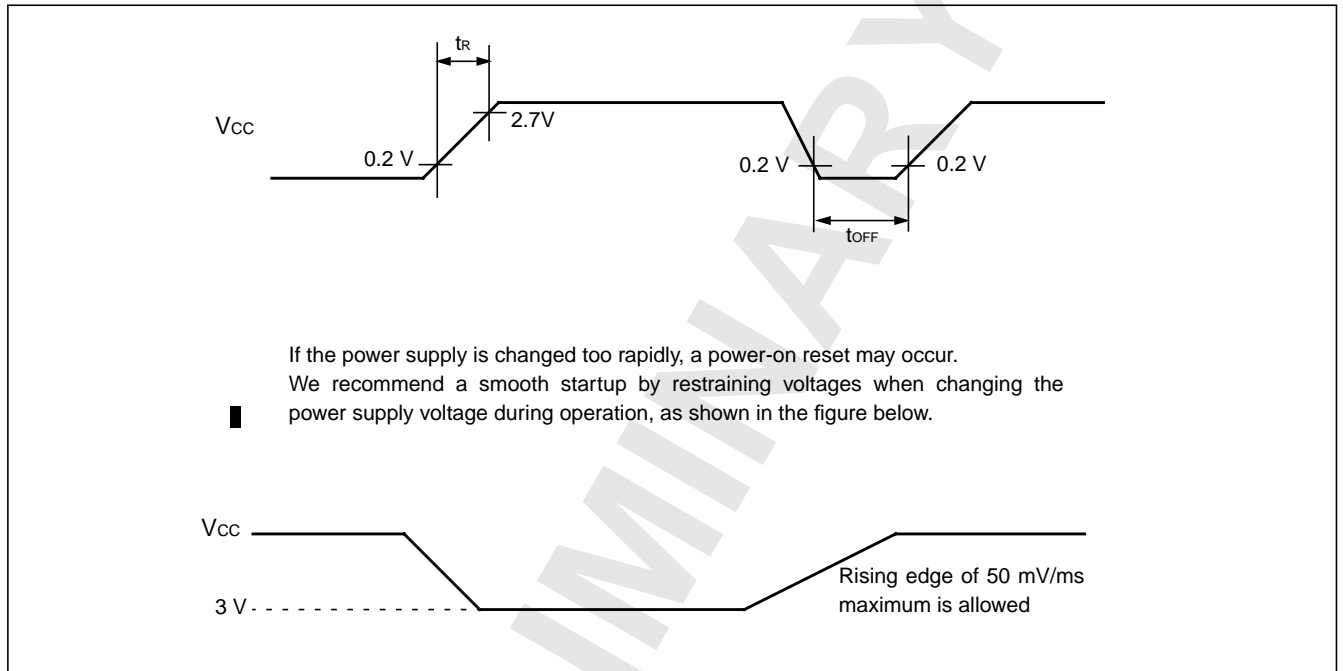
External Input timing

$(T_A = -40°C \text{ to } 125°C, V_{CC} = AV_{CC} = 3.0V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	**Max**		
Input pulse width	t_{INH} t_{INL}	INTn	—	200	—	ns	External Interrupt
		NMI					NMI
		Pnn_m		$2*t_{CLKP1} + 200$ $(t_{CLKP1}=1/f_{CLKP1})$	—	ns	General Purpose IO
		TINn					Reload Timer
		TTGn					PPG Trigger input
		ADTG					AD Converter Trigger
		FRCKn					Free Running Timer external clock
		INn					Input Capture

Note : Relocated Resource Inputs have same characteristics

2008-2-7
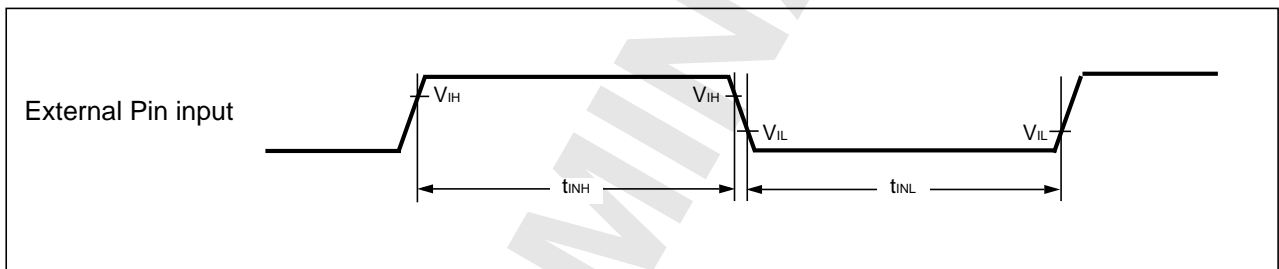
External Bus timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

Basic Timing
$(T_A = -40 \,°C \text{ to } +125 \,°C,$ V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-15	15	ns	
	t_{CLAV}			-15	15		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

$(T_A = -40 \,°C \text{ to } +125 \,°C,$ V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		

($T_A = -40\ °C\ to +125\ °C,$ $V_{CC} = 3.0\ to\ 4.5V,$ $V_{SS} = 0.0\ V,$ $IO_{drive} = 5mA,$ $C_L = 50pF$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-20	20	ns	
	t_{CLAV}			-20	20		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		
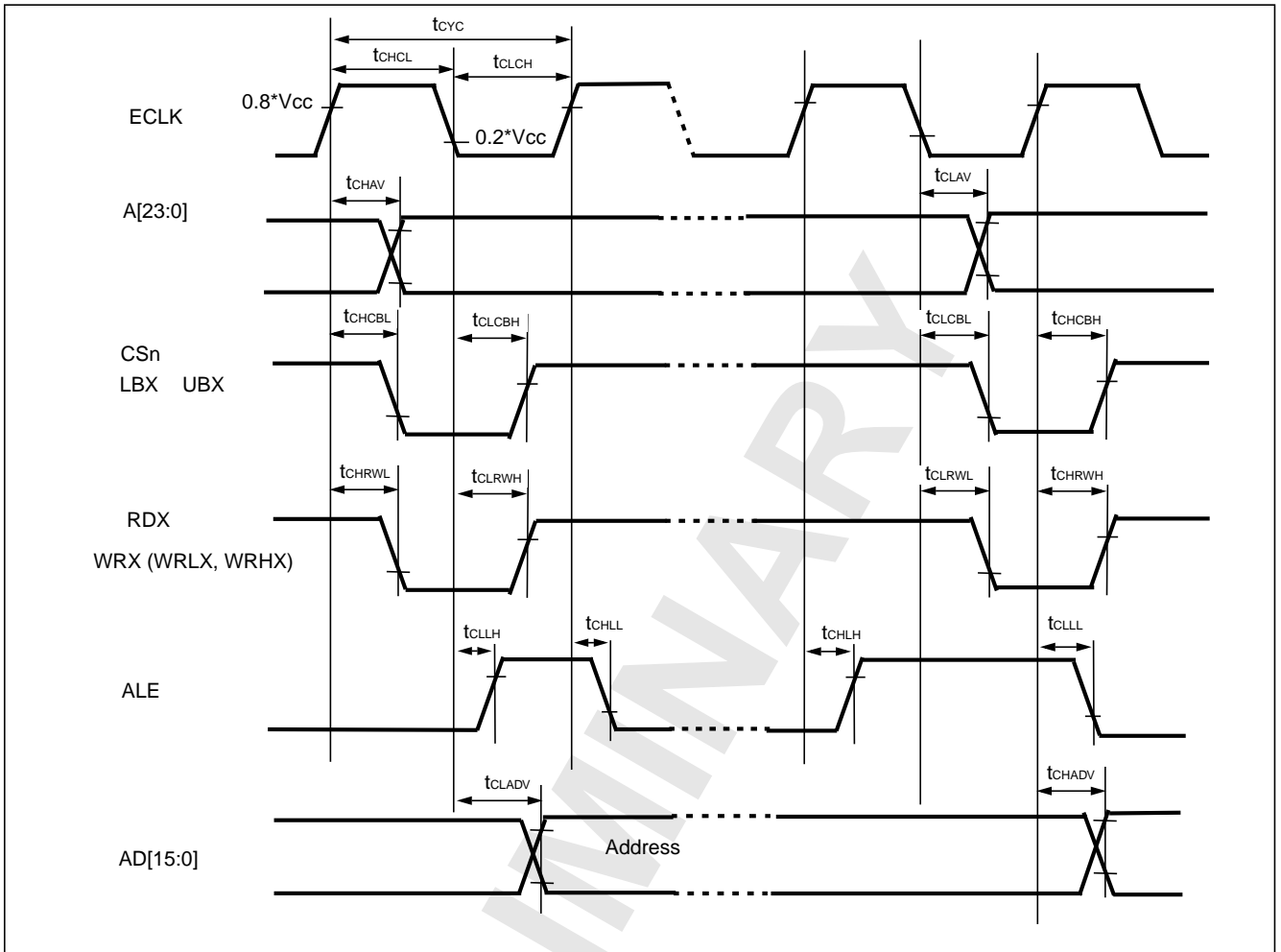
Refer to the Hardware Manual for detailed Timing Charts.

Bus Timing (Read)

($T_A = -40\ °C\ to\ +125\ °C$, $V_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = 0.0\ V$, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Sym-bol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	—	ns	
			EACL:STS=1	$t_{CYC} - 5$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	—		
Valid address $\Rightarrow$ ALE $\downarrow$ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	—	ns	EBM:NMS=0
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	—		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	—		
ALE $\downarrow$ $\Rightarrow$ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
Valid address $\Rightarrow$ RDX $\downarrow$ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 15$	—	ns	
Valid address $\Rightarrow$ RDX $\downarrow$ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$	—		
Valid address $\Rightarrow$ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 55$	ns	w/o cycle extension

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Symbol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 55$		w/o cycle extension
	t_{ADVDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 55$		w/o cycle extension
RDX pulse width	t_{RLRH}	RDX	—	$3\ t_{CYC}/2 - 5$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0], AD[15:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, CLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	$- 10$	—		
ECLK ↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

$(T_A = -40 °C \text{ to } +125 °C, V_{CC} = 3.0 \text{ to } 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)$

Parameter	Sym-bol	Pin	Conditions	Value Min	Value Max	Unit	Remarks
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address ⇒ ALE ↓ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	EBM:NMS=0
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE ↓ ⇒ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		
Valid address ⇒ RDX ↓ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 20$	—	ns	
Valid address ⇒ RDX ↓ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
Valid address ⇒ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 60$	ns	w/o cycle extension

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 3.0\ to\ 4.5V,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, CLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	$- 15$	—		
ECLK ↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	
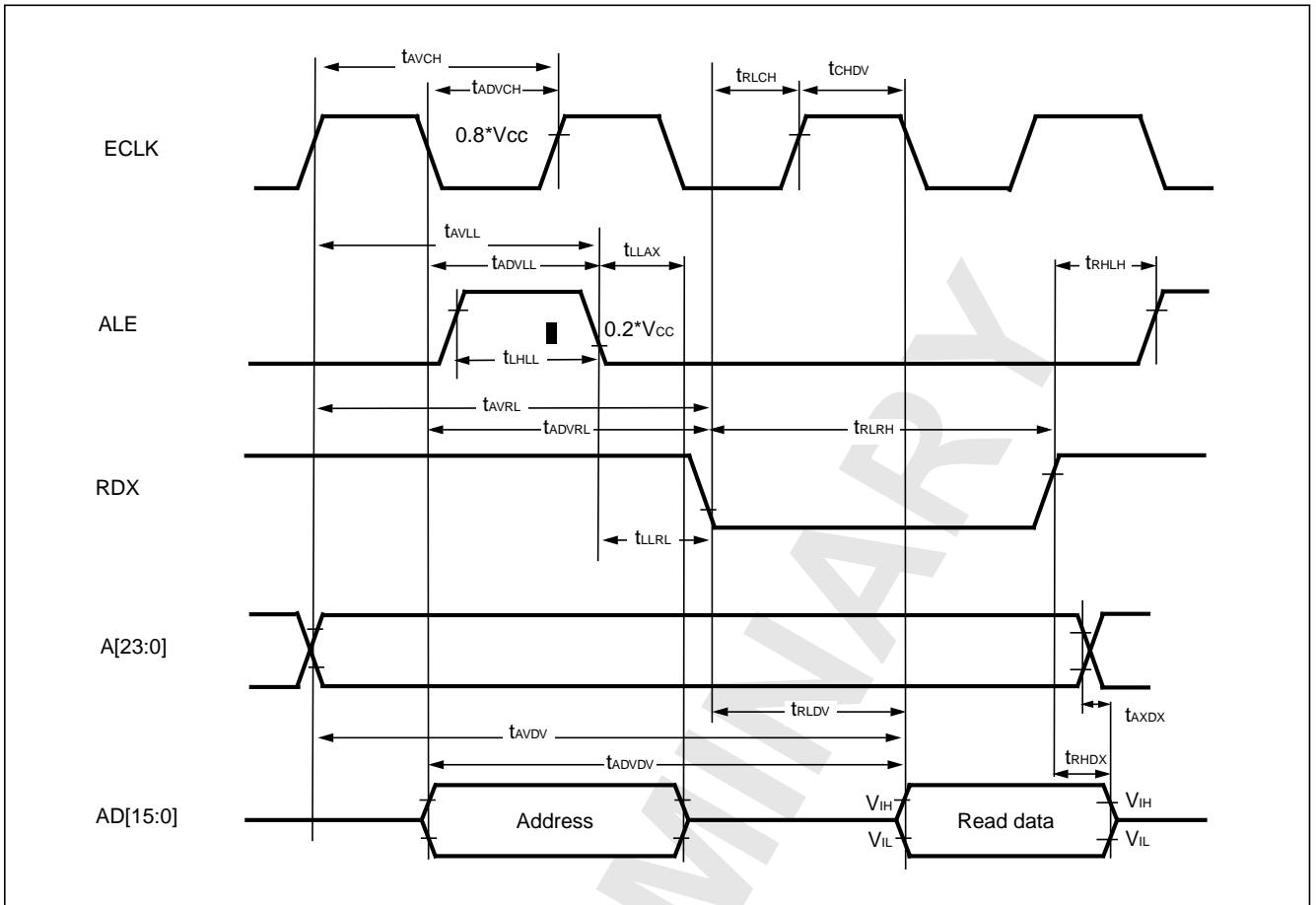
Refer to the Hardware Manual for detailed Timing Charts.

Bus Timing (Write)

($T_A = -40\ °C$ to $+125\ °C$, $V_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = 0.0\ V$, $IO_{drive} = 5mA$, $C_L = 50pF$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\Rightarrow$ WRX ↓ time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 15$	—		
Valid address $\Rightarrow$ WRX ↓ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 15$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 15$		ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 15$			
WRX pulse width	t_{WLWH}	WRX, WRLX, WRHX	—	$t_{CYC} - 5$	—	ns	w/o cycle extension

$(T_A = -40\ °\text{C to} +125\ °\text{C},\ V_{CC} = 5.0\ \text{V} \pm 10\%,\ V_{SS} = 0.0\ \text{V},\ IO_{drive} = 5\text{mA},\ C_L = 50\text{pF})$

Parameter	Symbol	Pin	Condition	Value Min	Value Max	Unit	Remarks
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 20$	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	$- 15$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ ALE ↑ time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	—		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
CSn ⇒ WRX time (non-multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	$t_{CYC}/2 - 15$	ns	
			EACL:STS=1 EBM:NMS=1	—	$t_{CYC} - 15$		
CSn ⇒ WRX time (multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1 EBM:NMS=0	—	$5t_{CYC}/2 - 15$		
WRX ⇒ CSn time (non-multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	$- 15$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 15$	—	ns	
WRX ⇒ CSn time (multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2 - 15$	—	ns	

$(T_A = -40\ °\text{C to} +125\ °\text{C},\ V_{CC} = 3.0\ \text{to}\ 4.5\text{V},\ V_{SS} = 0.0\ \text{V},\ IO_{drive} = 5\text{mA},\ C_L = 50\text{pF})$

Parameter	Symbol	Pin	Condition	Value Min	Value Max	Unit	Remarks
Valid address ⇒ WRX ↓ time (non-multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 EBM:NMS=1	$t_{CYC} - 20$	—		

Parameter	Symbol	Pin	Condition	Value Min	Value Max	Unit	Remarks
Valid address ⇒ WRX ↓ time (multiplexed)	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—	ns	
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$		ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$		ns	
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 8$	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 25$	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ Address valid time (non-multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:0]	EACL:STS=1 EBM:NMS=1	$- 20$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ Address valid time (multiplexed)	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ ALE ↑ time (multiplexed)	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	—	ns	EBM:NMS=0
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	—	ns	
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
CSn ⇒ WRX time (non-multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:STS=0 EBM:NMS=1	—	$t_{CYC}/2 - 20$	ns	
			EACL:STS=1 EBM:NMS=1	—	$t_{CYC} - 20$	ns	
CSn ⇒ WRX time (multiplexed)	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1 EBM:NMS=0	—	$5t_{CYC}/2 - 20$	ns	
WRX ⇒ CSn time (non-multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=1 EBM:NMS=1	$- 20$	—	ns	
			EACL:STS=0 EBM:NMS=1	$t_{CYC}/2 - 20$	—	ns	
WRX ⇒ CSn time (multiplexed)	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EBM:NMS=0	$t_{CYC}/2 - 20$	—	ns	
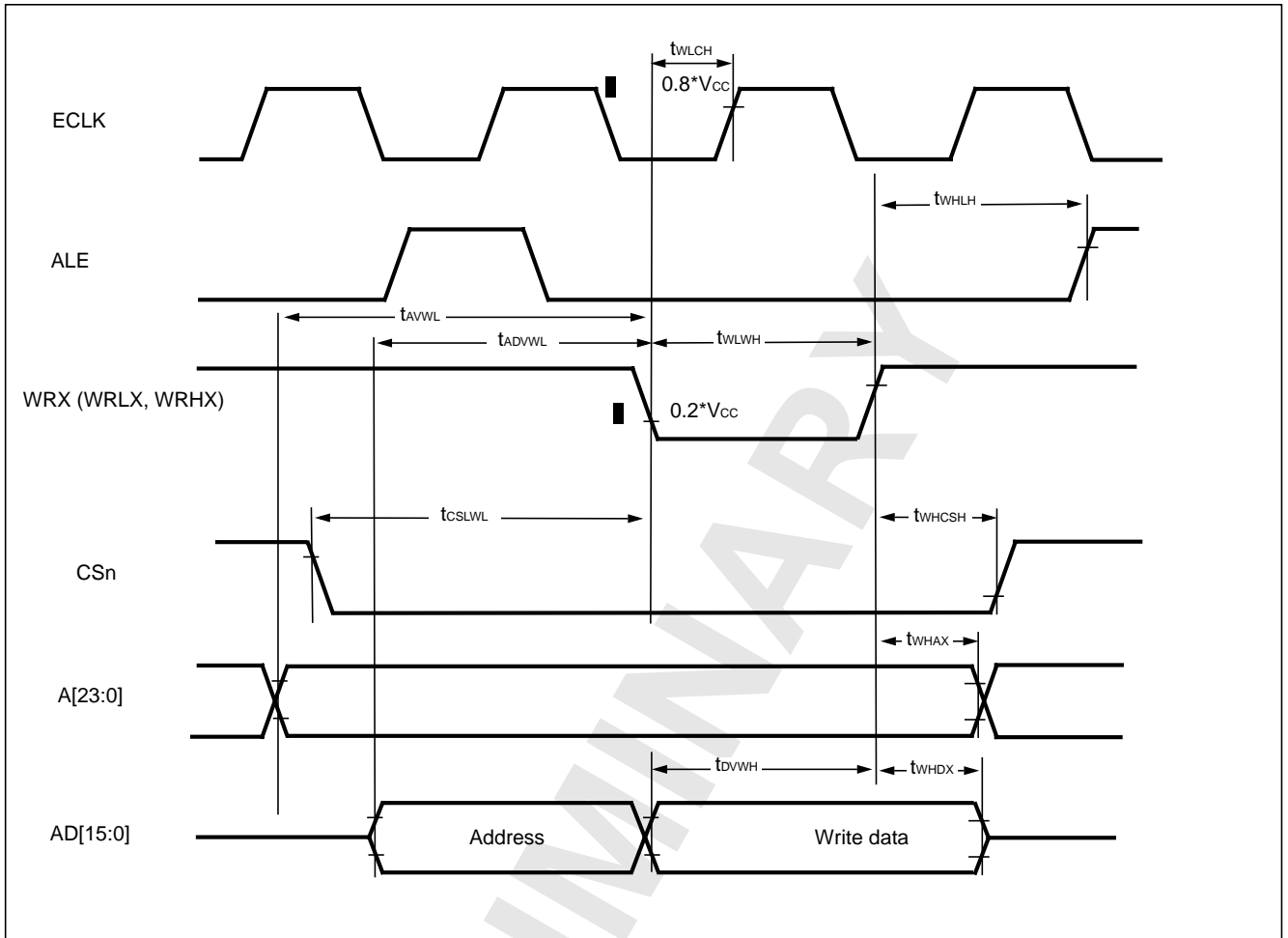
Refer to the Hardware Manual for detailed Timing Charts.

Ready Input Timing

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

$(T_A = -40\ °C\ to\ +125\ °C,\ V_{CC} = 3.0\ to\ 4.5V,\ V_{SS} = 0.0\ V,\ IO_{drive} = 5mA,\ C_L = 50pF)$

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

ECLK

RDY
When WAIT is not used.

RDY
When WAIT is used.

0.8*Vcc

tRYHS   tRYHH

VIH   VIH

VIL
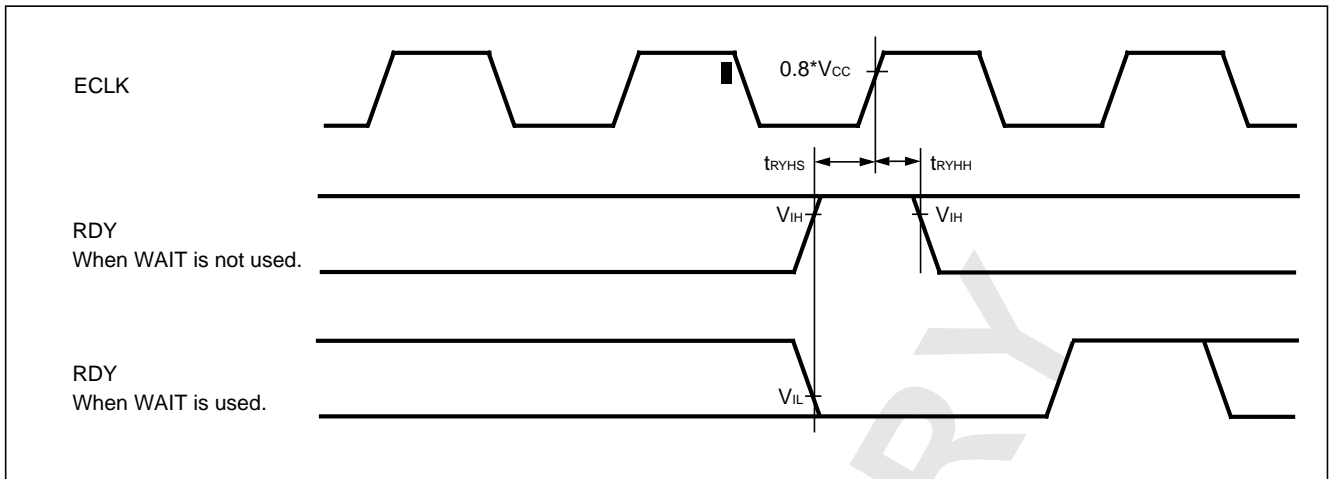
Refer to the Hardware Manual for detailed Timing Charts.

Hold Timing

(T$_A$ = −40 °**C to** +125 °**C,** V$_{CC}$ = 5.0 V ± 10%**,** V$_{SS}$ = 0.0 V**,** IO$_{drive}$ = 5mA, C$_I$ = 50pF**)**

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t$_{XHAL}$	HAKX	—	t$_{CYC}$ − 20	t$_{CYC}$ + 20	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t$_{HAHV}$	HAKX		t$_{CYC}$ − 20	t$_{CYC}$ + 20	ns	

(T$_A$ = −40 °**C to** +125 °**C,** V$_{CC}$ = 3.0 to 4.5V**,** V$_{SS}$ = 0.0 V**,** IO$_{drive}$ = 5mA, C$_I$ = 50pF**)**

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating $\Rightarrow$ HAKX $\downarrow$ time	t$_{XHAL}$	HAKX	—	t$_{CYC}$ − 25	t$_{CYC}$ + 25	ns	
HAKX $\uparrow$ time $\Rightarrow$ Pin valid time	t$_{HAHV}$	HAKX		t$_{CYC}$ − 25	t$_{CYC}$ + 25	ns	

HAKX

0.2*Vcc   0.8*Vcc

txHAL   tHAHV

Each pin   High-Z

0.8*Vcc

0.2*Vcc
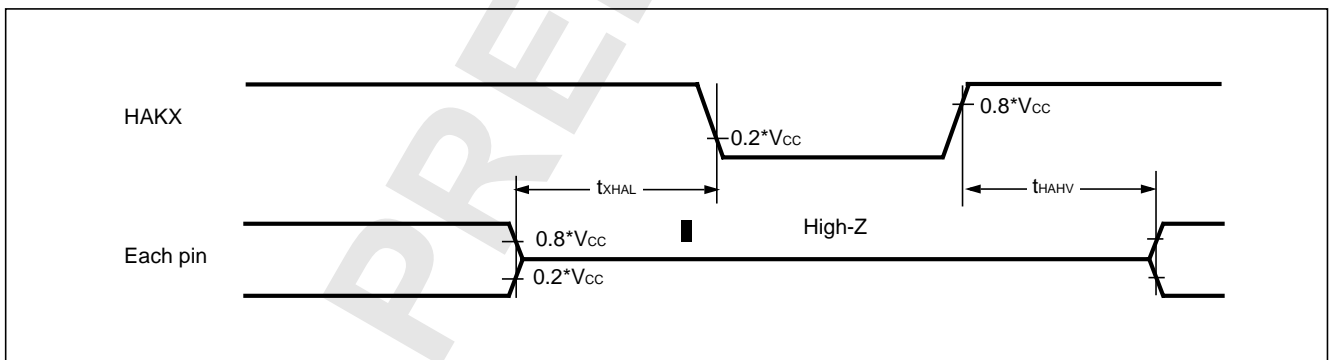
Refer to the Hardware Manual for detailed Timing Charts.

USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N*t_{CLKP1}$ - 20 [*1]	—	$N*t_{CLKP1}$ - 30 [*1]	—	
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock "L" pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock "H" pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes: • AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96300 Super series HARDWARE MANUAL"
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = $2*k*t_{CLKP1}$, then N = k, where k is an integer > 2
- if t_{SCYCI} = $(2*k+1)*t_{CLKP1}$, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
$4*t_{CLKP1}$	2
$5*t_{CLKP1}$, $6*t_{CLKP1}$	3
$7*t_{CLKP1}$, $8*t_{CLKP1}$	4
...	...

Internal Shift Clock Mode

External Shift Clock Mode
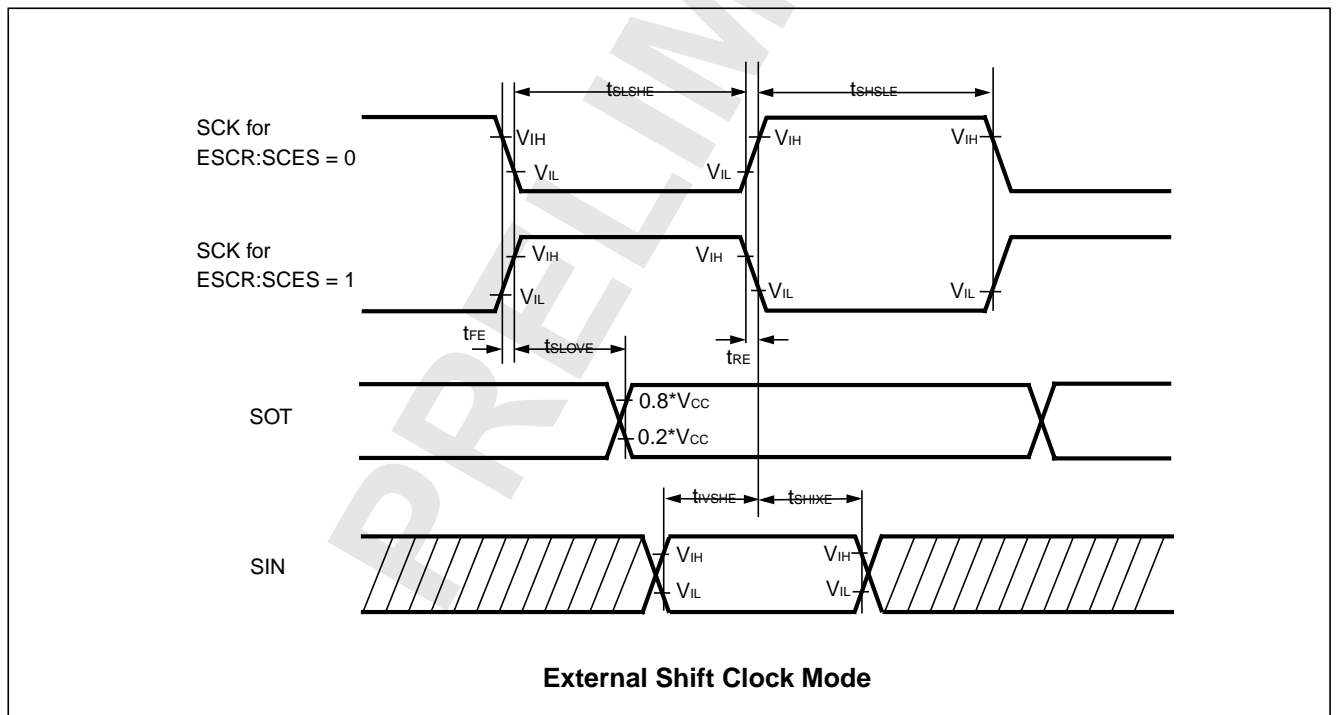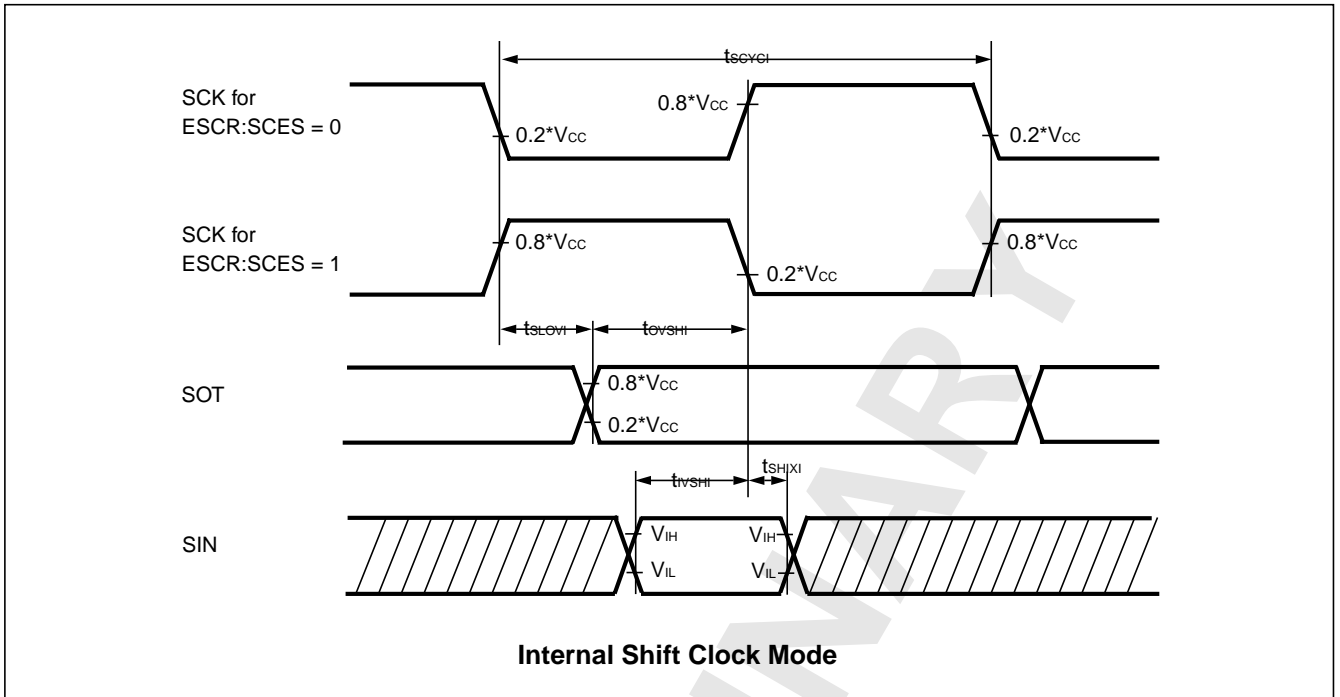
I²C Timing

(T$_A$ = -40°C to 125°C, V$_{CC}$ = AV$_{CC}$ = 3.0V to 5.5V, V$_{SS}$ = AV$_{SS}$ =0V)

Parameter	Symbol	Condition	Standard-mode Min	Max	Fast-mode[4] Min	Max	Unit
SCL clock frequency	f$_{SCL}$		0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t$_{HDSTA}$		4.0	—	0.6	—	µs
"L" width of the SCL clock	t$_{LOW}$		4.7	—	1.3	—	µs
"H" width of the SCL clock	t$_{HIGH}$		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t$_{SUSTA}$	R = 1.7 kΩ, C = 50 pF[1]	4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t$_{HDDAT}$		0	3.45[2]	0	0.9[3]	µs
Data set-up time SDA↓↑→SCL↑	t$_{SUDAT}$		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t$_{SUSTO}$		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t$_{BUS}$		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t$_{HDDAT}$ have only to be met if the device does not stretch the "L" width (t$_{LOW}$) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t$_{SUDAT}$ ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.
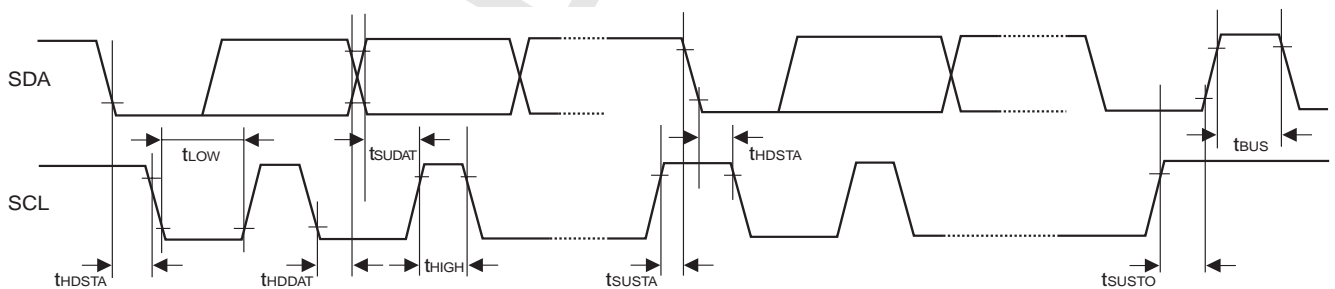
5. USB Characteristics

(T_A = -40˚C to 105˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, V_{CC3} = 3.0V to 3.6V)

	Parameter	Symbol	Min	Max	Unit	Note
Input characteristics	Input High level voltage	V_{IH}	2.0	-	V	
	Input Low level voltage	V_{IL}	-	0.8	V	
	Differential Input Sensitivity	V_{DI}	0.2	-	V	
	Differential Common Mode Range	V_{CM}	0.8	2.5	V	
Output characteristics	Output High level voltage	V_{OH}	2.8	3.6	V	I_{OH} = -100µA
	Output Low level voltage	V_{OL}	0.0	0.3	V	I_{OL} = 100µA
	Cross over voltage	V_{CRS}	1.3	2.0	V	
	Rise time	t_{FR}	4	20	ns	
	Fall time	t_{FF}	4	20	ns	
	Rising/Falling time matching	t_{RFM}	90	111.11	%	T_{FR}/T_{FF}
	Output resistance	Z_{DRV}	28	44	Ω	includes R_S = 27Ω

Data Signal Timing
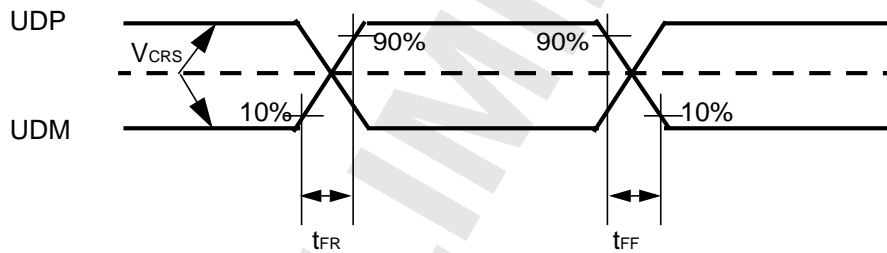
Load Condition:
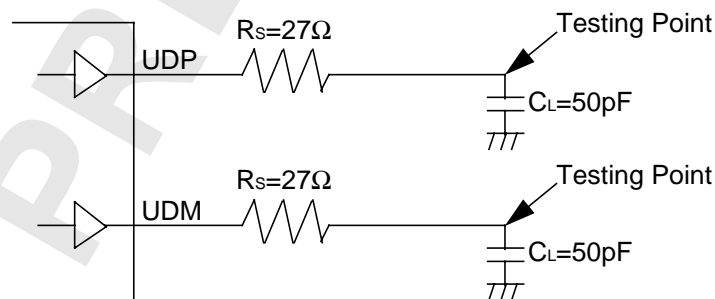
PRELIMINARY

6. Analog Digital Converter

(T_A = -40 ˚C to +125 ˚C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5	AVRL+ 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5	AVRH - 1.5	AVRH + 0.5	LSB	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input current	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH2	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	AD Converter active
	I_{AH}	AV_{CC}	-	-	5	µA	AD Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	AD Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	AD Converter not operated
Offset between input channels	-	ANn	-	-	TBD	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and linear error.

Nonlinearity error: Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.

Differential linearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.
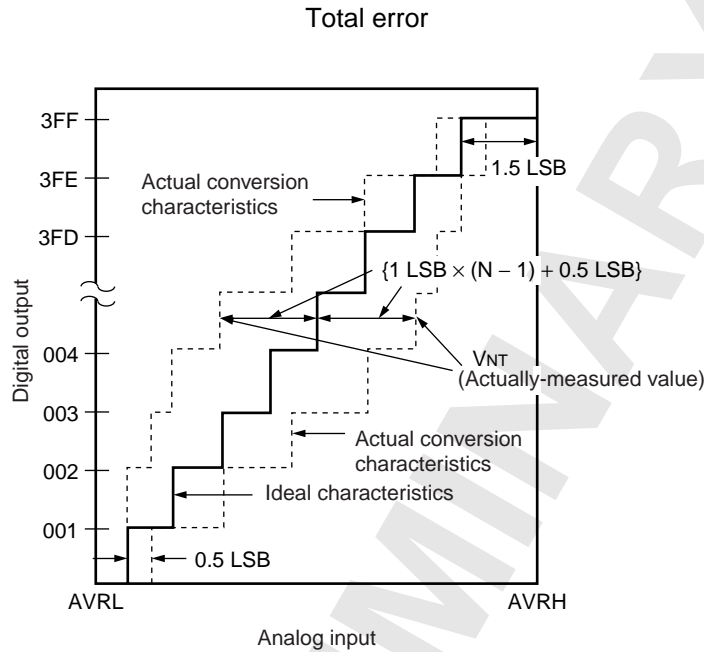
Total error

$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\,\text{LSB} \times (N-1) + 0.5\,\text{LSB}\}}{1\,\text{LSB}} \ [\text{LSB}]$$

$$1\,\text{LSB} = (\text{Ideal value}) \ \frac{AVRH - AVRL}{1024} \ [\text{V}]$$

N: A/D converter digital output value

V_{OT} (Ideal value) $= AVRL + 0.5\,\text{LSB}$ [V]

V_{FST} (Ideal value) $= AVRH - 1.5\,\text{LSB}$ [V]

V_{NT} : A voltage at which digital output transitions from $(N - 1)$ to N.

Non linearity error

Differential linearity error
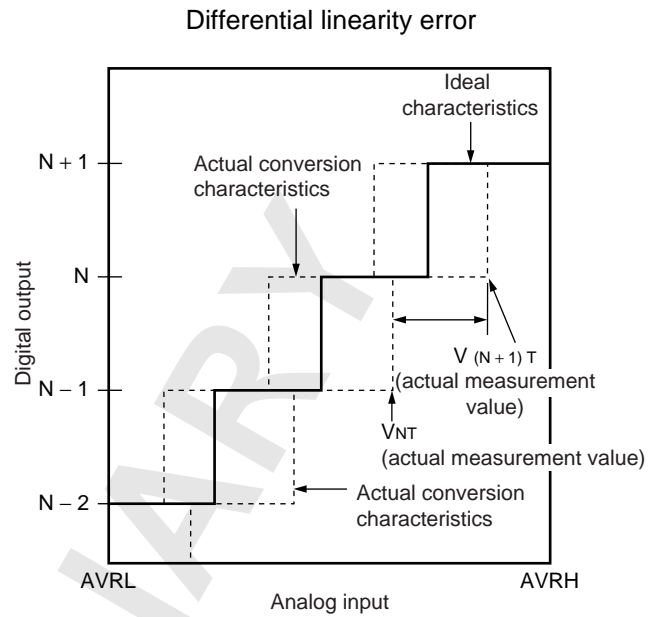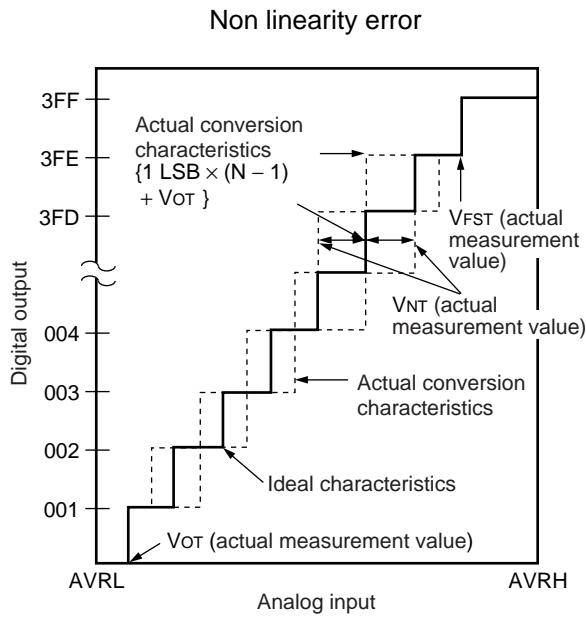
$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1\text{ LSB} \times (N-1) + V_{OT}\}}{1\text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{ LSB}} - 1\text{ LSB [LSB]}$$

$$1\text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output transits from "000H" to "001H."

V_{FST} : Voltage at which digital output transits from "3FEH" to "3FFH."

Notes on A/D Converter Section

- About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- analog input circuit model:
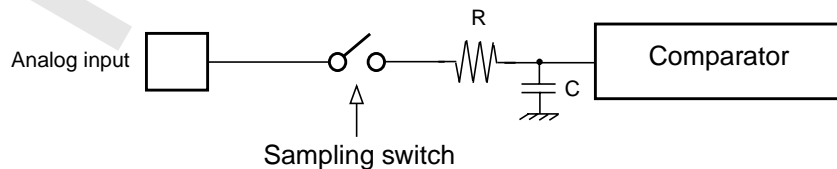
Reference value:
- C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = $7 \times (R_{ext} + 2.6k\Omega) \times C$ for $4.5 \leq AV_{cc} \leq 5.5$

T_{samp} [min] = $7 \times (R_{ext} + 12.1k\Omega) \times C$ for $3.0 \leq AV_{cc} \leq 4.5$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

7. Alarm Comparator

$(T_A = -40\ °C$ to $+125\ °C$, $V_{CC} = AV_{CC} = 3.0V - 5.5V$, $V_{SS} = AV_{SS} = 0V)$

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	40	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	10	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	$T_A = 25\ °C$
			-3	-	+3	µA	$T_A = 125\ °C$
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		$0.36 * AV_{CC}$ -0.25	$0.36 * AV_{CC}$ -0.1		V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$			$0.36 * AV_{CC}$ +0.1	$0.36 * AV_{CC}$ +0.25	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		$0.78 * AV_{CC}$ -0.25	$0.78 * AV_{CC}$ -0.1		V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			$0.78 * AV_{CC}$ +0.1	$0.78 * AV_{CC}$ +0.25	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.3	2	µs	CMD = 1 (fast)
	t_{COMPS}		-	2	100	µs	CMD = 0 (slow)
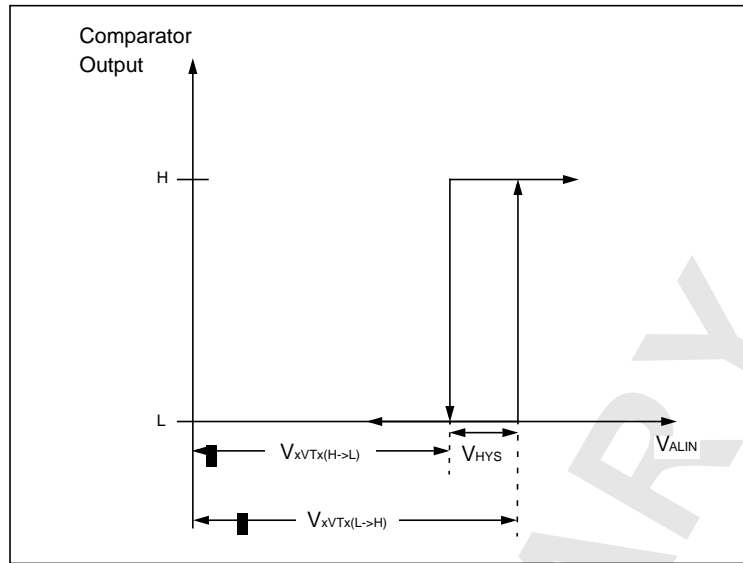
8. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	60	75	µs	
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\dfrac{dV}{dt}\right| \leq 0.004\dfrac{V}{\mu s}$.
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of
Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.
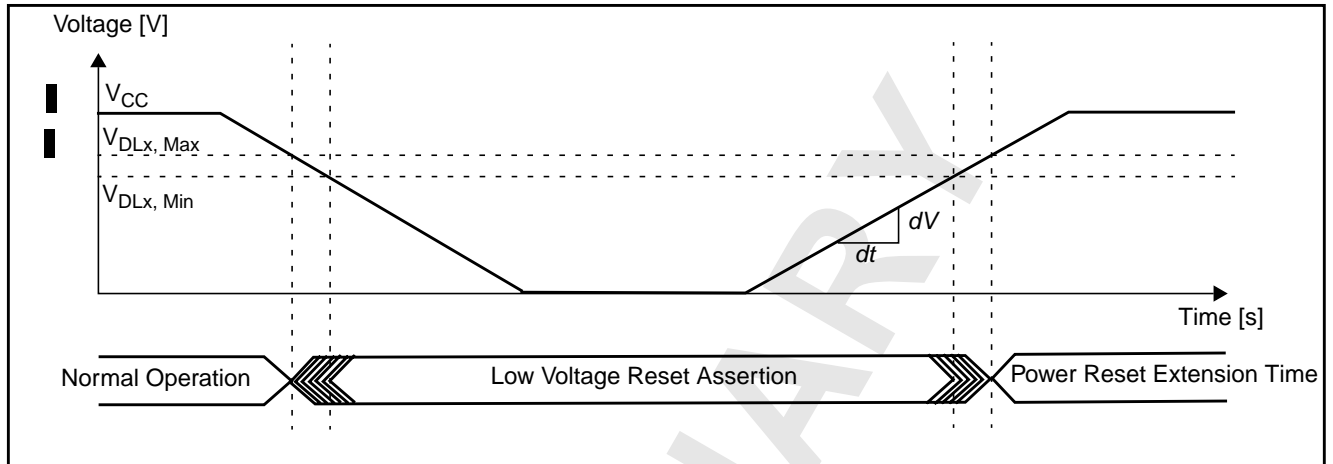
9. FLASH memory program/erase characteristics

($T_A = 25^oC$, $V_{cc} = 5.0V$)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	us	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

■ **EXAMPLE CHARACTERISTICS**
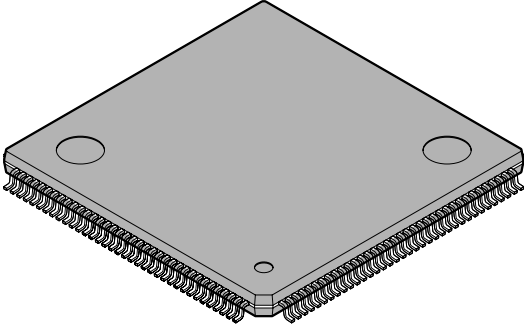
To be prepared

PRELIMINARY

■ PACKAGE DIMENSION MB96(F)33x LQFP 144P

144-pin plastic LQFP	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20g
(FPT-144P-M08)	Code (Reference)	P-LFQFP144-20×20-0.50

144-pin plastic LQFP
(FPT-144P-M08)

22.00±0.20(.866±.008)SQ

* 20.00±0.10(.787±.004)SQ

0.145±0.055
(.006±.002)

108   73

109   72

144   37

INDEX

LEAD No. 1   36

0.50(.020)

0.22±0.05
(.009±.002)

⊕ 0.08(.003) Ⓜ

0.08(.003)

"A"

Details of "A" part

1.50 +0.20/−0.10 (Mounting height)
(.059 +.008/−.004)

0°~8°

0.10±0.10
(.004±.004)
(Stand off)

0.25(.010)

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

© 2003 FUJITSU LIMITED F144019S-c-4-6

Dimensions in mm (inches).
Note: The values in parentheses are reference values.
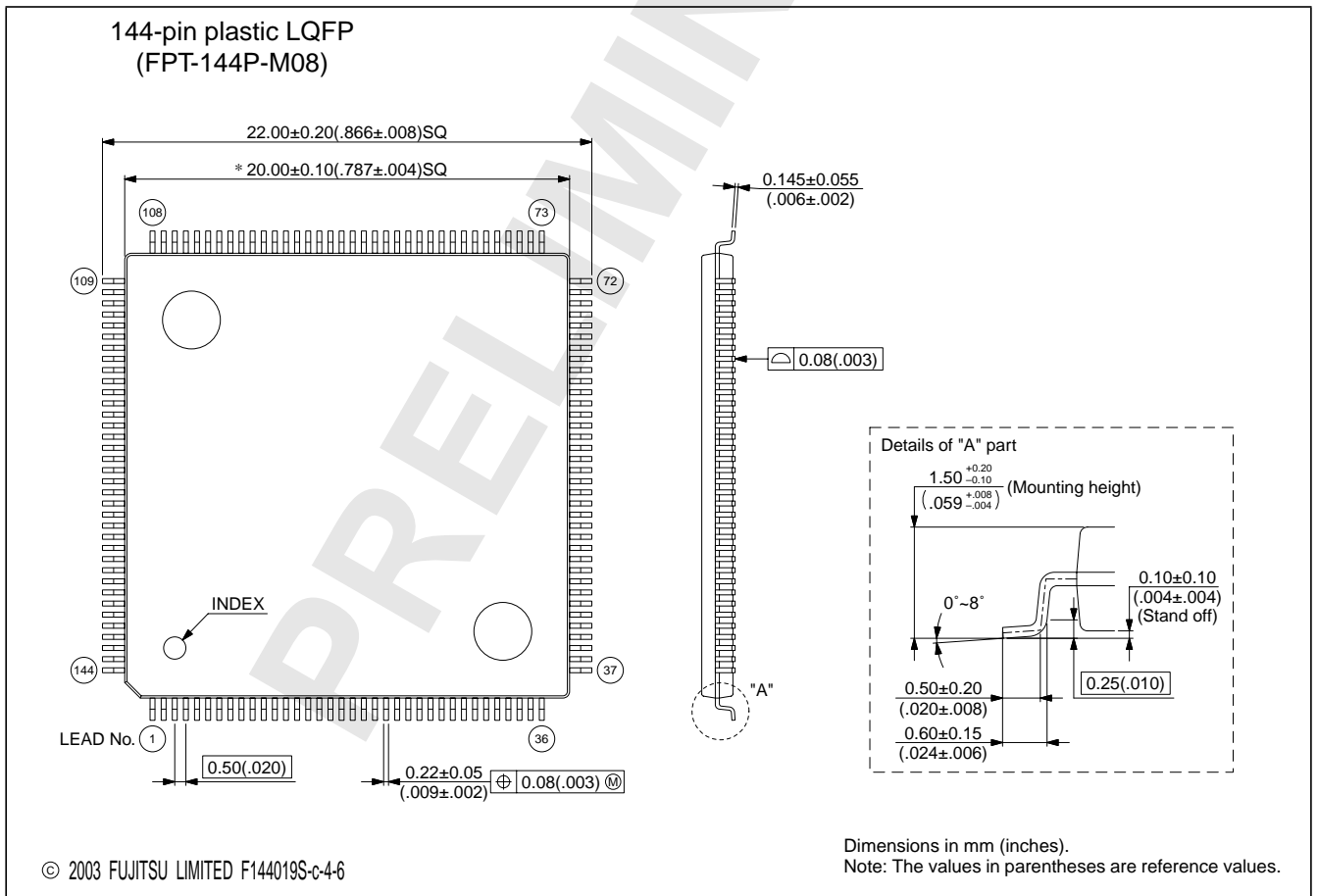
■ ORDERING INFORMATION

Part number	Subclock	Persistent Low Voltage Reset	Package	Remarks
MB96336YSA PMC-GSE2 *1	No	Yes	144 pin Plastic LQFP (FPT-144P-M08)	
MB96336RSA PMC-GSE2 *1	No	No		
MB96336YWA PMC-GSE2 *1	Yes	Yes		
MB96336RWA PMC-GSE2 *1	Yes	No		
MB96338YSA PMC-GSE2 *1	No	Yes	144 pin Plastic LQFP (FPT-144P-M08)	
MB96338RSA PMC-GSE2 *1	No	No		
MB96338YWA PMC-GSE2 *1	Yes	Yes		
MB96338RWA PMC-GSE2 *1	Yes	No		
MB96F338YSA PMC-GSE2 *1	No	Yes	144 pin Plastic LQFP (FPT-144P-M08)	
MB96F338RSA PMC-GSE2 *1	No	No		
MB96F338YWA PMC-GSE2 *1	Yes	Yes		
MB96F338RWA PMC-GSE2 *1	Yes	No		
MB96F338USA PMC-GSE2 *1	No	No	144 pin Plastic LQFP (FPT-144P-M08)	with USB
MB96F338UWA PMC-GSE2 *1	Yes			
MB96V300BRB-ES	Yes	No	416 pin Plastic BGA (BGA416-M02)	For evaluation

*1: These devices are under development. All information in this datasheet is preliminary for the devices under development.

■ REVISION HISTORY

Revision	Date	Modification
Prelim 0.1	2007-05-23	Creation
Prelim 0.2	2007-08-14	- information about MB96F338U (with USB function) is added - DMA 8ch --> 16ch - ADC reference switch is removed
Prelim 0.3	2007-09-11	- Circuit Type of Device with "U" suffix is added - Circuit Type diagram: TTL input cell type was changed from NOR to NAND - IO Map, IRQ table are updated - Parallel Programing Flash Memory Control Signals is updated - DC/AC spec of USB I/O is added
Prelim 0.4	2007-09-24	- Block diagram for MB96F338U was corrected: USB PB1 -> PB3 - IRQ table was modified: Vector number 111 was inserted (reserved) - Pin assignment was corrected: not used resource name was removed
Prelim 0.5	2007-11-02	- Internal Max Freq 56MHz --> 48MHz - DMA 12ch --> 10ch - FPT-144P-M12 package was removed
Prelim 1	2007-12-20	Update of the block diagram to include USB block. Update DC characteristics to include all USB pins characteristics. IOMAP regenerated. Memory maps and Flash configuration reworked. Typos corrected accross the document. Renaming of the Flash banks.

Revision	Date	Modification
Prelim 2	2008-02-07	• Features: - Removed ADC reference switch - changed USB description • Lineup: - option description added - Part number names corrected - Flash B removed - RLT6 added • Block diagrams: - Flash B removed - OUT5_R -> OUT6_R - TX2_R, RX2_R added - SIN2_R, SOT2_R, SCK2_R and SOT9 added - not existing TTGx, TTGx_R and PPGx_R pins deleted - RLT6 added • Pin function description: relocated clock output and CAN pins added • I/O ciruit types updated • Memory maps replaced by new standard maps • Parallel Flash programming pinning removed • IOMAP regenerated (naming style changed, all reserved registers added) • DC current limits updated with new setting and corrected frequencies • External bus timings: missing conditions added and readability improved • Alarm comparator spec updated (transition voltages defined) • Ordering information updated • Typos and formatting corrected

FUJITSU LIMITED