



3.3V Zero Delay Buffer

General Features

- 20 MHz to 70MHz operating range, compatible with CPU and PCI bus frequencies.
- Zero input - output propagation delay
- Multiple low-skew outputs
 - Output-output skew less than 250 ps
 - Device-device skew less than 700 ps
 - One input drives 9 outputs, grouped as 4 + 4 + 1
- Less than 200 ps cycle-to-cycle jitter is compatible with Pentium® based systems
- Test Mode to bypass PLL
- Available in 16-pin, 150-mil SOIC, 4.4 mm TSSOP and 150-mil SSOP packages
- 3.3V operation, advanced 0.35μ CMOS technology
- 'SpreadTrak'.

Functional Description

The PCC028-02A is a low-cost 3.3V zero delay buffer designed to distribute high-speed clocks and is available in a 16-pin SOIC package. All parts have on-chip PLLs that lock to an input clock on the REF pin.

The PLL feedback is on-chip and is obtained from the CLKOUT pad.

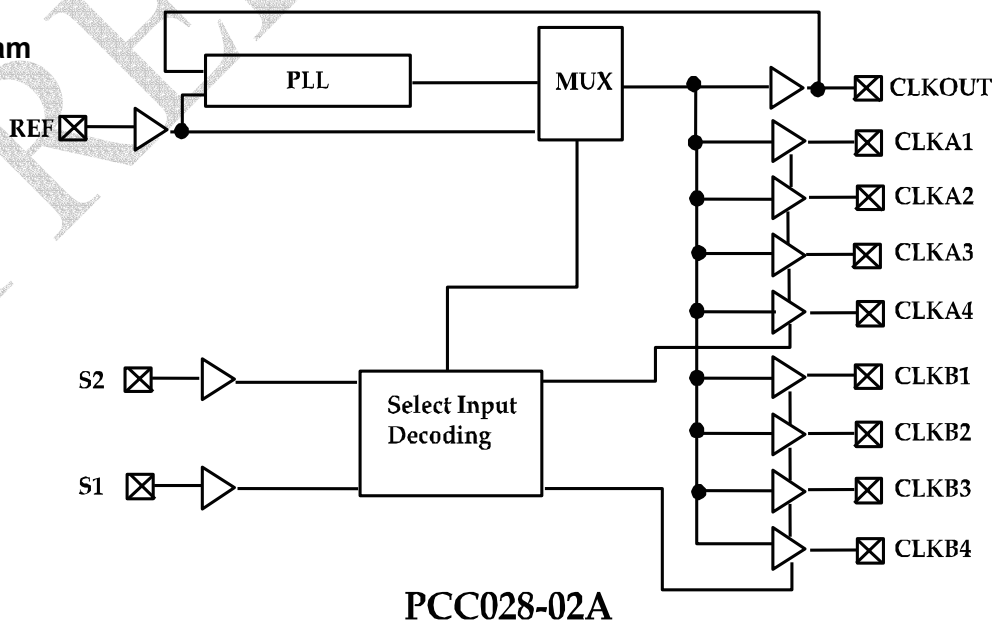
The PCC028-02A has two banks of four outputs each, which can be controlled by the Select inputs as shown in the Select Input Decoding Table. If all the output clocks are not required, Bank B can be three-stated. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

The PCC028-02A PLL shuts down in one case, as shown in the *Select Input Decoding Table*.

Multiple PCC028-02A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input to output propagation delay is guaranteed to be less than 350 ps, and the output to output skew is guaranteed to be less than 250ps.

Block Diagram





Select Input Decoding for PCC028-02A

S2	S1	Clock A1 - A4	Clock B1 - B4	CLKOUT ¹	Output Source	PLL Shut-Down
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Notes:

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and the output

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

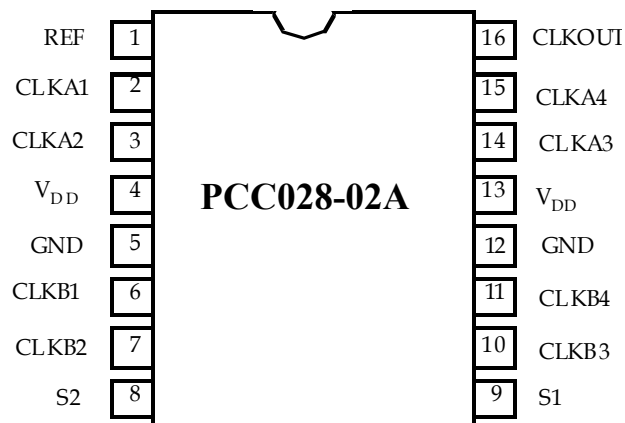
For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, for obtaining zero-input-output delay.

'SpreadTrak'

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation.

PCC028-02A is designed so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the Spread Spectrum feature through, the result is a significant amount of tracking skew which may cause problems in the systems requiring synchronization.

Pin Configuration





Pin Description

Pin #	Pin Name	Description
1	REF	Input reference frequency, 5V-tolerant input
2	CLKA1	Buffered clock output, bank A
3	CLKA2	Buffered clock output, bank A
4	V _{DD}	3.3V supply
5	GND	Ground
6	CLKB1	Buffered clock output, bank B
7	CLKB2	Buffered clock output, bank B
8	S2 ²	Select input, bit 2
9	S1 ²	Select input, bit 1
10	CLKB3	Buffered clock output, bank B
11	CLKB4	Buffered clock output, bank B
12	GND	Ground
13	V _{DD}	3.3V supply
14	CLKA3	Buffered clock output, bank A
15	CLKA4	Buffered clock output, bank A
16	CLKOUT	Buffered output, internal feedback on this pin

Notes:

2. Weak pull-up on these inputs



Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	-0.5	+7.0	V
DC Input Voltage (Except REF)	-0.5	$V_{DD} + 0.5$	V
DC Input Voltage (REF)	-0.5	7	V
Storage Temperature	-65	+150	°C
Max. Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)		2000	V
Note: These are stress ratings only and are not implied for functional operation. Exposure to absolute maximum ratings for prolonged time can affect device reliability.			

Operating Conditions for PCC028-02ASC-XX Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		TBD	pF
C_{IN}	Input Capacitance		TBD	pF



Electrical Characteristics for PCC028-02ASC-XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage ³			0.8	V
V_{IH}	Input HIGH Voltage ³		2.0		V
I_{IL}	Input LOW Current	$V_{IN} = 0V$		50.0	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$		100.0	μA
V_{OL}	Output LOW Voltage ⁴	$I_{OL} = 8mA$		0.4	V
V_{OH}	Output HIGH Voltage ⁴	$I_{OL} = -8mA$	2.4		V
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}		32.0	mA

Switching Characteristics for PCC028-02ASC-1 Commercial Temperature Devices ⁵

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$1/t_1$	Output Frequency	30-pF load	20		70	MHz
	Duty Cycle ⁴ = $(t_2 / t_1) * 100$	Measured at 1.4V, $F_{OUT} = 66.67$ MHz	40.0	50.0	60.0	%
t_3	Rise Time ⁴	Measured between 0.8V and 2.0V			2.50	ns
t_4	Fall Time ⁴	Measured between 2.0V and 0.8V			2.50	ns
t_5	Output-to-output skew ⁴	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge ⁴	Measured at $V_{DD} / 2$		0	± 350	ps
t_7	Device-to-Device Skew ⁴	Measured at $V_{DD} / 2$ on the CLKOUT pins of the device		0	700	ps
t_8	Output Slew Rate ⁵	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t_J	Cycle-to-cycle jitter ⁴	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time ⁴	Stable power supply, valid clock presented on REF pin			1.0	ms

Switching Characteristics for PCC028-02ASC-1 Industrial Temperature Devices ⁵

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
1/t ₁	Output Frequency	30-pF load	20		70	MHz
	Duty Cycle ⁴ = (t ₂ / t ₁) * 100	Measured at 1.4V, F _{OUT} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle ⁴ = (t ₂ / t ₁) * 100	Measured at 1.4V, F _{OUT} < 50.0 MHz	45.0	50.0	55.0	%
t ₃	Rise Time ⁴	Measured between 0.8V and 2.0V			1.50	ns
t ₄	Fall Time ⁴	Measured between 2.0V and 0.8V			1.50	ns
t ₅	Output-to-output skew ⁴	All outputs equally loaded			250	ps
t ₆	Delay, REF Rising Edge to CLKOUT Rising Edge ⁴	Measured at V _{DD} / 2		0	±350	ps
t ₇	Device-to-Device Skew ⁴	Measured at V _{DD} /2 on the CLKOUT pins of the device		0	700	ps
t ₈	Output Slew Rate ⁵	Measured between 0.8V and 2.0V using Test Circuit #2	1			V/ns
t _J	Cycle-to-cycle jitter ⁴	Measured at 66.67 MHz, loaded outputs			200	ps
t _{LOCK}	PLL Lock Time ⁴	Stable power supply, valid clock presented on REF pin			1.0	ms

Notes:

3. REF input has a threshold voltage of V_{DD}/2

4. Parameter is guaranteed by design and characterization. Not 100% tested in production

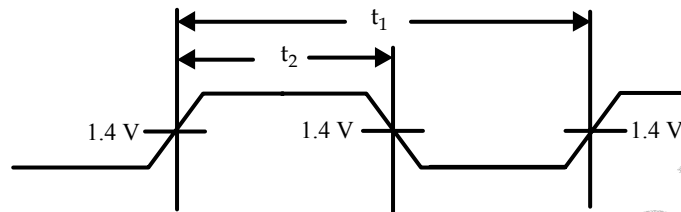
5. All parameters specified with loaded outputs.



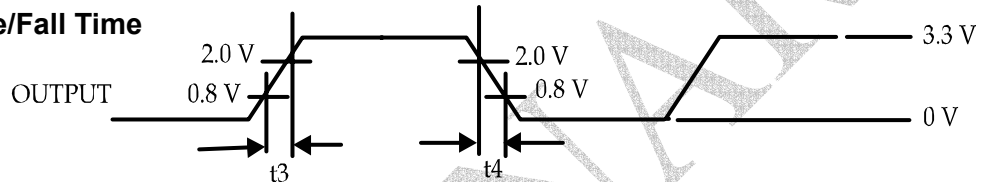
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Switching Waveforms

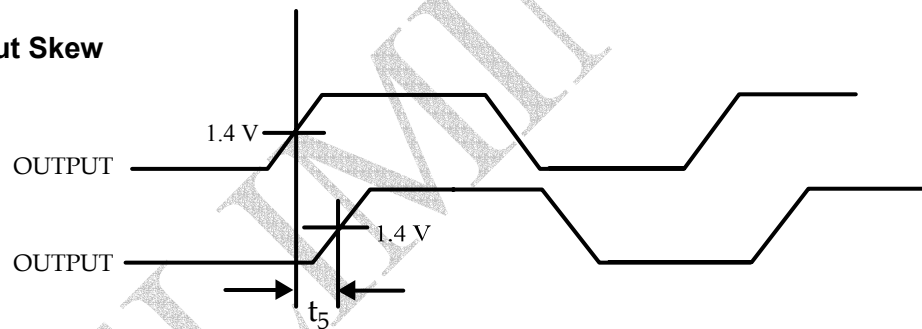
Duty Cycle Timing



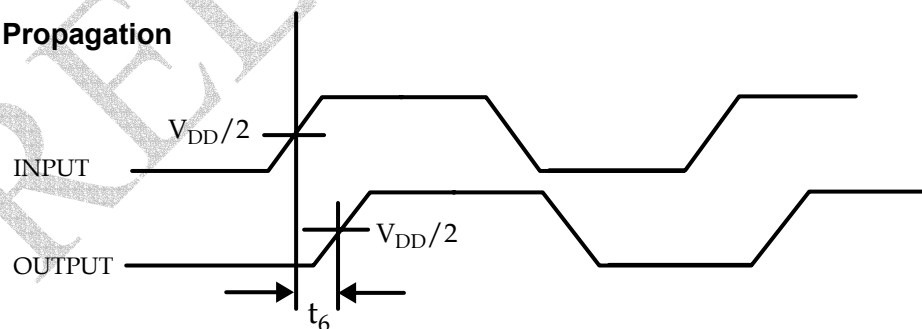
All Outputs Rise/Fall Time



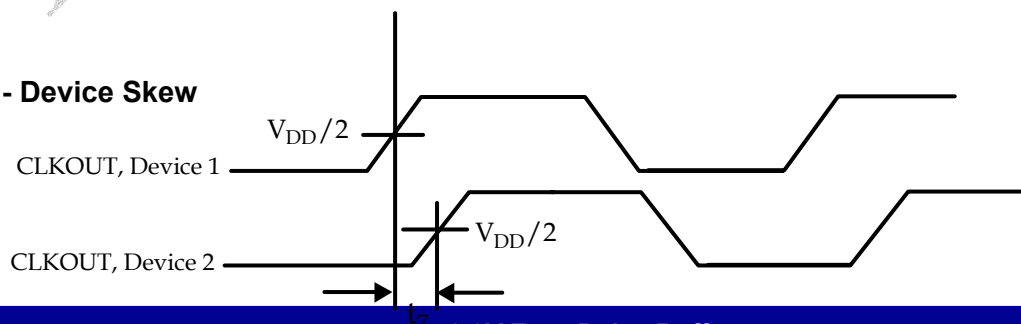
Output - Output Skew



Input - Output Propagation

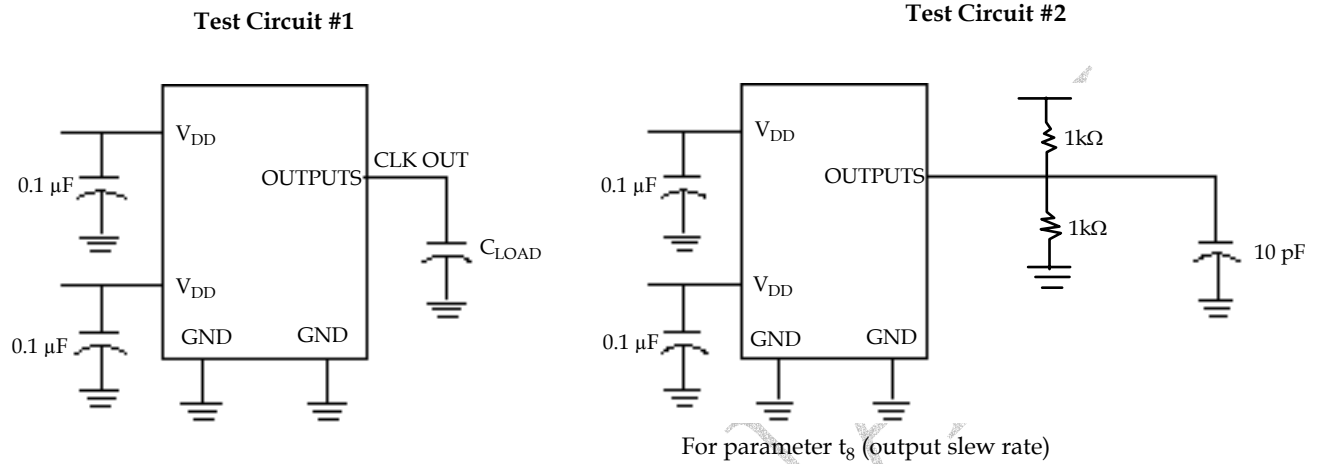


Device - Device Skew





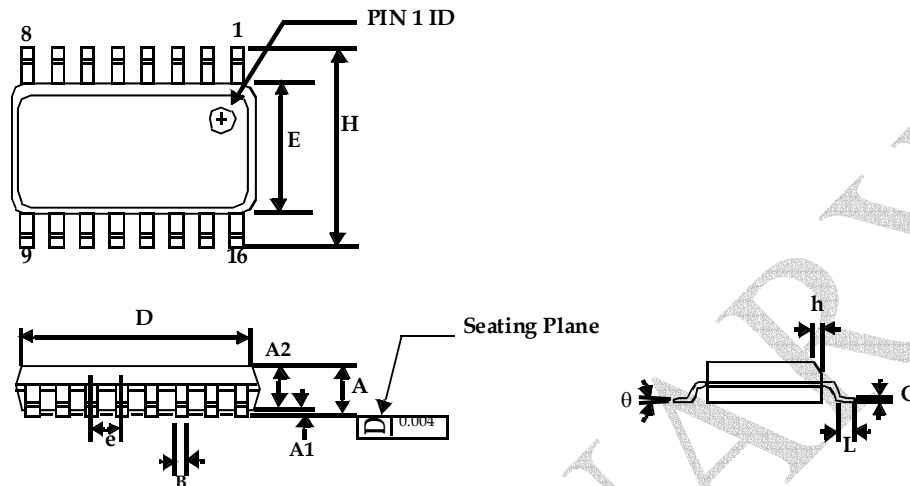
Test Circuits





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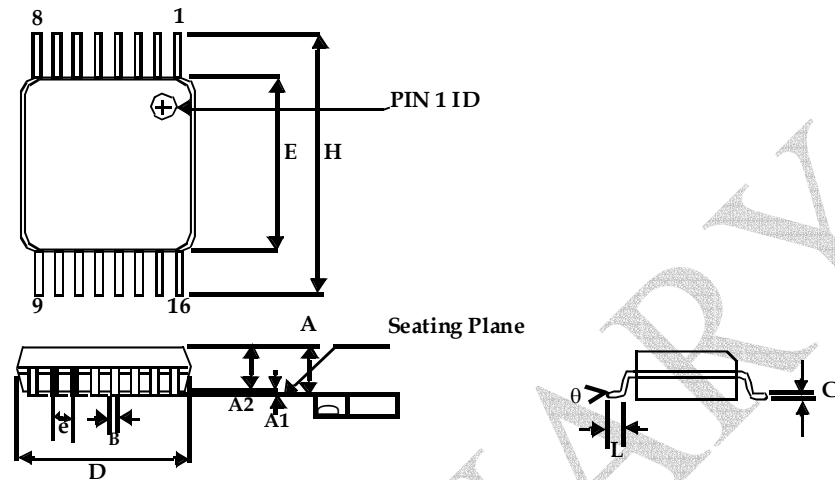
Package Information: 16-lead (150 Mil) Molded SOIC S16



	Dimensions in inches		Dimensions in millimeters	
	MIN	MAX	MIN	MAX
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
θ	0°	8°	0°	8°



rev 1.1

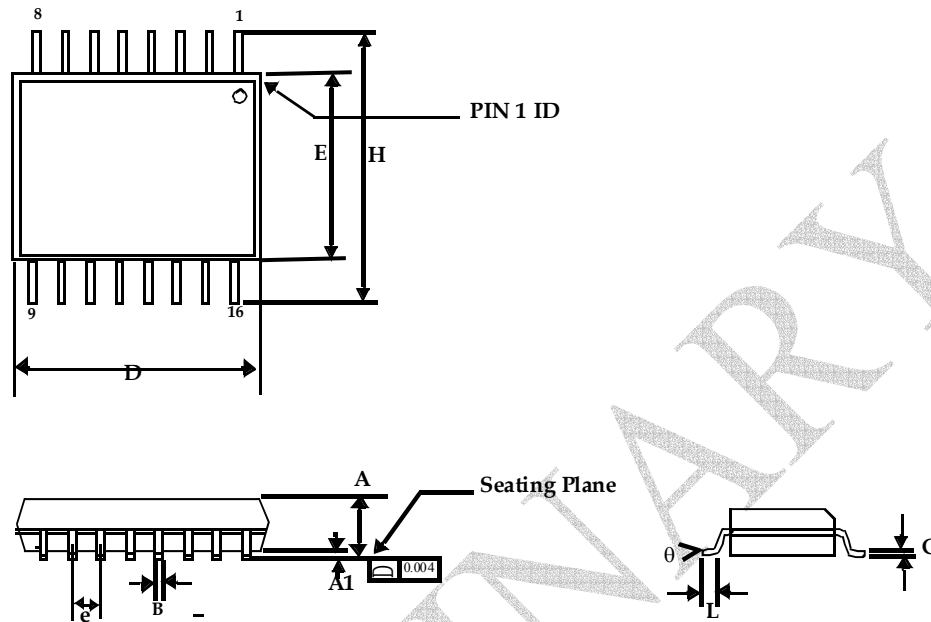
Package Information: 16-lead Thin Shrink Small Outline Package (4.40-MM Body)


	Dimensions in inches		Dimensions in millimeters	
	MIN	MAX	MIN	MAX
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.003	0.37	0.85	0.95
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	2.008	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.246	0.256	6.25	6.50
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°



rev 1.1

Package Information: 16-lead (150-mil) SSOP



Symbol	Dimensions in inches		Dimensions in millimeters	
	MIN	MAX	MIN	MAX
A	0.049	0.065	1.245	1.651
A1	0.004	0.010	0.102	0.254
B	0.008	0.012	0.203	0.305
C	0.007	0.010	0.178	0.254
D	0.189	0.197	4.801	5.004
E	0.150	0.157	3.81	3.988
e	0.025 BSC		0.635 BSC	
H	0.228	0.244	5.791	6.198
L	0.016	0.050	0.406	1.27
θ	0°	8°	0°	8°

**Ordering Codes**

Ordering Code	Package Name	Package Type	Operating Range
PCC028-02A SC-1	S16	16-pin 150 - mil SOIC	Commercial
PCC028-02A SI-1	S16	16-pin 150 - mil SOIC	Industrial
PCC028-02A ZC-1	Z16	16-pin 4.4mm TSSOP	Commercial
PCC028-02A ZI-1	Z16	16-pin 4.4mm TSSOP	Industrial
PCC028-02A OC-1	O16	16-pin 150 - mil SSOP	Commercial
PCC028-02A OI-1	O16	16-pin 150 - mil SSOP	Industrial

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Document Version: v1.1

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Dan Hariton / Alliance Semiconductor, dated 11-11-2003

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