QuickLogic® PolarPro® Device Data Sheet — QL1P600 and QL1P1000

Combining Low Power, Performance, Density, and Embedded RAM

Device Highlights

Low Power Programmable Logic

- As low as 25 µA
- 0.18 µm, six layer metal CMOS process
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- Up to 221 kilobits of SRAM
- Up to 244 I/Os available
- Up to one million system gates
- Nonvolatile, instant-on
- IEEE 1149.1 boundary scan testing compliant

Embedded Dual-Port SRAM

- Up to twenty-four dual-port 8-kilobit high performance SRAM blocks
- True dual-port capability
- Embedded synchronous/asynchronous FIFO controller
- Configurable and cascadable aspect ratio

Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Native support for DDR I/Os
- Bank programmable I/O standards: LVTTL, LVCMOS, LVCMOS18, PCI, SSTL2, SSTL3 and SSDL18

Advanced Clock Network

- Multiple low skew clock networks
  - 1 dedicated global clock network
  - 4 programmable global clock networks
- Quadrant-based segmentable clock networks
  - 80 quad clock networks per device
  - 16 quad clock networks per quadrant
- Two user Configurable Clock Managers (CCMs)

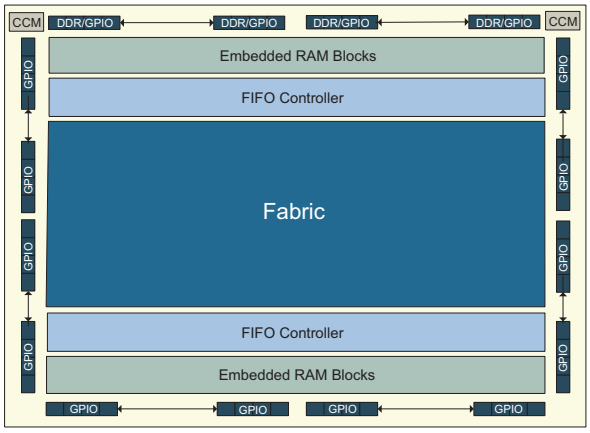
Very Low Power (VLP) Mode

- QuickLogic PolarPro has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby
- Enter VLP mode from normal operation in less than 250 µs (typical)
- Exit from VLP mode to normal operation in less than 250 µs (typical)

Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

Figure 1: QuickLogic PolarPro Block Diagram



Ultra-Low Power FPGA Combining Performance, Density, and Embedded RAM

Table 1: PolarPro QL1P600 and QL1P1000 Devices

Features	QL1P600	QL1P1000
Max Gates	600,000	1,000,000
Logic Cells	4,224	7,680
Max I/O	232	244
RAM Modules	24	24
FIFO Controllers	24	24
RAM bits	221,184	221,184
CCMs	2	2
Packages – LBGA (1.0 mm)	324	324

Process Data

The QuickLogic PolarPro is fabricated on a 0.18µ, six layer metal CMOS process. The core voltage is 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

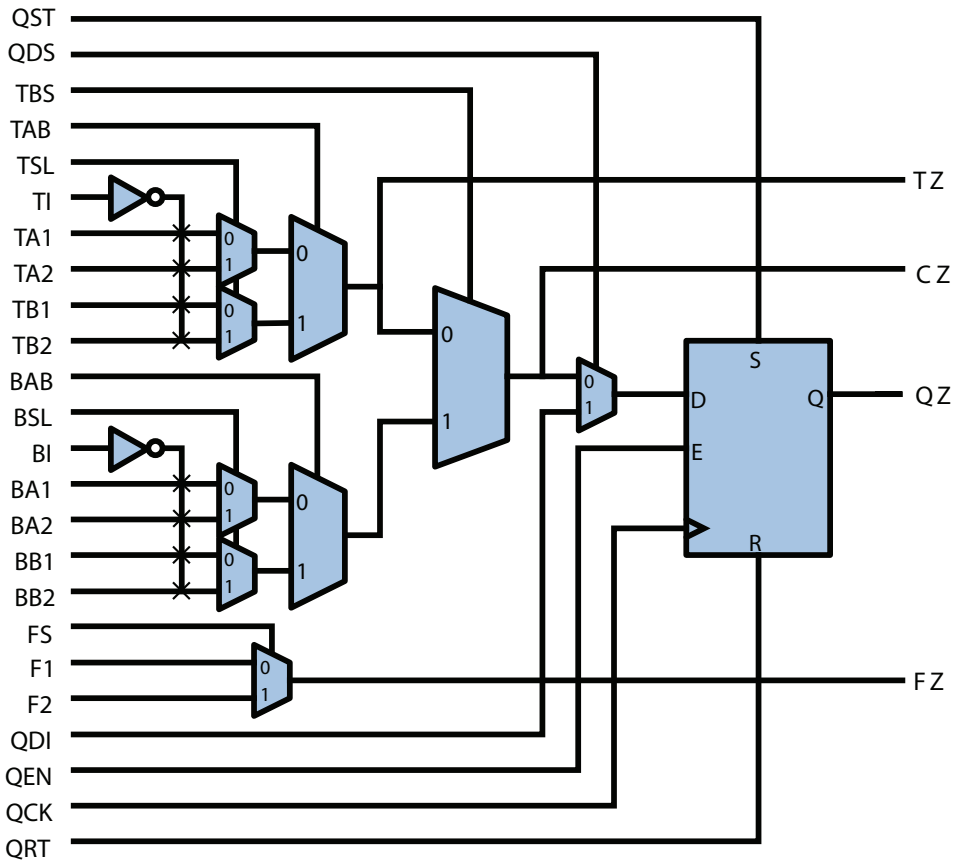
Programmable Logic Architectural Overview

The QuickLogic PolarPro logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 24 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The QuickLogic PolarPro logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Single dedicated register with clock enable, active high set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic that can also be configured as an edge-triggered master-slave D flip-flop

Figure 2: PolarPro Logic Cell



RAM Modules

The PolarPro QL1P600 and QL1P1000 devices have 8-kilobit (9,216 bits) RAM blocks.

The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data

Figure 3: 8-Kilobit Dual-Port RAM Block

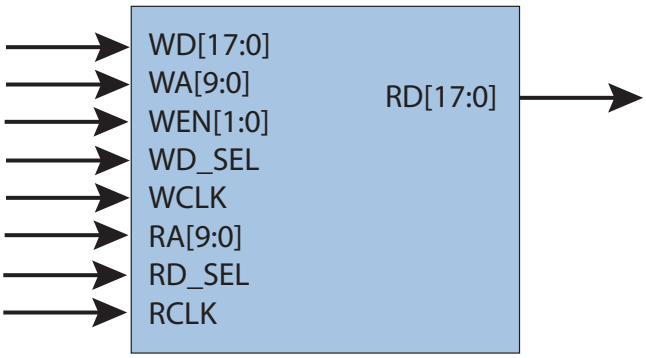


Table 2: RAM Interface Signals

Signal Name	Function
Inputs	
WD [17:0]	Write Data
WA [9:0]	Write Address
WEN [1:0]	Write Enable (two 9-bit enables)
WD_SEL	Write Chip Select
WCLK	Write Clock
RA [9:0]	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
Output	
RD [17:0]	Read Data

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 8-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal 8-kilobit dual-port RAM blocks can be concatenated vertically to create a 1024x18 RAM block or horizontally to create a 512x36 RAM block. A block diagram of horizontal and vertical concatenation is displayed in **Figure 4**.

Figure 4: Horizontal and Vertical Concatenation Examples

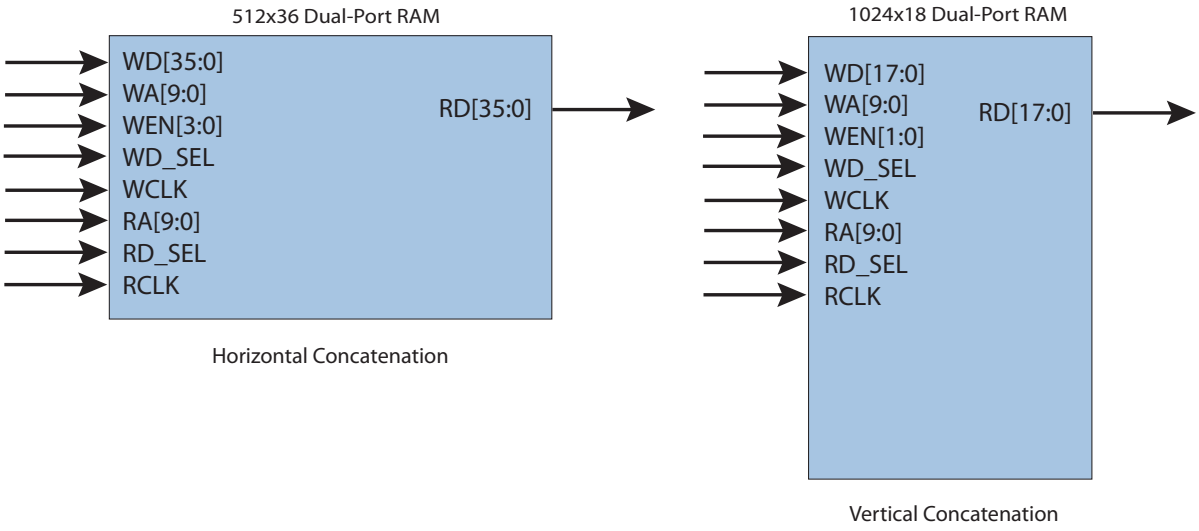


Table 3 shows the various RAM configurations supported by the PolarPro RAM modules.

Table 4: Available Dual-Port RAM Configurations

Device	Number of RAM Blocks	Depth	Width
QL1P600 QL1P1000	1	512	1-18
	1	1024	1-9
	2	512	1-36
	2	1024	1-18
	2	2048	1-9

True Dual-Port RAM

PolarPro dual-port RAM modules can also be concatenated to generate true dual-port RAMs. The true dual-port RAM module's Port1 and Port2 have completely independent read and write ports, and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, it is up to the designer to ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address must not be written to from both ports at the same time. However, it is possible to read from the same address. **Figure 5** shows an example of a 512x36 true dual-port RAM.

Figure 5: 512x36 8-Kilobit True Dual-Port RAM Block

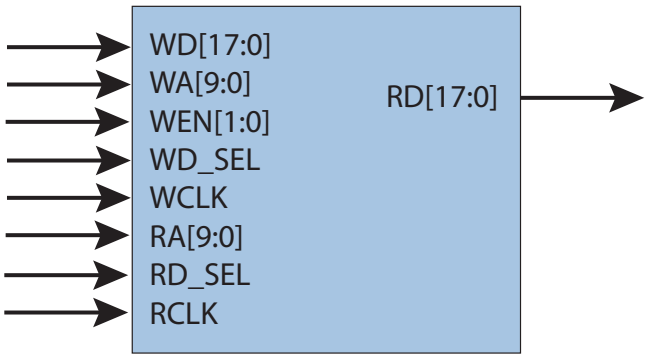


Table 5: Available True Dual-Port RAM Configurations

Device	Depth	Width
QL1P600 QL1P1000	512	1-36
	1024	1-18
	2048	1-9

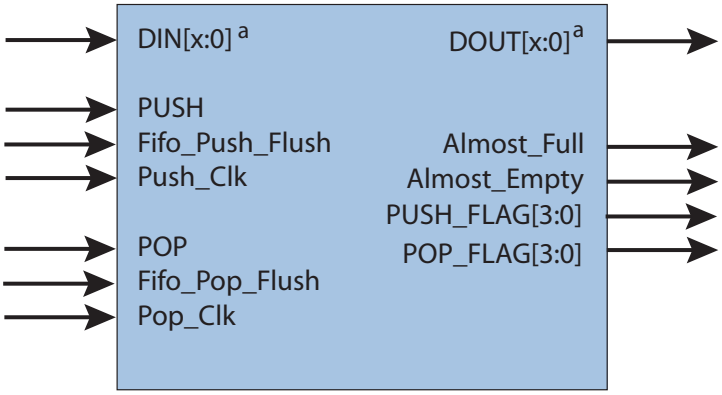
Embedded FIFO Controllers

Every RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The PolarPro FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Figure 6: FIFO Module



a. x = {1,2,3,....35}.

Table 6: Available FIFO Configurations

Device	Number of RAM Blocks	Depth	Supported Widths
QL1P600 QL1P1000	1	512	1-18 bits
	1	1024	1-9 bits
	2	512	1-36 bits
	2	1024	1-18 bits
	2	2048	1-9 bits

Table 7 lists the FIFO controller interface signals.

Table 7: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input
PUSH	1	I	Initiates a data push
Fifo_Push_Flush	1	I	Empties the FIFO
Push_Clk	1	I	Push data clock
POP Signals			
DOUT	1 to 36	O	Data bus output
POP	1	I	Initiates a data pop
Fifo_Pop_Flush	1	I	Empties the FIFO
Pop_Clk	1	I	Pop data clock
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available
Almost_Empty	1	O	Asserted when FIFO has one location used
PUSH_FLAG[3:0]	4	O	FIFO PUSH level indicator
POP_FLAG[3:0]	4	O	FIFO POP level indicator

Table 8 and **Table 9** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 8: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
1000	Room for 8 or more
1001	Room for 7
1010	Room for 6
1011	Room for 5
1100	Room for 4
1101	Room for 3
1110	Room for 2
1111	Room for 1
Others	Reserved

Table 9: FIFO POP Level Interface Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	2 entries in FIFO
0011	3 entries in FIFO
0100	4 entries in FIFO
0101	5 entries in FIFO
0110	6 entries in FIFO
0111	7 entries in FIFO
1000	8 or more entries in FIFO
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

FIFO Flush Procedure

Both PUSH and POP domains are provided with a flush input signal synchronized to their respective clocks. When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 7** and **Figure 8**).

As shown in **Figure 7**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 7 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), four POP clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (8), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.

Figure 7: FIFO Flush from PUSH Side

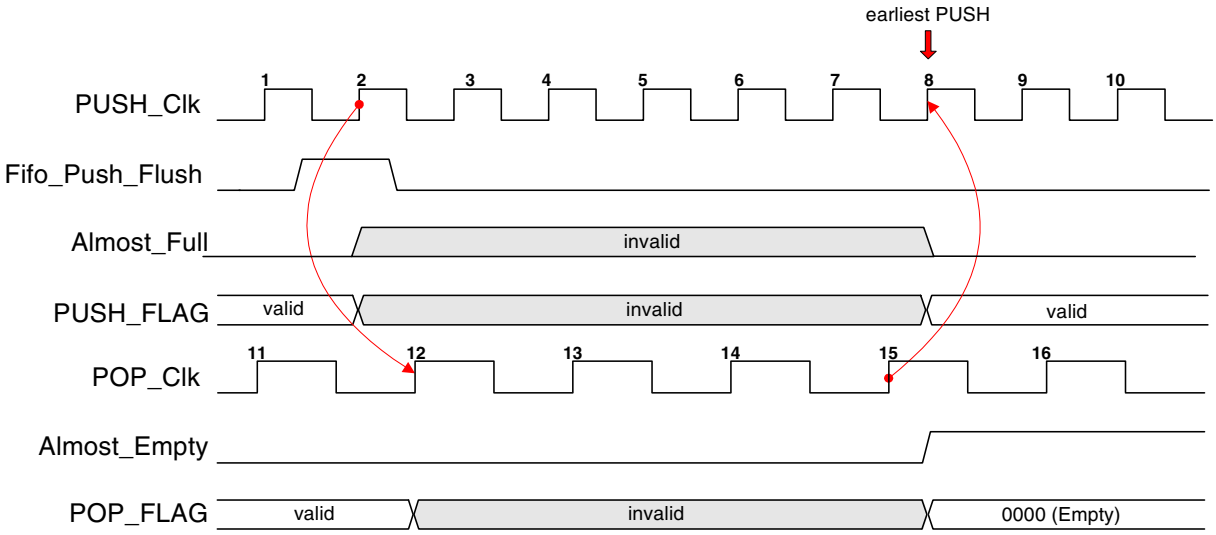


Figure 8 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), four PUSH clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (8), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.

Figure 8: FIFO Flush from POP Side

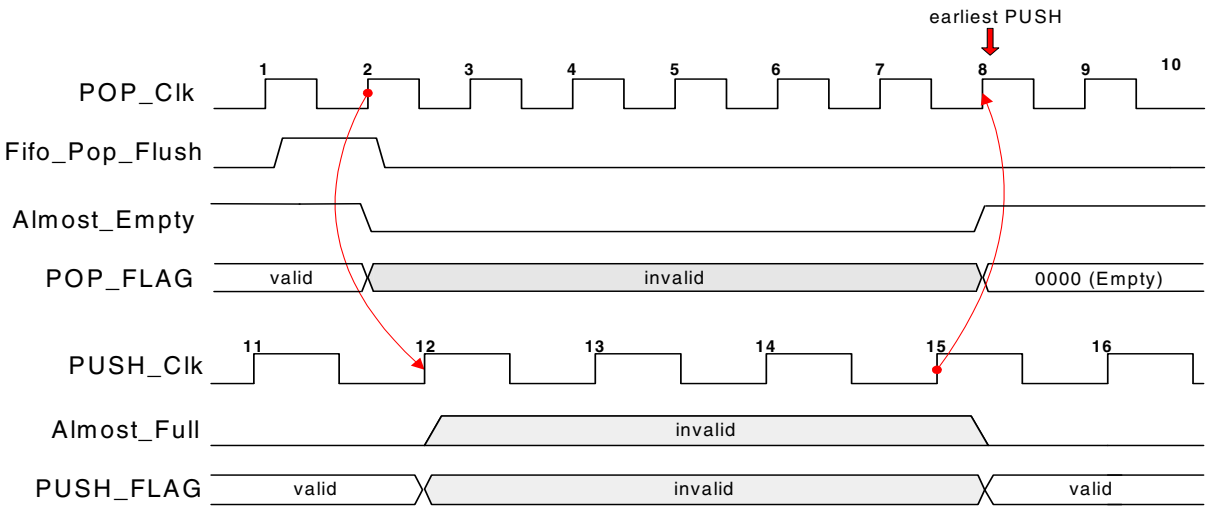


Figure 7 and **Figure 8** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

QL1P600 and QL1P1000 Clock Network Architecture

Distributed Clock Networks

The PolarPro QL1P600 and QL1P1000 clock network architecture consists of a 3-level H-tree network. The first level of each clock tree (shown as red in **Figure 9**), spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level (shown as magenta in **Figure 10**), spans from the quadrant clock network to the center of each sub-quadrant of the chip. The third level (shown as blue in **Figure 10**), spans from the sub-quadrant clock network to every logic cell inside that sub-quadrant. There are 4 sub-quadrants in each quadrant. Therefore, there are a total of 16 sub-quadrants in an entire device.

In each device there are five global clocks, 20 quadrant clocks, and 80 sub-quadrant clocks. All global clocks drive the quadrant clock network inputs, while all quadrant clock networks drive the sub-quadrant clock network inputs. The sub-quadrant clocks output to clock inversion muxes, which pass either the original input clock or an inverted version of the input clock to the logic cells in that sub-quadrant. The clock networks can drive RAM block clock inputs as well as the reset, set, enable, and clock inputs to I/O registers. Furthermore, the sub-quadrant clock outputs can be routed to all logic cell inputs.

Figure 9: Global Clock Network Architecture

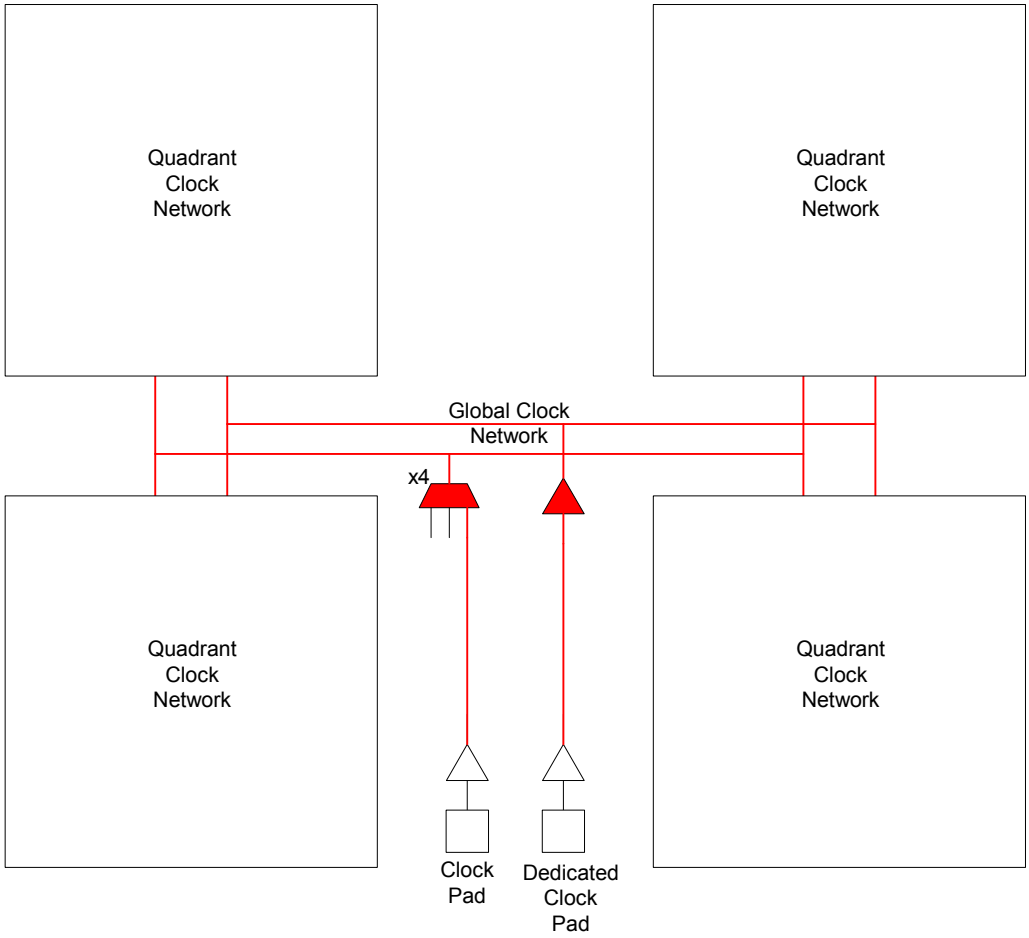
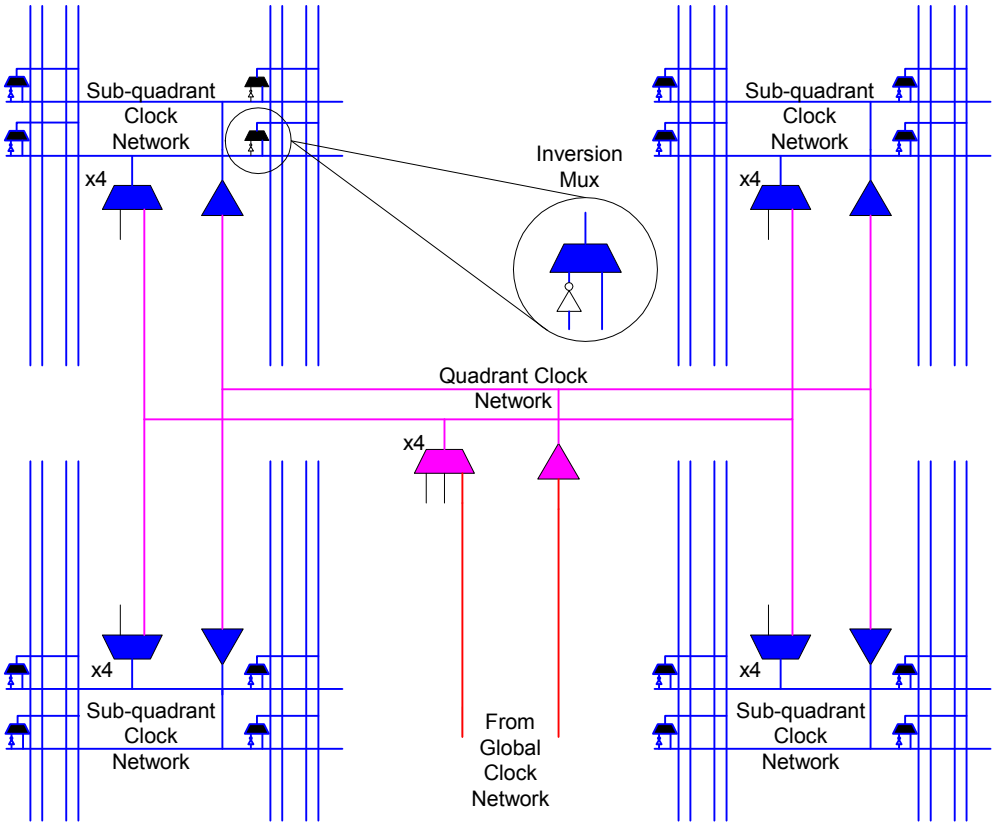


Figure 10: Quadrant Clock Network Architecture



Of the five global clock networks, four can be either driven directly by clock pads, Configurable Clock Manager (CCM) outputs, or internally generated signals. These four clock nets go through 3-input global clock muxes located in the middle of the die. See **Figure 11** for a diagram of a 3-input global clock mux. The fifth is a dedicated global clock network that goes directly to the quadrant quad-net clock network and is used as a dedicated fast clock.The dedicated clock network cannot be driven by internally routed signals. It can only be driven from the dedicated clock pad, DEDCLK(D).

Figure 11: Global Clock Structure

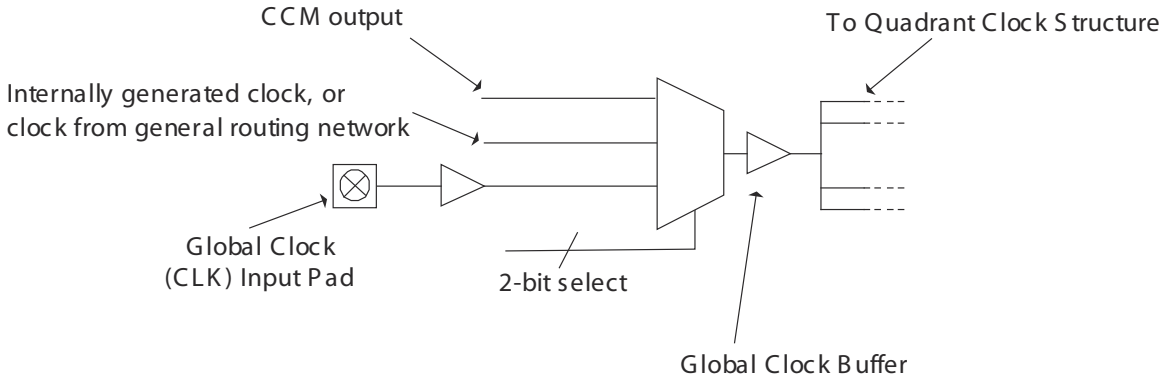
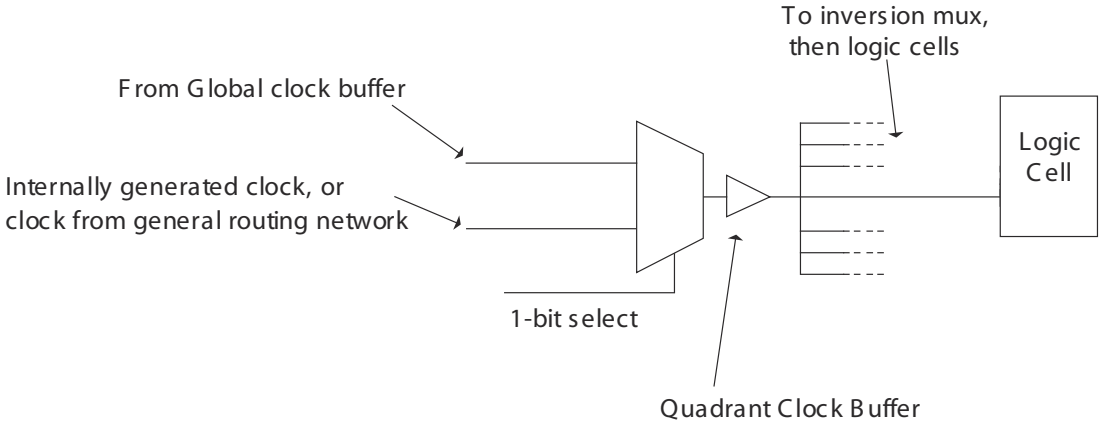


Figure 12 illustrates the quadrant clock 2-input mux.

Figure 12: Quadrant Clock Structure



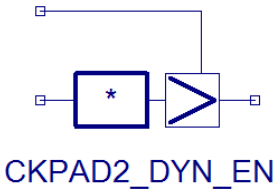
It is important to note that the select lines for the global clock and quad-net muxes are static signals and cannot be changed dynamically during device operation. For more information about global and quad-net clock networks and how to use them, refer to *Application Note 85 Clock Networks in PolarPro Devices*.

Dynamic Clock Enable

The QuickLogic PolarPro QL1P600 and QL1P1000 devices provide a powerful dynamic clock enable feature that allows designers to dynamically enable and disable clocks routed into the QuickLogic device. Associated with each of the five clock inputs is a clock enable, which is an interface signal that can be either dynamically controlled via a routable signal or tied high or low. Once an incoming clock is disabled, the clock is driven low internally. All the logic that is driven by the clock is held at the state when the clock was disabled. If a reset signal is passed through the clock pad, the dynamic disable should not be used.

As an additional feature, PolarPro devices have built-in deglitching circuitry to prevent clock glitching during transitions so that clocks can be enabled or disabled asynchronously without the possibility of false edge detection within the internal logic. The dynamic clock disable feature can be implemented in Verilog, VHDL, and schematic designs by instantiating the dynamic clock enable macro, CKPAD2_DYN_EN. **Figure 13**, shows the schematic representation of the dynamic clock enable macro.

Figure 13: Clock Pad Macro for Dynamic Clock Enable

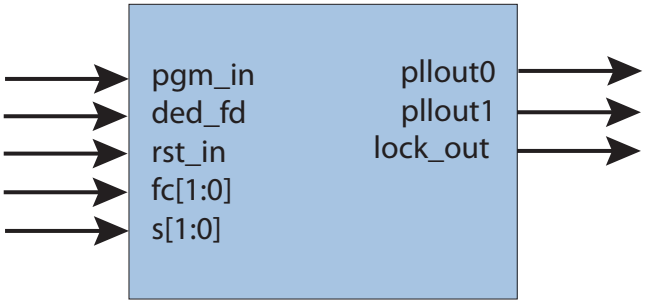


Configurable Clock Managers (CCMs)

The CCM features include:

- Input frequency range from 10 MHz to 150 MHz
- Output frequency range from 25 MHz to 160 MHz
- Output jitter is less than 200 ps peak-to-peak
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift).
- Fixed feedback path
- Output frequency lock time in less than 10 µs

Figure 14: Configurable Clock Manager



The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10 µs after reset to assert lock_out. The PolarPro CCMs have three modes of operation, based on the input frequency and desired output frequency. **Table 10** indicates the features of each mode.

Table 10: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 150 MHz	25 MHz to 150 MHz	PLL_MULT1
x2	15 MHz to 80 MHz	30 MHz to 160 MHz	PLL_MULT2
x4	10 MHz to 40 MHz	40 MHz to 160 MHz	PLL_MULT4

CCM Signals

Table 11 provides the name, direction, function and description of the CCM ports.

Table 11: CCM Signals

Signal Name	Direction	Function	Description
Routable Ports			
pgm_in	I	Programmable Input	CCM input source.
ded_fd	I	Dedicated Feedback	Automatically calculated and routed by the software tools.
rst_in	I	Reset	Active high reset: If rst_in is asserted, pllout0 and pllout1 are reset to 0. This signal must be asserted and then released for lock_out to assert.
pllout0	O	0° Phase Clock	0° phase clock output.
pllout1	O	Configurable Phase Clock	0°, 90°,180°, or 270° phase clock output with programmable delay.
lock_out	O	Lock Detect	Active high lock detection signal. Active when the pllout signals correctly output the configured functionality.
Static Ports			
fc[1:0]	I	Phase Shift Control	Determines whether pllout1 is 0°, 90°, 180°, or 270° degrees out of phase with pllout0[a].
s[1:0]	I	Set Mode	Determines pllout1 and pllout0 frequency multiplier (x1, x2, or x4).

a. The pllout1 output can vary up to -5% with respect to the pllout0 output. Therefore, QuickLogic recommends thorough post-layout simulation in order to verify satisfactory operation of the CCMs.

Table 12 and **Table 13** give the values used to configure the Set Mode and Phase Shift Control bits.

Table 12: Set Mode Values

s[1:0]	Multiplier
00	x1
01	x2
10	x4
11	Reserved

Table 13: Phase Shift Control Values

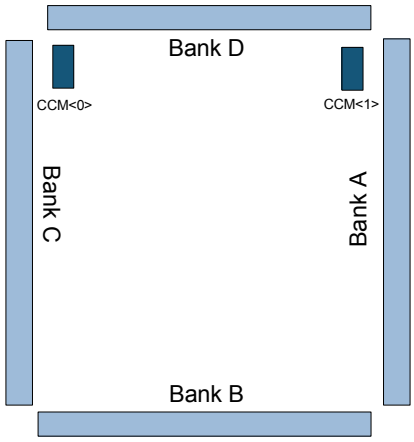
fc[1:0]	Phase Shift (Deg.)
00	0
01	90
10	180
11	270

Simultaneously Switching Outputs (SSOs) While Using a CCM

SSOs are outputs that transition at the same time in the same direction (either from VCC to GND or GND to VCC). To ensure that the CCMs never lose lock over all possible frequencies of operation, designers must follow the guidelines specified in this section when using the FPGA outputs as SSOs. These guidelines include the number of SSOs placed adjacent to the CCMs and the quality of the power filtering circuit sourcing the CCM block.

Figure 15 shows a basic layout of the four I/O banks (Bank A, Bank B, Bank C and Bank D) available in PolarPro devices and the relative placement of the two CCMs (CCM<0> and CCM<1>).

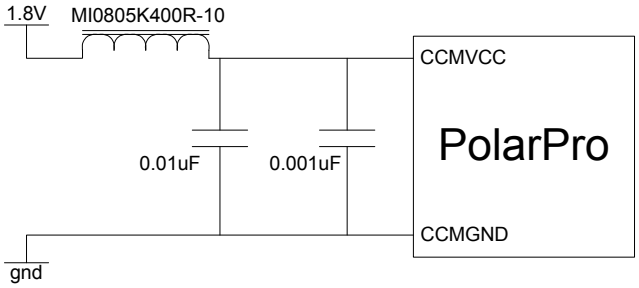
Figure 15: Basic Layout of I/O Banks and CCMs



For further information, contact QuickLogic support.

The power supply to the CCMs must have adequate noise filtering circuits. QuickLogic Reference Design boards use the noise filtering circuit shown in **Figure 16**.

Figure 16: Noise Filtering Circuit

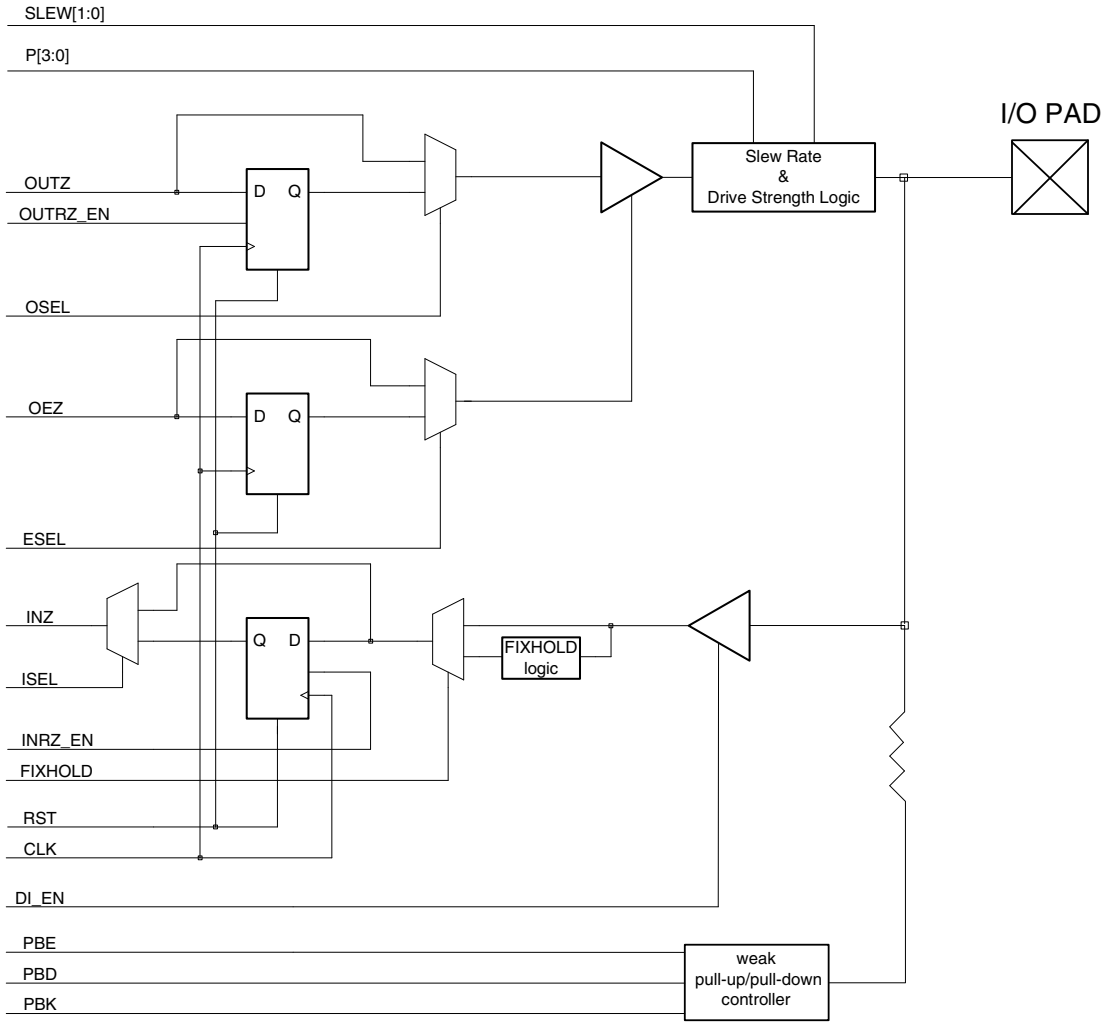


General Purpose Input Output (GPIO) Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Programmable weak keeper, programmable pull-up/pull-down control
- Programmable drive strength
- Configurable slew rate
- Support for JTAG boundary scan

Figure 17: PolarPro GPIO Cell



With bi-directional I/O pins and global clock input pins, the PolarPro device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single-ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage. Drive strength and slew rate are configured for an entire bank. Weak keeper, pull-up, and pull-down functions can be configured for individual I/O. The default configuration for QuickLogic QuickWorks software has the drive strength set to 4 and the slew rate set to wow.

Table 14: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
OUTZ	I	Data out from internal logic
OUTRZ_EN	I	Enable for registered OUTZ
OEZ	I	Tristate enable for the output signal
INZ	O	Input signal to the internal logic
INRZ_EN	I	Enable for registered INZ
RST	I	Reset for optional registers
CLK	I	Clock signal for optional registers
DI_EN	I	Enable for I/O input signal. Drives a 1 to internal logic when disabled.
Static Signals		
SLEW[1:0]	I	2-bit slew rate control
P[3:0]	I	Programmable drive strength
OSEL	I	Select signal for registered or flow through OUTZ
ESEL	I	Select signal for registered or flow-through OEZ
ISEL	I	Select signal for registered or flow-through INZ
FIXHOLD	I	Enable control for I/O input delay for hold fixing
PBE	I	Input signals for the weak keeper, pull-up/pull-down controller, see **Table 15** for functional behavior
PBD	I	
PBK	I	

Programmable Weak Keeper, Pull-Up, and Pull-Down

A programmable Weak Keeper, Pull-Up or Pull-Down controller is also available on each General Purpose I/O bank. When implementing the Weak Keeper, Pull-Up, and Pull-Down functions, each I/O can be configured separately. The I/O Weak Pull-Up and Pull-Down eliminates the need for external resistors. When PBK=1 the keeper block is placed into keeper mode. In the keeper mode, the pad pin (if the driver is tristated), will be kept at whichever level it was last forced, either by the driver itself, or by an external driver.

Table 15: Weak Pull-Up, and Pull-Down Controller

PBK	PBD	PBE	Function
0	0	0	Tristate (floating)
0	0	1	Weak Pull-Down
0	1	1	Weak Pull-Up
1	X	X	Weak Keeper (retains state)
0	1	0	Reserved

Programmable Drive Strength

Every GPIO has independent drive strength control. Twelve different drive strength levels are available for designers to choose from. For additional information about corresponding drive strength see **DC Characteristics** on page 27.

Programmable Slew Rate

Each I/O has programmable slew rate capability. The PolarPro GPIOs allow up to four different slew rate speeds (slow, fast, vfast, and wow). Slower slew rates can be used to reduce noise caused by I/O switching.

I/O interface standards are programmable on a per bank basis. **Table 16** illustrates the I/O bank configurations available. Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO supply inputs. A mixture of different I/O standards can be used on a PolarPro device. However, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO can be shared within the same bank (e.g., PCI and LVTTL).

Table 16: I/O Standards and Applications

I/O Standard	VCCIO Voltage	Application
LVTTL	3.3 V	General Purpose
LVCMOS25	2.5 V	General Purpose
LVCMOS18	1.8 V	General Purpose
PCI	3.3 V	PCI Bus Applications

DDRIO Cell Structure

QuickLogic PolarPro devices support DDRIOs, which allows clocking data on both the positive and negative clock edges. All PolarPro devices have one I/O bank (Bank D) that can be configured in either a GPIO bank or a DDRIO mode. When bank D is configured to DDRIO mode, it is further divided into DDRIO sets. Each set contains 12 I/Os, which include 8 DQs, 1 DQM, 1 DQS, 1 DQCK_N and 1 DQCK_P (for the differential clocks, refer to **Table 17**).

Figure 18: PolarPro DDRIO Block Diagram

Table 17: Available DDR Sets

PolarPro Device	Package	Number of DDR Sets
QL1P600	PS324	4
QL1P1000	PS324	4

Double Data Rate (DDR) I/O

The DDR features include:

- Programmable slew rate
- Programmable drive strength
- Programmable pull-up

Figure 19: DDRIO DQ Configuration

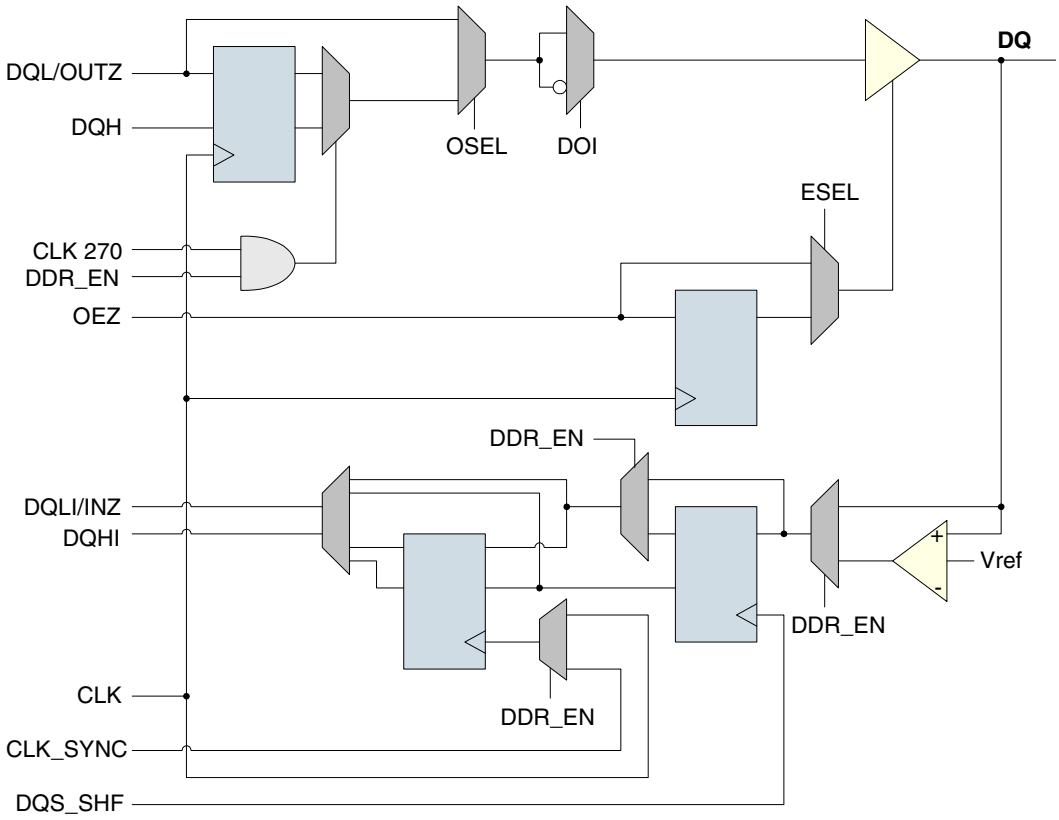


Figure 20: DDRIO DQS Configuration

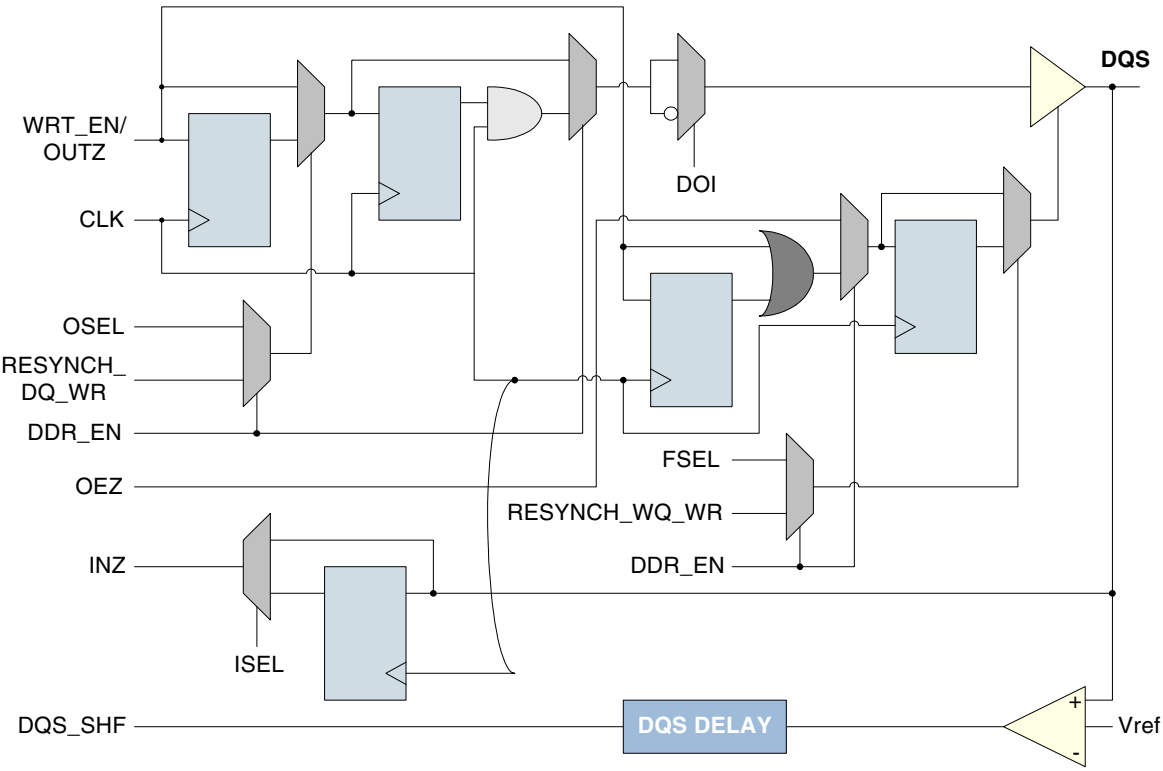


Table 18: DDR DQ Fabric Interface Signals

Signal Name	Direction	Function
Routable Signals		
DDR_EN	I	Enable DDR function, otherwise function will be that of GPIO.
CLK270	I	Shifted clock used in center-aligning data with DQS in writing out data.
PDB	I	Used as control for differential power-down.
CLK	I	System clock signal from the programmable fabric.
RST	I	Reset signal for registers inside the I/O.
INRZ_EN	I	Enable for registered DQLI / INZ.
DQH	I	Higher bit DQ signal output from core.
OUTRZ_EN	I	GPIO: enable for registered OUTZ signal.
DQL / OUTZ	I	DDR(DQL): lower bit DQ signal output from core. GPIO(OUTZ): data out from core with optional register.
OEZ	I	Tristate enable for the output signal with optional register.
DQHI	O	Higher bit DQ signal input to core with optional register for resynchronization.
DQLI / INZ	O	DDR(DQLI): lower bit DQ signal input to core with optional register for resynchronization. GPIO(INZ): data in signal to core with optional register.

Table 18: DDR DQ Fabric Interface Signals *(Continued)*

Signal Name	Direction	Function
Static Signals		
resync_DQ_rd	I	Signal to enable resynching of DQ being read to avoid setup violations inside the programmable fabric.
resync_DQ_wr	I	Signal to enable resynching of DQ being written to avoid setup violations inside the I/O.
SLEW[1:0]	I	2-bit slew rate control.
P[3:0]	I	Pull-up programmable drive strength.
N[3:0]	I	Pull-down programmable drive strength.
FIXHOLD	I	Enable control for I/O input delay for hold fixing.
PBE	I	Input signal for weak pull-up controller.
DOI	I	Used as control for data out inversion.
ISEL	I	Select signal for registered or flow through INZ.
OSEL	I	Select signal for registered or flow through OUTZ.
ESEL	I	Select signal for registered or flow through OEZ.

Table 19: DDR DQS Interface Signals

Signal Name	Direction	Function
Routable Signals		
CLK_SYNC	I	Optional resynchronization clock to sync incoming data with the programmable fabric system clock.
PDB	I	Control for differential power-down.
CLK	I	System clock signal from the programmable fabric.
RST	I	Reset signal for registers inside the I/O.
INRZ_EN	I	GPIO: enable for registered INZ.
INZ	O	GPIO: data in signal to core with optional register.
DQS_BR_REL	I	A read burst signal used to mask the end of DQS pulses to avoid unnecessary glitches that will result in clocking-in unwanted data.
OEZ	I	Tristate enable for the output signal with optional register.
OUTRZ_EN	I	Enable for registered or flow-through WRT_EN/OUTZ.
WRT_EN	I	DDR(WRT_EN): write enable signal. GPIO(OUTZ): data out from core with optional register.
Static Signals		
CLK_SYNC_DEL_CTRL[4:0]	I	Setting to program delay for CLK_SYNC.
CLK_SYNC_INV	I	Option to invert CLK_SYNC.
resync_DQ_wr	I	Signal to enable resynching of DQ being written to avoid setup violations inside I/O.
DDR_EN	I	Enable DDR function, otherwise function will be that of GPIO.
FIXHOLD	I	Enable control for I/O input delay for hold fixing.

Table 19: DDR DQS Interface Signals *(Continued)*

Signal Name	Direction	Function
PBE	I	Input signal for weak pull-up controller.
SLEW[1:0]	I	Slew rate control setting.
P[3:0]	I	Pull-up programmable drive strength.
N[3:0]	I	Pull-down programmable drive strength.
DOI	I	Control for data out inversion.
ISEL	I	DDR: selects between VREF (ISEL=0) or PADI (ISEL=1), to connect to the inverting-input of a differential amplifier inside the DDR I/O driver. GPIO: Select signal for registered or flow-through INZ.
OSEL	I	Select signal for registered or flow-through WRT_EN/OUTZ.
ESEL	I	Select signal for registered or flow-through DQS_OE/OEZ.
DQS_DEL_ CTRL[3:0]	I	Setting to program delay of DQS signal.

DDRIO in GPIO Mode

DDR in GPIO mode features include programmable I/O standards via the VCCIO input pins (1.8V LVCMOS, 2.5V LVCMOS, and 3.3V LVTTL).

NOTE: DDRIOs do not support PCI. For PCI support use the general purpose I/Os.

Very Low Power (VLP) Mode

The QuickLogic PolarPro devices have a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the total standby current down to less than 10 µA at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

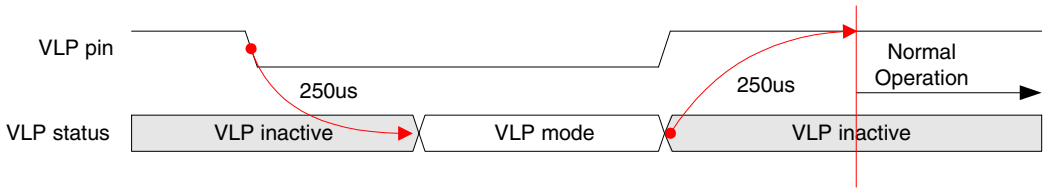
When a PolarPro device goes into VLP mode, the following occurs:

- All logic cell registers and GPIO registers values are held
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- DDRIO outputs are pulled down through a weak pull down circuit
- Clock pad inputs are gated
- CCMs are held in the reset state

The entire operation from normal mode to VLP mode requires 250 µs (300 µs maximum). As mentioned in the VLP behavioral description above, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve data retention GPIO should not be used for a set, reset, or clock signal. During the transition from VLP mode to normal operation, the VLP pin can draw up to 1.5 mA. Consequently, if using a pull-up resistor, use a pull-up resistor with a value that is less than 2 KΩ .

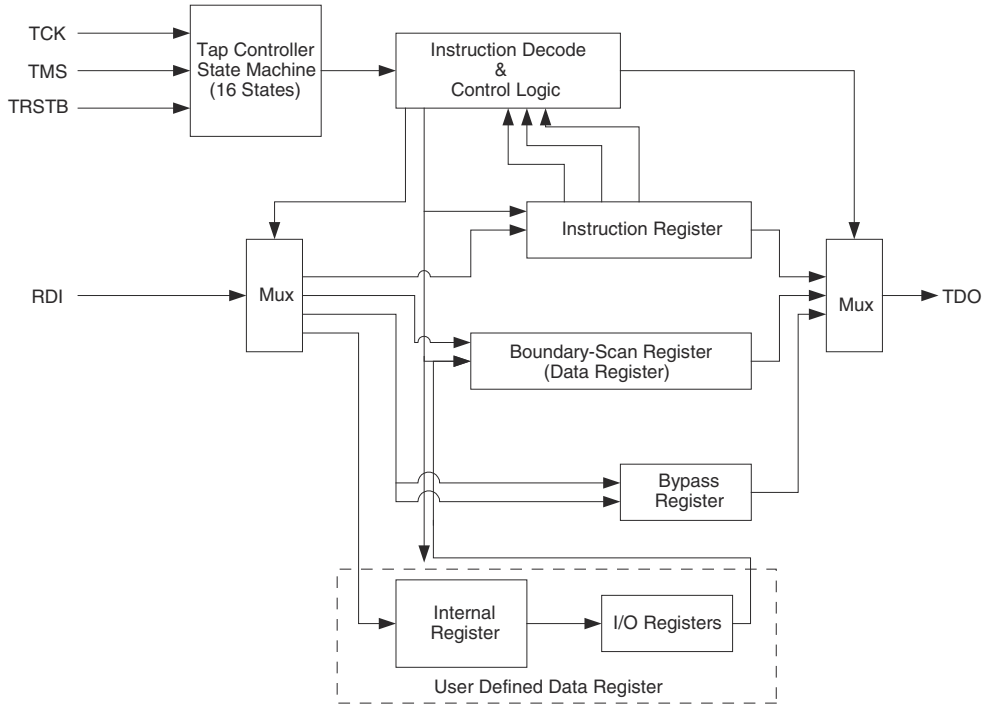
As the device exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the device. Furthermore, since the CCMs were in a reset state during VLP mode, they will have to re-acquire the correct output signals before asserting lock_out. The time required to go from VLP mode to normal operation is 250 µs (300 µs maximum). **Figure 21** displays the delays associated with entering and exiting VLP mode.

Figure 21: Typical VLP Mode Timing



Joint Test Access Group (JTAG) Information

Figure 22: JTAG Block Diagram



QuickLogic's PolarPro devices comply with IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture. The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests. JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for comprehensive verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG BSDL Support

- Boundary Scan Description Language (BSDL)
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 20** through **Table 23**.

Table 20: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.2 V	Latch-up Immunity	±100 mA
VCCIO Voltage	-0.5 V to 4.0 V	ESD Pad Protection	2 kV
VREF Voltage	-0.5 V to 2.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 21: Recommended Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
VCC	Supply Voltage	1.71	1.89	1.71	1.89	1.71	1.89	V
VCCIO	I/O Input Tolerance Voltage	1.71	3.60	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature	-55	125	-40	100	0	85	°C

Table 22: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-	-	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	-	1	µA
C_I	I/O Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
C_{CLOCK}	Clock Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
I_{REF}	Quiescent Current on INREF	-	-	-	5	µA
I_{PD}	Current on programmable pull-down	VCCIO = 3.6 V	-200	-	-50	µA
		VCCIO = 2.75 V	-150	-	-25	µA
		VCCIO = 1.89 V	-100	-	-10	µA
I_{PU}	Current on programmable pull-up	VCCIO = 3.6 V	50	-	200	µA
		VCCIO = 2.75 V	25	-	150	µA
		VCCIO = 1.89 V	10	-	100	µA
I_{VLP}	Quiescent Current on VLP pin	VLP=3.3	-	1	10	µA
I_{CCM}	Quiescent Current on each CCMVCC	VCC=1.89 V	-	1	10	µA
I_{VCC}	Quiescent Current	VLP=GND	-	25	-	µA
		VLP=3.3V	-	200	-	µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V	-	2	20	µA
		VCCIO = 2.75 V	-	2	20	µA
		VCCIO = 1.89 V	-	2	20	µA

Table 23: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 23** represents the JEDEC and PCI specification. QuickLogic devices either meet or exceed these requirements.

Table 24 and **Table 25** lists the worst case process (T_J=125°C) output currents (in mA) across the output driver at three levels of I/O voltages. All drive strength data was measured at I/O voltages of 0.4 V and VCCIO - 0.4 V.

Table 24: GPIO Programmable Drive Strength

Drive Strength	IOH (mA)			IOL (mA)		
	1.8V	2.5V	3.3V	1.8V	2.5V	3.3V
1	2.2	2.8	3.2	1.7	2.3	2.7
2	4.1	5.2	5.9	3.4	4.4	5
3	6.2	7.8	8.8	5.1	6.7	7.6
4	8	10	11.2	6.6	8.6	9.7
5	10	12.4	13.9	8.3	10.7	12.1
6	11.8	14.6	16.3	9.8	12.7	14.2
7	13.7	16.9	18.9	11.5	14.7	16.6
8	15.3	18.9	21	12.9	16.5	18.5
9	17.1	21.1	23.4	14.5	18.5	20.7
10	18.8	23	25.5	15.9	20.2	22.6
11	20	25	27.6	17.4	22	24.6
12	21.7	26.4	29.1	18.6	23.5	26.1
N/A	Reserved					

Table 25: DDRIO Programmable Drive Strength

Drive Strength	IOH			IOL		
	1.8V	2.5V	3.3V	1.8V	2.5V	3.3V
1	1.9	2.7	3.1	2.1	2.8	3.3
2	3.4	4.4	4.9	2.9	3.8	4.4
3	5.4	7	7.9	4.9	6.5	7.4
4	6.8	8.6	9.6	5.7	7.3	8.2
5	8.6	11	12.4	7.6	9.9	11.2
6	9.9	12.5	14	8.3	10.7	12
7	11.8	14.8	16.6	10.2	13.2	14.9
8	11.6	14.6	16.3	10.2	13.2	14.9
9	12.9	16	17.7	10.9	14	15.7
10	14.7	18.2	20.2	12.7	16.3	18.3
11	15.9	19.5	21.6	13.4	17.1	19
12	17.4	21.6	23.9	15.1	19.2	21.3
13	19.2	23.7	26.2	16.3	20.9	23.5
14	21.5	26.3	28.9	18.2	23	25.6
15	22	27.1	29.8	18.7	23.9	26.8
N/A	Reserved					

AC Characteristics

AC specifications are provided in **Table 26** through **Table 38**. Logic cell diagrams and waveforms are provided in **Figure 23** through **Figure 36**. All of the following AC timing numbers are for worst case Commercial (T = 85°C Junction, V= 1.71V), and worst case Industrial (T = 100°C Junction, V=1.71V) conditions.

Figure 23: PolarPro Logic Cell

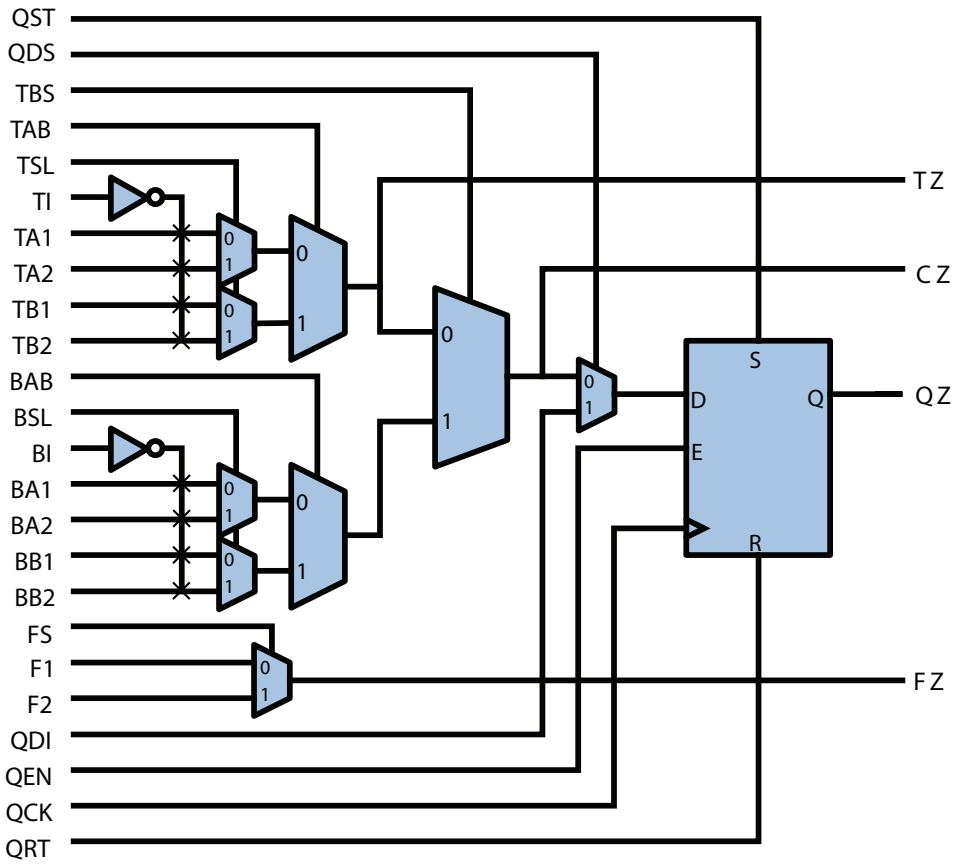


Table 26: Logic Cell Delays

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{PD}	Combinatorial delay of the longest path: time taken by the combinatorial circuit to output	0.32 ns	0.59 ns	0.34 ns	0.62 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.23 ns	0.56 ns	0.24 ns	0.58 ns
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	N/A	0 ns	N/A
t_{ESU}	Enable setup time: time the enable input of the flip-flop must be stable before the active clock edge	0.23 ns	0.85 ns	0.89 ns	0.24 ns
t_{EHL}	Enable hold time: time the enable input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	0.48 ns	0.52 ns	0.50 ns	0.55 ns
t_{CWHI}	Clock high time: required minimum time the clock stays high	0.46 ns	0.46 ns	0.46 ns	0.46 ns
t_{CWLO}	Clock low time: required minimum time that the clock stays low	0.46 ns	0.46 ns	0.46 ns	0.46 ns
t_{SET}	Set delay: time between when the flip-flop is “set” (high) and when the output is consequently “set” (high)	0.60 ns	0.60 ns	0.61 ns	0.61 ns
t_{RESET}	Reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	0.68 ns	0.68 ns	0.71 ns	0.71 ns
t_{SW}	Set width: time that the SET signal must remain high/low	0.30 ns	0.30 ns	0.30 ns	0.30 ns
t_{RW}	Reset width: time that the RESET signal must remain high/low	0.30 ns	0.30 ns	0.30 ns	0.30 ns

Figure 24: Logic Cell Flip-Flop Timings—First Waveform

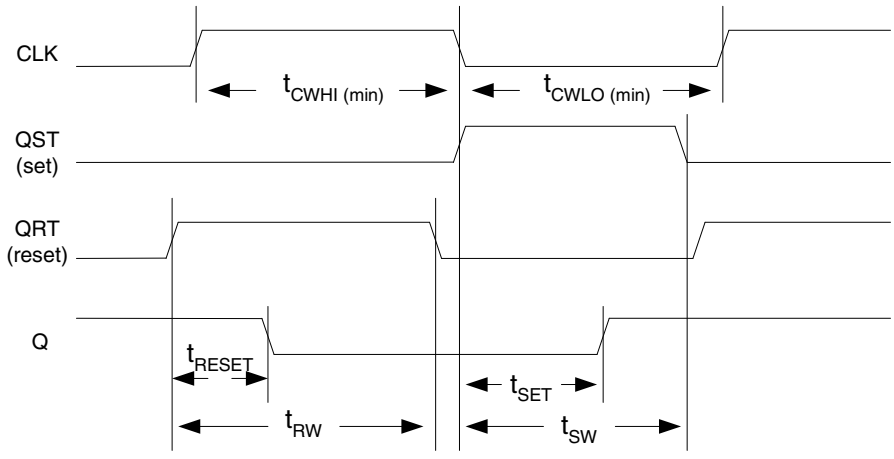


Figure 25: Logic Cell Flip-Flop Timings—Second Waveform

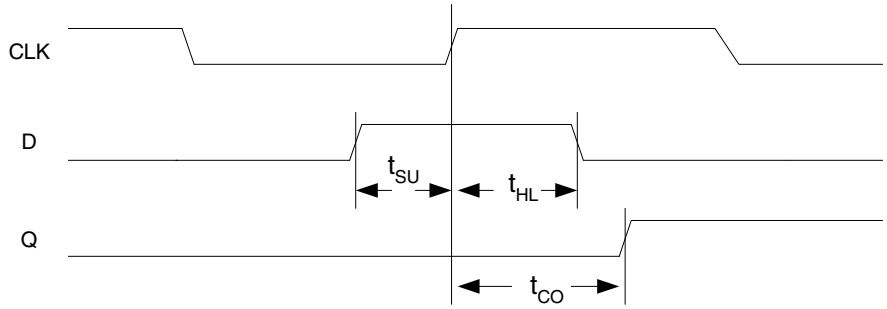


Figure 26: PolarPro Clock Network

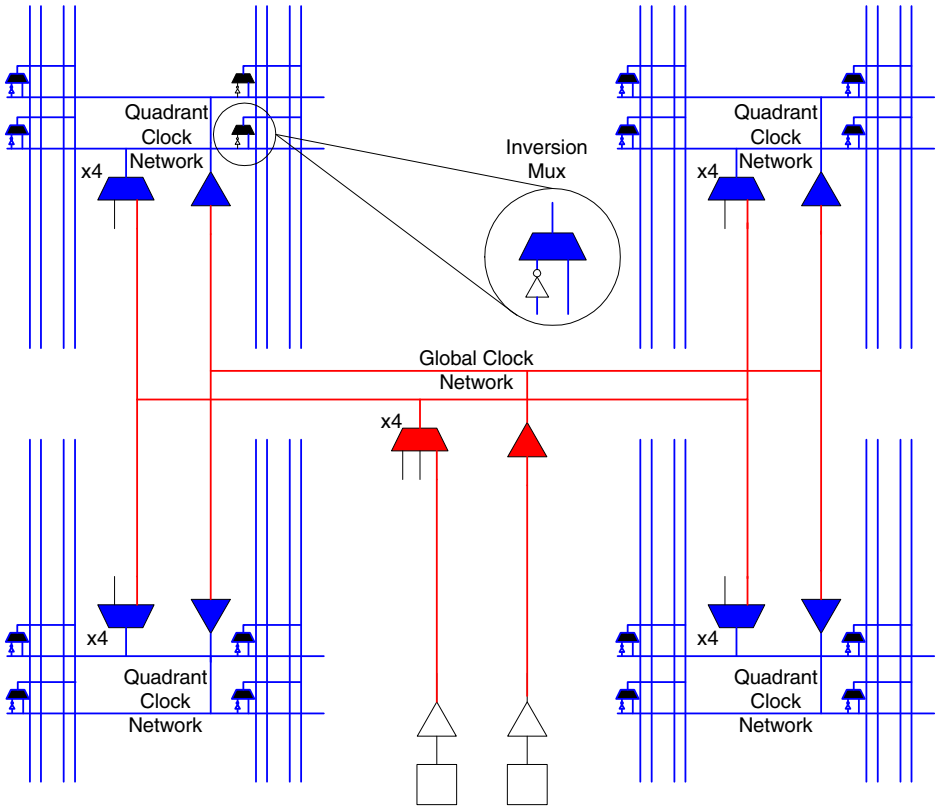


Table 27: PolarPro Tree Clock Delay

Clock Segment	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{PGCK}	Delay from global clock pad input to quadrant network	TBD	TBD	TBD	TBD
t_{PDCK}	Delay from dedicated clock pad input to quadrant network	TBD	TBD	TBD	TBD
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	TBD	TBD	TBD	TBD
t_{GSKEW}	Global delay clock skew	TBD	TBD	TBD	TBD
t_{DSKEW}	Dedicated clock skew	TBD	TBD	TBD	TBD

RAM Timing

Figure 27: RAM Module

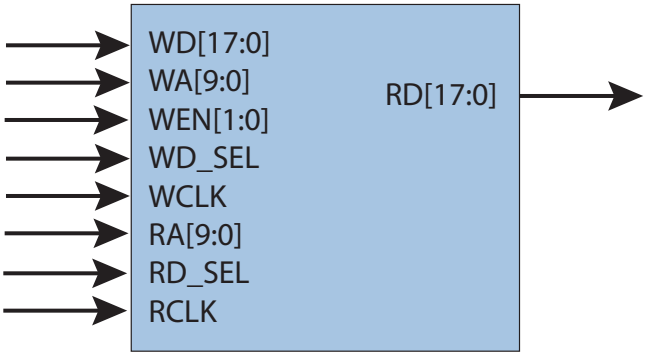


Table 28: RAM Cell Synchronous Write Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.29 ns	1.10 ns	0.31 ns	1.28 ns
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	0.21 ns	0 ns	0.20 ns
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.31 ns	1.74 ns	0.40 ns	2.21 ns
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	0.22 ns	0 ns	0.17 ns
t_{SWS}	WD_SEL setup time to WCLK: time WRITE CHIP SELECT must be stable before the active edge of the WRITE CLOCK	0.42 ns	1.10 ns	0.49 ns	1.28 ns
t_{HWS}	WD_SEL hold time to WCLK: time WRITE CHIP SELECT must be stable after the active edge of the WRITE CLOCK	0 ns	0.04 ns	0 ns	0.04 ns
t_{SWE}	WEN setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.63 ns	1.10 ns	0.74 ns	1.28 ns
t_{HWE}	WEN hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	0 ns	0 ns	0 ns

Figure 28: RAM Cell Write Timing

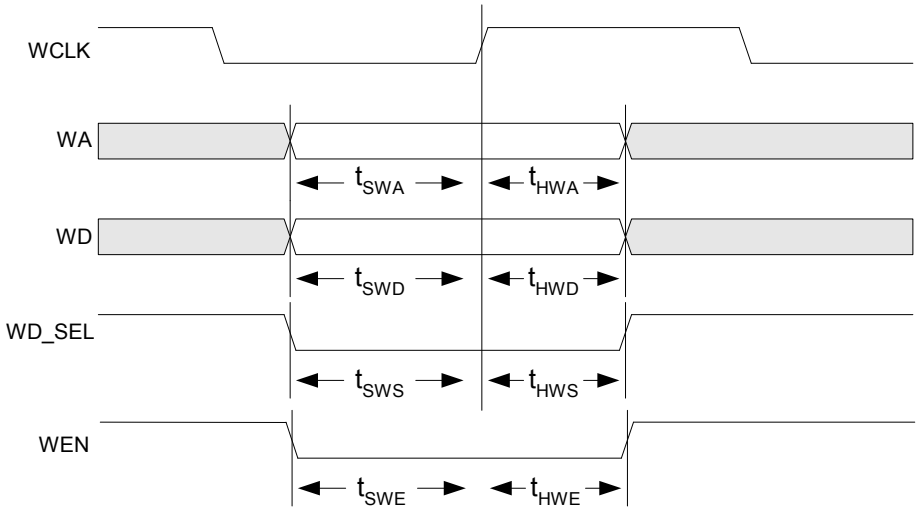
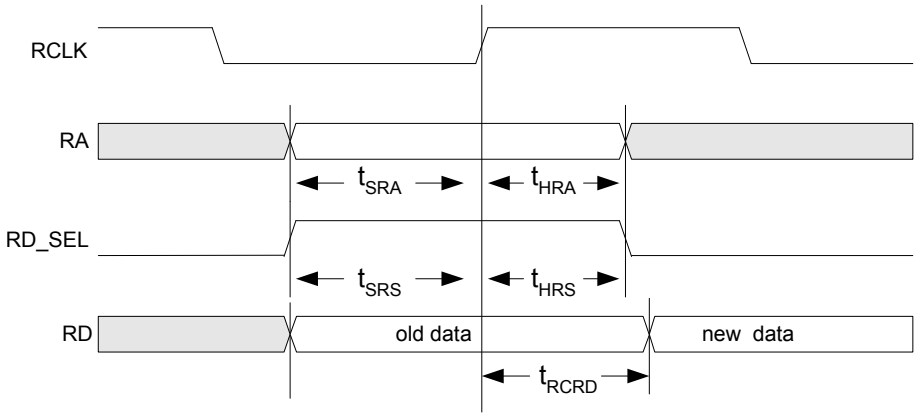


Table 29: RAM Cell Synchronous Read Timing

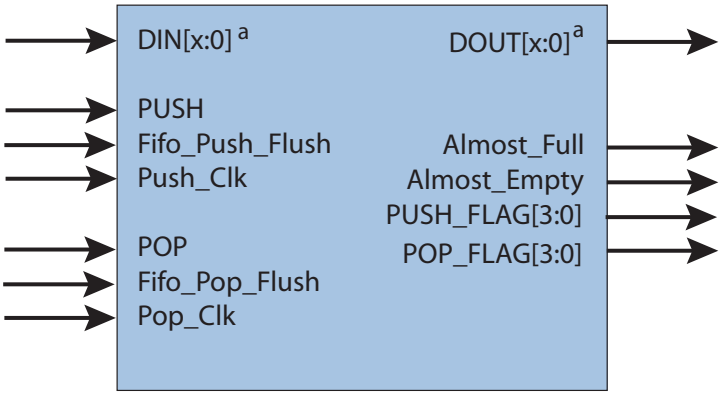
Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.29 ns	1.10 ns	0.31 ns	1.28 ns
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	0.21 ns	0 ns	0.20 ns
t_{SRS}	RD_SEL setup time to RCLK: time the READ CHIP SELECT must be stable before the active edge of the READ CLOCK	0.42 ns	1.10 ns	0.49 ns	1.28 ns
t_{HRS}	RD_SEL hold time to RCLK: time the READ CHIP SELECT must be stable after the active edge of the READ CLOCK	0 ns	0.04 ns	0 ns	0.04 ns
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	2.62 ns	5.67 ns	2.69 ns	5.88 ns

Figure 29: RAM Cell Read Timing



FIFO Timing

Figure 30: FIFO Module



a. x = {1,2,3,....35}.

Table 30: FIFO PUSH Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SPUSHD}	DIN setup time to Push_Clk: time DIN must be stable before the active edge of the FIFO Push clock	0.31 ns	1.74 ns	0.40 ns	2.21 ns
t_{HPUSHD}	DIN hold time to Push_Clk: time DIN must be stable after the active edge of the FIFO Push clock	0 ns	0.22 ns	0 ns	0.17 ns
$t_{SPUSHEN}$	PUSH setup time to Push_Clk: time PUSH must be stable before the active edge of the FIFO Push clock	1.07 ns	1.57 ns	1.38 ns	2.0 ns
$t_{HPUSHEN}$	PUSH hold time to Push_Clk: time PUSH must be stable after the active edge of the FIFO Push clock	0 ns	0 ns	0 ns	0 ns
$t_{SPUSHFLUSH}$	FLUSH setup time to Push_Clk: time Fifo_Push_Flush must be stable before the active edge of the FIFO Push clock	1.11 ns	1.74 ns	1.43 ns	2.21 ns
$t_{HPUSHFLUSH}$	FLUSH hold time to Push_Clk: time Fifo_Push_Flush must be stable after the active edge of the FIFO Push clock	0 ns	0 ns	0 ns	0 ns
t_{COAF}	Clock-to-out of Almost Full	2.66 ns	3.34 ns	2.72 ns	3.42 ns
$t_{COPUSHFLAG}$	Clock-to-out of FIFO Push level indicator	2.36 ns	4.20 ns	2.41 ns	4.32 ns

Figure 31: FIFO PUSH Timing

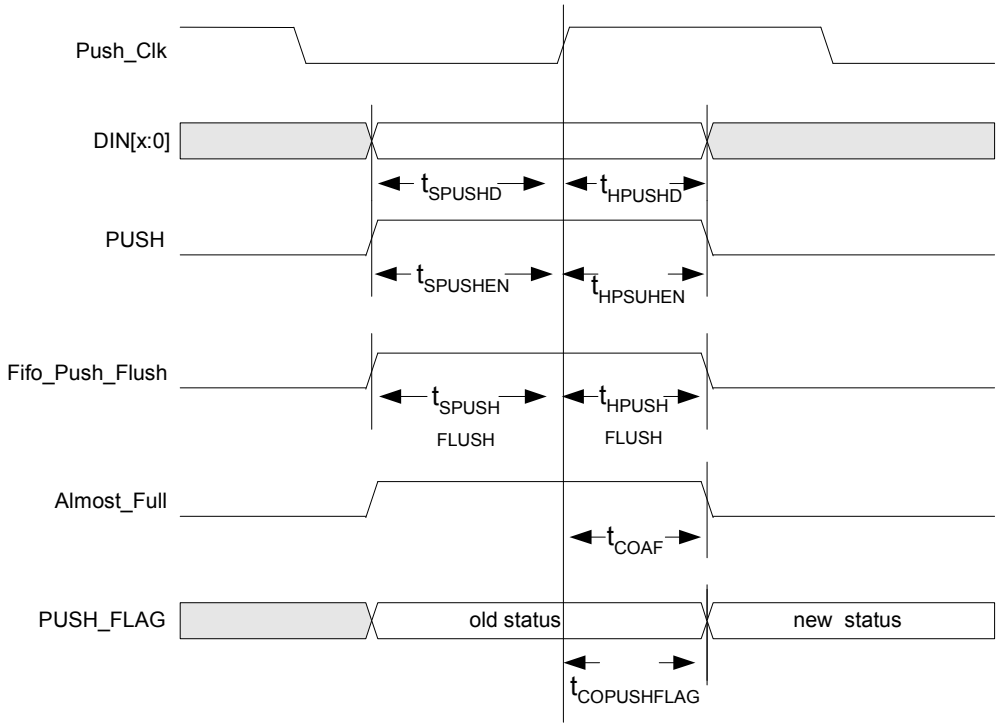
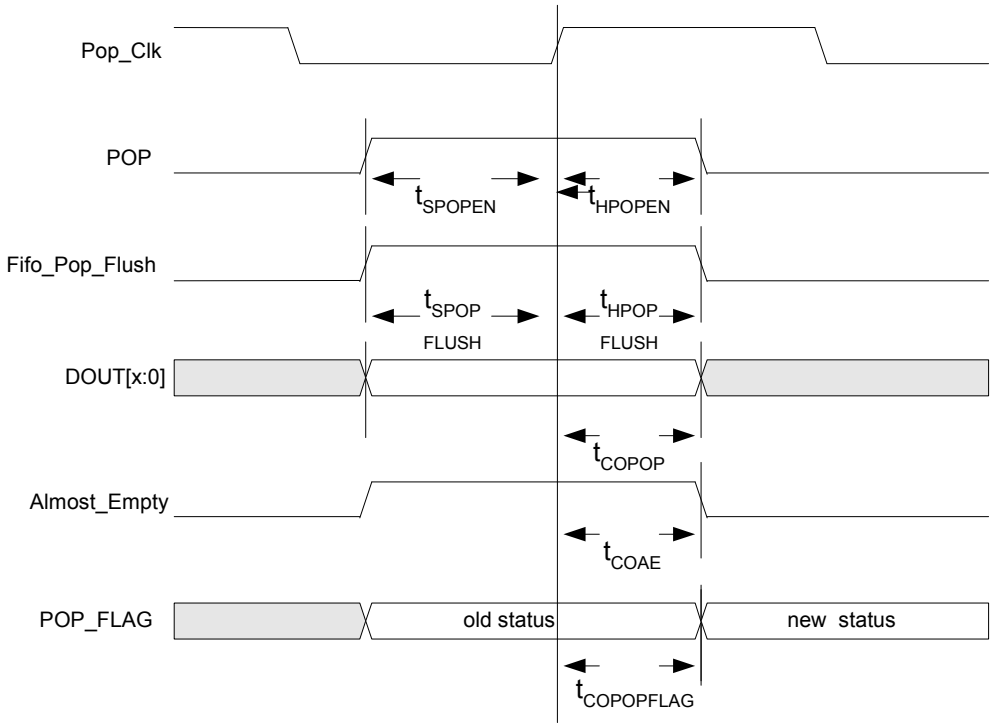


Table 31: FIFO POP Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SPOPEN}	POP setup time to Pop_Clk: time POP must be stable before the active edge of the FIFO Pop clock	1.01 ns	1.13 ns	1.19 ns	1.32 ns
t_{HPOPEN}	POP hold time to Pop_Clk: time POP must be stable after the active edge of the FIFO Pop clock	0 ns	0 ns	0 ns	0 ns
$t_{SPOPFLUSH}$	FLUSH setup time to Pop_Clk: time Fifo_Pop_Flush must be stable before the active edge of the FIFO Pop clock	1.11 ns	1.74 ns	1.43 ns	2.21 ns
$t_{HPOPFLUSH}$	FLUSH hold time to Pop_Clk: time Fifo_Pop_Flush must be stable after the active edge of the FIFO Pop clock	0 ns	0 ns	0 ns	0 ns
t_{FPOP}	Pop_Clk to Pop: Clock-to-out from the active FIFO CLOCK edge and the time when the data is popped from the FIFO at DOUT	2.32 ns	5.61 ns	2.37 ns	5.88 ns
t_{COAE}	Clock-to-out of Almost Empty	2.64 ns	3.58 ns	2.70 ns	3.66 ns
$t_{COPOPFLAG}$	Clock-to-out of FIFO Pop level indicator	2.32 ns	3.93 ns	2.38 ns	4.03 ns

Figure 32: FIFO POP Timing



GPIO Cell Timing

Figure 33: PolarPro I/O Cell Output Path

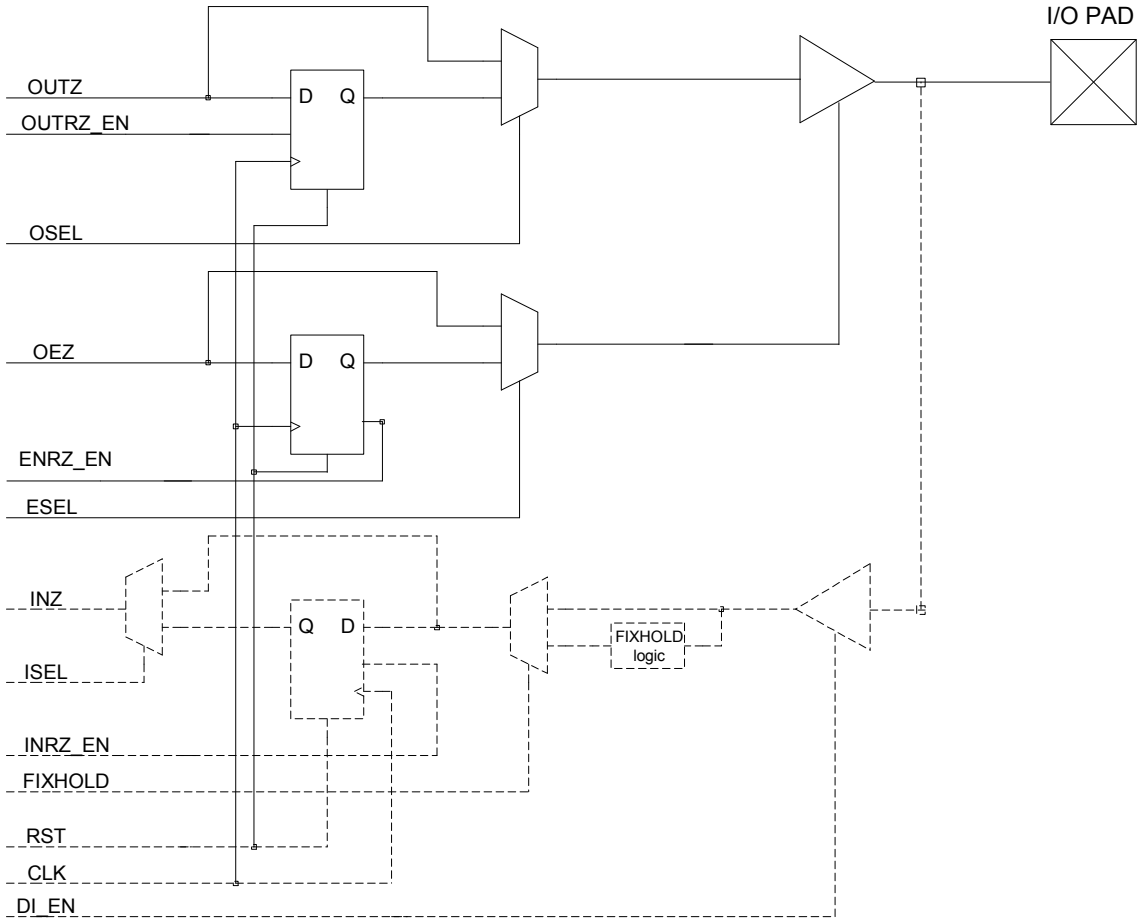


Figure 34: PolarPro I/O Cell Output Enable Timing

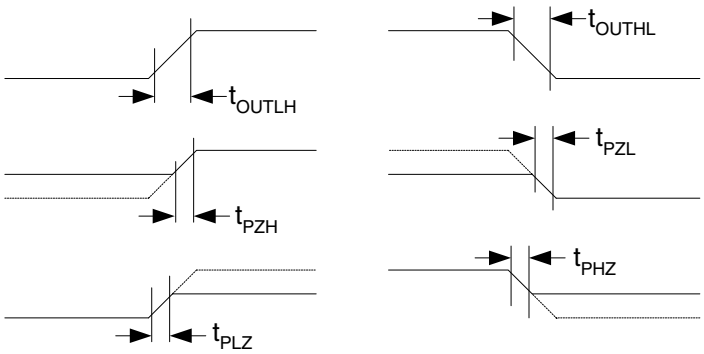


Table 32: Output Timing Characteristics @ VCCIO = 3.3 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	8.10	1.00
t_{OUTHL}	Output Delay high to low (10% of L)	9.60	0.90
t_{PZH}	Output Delay tri-state to high (90% of H)	3.40	0.30
t_{PZL}	Output Delay tri-state to low (10% of L)	3.90	0.30
t_{PHZ}	Output Delay high to tri-state	3.60	0.36
t_{PLZ}	Output Delay low to tri-state	4.1	0.41

Table 33: Output Timing Characteristics @ VCCIO = 2.5 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	12.20	1.10
t_{OUTHL}	Output Delay high to low (10% of L)	18.80	1.00
t_{PZH}	Output Delay tri-state to high (90% of H)	4.50	0.45
t_{PZL}	Output Delay tri-state to low (10% of L)	8.40	0.52
t_{PHZ}	Output Delay high to tri-state	8.10	0.52
t_{PLZ}	Output Delay low to tri-state	5.30	0.53

Table 34: Output Timing Characteristics @ VCCIO = 1.8 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	2.50	2.20
t_{OUTHL}	Output Delay high to low (10% of L)	1.70	1.40
t_{PZH}	Output Delay tri-state to high (90% of H)	8.30	0.70
t_{PZL}	Output Delay tri-state to low (10% of L)	24.70	1.05
t_{PHZ}	Output Delay high to tri-state	23.50	1.25
t_{PLZ}	Output Delay low to tri-state	10.80	0.78

Table 35 lists the typical output slew rates (in V/ns) across three levels of output voltages, with a drive strength of 4, and a load capacitor of 10 pF.

Table 35: GPIO Output Slew Rate

Slew	Output Slew Rate (V/ns) at VCCIO =		
	1.8 V	2.5 V	3.3 V
slow	n/a	0.20	0.36
fast	n/a	0.31	0.66
vfast	0.17	0.61	1.32
wow	0.25	1.18	2.03

Table 36: I/O Output Register Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.33 ns	0.38 ns	0.34 ns	0.36 ns
t_{OHL}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the flip-flop to output after the active clock edge	5.25 ns	5.99 ns	5.46 ns	6.29 ns
t_{ORST}	Output register reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	5.85 ns	5.85 ns	6.03 ns	6.03 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.33 ns	0.51 ns	0.30 ns	0.54 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OEZSU}	Output register clock enable setup time: time OEZ must be stable before the active clock edge	0.14 ns	0.20 ns	0.15 ns	0.18 ns
t_{OEZH}	Output register clock enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output signal propagation delay: propagation delay of OUTZ to the output pad	4.82 ns	5.44 ns	5.03 ns	5.72 ns

Figure 35: PolarPro I/O Cell Input Path

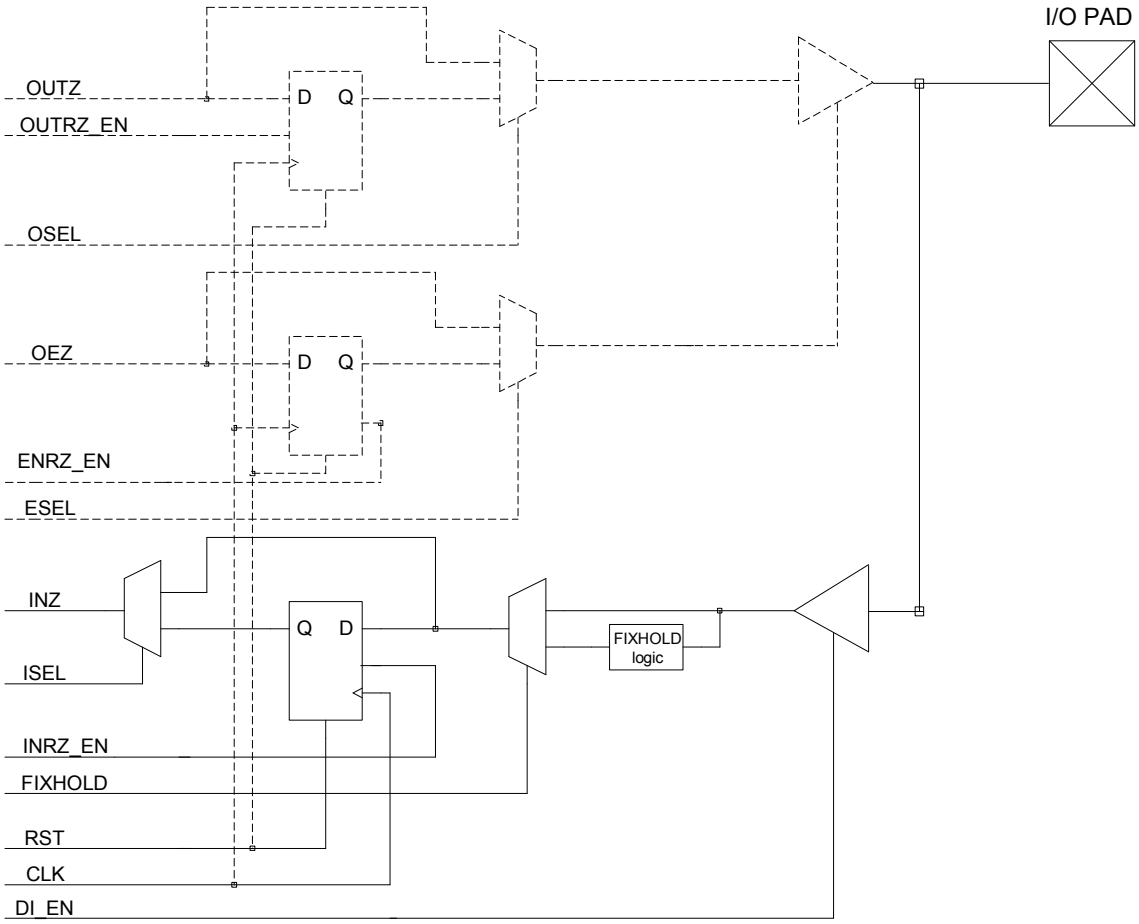


Figure 36: PolarPro Input Register Cell Timing

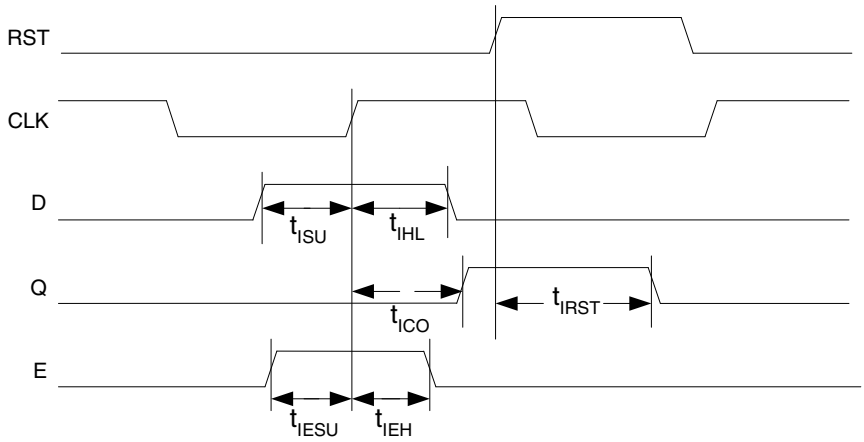


Table 37: I/O Input Register Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.51 ns	2.85 ns	2.80 ns	2.82 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	1.68 ns	2.66 ns	1.58 ns	2.70 ns
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	1.59 ns	1.59 ns	1.53 ns	1.53 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.25 ns	0.40 ns	0.23 ns	0.43 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
$t_{IDIENSU}$	Input data enable setup time: time DI_EN must be stable before the active clock edge	2.39 ns	5.38 ns	2.28 ns	5.63 ns
t_{IDIENH}	Input data enable hold time: time DI_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IFHSU}	Input fixhold setup time: time FIXHOLD must be stable before the active clock edge	2.39 ns	5.38 ns	2.28 ns	5.63 ns
t_{IFHH}	Input fixhold hold time: time FIXHOLD must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns

Table 38: I/O Input Buffer Delays

Symbol	Parameter	Value	
	To get the total input delay add this delay to t_{ISU}	Min.	Max.
t_{SID} (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3 V applications	TBD	TBD
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	TBD	TBD
t_{SID} (LVCMOS18)	LVCMOS18 input delay: Low Voltage CMOS for 1.8 V applications	TBD	TBD
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	TBD	TBD
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	TBD	TBD
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	TBD	TBD
t_{SID} (PCI)	PCI input delay: Peripheral Component Interconnect for 3.3 V	TBD	TBD

DDR Cell Timing

Figure 37: DDRIO DQ Configuration

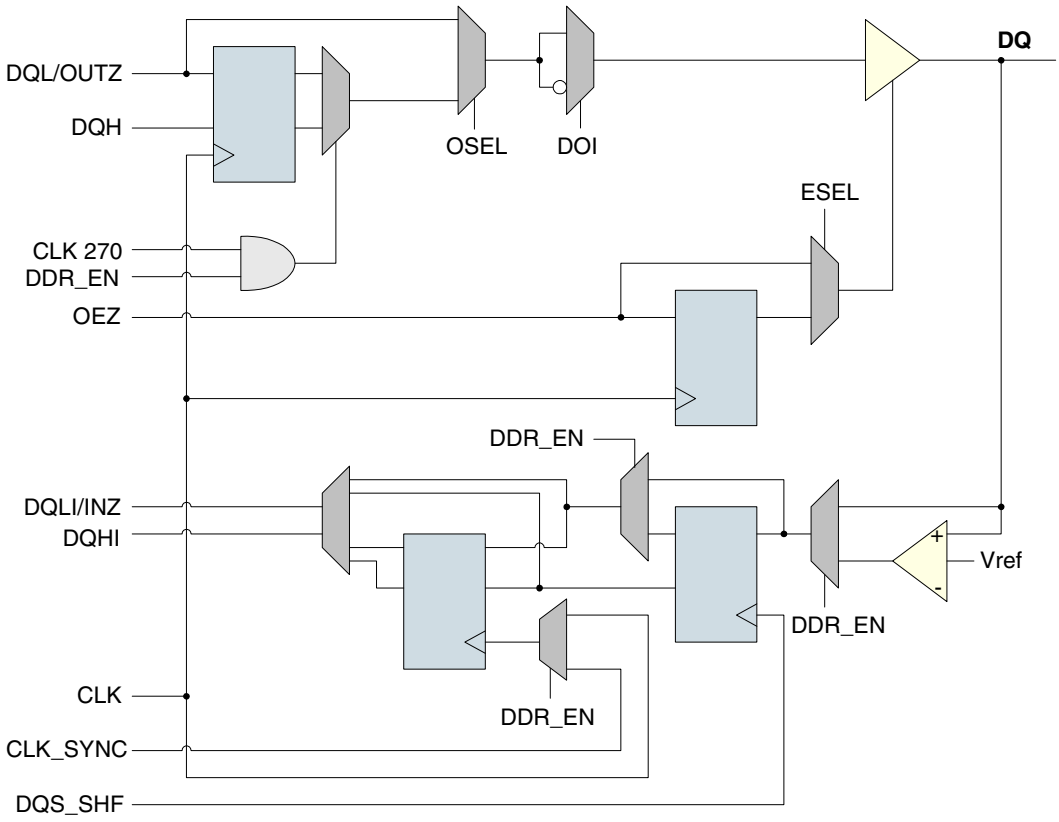


Table 39: DQ Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{DQLSU}	Output register setup time: time the synchronous DQL input of the flip-flop must be stable before the active clock edge	0.37 ns	0.38 ns	0.35 ns	0.39 ns
t_{DQLH}	Output register hold time: time the synchronous DQL input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the DQL flip-flop to output to the DQ pad after the active clock edge	4.13 ns	4.39 ns	4.48 ns	4.85 ns
t_{ODQHSU}	Output higher bit register clock setup time: time DQH must be stable before the active clock edge	0.32 ns	0.34 ns	0.31 ns	0.35 ns
t_{ODQHH}	Output higher bit register clock hold time: time DQH must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output propagation delay: propagation time from DQL to the output pad	3.64 ns	3.92 ns	4.17 ns	4.20 ns

Table 39: DQ Cell Timing *(Continued)*

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{IDQSU}	Input register setup time: time DQ must be stable before the active clock edge	1.45 ns	1.48 ns	1.24 ns	1.69 ns
t_{IDQH}	Input register hold time: time DQ must be stable after the active clock edge	0.62 ns	0.65 ns	0.47 ns	0.83 ns
t_{IPD}	Input propagation delay: propagation time from DQ to DQLI	2.35 ns	2.63 ns	2.19 ns	2.75 ns

Table 40: DQ Cell Configured as a GPIO Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.37 ns	0.38 ns	0.35 ns	0.39 ns
t_{OH}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the OUTZ flip-flop to output to the output pad after the active clock edge	4.17 ns	4.43 ns	4.61 ns	4.80 ns
t_{OESU}	Output data enable setup time: time OEZ must be stable before the active clock edge	0.43 ns	0.54 ns	0.42 ns	0.55 ns
t_{OEH}	Output data enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.38 ns	0.64 ns	0.35 ns	0.67 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output propagation delay: propagation time from OUTZ to the output pad	3.65 ns	3.87 ns	4.06 ns	4.24 ns
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.54 ns	2.63 ns	2.46 ns	2.62 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output to INZ after the active clock edge	2.88 ns	3.12 ns	2.73 ns	3.21 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.26 ns	0.55 ns	0.23 ns	0.58 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IPD}	Input propagation delay: propagation time from the input pad to INZ	2.35 ns	3.12 ns	2.19 ns	3.21 ns

Figure 38: DDRIO DQS Configuration

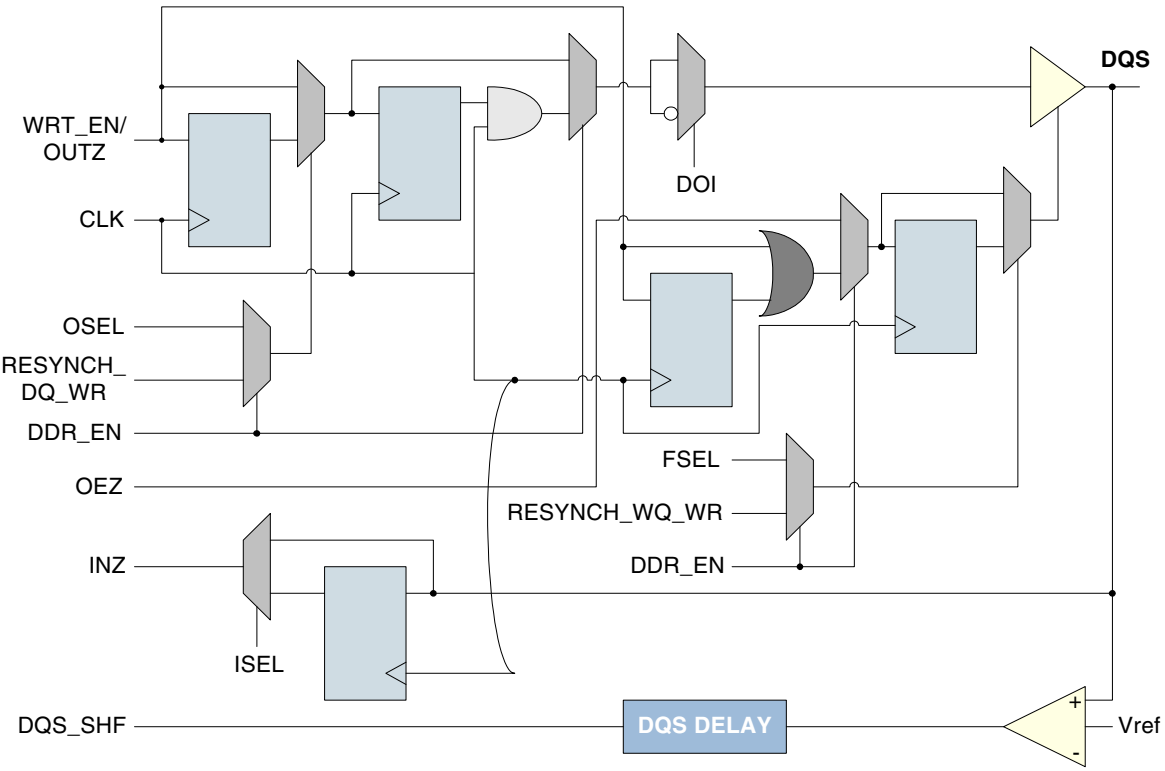


Table 41: DQS Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{WESU}	Output register setup time: time the synchronous WRT_EN input of the flip-flop must be stable before the active clock edge	0.61 ns	0.64 ns	0.61 ns	0.64 ns
t_{WEH}	Output register hold time: time the synchronous WRT_EN input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{WEPD}	Output propagation delay: propagation time from WRT_EN to the output pad	3.56 ns	3.62 ns	3.85 ns	3.99 ns
t_{IDQSPD}	Input propagation delay: propagation time from DQS to DQS_SHF	1.58 ns	3.53 ns	1.37 ns	3.77 ns

Table 42: DQS Cell Configured as a GPIO Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.47 ns	0.48 ns	0.45 ns	0.50 ns
t_{OH}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the OUTZ flip-flop to output to the output pad after the active clock edge	4.14 ns	4.46 ns	4.66 ns	4.77ns
t_{OESU}	Output data enable setup time: time OEZ must be stable before the active clock edge	0.47 ns	0.49 ns	0.49 ns	0.49 ns
t_{OEH}	Output data enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.35 ns	0.66 ns	0.33 ns	0.77 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output propagation delay: propagation time from OUTZ to the output pad	3.88 ns	4.13 ns	4.41 ns	4.42 ns
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.38 ns	2.45 ns	2.47 ns	2.29 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output to INZ after the active clock edge	2.76 ns	2.78 ns	2.73 ns	3.21 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.40 ns	0.71 ns	0.23 ns	0.58 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IPD}	Input propagation delay: propagation time from the input pad to INZ	2.25 ns	2.78 ns	2.19 ns	3.21 ns

Package Thermal Characteristics

The PolarPro device is available for Commercial (0°C to 85°C Junction), Industrial (-40°C to 100°C Junction), and Military (-55°C to 125°C Junction) temperature ranges.

Thermal Resistance Equations:

$\theta_{JA} = (TJ - TA)/P$

$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 43**, pick an appropriate T_{AMAX} and use: $P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA}$

Table 43: Package Thermal Characteristics

Package Description				Theta-JA (° C/W)		
Device	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL1P600	PS	LBGA	324	24	18	17
QL1P1000	PS	LBGA	324	24	18	17

Moisture Sensitivity Level

All PolarPro devices are Moisture Sensitivity Level 3.

Table 44: Solder and Lead Finish Composition

	Lead Included	Lead-Free
BGA Solder	63% Pb, 37% Sn	Sn3AgCu:Sn4AgCu[a]
QFP Lead Finish	85% Pb, 15% Sn	Sn (matte)

a. Sn3AgCu:Sn4AgCu means that Ag can range from 3% to 4%. Cu is always 0.5%.

Power-Up Sequencing

Figure 39: Power-Up Sequencing

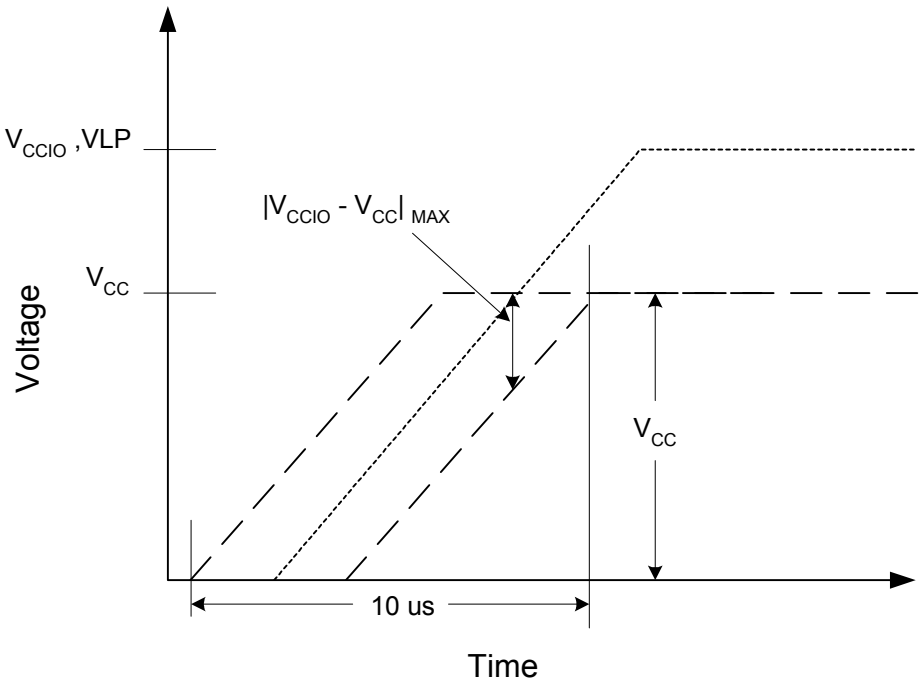


Figure 39 shows an example where all VCCIO = 3.3 V. When powering up a PolarPro device, VCC, VCCIO rails must take 10 µs or longer to reach the maximum value (refer to **Figure 39**). Ramping VCC and VCCIO faster than 10 µs can cause the device to behave improperly.

It is also important to ensure VCCIO and VLP are within 500 mV of VCC when ramping up the power supplies. In the case where VCCIO or VLP are greater than VCC by more than 500 mV an additional current draw can occur as VCC passes its threshold voltage. In a case where VCC is greater than VCCIO by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors. As noted in the VLP section, during the transition from VLP mode to normal operation, the VLP pin can draw up to 1.5 mA. Consequently, if using a pull-up resistor, use a pull-up resistor with a value that is less than 2 KΩ .

Programming Stipulation

For PolarPro devices to correctly program, there must not be any race conditions or internally generated free-running oscillators in the design. This will cause an ICC programming failure during the programming process. QuickLogic cannot guarantee the operation of any device that fails programming. Therefore, race conditions and free-running oscillators must be removed from designs so that PolarPro devices can correctly pass programming.

Pin Descriptions

Table 45: Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(C:A)	I/O	General purpose input/output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the bank with that letter. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
CLK(C:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(C:A).
DEDCLK(D)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(D).
CCMIN(1:0)	I	CCM clock input	Input clock for CCM. The voltage tolerance for this pin is specified by the VCCIO of the same bank.
CCMVCC (1:0)	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only.
CCMGND(1:0)	I	Ground pin for CCM	Connect to ground.
VLP	I	Voltage low power	Active low. Therefore, when VLP pin is low, the device will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
DQ[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQS[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQS or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.

Table 45: Pin Descriptions *(Continued)*

Pin	Direction	Function	Description
DQCK_N[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR negative clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_P[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR positive clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.
VREF(D)	I	Differential reference voltage	The INREF is the reference voltage pin for the SSTL1.8 and SSTL2 standards. The D inside the parenthesis means that INREF is located in Bank D. Tie this pin to GND if voltage referenced standards are not used.
JTAG Pin Descriptions			
TDI/RSI	I	Test data in for JTAG/RAM init. serial data in	Hold HIGH during normal operation. Connect to VCCIO(B) if unused.
TRSTB	I	Active low reset for JTAG	Hold LOW during normal operation. Connect to GND if unused. During JTAG, a high voltage is based on VCCIO(B).
TMS	I	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCCIO(B) if not used for JTAG.
TCK	I	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCCIO(B) or GND if not used for JTAG.
TDO	O	Test data out for JTAG	Must be left unconnected if not used for JTAG. The output voltage drive is specified by VCCIO(B).

a. The number following the DDRIO signal names in the pinout tables indicates the DDRIO set the pin corresponds to.

Recommended Unused Pin Terminations for PolarPro Devices

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 46**.

Table 46: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
VREF	If an I/O bank does not require the use of the INREF signal, connect the pin to GND.
CLK <x>[a]	Connect to GND or VCCIO(x) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
CCMVCC(1:0)	If a CCM is not used, the corresponding CCMVCC may be tied to GND to reduce power consumption. If a CCM is used, do not try to disable the CCM by tying the CCMVCC to GND.
TDI	Connect to VCCIO(B) if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to VCCIO(B) if not used for JTAG
TCK	Connect to VCCIO(B) or GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.

a. x represents A, B, C or D.

Packaging Pinout Tables

PolarPro QL1P600 - 324 LBGA Pinout Table

Table 47: PolarPro QL1P600 – 324 LBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GPIO(C)	D1	NC	G1	GPIO(C)	K1	GPIO(C)	N1	GPIO(C)	T1	GPIO(C)
A2	DQ1/GPIO(D)	D2	GPIO(C)	G2	GPIO(C)/ CCMIN(0)	K2	GPIO(C)	N2	GPIO(C)	T2	NC
A3	DQ1/GPIO(D)	D3	GPIO(C)	G3	GPIO(C)	K3	GPIO(C)	N3	NC	T3	GND
A4	DQ1CK_P/GPIO(D)	D4	GND	G4	GPIO(C)	K4	VCC	N4	VCC	T4	GPIO(B)
A5	DQ1CK_N/GPIO(D)	D5	VCCIO(D)	G5	GPIO(C)	K5	VCCIO(C)	N5	GPIO(C)	T5	GPIO(B)
A6	DQ1/GPIO(D)	D6	DQ1/GPIO(D)	G6	GPIO(C)	K6	GPIO(C)	N6	GND	T6	VCC
A7	DQ2/GPIO(D)	D7	VCCIO(D)	G7	NC	K7	GPIO(C)	N7	GND	T7	GPIO(B)
A8	DQ2CK_P/GPIO(D)	D8	DQ2/GPIO(D)	G8	VREF	K8	GND	N8	GPIO(B)	T8	GPIO(B)
A9	DQ2CK_N/GPIO(D)	D9	VCCIO(D)	G9	DQ3/GPIO(D)	K9	GND	N9	GPIO(B)	T9	GPIO(B)
A10	DEDCLK(D)	D10	DQ3/GPIO(D)	G10	TMS	K10	GND	N10	GPIO(B)	T10	VCC
A11	DQ3CK_P/GPIO(D)	D11	VCCIO(D)	G11	DQ3/GPIO(D)	K11	GND	N11	GPIO(B)	T11	GPIO(B)
A12	DQ3CK_N/GPIO(D)	D12	DQ4/GPIO(D)	G12	GPIO(A)	K12	GPIO(A)	N12	GPIO(B)	T12	GPIO(B)
A13	DQ4/GPIO(D)	D13	VCCIO(D)	G13	NC	K13	GPIO(A)	N13	GND	T13	VCC
A14	DQ4CK_P/GPIO(D)	D14	DQ4/GPIO(D)	G14	VCCIO(A)	K14	GPIO(A)	N14	VCCIO(A)	T14	GPIO(B)
A15	DQ4CK_N/GPIO(D)	D15	GND	G15	GPIO(A)	K15	GPIO(A)	N15	VCC	T15	GPIO(B)
A16	DQ4/GPIO(D)	D16	GPIO(A)	G16	GPIO(A)	K16	GPIO(A)	N16	GPIO(A)	T16	GND
A17	GPIO(D)	D17	GPIO(A)	G17	GPIO(A)	K17	GPIO(A)	N17	GPIO(A)	T17	GPIO(A)
A18	GPIO(A)	D18	GPIO(A)	G18	TRSTB	K18	GPIO(A)	N18	GPIO(A)	T18	GPIO(A)
B1	GPIO(C)	E1	GPIO(C)	H1	CLK(C)	L1	GPIO(C)	P1	GPIO(C)	U1	GPIO(C)
B2	CCMVCC(0)	E2	GPIO(C)	H2	GPIO(C)	L2	GPIO(C)	P2	GPIO(C)	U2	GPIO(C)
B3	GPIO(D)	E3	GPIO(C)	H3	GPIO(C)	L3	GPIO(C)	P3	GPIO(C)	U3	GPIO(C)
B4	DQ1/GPIO(D)	E4	GPIO(C)	H4	GPIO(C)	L4	GPIO(C)	P4	GPIO(C)	U4	GPIO(B)
B5	GPIO(D)	E5	GPIO(C)	H5	VCCIO(C)	L5	GPIO(C)	P5	VCCIO(C)	U5	GPIO(B)
B6	DQ1/GPIO(D)	E6	DQ1/GPIO(D)	H6	GPIO(C)	L6	GPIO(C)	P6	GPIO(B)	U6	GPIO(B)
B7	DQ2/GPIO(D)	E7	DQ1/GPIO(D)	H7	GPIO(C)	L7	GPIO(C)	P7	GPIO(B)	U7	GPIO(B)
B8	DQ2/GPIO(D)	E8	DQ2/GPIO(D)	H8	GND	L8	GND	P8	GPIO(B)	U8	GPIO(B)
B9	DQ2/GPIO(D)	E9	DQ2/GPIO(D)	H9	GND	L9	GND	P9	GPIO(B)	U9	GPIO(B)
B10	DQ3/GPIO(D)	E10	DQ3/GPIO(D)	H10	GND	L10	GND	P10	GPIO(B)	U10	GPIO(B)
B11	DQ3/GPIO(D)	E11	VREF	H11	GND	L11	GND	P11	GPIO(B)	U11	GPIO(B)
B12	DQ4/GPIO(D)	E12	DQ4/GPIO(D)	H12	GPIO(A)	L12	GPIO(A)	P12	GPIO(B)	U12	GPIO(B)
B13	DQ4/GPIO(D)	E13	DQS4/GPIO(D)	H13	GPIO(A) CCMIN(1)	L13	GPIO(A)	P13	GPIO(B)	U13	GPIO(B)
B14	DQ4/GPIO(D)	E14	VCCIO(A)	H14	GPIO(A)	L14	VCCIO(A)	P14	GPIO(A)	U14	GPIO(B)
B15	GPIO(D)	E15	GPIO(A)	H15	GPIO(A)	L15	GPIO(A)	P15	GPIO(A)	U15	GPIO(B)
B16	CCMGND(1)	E16	GPIO(A)	H16	GPIO(A)	L16	GPIO(A)	P16	NC	U16	GPIO(B)
B17	CCMVCC(1)	E17	GPIO(A)	H17	GPIO(A)	L17	GPIO(A)	P17	GPIO(A)	U17	GPIO(A)
B18	GPIO(A)	E18	GPIO(A)	H18	GPIO(A)	L18	GPIO(A)	P18	GPIO(A)	U18	GPIO(A)
C1	GPIO(C)	F1	GPIO(C)	J1	TCK	M1	GPIO(C)	R1	NC	V1	GPIO(C)
C2	CCMGND(0)	F2	NC	J2	GPIO(C)	M2	GPIO(C)	R2	GND	V2	GPIO(B)

Table 47: PolarPro QL1P600 – 324 LBGA Pinout Table *(Continued)*

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
C3	GND	F3	NC	J3	GPIO(C)	M3	GPIO(C)	R3	NC	V3	GPIO(B)
C4	GPIO(D)	F4	VCC	J4	GPIO(C)	M4	GPIO(C)	R4	GPIO(C)	V4	GPIO(B)
C5	GPIO(D)	F5	VCCIO(C)	J5	VCCIO(B)	M5	VCCIO(C)	R5	TDO	V5	GPIO(B)
C6	VCC	F6	GND	J6	GPIO(C)	M6	GPIO(C)	R6	VCCIO(B)	V6	GPIO(B)
C7	DQ1/GPIO(D)	F7	DQS1/GPIO(D)	J7	GPIO(C)	M7	GPIO(C)	R7	GPIO(B)	V7	GPIO(B)
C8	DQS2/GPIO(D)	F8	DQ2/GPIO(D)	J8	GND	M8	GPIO(B)	R8	VCCIO(B)	V8	CLK(B)
C9	VCC	F9	DQ2/GPIO(D)	J9	GND	M9	TDI	R9	GPIO(B)	V9	CLK(B)
C10	DQ3/GPIO(D)	F10	DQS3/GPIO(D)	J10	GND	M10	GPIO(B)	R10	VCCIO(B)	V10	GPIO(B)
C11	DQ3/GPIO(D)	F11	DQ3/GPIO(D)	J11	GND	M11	GPIO(B)	R11	GPIO(B)	V11	GPIO(B)
C12	DQ4/GPIO(D)	F12	GPIO(A)	J12	GPIO(A)	M12	GPIO(A)	R12	VCCIO(B)	V12	GPIO(B)
C13	VCC	F13	GND	J13	GPIO(A)	M13	GND	R13	GPIO(B)	V13	GPIO(B)
C14	GPIO(D)	F14	NC	J14	VCCIO(A)	M14	GPIO(A)	R14	VCCIO(B)	V14	GPIO(B)
C15	GPIO(D)	F15	VCC	J15	VCC	M15	GPIO(A)	R15	VLP	V15	GPIO(B)
C16	GND	F16	GPIO(A)	J16	GPIO(A)	M16	GPIO(A)	R16	NC	V16	GPIO(B)
C17	GPIO(A)	F17	GPIO(A)	J17	VCCIO(B)	M17	GPIO(A)	R17	GPIO(A)	V17	GPIO(B)
C18	GPIO(A)	F18	CLK(A)	J18	GPIO(A)	M18	GPIO(A)	R18	GPIO(A)	V18	GPIO(A)

PolarPro QL1P1000 - 324 LBGA Pinout Table

Table 48: PolarPro QL1P1000 – 324 LBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GPIO(C)	D1	GPIO(C)	G1	GPIO(C)	K1	GPIO(C)	N1	GPIO(C)	T1	GPIO(C)
A2	DQ1/GPIO(D)	D2	GPIO(C)	G2	GPIO(C)/ CCMIN(0)	K2	GPIO(C)	N2	GPIO(C)	T2	GPIO(C)
A3	DQ1/GPIO(D)	D3	GPIO(C)	G3	GPIO(C)	K3	GPIO(C)	N3	GPIO(C)	T3	GND
A4	DQ1CK_P/GPIO(D)	D4	GND	G4	GPIO(C)	K4	VCC	N4	VCC	T4	GPIO(B)
A5	DQ1CK_N/GPIO(D)	D5	VCCIO(D)	G5	GPIO(C)	K5	VCCIO(C)	N5	GPIO(C)	T5	GPIO(B)
A6	DQ1/GPIO(D)	D6	DQ1/GPIO(D)	G6	GPIO(C)	K6	GPIO(C)	N6	GND	T6	VCC
A7	DQ2/GPIO(D)	D7	VCCIO(D)	G7	GPIO(C)	K7	GPIO(C)	N7	GND	T7	GPIO(B)
A8	DQ2CK_P/GPIO(D)	D8	DQ2/GPIO(D)	G8	VREF	K8	GND	N8	GPIO(B)	T8	GPIO(B)
A9	DQ2CK_N/GPIO(D)	D9	VCCIO(D)	G9	DQ3/GPIO(D)	K9	GND	N9	GPIO(B)	T9	GPIO(B)
A10	DEDCLK(D)	D10	DQ3/GPIO(D)	G10	TMS	K10	GND	N10	GPIO(B)	T10	VCC
A11	DQ3CK_P/GPIO(D)	D11	VCCIO(D)	G11	DQ3/GPIO(D)	K11	GND	N11	GPIO(B)	T11	GPIO(B)
A12	DQ3CK_N/GPIO(D)	D12	DQ4/GPIO(D)	G12	GPIO(A)	K12	GPIO(A)	N12	GPIO(B)	T12	GPIO(B)
A13	DQ4/GPIO(D)	D13	VCCIO(D)	G13	GPIO(A)	K13	GPIO(A)	N13	GND	T13	VCC
A14	DQ4CK_P/GPIO(D)	D14	DQ4/GPIO(D)	G14	VCCIO(A)	K14	GPIO(A)	N14	VCCIO(A)	T14	GPIO(B)
A15	DQ4CK_N/GPIO(D)	D15	GND	G15	GPIO(A)	K15	GPIO(A)	N15	VCC	T15	GPIO(B)
A16	DQ4/GPIO(D)	D16	GPIO(A)	G16	GPIO(A)	K16	GPIO(A)	N16	GPIO(A)	T16	GND
A17	GPIO(D)	D17	GPIO(A)	G17	GPIO(A)	K17	GPIO(A)	N17	GPIO(A)	T17	GPIO(A)
A18	GPIO(A)	D18	GPIO(A)	G18	TRSTB	K18	GPIO(A)	N18	GPIO(A)	T18	GPIO(A)
B1	GPIO(C)	E1	GPIO(C)	H1	CLK(C)	L1	GPIO(C)	P1	GPIO(C)	U1	GPIO(C)
B2	CCMVCC(0)	E2	GPIO(C)	H2	GPIO(C)	L2	GPIO(C)	P2	GPIO(C)	U2	GPIO(C)
B3	GPIO(D)	E3	GPIO(C)	H3	GPIO(C)	L3	GPIO(C)	P3	GPIO(C)	U3	GPIO(C)
B4	DQ1/GPIO(D)	E4	GPIO(C)	H4	GPIO(C)	L4	GPIO(C)	P4	GPIO(C)	U4	GPIO(B)
B5	GPIO(D)	E5	GPIO(C)	H5	VCCIO(C)	L5	GPIO(C)	P5	VCCIO(C)	U5	GPIO(B)
B6	DQ1/GPIO(D)	E6	DQ1/GPIO(D)	H6	GPIO(C)	L6	GPIO(C)	P6	GPIO(B)	U6	GPIO(B)
B7	DQ2/GPIO(D)	E7	DQ1/GPIO(D)	H7	GPIO(C)	L7	GPIO(C)	P7	GPIO(B)	U7	GPIO(B)
B8	DQ2/GPIO(D)	E8	DQ2/GPIO(D)	H8	GND	L8	GND	P8	GPIO(B)	U8	GPIO(B)
B9	DQ2/GPIO(D)	E9	DQ2/GPIO(D)	H9	GND	L9	GND	P9	GPIO(B)	U9	GPIO(B)
B10	DQ3/GPIO(D)	E10	DQ3/GPIO(D)	H10	GND	L10	GND	P10	GPIO(B)	U10	GPIO(B)
B11	DQ3/GPIO(D)	E11	VREF	H11	GND	L11	GND	P11	GPIO(B)	U11	GPIO(B)
B12	DQ4/GPIO(D)	E12	DQ4/GPIO(D)	H12	GPIO(A)	L12	GPIO(A)	P12	GPIO(B)	U12	GPIO(B)
B13	DQ4/GPIO(D)	E13	DQS4/GPIO(D)	H13	GPIO(A)/ CCMIN(1)	L13	GPIO(A)	P13	GPIO(B)	U13	GPIO(B)
B14	DQ4/GPIO(D)	E14	VCCIO(A)	H14	GPIO(A)	L14	VCCIO(A)	P14	GPIO(A)	U14	GPIO(B)
B15	GPIO(D)	E15	GPIO(A)	H15	GPIO(A)	L15	GPIO(A)	P15	GPIO(A)	U15	GPIO(B)
B16	CCMGND(1)	E16	GPIO(A)	H16	GPIO(A)	L16	GPIO(A)	P16	GPIO(A)	U16	GPIO(B)
B17	CCMVCC(1)	E17	GPIO(A)	H17	GPIO(A)	L17	GPIO(A)	P17	GPIO(A)	U17	GPIO(A)
B18	GPIO(A)	E18	GPIO(A)	H18	GPIO(A)	L18	GPIO(A)	P18	GPIO(A)	U18	GPIO(A)
C1	GPIO(C)	F1	GPIO(C)	J1	TCK	M1	GPIO(C)	R1	GPIO(C)	V1	GPIO(C)
C2	CCMGND(0)	F2	GPIO(C)	J2	GPIO(C)	M2	GPIO(C)	R2	GND	V2	GPIO(B)
C3	GND	F3	GPIO(C)	J3	GPIO(C)	M3	GPIO(C)	R3	GPIO(C)	V3	GPIO(B)
C4	GPIO(D)	F4	VCC	J4	GPIO(C)	M4	GPIO(C)	R4	GPIO(C)	V4	GPIO(B)
C5	GPIO(D)	F5	VCCIO(C)	J5	VCCIO(B)	M5	VCCIO(C)	R5	TDO	V5	GPIO(B)

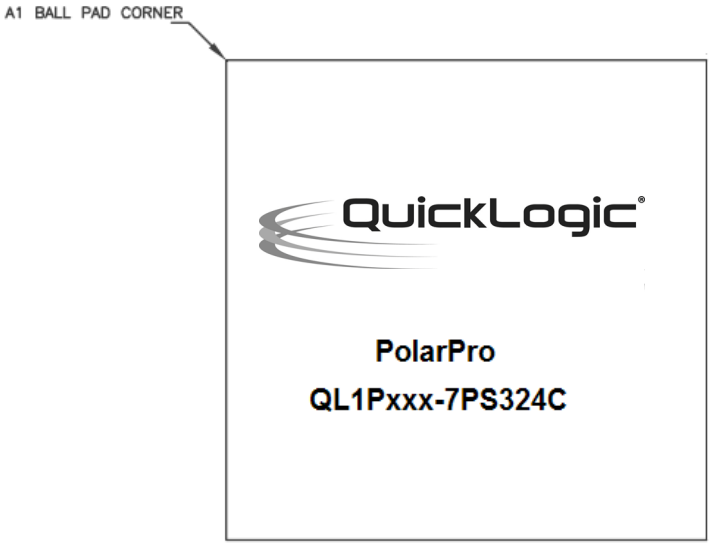
Table 48: PolarPro QL1P1000 – 324 LBGA Pinout Table *(Continued)*

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
C6	VCC	F6	GND	J6	GPIO(C)	M6	GPIO(C)	R6	VCCIO(B)	V6	GPIO(B)
C7	DQ1/GPIO(D)	F7	DQS1/GPIO(D)	J7	GPIO(C)	M7	GPIO(C)	R7	GPIO(B)	V7	GPIO(B)
C8	DQS2/GPIO(D)	F8	DQ2/GPIO(D)	J8	GND	M8	GPIO(B)	R8	VCCIO(B)	V8	CLK(B)
C9	VCC	F9	DQ2/GPIO(D)	J9	GND	M9	TDI	R9	GPIO(B)	V9	CLK(B)
C10	DQ3/GPIO(D)	F10	DQS3/GPIO(D)	J10	GND	M10	GPIO(B)	R10	VCCIO(B)	V10	GPIO(B)
C11	DQ3/GPIO(D)	F11	DQ3/GPIO(D)	J11	GND	M11	GPIO(B)	R11	GPIO(B)	V11	GPIO(B)
C12	DQ4/GPIO(D)	F12	GPIO(A)	J12	GPIO(A)	M12	GPIO(A)	R12	VCCIO(B)	V12	GPIO(B)
C13	VCC	F13	GND	J13	GPIO(A)	M13	GND	R13	GPIO(B)	V13	GPIO(B)
C14	GPIO(D)	F14	GPIO(A)	J14	VCCIO(A)	M14	GPIO(A)	R14	VCCIO(B)	V14	GPIO(B)
C15	GPIO(D)	F15	VCC	J15	VCC	M15	GPIO(A)	R15	VLP	V15	GPIO(B)
C16	GND	F16	GPIO(A)	J16	GPIO(A)	M16	GPIO(A)	R16	GPIO(A)	V16	GPIO(B)
C17	GPIO(A)	F17	GPIO(A)	J17	VCCIO(B)	M17	GPIO(A)	R17	GPIO(A)	V17	GPIO(B)
C18	GPIO(A)	F18	CLK(A)	J18	GPIO(A)	M18	GPIO(A)	R18	GPIO(A)	V18	GPIO(A)

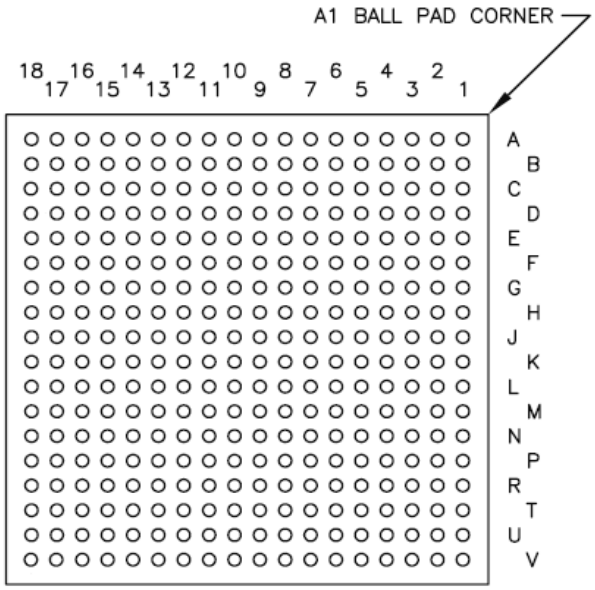
Packaging Pinout Diagram

PolarPro QL1Pxxx - 324 LBGA Pinout Diagram

Top

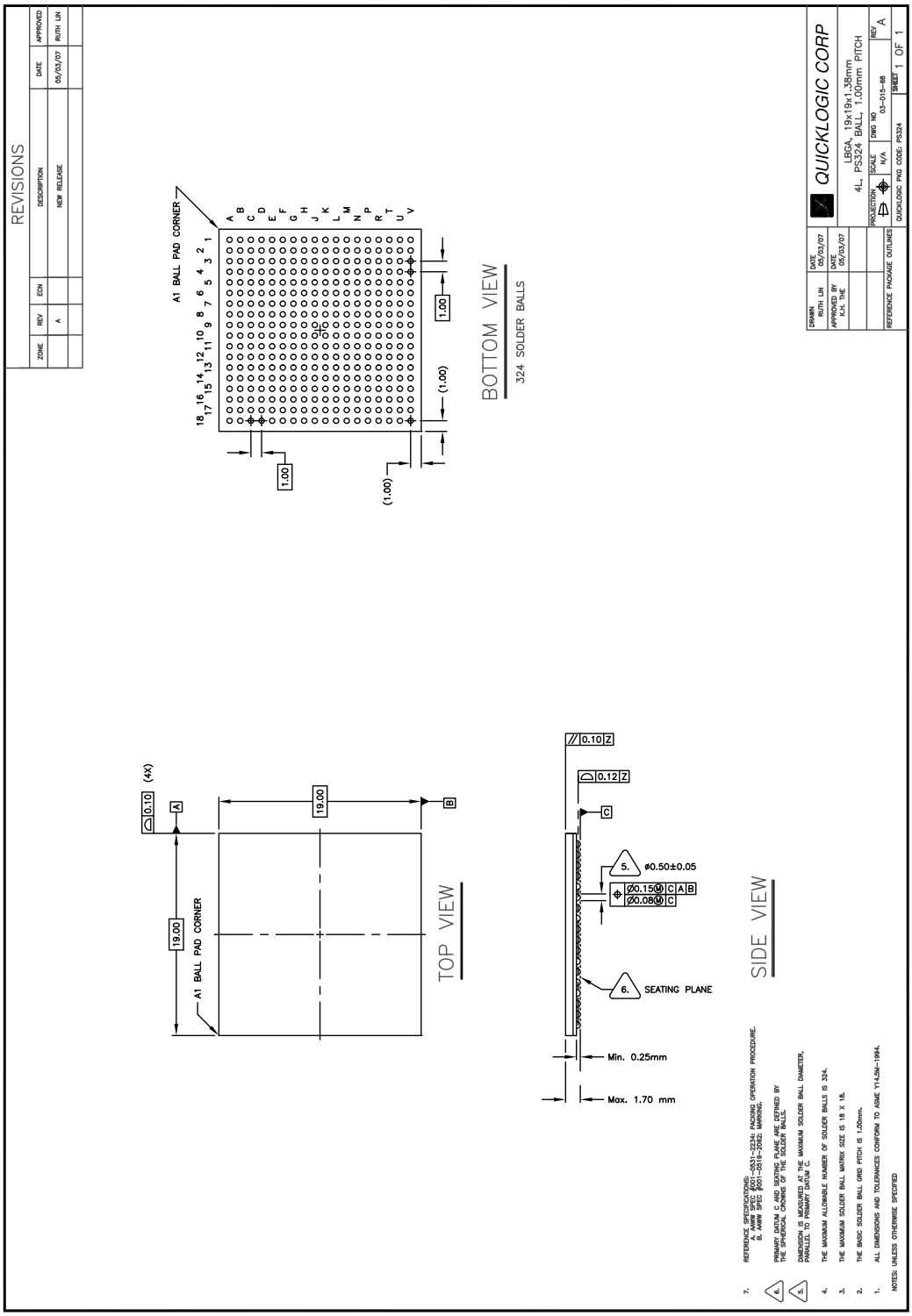


Bottom



Package Mechanical Drawing

324 LBGA Package Drawing



Packaging Information

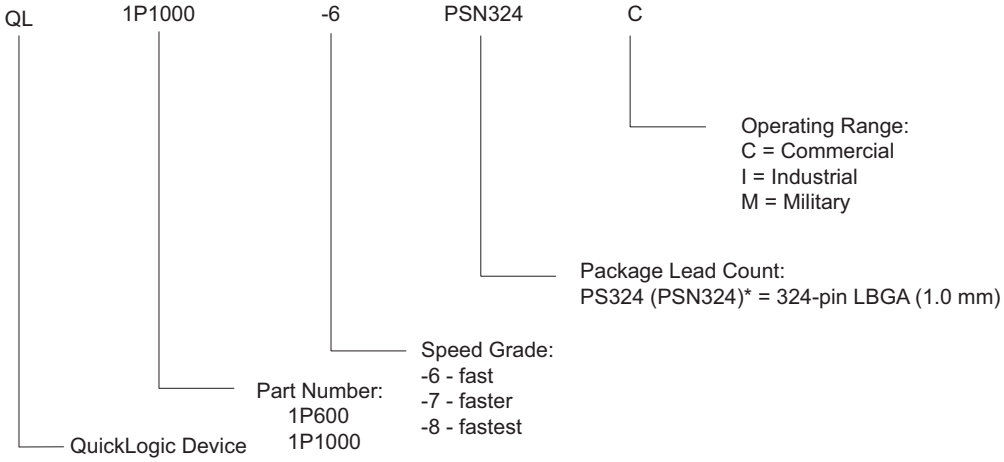
The PolarPro QL1P600 and QL1P1000 device packaging information is presented in **Table 49**.

Table 49: QL1P600 and QL1P1000Packaging Options

Device Information	Device		
	QL1P600 / QL1P1000		
	Pin	Pb	Pb-Free
Package Definitions[a]	324 LBGA (19 mm x 19 mm) Pitch - 1.0 mm	X	X

a. LBGA = Low Profile Ball Grid Array

Ordering Information



* Lead-free packaging is denoted by the character 'N' preceding the number of pins.

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Revision History

Revision	Date	Originator and Comments
A	September 2007	Jason Lew and Kathleen Murchek - First release.
B	December 2007	Jason Lew and Kathleen Murchek - Merged with other PolarPro data sheets using conditional text.
C	January 2008	Jason Lew and Kathleen Murchek - Clock Dynamic Enable section changed clock2_dyn_en to CKPAD2_DYN_EN. - PolarProQL1P1000 and QL1P600 – 324 LBGA Pinout tables, pin H1 changed from CLKPAD(C) to CLK(C) and pin F18 changed from CLKPAD(A) to CLK(A). - PolarProQL1P1000 and QL1P600 – 324 LBGA Pinout tables, pin A10 changed from CLK(D) to DEDCLK(D). - CCM Signals table changed pmg_in to pgm_in. - Logic Cell Delays table change t_{HL} Max. to N/A.
D	July 2008	Jason Lew and Kathleen Murchek - Removed PRELIMINARY. - Updated Copyright and Trademark Information. - Updated Contact Information. - Added Notice of Disclaimer
E	September 2010	Kathleen Bylsma - Updated Contact Information.

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