

RJK4006DPD

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1547-0100

Rev.1.00

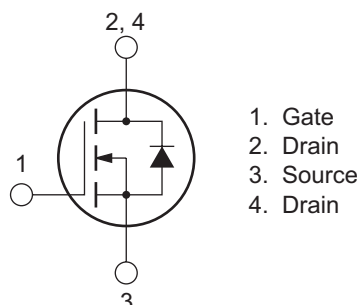
Dec 19, 2008

Features

- Low on-resistance
- Low leakage current
- High speed switching

Outline

RENESAS Package code: PRSS0004ZG-A
(Package name : MP-3A)



Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|---|----------------------------------|-------------|------|
| Drain to source voltage | V_{DSS} | 400 | V |
| Gate to source voltage | V_{GSS} | ±30 | V |
| Drain current | I_D ^{Note4} | 8 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note1} | 24 | A |
| Body-drain diode reverse drain current | I_{DR} | 8 | A |
| Body-drain diode reverse drain peak current | $I_{DR(pulse)}$ ^{Note1} | 24 | A |
| Avalanche current | I_{AP} ^{Note3} | 8 | A |
| Avalanche energy | E_{AR} ^{Note3} | 3.7 | mJ |
| Channel dissipation | P_{ch} ^{Note2} | 65 | W |
| Channel to case thermal impedance | θ_{ch-c} | 1.92 | °C/W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at $T_c = 25^\circ C$
3. $STch = 25^\circ C$, $Tch \leq 150^\circ C$
4. Limited by maximum safe operation area

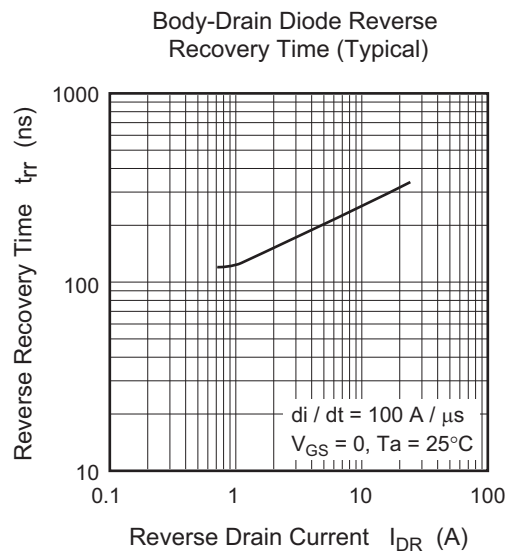
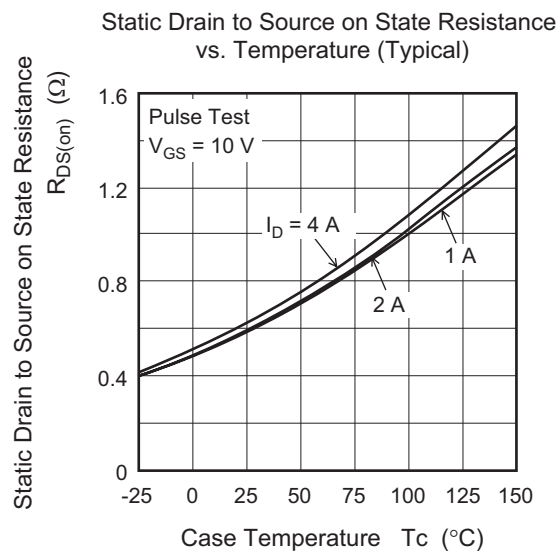
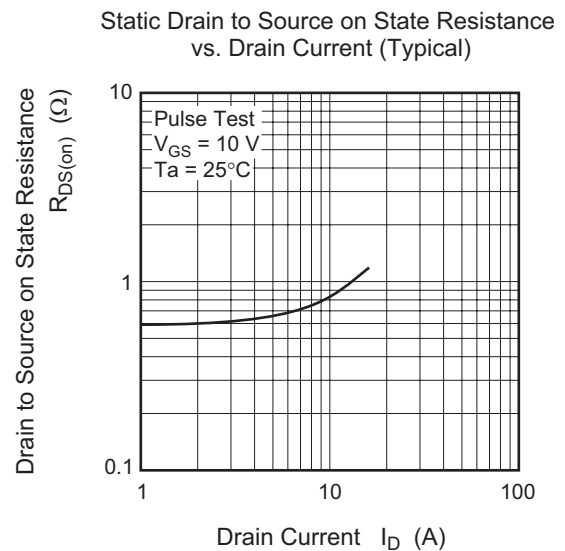
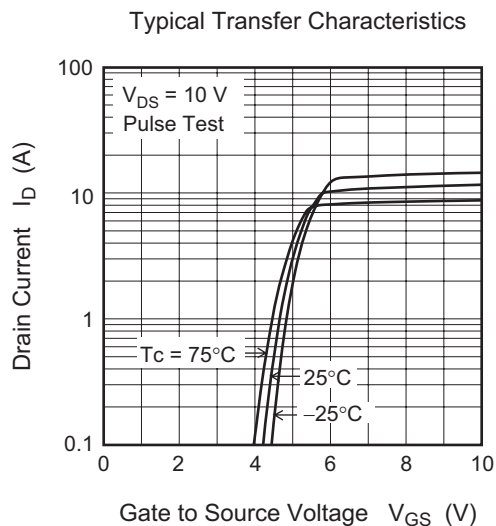
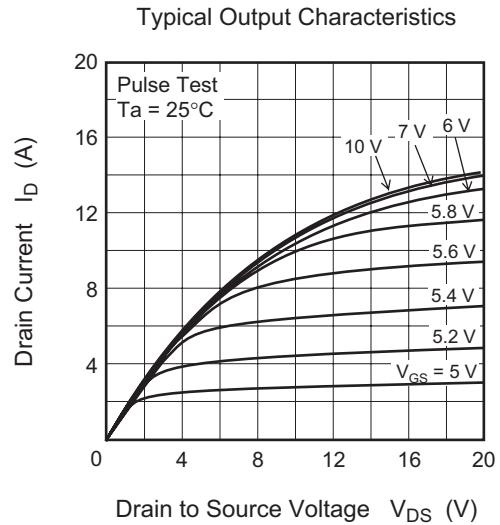
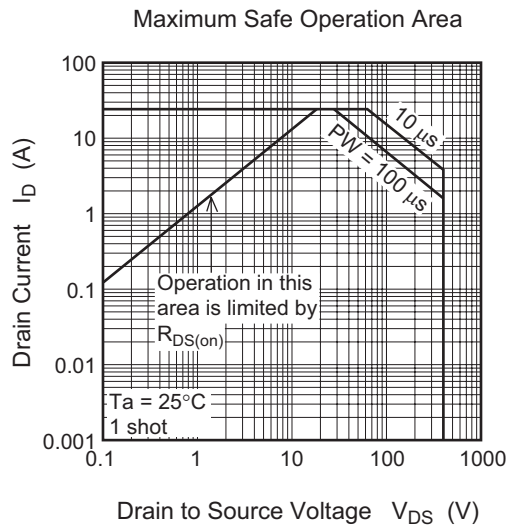
Electrical Characteristics

(Ta = 25°C)

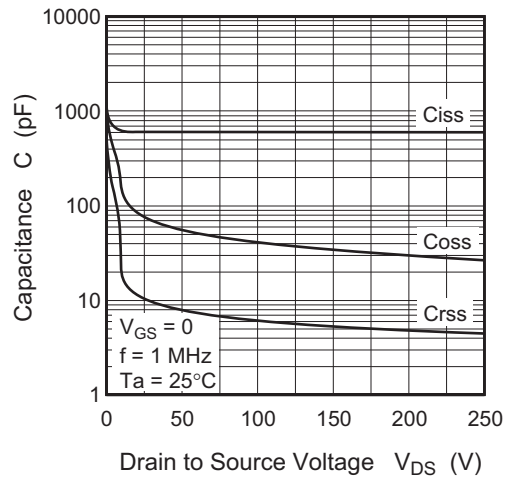
| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|---------------|-----|------|-----------|---------------|--|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 400 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 400 \text{ V}$, $V_{GS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 0.1 | μA | $V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 3.0 | — | 4.5 | V | $V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 0.69 | 0.80 | Ω | $I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note5} |
| Input capacitance | C_{iss} | — | 620 | — | pF | $V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$ |
| Output capacitance | C_{oss} | — | 80 | — | pF | |
| Reverse transfer capacitance | C_{rss} | — | 11 | — | pF | |
| Turn-on delay time | $t_{d(on)}$ | — | 30 | — | ns | $I_D = 4 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 50 \Omega$ $R_g = 10 \Omega$ |
| Rise time | t_r | — | 30 | — | ns | |
| Turn-off delay time | $t_{d(off)}$ | — | 60 | — | ns | |
| Fall time | t_f | — | 20 | — | ns | |
| Total gate charge | Q_g | — | 20 | — | nC | $V_{DD} = 320 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 8 \text{ A}$ |
| Gate to source charge | Q_{gs} | — | 4 | — | nC | |
| Gate to drain charge | Q_{gd} | — | 9 | — | nC | |
| Body-drain diode forward voltage | V_{DF} | — | 0.9 | 1.5 | V | $I_F = 8 \text{ A}$, $V_{GS} = 0$ ^{Note5} |
| Body-drain diode reverse recovery time | t_{rr} | — | 230 | — | ns | $I_F = 8 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$ |

Notes: 5. Pulse test

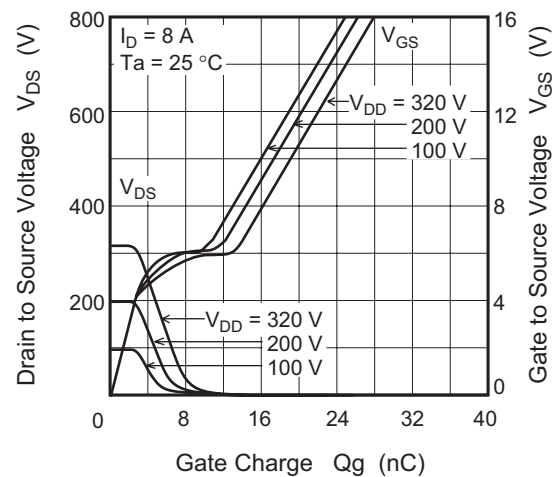
Main Characteristics



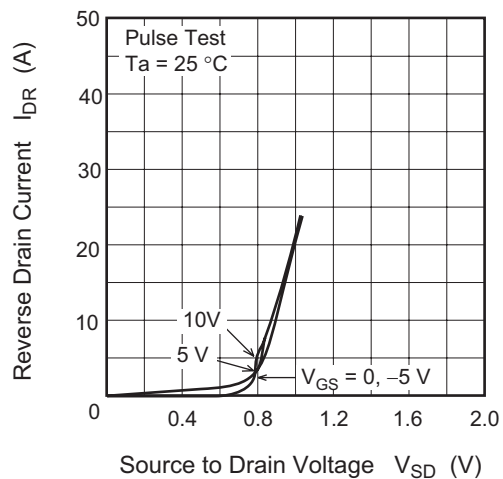
Typical Capacitance vs.
Drain to Source Voltage (Typical)



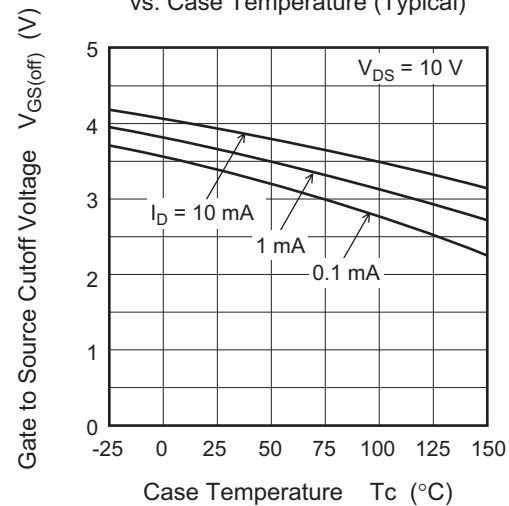
Dynamic Input Characteristics (Typical)

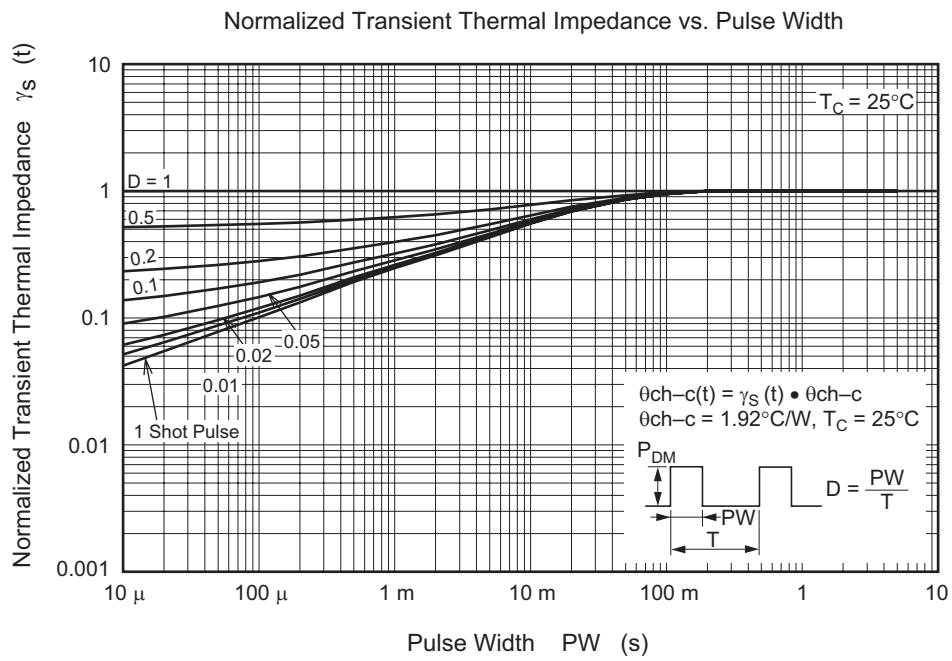


Reverse Drain Current vs.
Source to Drain Voltage (Typical)

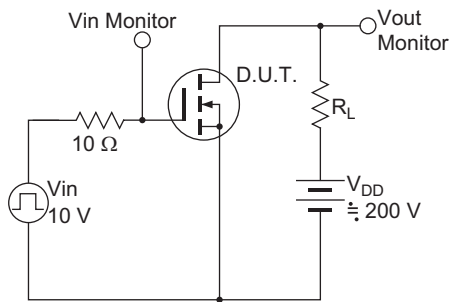


Gate to Source Cutoff Voltage
vs. Case Temperature (Typical)

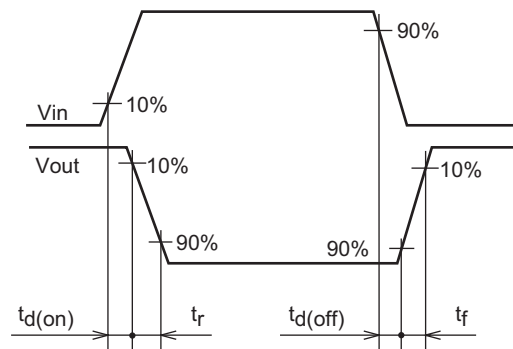




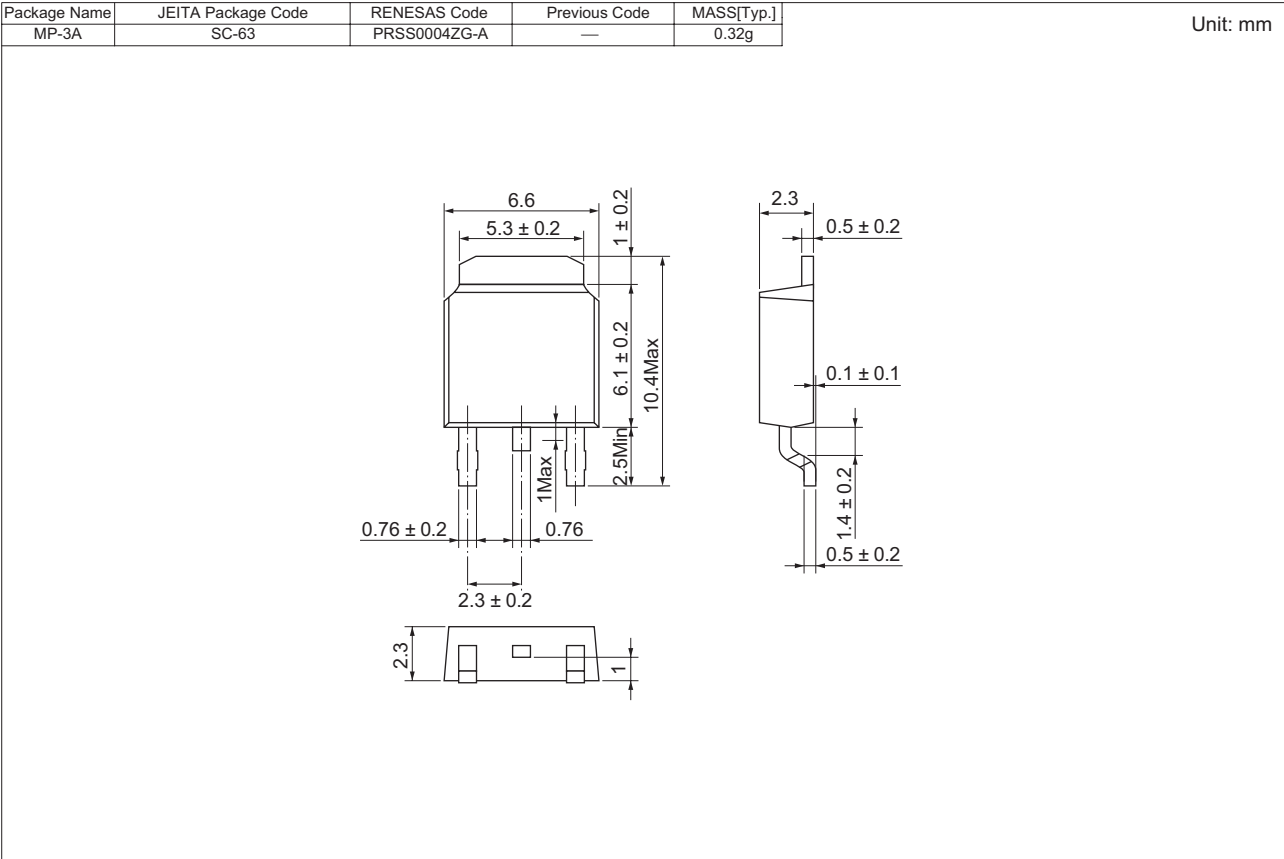
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

| Part No. | Quantity | Shipping Container |
|------------------|----------|--------------------|
| RJK4006DPD-00-J2 | 3000 pcs | Taping |

Notes:

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