



### Absolute Maximum Ratings

Voltages Referenced to  $-V_{IN}$  (Note:  $V_{CC} < +V_{IN} + 0.3\text{ V}$ )

$V_{CC}$ .....	15 V
$+V_{IN}$ .....	120 V
Logic Inputs (RESET, SHUTDOWN, OSC IN, OSC OUT) .....	$-0.3\text{ V}$ to $V_{CC} + 0.3\text{ V}$
Linear Inputs (FEEDBACK, SENSE, BIAS, $V_{REF}$ ) .....	$-0.3\text{ V}$ to $V_{CC} + 0.3\text{ V}$
HV Pre-Regulator Input Current (continuous) .....	5 mA
Storage Temperature .....	$-65$ to $150^{\circ}\text{C}$
Operating Temperature (A Suffix) .....	$-55$ to $125^{\circ}\text{C}$
(D Suffix) .....	$-40$ to $85^{\circ}\text{C}$
Junction Temperature ( $T_J$ ) .....	$150^{\circ}\text{C}$

Power Dissipation (Package)<sup>a</sup>

14-Pin CerDIP (K Suffix) <sup>b</sup> .....	1000 mW
14-Pin Plastic DIP (J Suffix) <sup>c</sup> .....	750 mW
14-Pin SOIC (Y Suffix) <sup>d</sup> .....	900 mW
Thermal Impedance ( $\Theta_{JA}$ )	
14-Pin CerDIP .....	$100^{\circ}\text{C/W}$
14-Pin Plastic DIP .....	$167^{\circ}\text{C/W}$
14-Pin SOIC .....	$140^{\circ}\text{C/W}$

#### Notes

- Device mounted with all leads soldered or welded to PC board.
- Derate  $10\text{ mW}/^{\circ}\text{C}$  above  $50^{\circ}\text{C}$ .
- Derate  $6\text{ mW}/^{\circ}\text{C}$  above  $25^{\circ}\text{C}$ .
- Derate  $7.2\text{ mW}/^{\circ}\text{C}$  above  $25^{\circ}\text{C}$ .

### Recommended Operating Range

Voltages Referenced to  $-V_{IN}$

$V_{CC}$ .....	9.5 V to 13.5 V
$+V_{IN}$ .....	10 V to 120 V
$f_{OSC}$ .....	40 kHz to 1 MHz

$R_{OSC}$ .....	25 k $\Omega$ to 1 M $\Omega$
Linear Inputs .....	0 to $V_{CC} - 3\text{ V}$
Digital Inputs .....	0 to $V_{CC}$

### Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified  DISCHARGE = -V <sub>IN</sub> = 0 V V <sub>CC</sub> = 10 V, +V <sub>IN</sub> = 48 V R <sub>BIAS</sub> = 390 kΩ, R <sub>OSC</sub> = 330 kΩ	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit	
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>		
Reference										
Output Voltage	V <sub>R</sub>	OSC IN = - V <sub>IN</sub> (OSC Disabled) R <sub>L</sub> = 10 MΩ	Si9110	Room	4.0	3.92	4.08	3.92	4.08	V
			Si9111	Room	4.0	3.60	4.40	3.60	4.40	
			Si9110	Full		3.82	4.16	3.86	4.14	
			Si9111	Full		3.50	4.48	3.52	4.46	
Output Impedance <sup>e</sup>	Z <sub>OUT</sub>		Room	30	15	45	15	45	kΩ	
Short Circuit Current	I <sub>SREF</sub>	V <sub>REF</sub> = -V <sub>IN</sub>	Room	100	70	130	70	130	μA	
Temperature Stability <sup>e</sup>	T <sub>REF</sub>		Full	0.50		1.0		1.0	mV/°C	
Oscillator										
Maximum Frequency <sup>e</sup>	f <sub>MAX</sub>	R <sub>OSC</sub> = 0	Room	3	1		1		MHz	
Initial Accuracy	f <sub>OSC</sub>	R <sub>OSC</sub> = 330 k, See Note f	Room	100	80	120	80	120	kHz	
		R <sub>OSC</sub> = 150 k, See Note f	Room	200	160	240	160	240		
Voltage Stability	Δf/f	Δf/f=f(13.5 V) - f(9.5 V)/f(9.5 V)	Room	10		15		15	%	
Temperature Coefficient <sup>e</sup>	T <sub>OSC</sub>		Full	200		500		500	ppm/°C	
Error Amplifier										
Feedback Input Voltage	V <sub>FB</sub>	FB Tied to COMP OSC IN = - V <sub>IN</sub> (OSC Disabled)	Si9110	Room	4.00	3.96	4.04	3.96	4.04	V
			Si9111	Room	4.00	3.60	4.40	3.60	4.40	
Input BIAS Current	I <sub>FB</sub>	OSC IN = - V <sub>IN</sub> , V <sub>FB</sub> = 4 V	Room	25		500		500	nA	

### Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified  DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ , $R_{OSC} = 330\text{ k}\Omega$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix –55 to 125°C		D Suffix –40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
Error Amplifier (Cont'd)									
Input OFFSET Voltage	V <sub>OS</sub>	OSC IN = ~ V <sub>IN</sub> (OSC Disabled)	Room	± 15		± 40		± 40	mV
Open Loop Voltage Gain <sup>e</sup>	A <sub>VOL</sub>		Room	80	60		60		dB
Unity Gain Bandwidth <sup>e</sup>	BW		Room	1.3	1		1		MHz
Dynamic Output Impedance <sup>e</sup>	Z <sub>OUT</sub>		Room	1000		2000		2000	Ω
Output Current	I <sub>OUT</sub>	Source (V <sub>FB</sub> = 3.4 V)	Room	–2.0		–1.4		–1.4	mA
		Sink (V <sub>FB</sub> = 4.5 V)	Room	0.15	0.12		0.12		
Power Supply Rejection	PSRR	9.5 V ≤ V <sub>CC</sub> ≤ 13.5 V	Room	70	50		50		dB
Current Limit									
Threshold Voltage	V <sub>SOURCE</sub>	V <sub>FB</sub> = 0 V	Room	1.2	1.0	1.4	1.0	1.4	V
Delay to Output <sup>e</sup>	t <sub>d</sub>	V <sub>SENSE</sub> = 1.5 V, See Figure 1	Room	100		150		150	ns
Pre-Regulator/Start-Up									
Input Voltage	+V <sub>IN</sub>	I <sub>IN</sub> = 10 μA	Room		120		120		V
Input Leakage Current	+I <sub>IN</sub>	V <sub>CC</sub> ≥ 9.4 V	Room			10		10	μA
Pre-Regulator Start-Up Current	I <sub>START</sub>	Pulse Width ≤ 300 μs, V <sub>CC</sub> = V <sub>ULVO</sub>	Room	15	8		8		mA
V <sub>CC</sub> Pre-Regulator Turn-Off Threshold Voltage	V <sub>REG</sub>	I <sub>PRE-REGULATOR</sub> = 10 μA	Room	8.6	7.8	9.4	7.8	9.4	V
Undervoltage Lockout	V <sub>UVLO</sub>		Room	8.1	7.0	8.9	7.0	8.9	
V <sub>REG</sub> – V <sub>UVLO</sub>	V <sub>DELTA</sub>		Room	0.6	0.3		0.3		
Supply									
Supply Current	I <sub>CC</sub>	C <sub>LOAD</sub> < 75 pF (Pin 4)	Room	0.6	0.45	1.0	0.45	1.0	mA
Bias Current	I <sub>BIAS</sub>		Room	15	10	20	10	20	μA
Logic									
SHUTDOWN Delay <sup>e</sup>	t <sub>SD</sub>	C <sub>L</sub> = 500 pF, V <sub>SENSE</sub> – V <sub>IN</sub> See Figure 2	Room	50		100		100	ns
SHUTDOWN Pulse Width <sup>e</sup>	t <sub>SW</sub>	See Figure 3	Room		50		50		
RESET Pulse Width <sup>e</sup>	t <sub>RW</sub>		Room		50		50		
Latching Pulse Width SHUTDOWN and RESET Low <sup>e</sup>	t <sub>LW</sub>	See Figure 3	Room		25		25		
Input Low Voltage	V <sub>IL</sub>		Room			2.0		2.0	V
Input High Voltage	V <sub>IH</sub>		Room		8		8		

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					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
Logic (Cont'd)									
Input Current Input Voltage High	I <sub>IH</sub>	V <sub>IN</sub> = 10 V	Room	1		5		5	μA
Input Current Input Voltage Low	I <sub>IL</sub>	V <sub>IN</sub> = 0 V	Room	-25	-35		-35		
Output									
Output High Voltage	V <sub>OH</sub>	I <sub>OUT</sub> ≈ -10 mA	Room Full		9.7 9.5		9.7 9.5		V
Output Low Voltage	V <sub>OL</sub>	I <sub>OUT</sub> = 10 mA	Room Full			0.30 0.50		0.30 0.50	
Output Resistance	R <sub>OUT</sub>	I <sub>OUT</sub> = 10 mA, Source or Sink	Room Full	20 25		30 50		30 35	Ω
Rise Time <sup>e</sup>	t <sub>r</sub>	C <sub>L</sub> = 500 pF	Room	40		75		75	ns
Fall Time <sup>e</sup>	t <sub>f</sub>		Room	40		75		75	

#### Notes

- Refer to PROCESS OPTION FLOWCHART for additional information.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Guaranteed by design, not subject to production test.
- CSTRAY Pin 8 =  $\leq 5\text{ pF}$ .

### Timing Waveforms

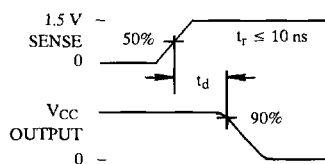


Figure 1.

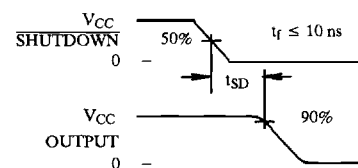


Figure 2.

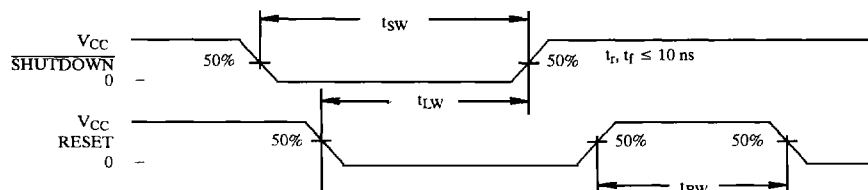
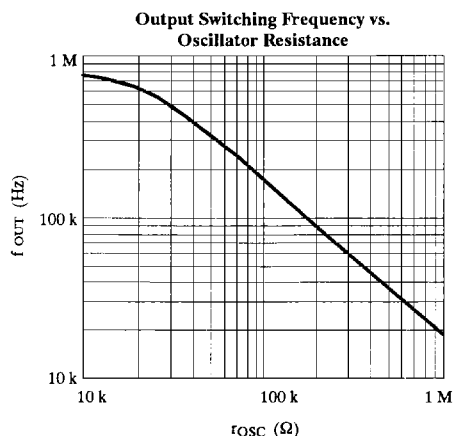
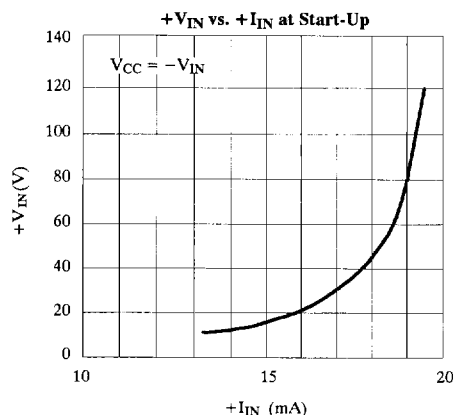
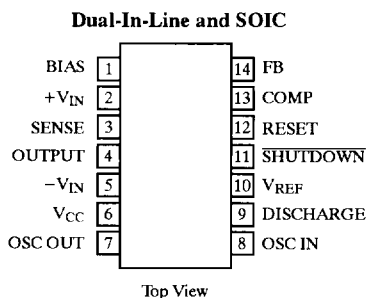


Figure 3.

### Typical Characteristics



### Pin Configurations



Order Numbers  
 CerDIP: Si9110AK  
 Plastic DIP: Si9110DJ, Si9111DJ  
 SOIC: Si9110DY, Si9111DY

### Detailed Description

#### Pre-Regulator/Start-Up Section

Due to the low quiescent current requirement of the Si9110/9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during start-up, +V<sub>IN</sub> (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between +V<sub>IN</sub> and V<sub>CC</sub> (pin 6). This start-up circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V<sub>CC</sub> pin. The constant current is disabled when V<sub>CC</sub> exceeds 8.6 V. If V<sub>CC</sub> is not forced to exceed the 8.6V

threshold, then V<sub>CC</sub> will be regulated to a nominal value of 8.6 V by the pre-regulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output driver disabled until V<sub>CC</sub> exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns on. The design of the IC is such that the undervoltage lockout threshold will be at least 300 mV less than the pre-regulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V<sub>CC</sub> such that the constant current source is always disabled.

### Detailed Description (Cont'd)

**Note:** During start-up or when  $V_{CC}$  drops below 8.6 V the start-up circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48-V input, approximately 1 W). Excessive start-up time caused by external loading of the  $V_{CC}$  supply can result in device damage. Figure 4 gives the typical pre-regulator current at BiC/DMOS as a function of input voltage.

#### BIAS

To properly set the bias for the Si9110/9111, a 390-k $\Omega$  resistor should be tied from BIAS (pin 1) to  $-V_{IN}$  (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the  $\overline{\text{SHUTDOWN}}$  and RESET pins. The current flowing in the bias resistor is nominally 15  $\mu\text{A}$ .

#### Reference Section

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within  $\pm 1\%$  of 4 V. This compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

#### Error Amplifier

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current.

The noninverting input to the error amplifier ( $V_{REF}$ ) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

#### Oscillator Section

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to  $-V_{IN}$  for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to  $\leq 50\%$  by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization is accomplished by capacitive coupling of a positive SYNC pulse into the OSC IN (pin 8) terminal. For a 5-V pulse amplitude and 0.5- $\mu\text{s}$  pulse width, typical values would be 100 pF in series with 3 k $\Omega$  to pin 8.

#### $\overline{\text{SHUTDOWN}}$ and RESET

$\overline{\text{SHUTDOWN}}$  (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET,  $\overline{\text{SHUTDOWN}}$  can be either a latched or unlatched input. The output is off whenever  $\overline{\text{SHUTDOWN}}$  is low. By simultaneously having  $\overline{\text{SHUTDOWN}}$  and RESET low, the latch is set and  $\overline{\text{SHUTDOWN}}$  has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Table 1: Truth Table for the  $\overline{\text{SHUTDOWN}}$  and RESET Pins

$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal Operation
H	$\overline{\text{L}}$	Normal Operation (No Change)
L	H	Off (Not Latched)
L	L	Off (Latched)
$\overline{\text{F}}$	L	Off (Latched, No Change)

Both pins have internal current source pull-ups and should be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the  $\overline{\text{SHUTDOWN}}$  or RESET pins to provide variable shutdown time.

### Detailed Description (Cont'd)

#### Output Driver

The push-pull driver output has a typical on-resistance of 20  $\Omega$ . Maximum switching times are specified at 75 ns for a 500-pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching

times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469A. The D469A can switch very large devices such as the SMM20N50 (500 V, 0.3  $\Omega$ ) in approximately 100 ns.

### Applications

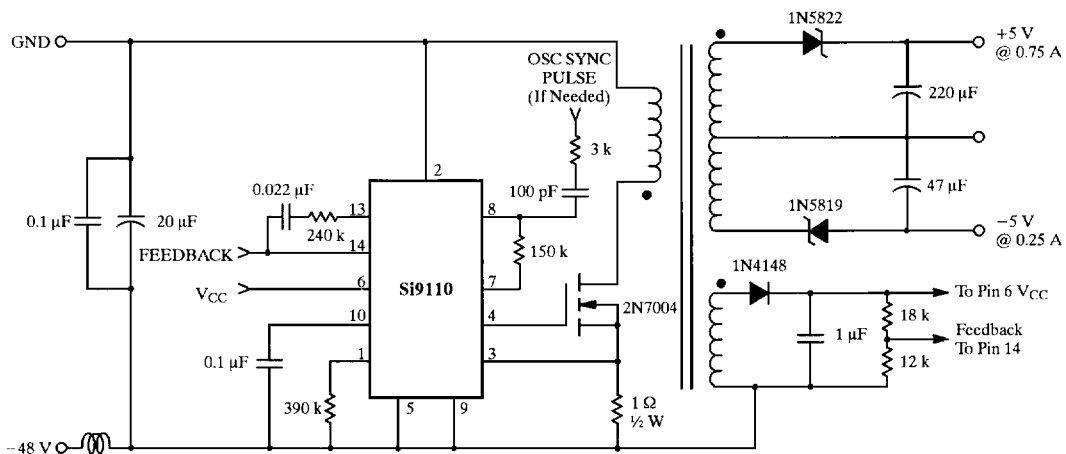


Figure 4. 5-Watt Power Supply for Telecom Applications