Elektronische Bauelemente

STT3471P

-2A, -100V, $R_{DS(ON)}$ 350 mΩ
P-Channel Enhancement Mode MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

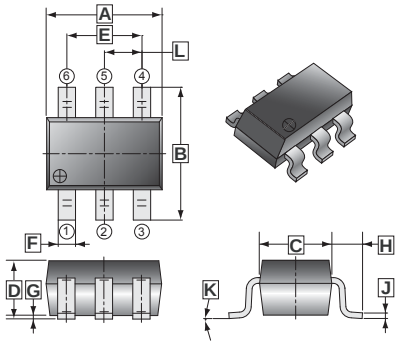
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe TSOP-6 saves board space.
- Fast switching speed.
- High performance trench technology.

APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

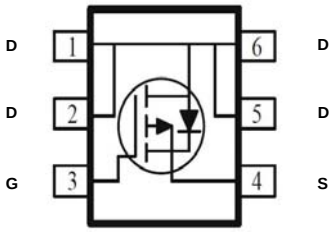
TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60 REF.	
C	1.40	1.80	J	0.12 REF.	
D	1.10 MAX.		K	0°	10°
E	1.90 REF.		L	0.95 REF.	
F	0.30	0.50			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7' inch



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_A= 25°C	I_D	2.0	A
	T_A= 70°C		1.6	
Pulsed Drain Current [2]		I_{DM}	-8	A
Continuous Source Current (Diode Conduction) [1]		I_S	-2.1	A
Power Dissipation [1]	T_A= 25°C	P_D	2.0	W
	T_A= 70°C		1.3	
Operating Junction and Storage Temperature Range		Tj, Tstg	-55~150	°C
Thermal Resistance Rating				
Maximum Junction to Ambient [1]	t ≦ 5 sec	$R_{\theta JA}$	62.5	°C / W
			110	

Notes:
1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	V_{DS}= V_{GS}, I_D= -250μA
Gate-Body Leakage	I_{GSS}	-	-	±100	nA	V_{DS}=0, V_{GS}= ±20V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	V_{DS}= -80V, V_{GS}=0
		-	-	-10		V_{DS}= -80V, V_{GS}=0, T_J= 55°C
On-State Drain Current [1]	$I_{D(on)}$	-20	-	-	A	V_{DS} = -5V, V_{GS}= -10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	350	mΩ	V_{GS}= -10V, I_D= -1.4A
		-	-	450		V_{GS}= -4.5V, I_D= -1.2A
Forward Transconductance [1]	g_{fs}	-	2.8	-	S	V_{DS}= -15V, I_D= -1.4A
Diode Forward Voltage	V_{SD}	-	-	-1	V	I_S= -1.4A, V_{GS}=0
Dynamic [2]						
Total Gate Charge	Q_g	-	6	-	nC	V_{DS}= -30V, V_{GS}= -4.5V, I_D= -1.4A
Gate-Source Charge	Q_{gs}	-	10	-		
Gate-Drain Charge	Q_{gd}	-	3	-		
Turn-on Delay Time	$T_{d(on)}$	-	3	-	nS	V_{DD}= -30V, V_{GEN}= -10V, R_L=30Ω, I_D= -1A, R_G= 6Ω
Rise Time	T_r	-	3	-		
Turn-off Delay Time	$T_{d(off)}$	-	13	-		
Fall Time	T_f	-	7	-		

Notes:
1. Pulse test：PW ≦ 300 us duty cycle ≦ 2%.
2. Guaranteed by design, not subject to production testing.