Military Standard Product

UT22VP10 Universal RADPAL™

Preliminary Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

July 1995

FEATURES

- ☐ High speed Universal RADPAL
  - t_{PD}: 25ns maximum
  - f_{MAX1}: 30MHz maximum external frequency
  - Supported by industry-standard programmer
  - Amorphous silicon anti-fuse
- ☐ Asynchronous & synchronous RADPAL operation
  - Synchronous PRESET
  - Asynchronous RESET
- ☐ Up to 22 input and 10 output drivers may be configured
  - CMOS & TTL-compatible input and output levels
  - Three-state output drivers
- ☐ Variable product terms, 8 to 16 per output
- ☐ 10 user-programmable output macrocells
  - Registered or combinatorial operation
  - Output driver polarity control selectable
  - 2 feedback paths available
- ☐ Low operating current
  - I_{DD}: 60mA @ 1MHz
- ☐ V_{DD}: 5.0 volts ± 10%
- ☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 1.0E6 rads(Si)
  - Single event effects:
    Upset threshold 50 MeV-cm²/mg (min)
    Latchup immune
  - Neutron fluence: 1.0E14 n/cm²
- ☐ QML Q & V compliant part (check factory for availability)
- ☐ Packaging options:
  - 24-pin 100-mil center DIP (0.300 x 1.2)
  - 24-lead flatpack (.45 x .64)
  - 28-lead quad-flatpack (.45 x .45)
- ☐ Standard Military Drawing 5962-94754 available

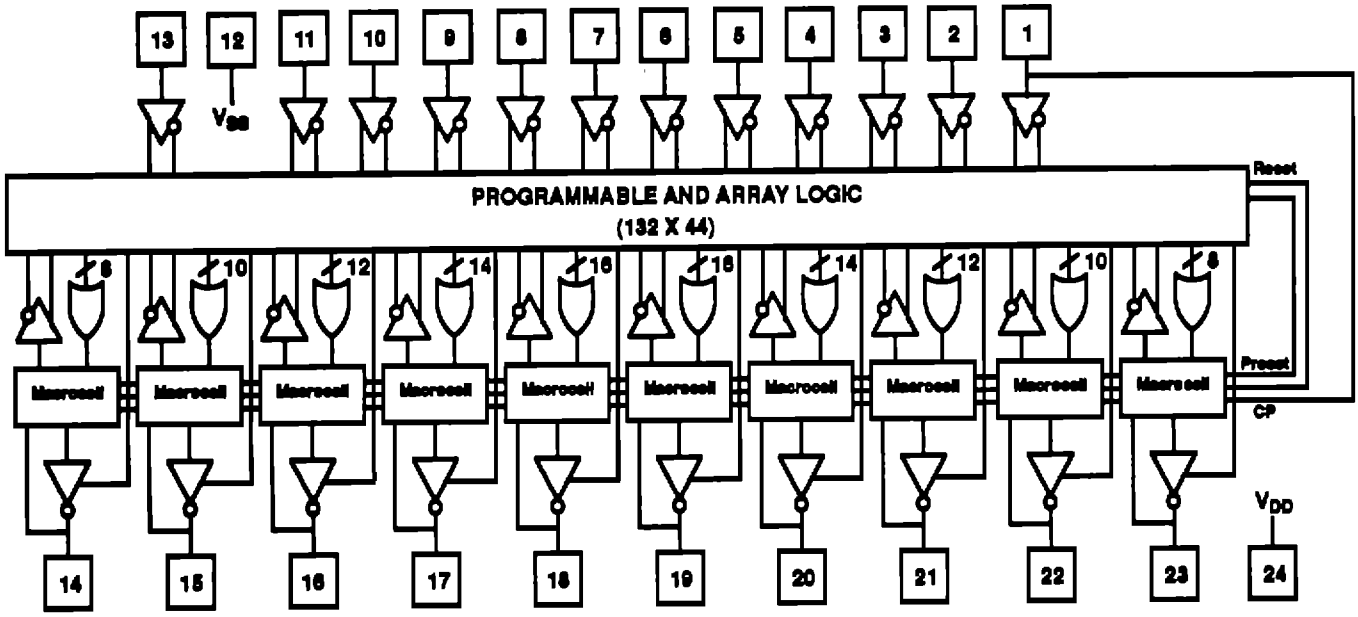


Figure 1. Block Diagram

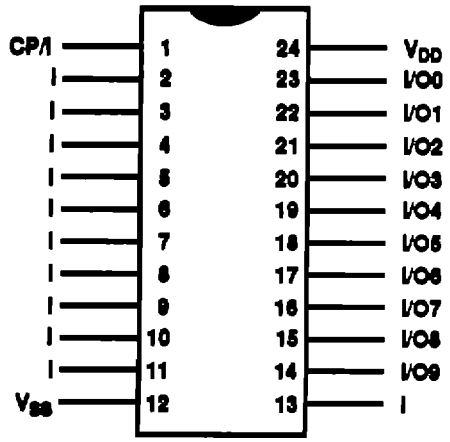
PRODUCT DESCRIPTION

The UT22VP10 RADPAL is a fuse programmable logic array device. The familiar sum-of-products (AND-OR) logic structure is complemented with a programmable macrocell. The UT22VP10 is available in 24-pin DIP, 24-lead flatpack, and 28-lead quad-flatpack package offerings providing up to 22 inputs and 10 outputs. Amorphous silicon anti-fuse technology provides the programming of each output. The user specifies whether each of the potential outputs is registered or combinatorial. Output polarity is also individually selected, allowing for greater flexibility for output configuration. A unique output enable function allows the user to configure bidirectional I/O on an individual basis.

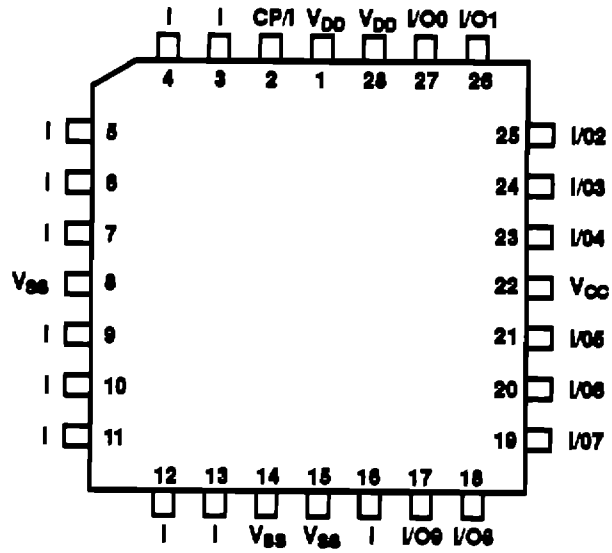
The UT22VP10 architecture implements variable product terms providing 8 to 16 product terms to outputs. This feature provides the user with increased logic function flexibility. Other features include common synchronous preset and asynchronous reset. These features eliminate the need for performing the initialization function.

The UT22VP10 provides a device with the flexibility to implement logic functions in the 500 to 800 gate complexity. The flexible architecture supports the implementation of logic functions requiring up to 21 inputs and only a single output or down to 12 inputs and 10 outputs.

DIP & FLATPACK PIN CONFIGURATION



QUAD-FLATPACK PIN CONFIGURATION



PIN NAMES

CP/I	Clock/Data Input
I	Data Input
I/O	Data Input/Output
V_{DD}	Power
V_{SS}	Ground

FUNCTION DESCRIPTION

The UT22VP10 RADPAL implements logic functions as sum-of-products expressions in a one-time programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Table 1. Macrocell Configuration Table

C_2	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O
1	0	1	Registered	Active HIGH	I/O

OVERVIEW

The UT22VP10 RADPAL architecture (figure 1) has 12 dedicated inputs and 10 I/Os to provide up to 22 inputs and 10 outputs for creating logic functions. At the core of the device is a one-time programmable anti-fuse AND array that drives a fixed OR array. With this structure, the UT22VP10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is a macrocell which is independently programmed to one of six different configurations. The one-time programmable macro cells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

LOGIC ARRAY

The one-time programmable AND array of the UT22VP10 RADPAL is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines

- 24 input lines carry the true and complement of the signals applied to the input pins
- 20 lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logic sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous reset term

At each input-line/product-term intersection there is an anti-fuse cell which determines whether or not there is a logical connection at that intersection. A product term which is connected to both the true and complement of an input signal will always be logical zero, and thus will not effect the OR function that it derives. When there are no connections on a product term, a Don't Care state exists and that term will always be a logical one.

PRODUCT TERMS

The UT22VP10 provides 120 product terms that drive the 10 OR functions. The 120 product terms connect to the outputs in groups of 8, 10, 12, 14, and 16 to from logical sums.

MACROCELL ARCHITECTURE

The output macrocell provides complete control over the architecture of each output. Configuring each output independently permits users to tailor the configuration of the UT22VP10 to meet design requirements.

Each I/O macrocell (see figure 2) consists of a D flip-flop and two signal-select multiplexers. Three configuration select bits controlling the multiplexers determine the configuration of each UT22VP10 macrocell. The configuration select bits determine output polarity, output type (registered or combinatorial) and input feedback type (registered or I/O). See figure 3 for equivalent circuits for the macrocell configurations.

OUTPUT FUNCTIONS

The signal from the OR array may be fed directly to the output pin (combinatorial function) or latched in the D flip-flop (registered function). The D flip-flop latches data on the rising edge of the clock. When the synchronous preset term is satisfied, the Q output of the D flip-flop output will be set logical one at the next rising edge of the clock input. Satisfying the asynchronous clear term sets Q logical zero, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

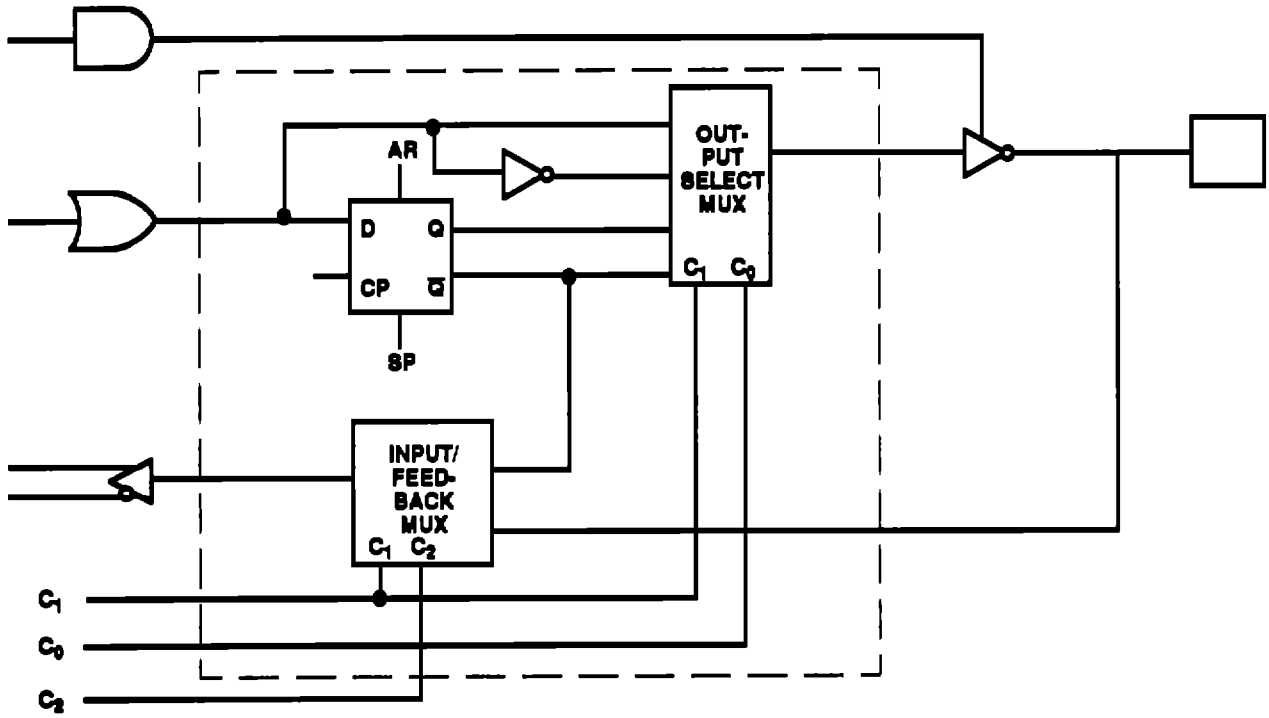


Figure 2. Macrocell

OUTPUT POLARITY

Each macrocell can be configured to implement Active-High or Active Low logic. Programmable polarity eliminates the need for external inverters. Unprogrammed device outputs are logical one (inputs don't care).

OUTPUT ENABLE

The output of each I/O macrocell can be enabled or disabled under the control a programmable output enable product term. The output signal is propagated to the I/O pin when the logical conditions programmed on the output enable term are satisfied. Otherwise, the output buffer is driven into the high-impedance state.

The output enable term allows the I/O pin to function as a dedicated input, dedicated output, or bidirectional I/O. When every connection is unprogrammed, the output enable product term permanently enables the output buffer and yields a dedicated output. If every connection is programmed, the enable term is logically low and the I/O functions as a dedicated input.

REGISTER FEEDBACK

The feedback signal to the AND array is taken from the $\overline{Q}$ output when the I/O macrocell implements a registered function ($C_2 = 0$, $C_1 = 0$).

BIDIRECTIONAL I/O

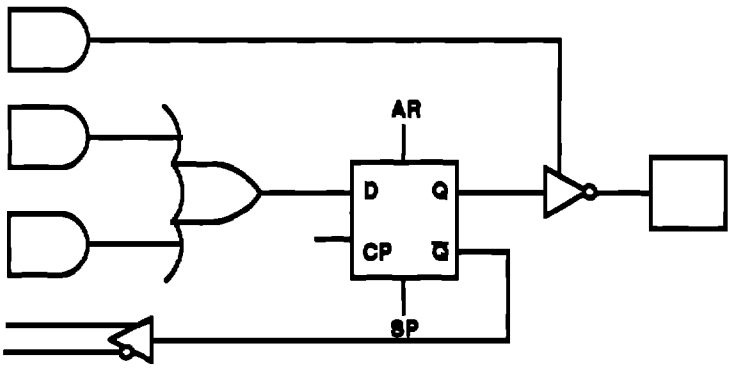
The feedback signal is taken from the I/O pin when the macrocell implements a combinatorial function ($C_1 = 1$) or a registered function ($C_2 = 1$, $C_1 = 0$). In this case, the pin can be used as a dedicated input, a dedicated output, or a bidirectional I/O.

POWER-ON RESET

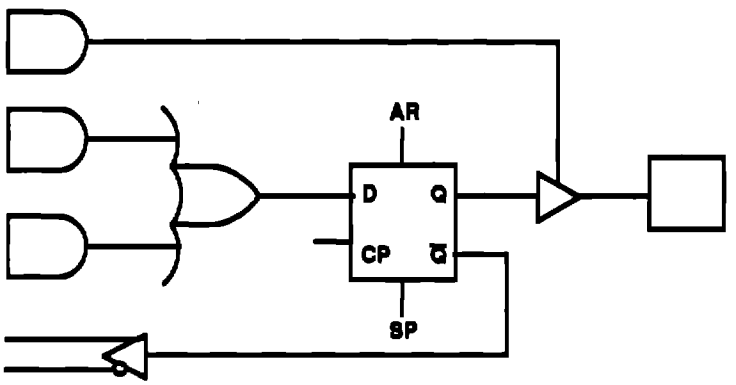
To ease system initialization, all D flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the UT22VP10 will depend on the programmed output polarity. The V_{DD} rise must be monotonic and the reset delay time is 5µs maximum.

ANTI-FUSE SECURITY

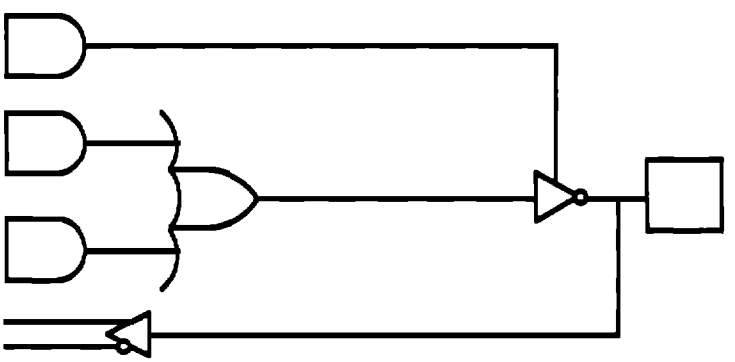
The UT22VP10 provides a special security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, at the conclusion of the programming cycle. Once the security bit is set it is impossible to verify (read) or program the UT22VP10.



Registered Feedback, Registered, Active-Low Output ($C_2 = 0, C_1 = 0, C_0 = 0$)

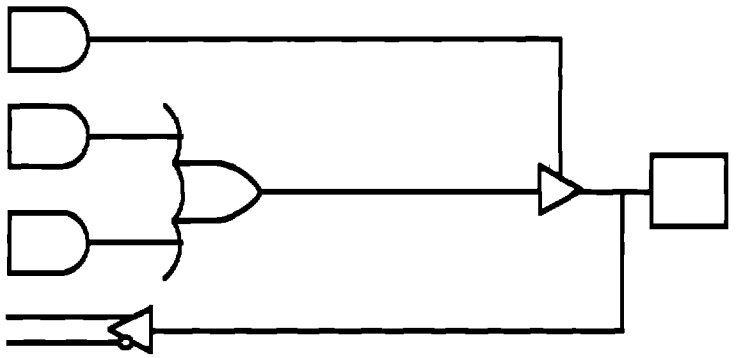


Registered Feedback, Registered, Active-High Output ($C_2 = 0, C_1 = 0, C_0 = 1$)

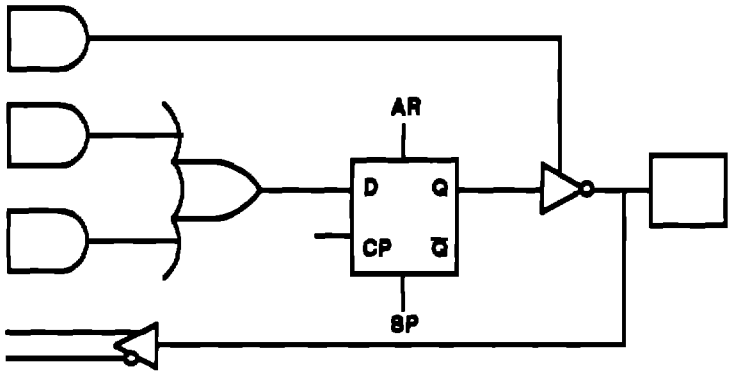


I/O Feedback, Combinatorial, Active-Low Output ($C_2 = X, C_1 = 1, C_0 = 0$)

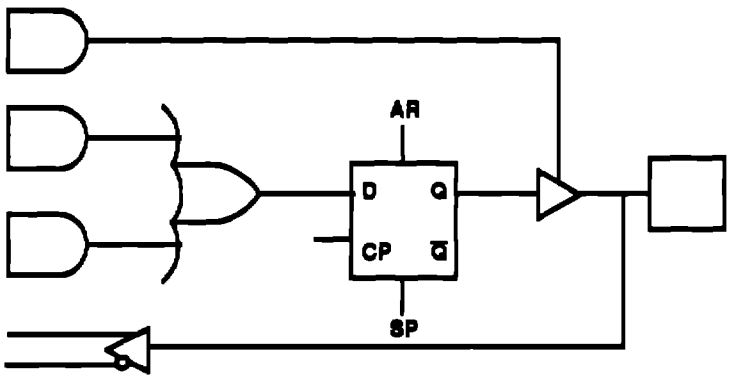
Figure 3. Macrocell Configuration *(continued on next page)*



I/O Feedback, Combinatorial, Active-High Output ($C_2 = X$, $C_1 = 1$, $C_0 = 1$)



I/O Feedback, Registered, Active-Low Output ($C_2 = 1$, $C_1 = 0$, $C_0 = 0$)



I/O Feedback, Registered, Active-High Output ($C_2 = 1$, $C_1 = 0$, $C_0 = 1$)

Figure 3. Macrocell Configuration

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Input voltage any pin	-0.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_S	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	± 10	mA
P_D[2]	Maximum power dissipation	1.6	W

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. (I_{CC} max + I_{OS}) 5.5V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [2]
(V_{DD} = 5.0V ± 10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

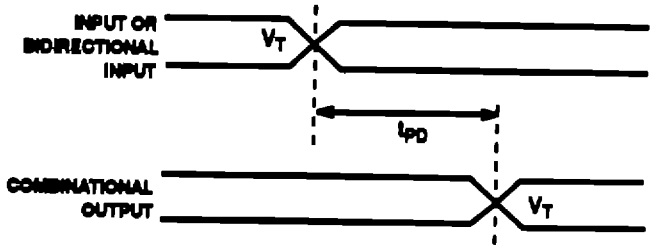
SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage	TTL	--	.8	V
V_{IH}	High-level input voltage	TTL	2.2	--	V
V_{IL}	Low-level input voltage	CMOS	--	.3*V_{DD}	V
V_{IH}	High-level input voltage	CMOS	.7*V_{DD}	--	V
V_{OL}	Low-level output voltage	I_{OL} = 12.0mA, V_{DD} = 4.5V (TTL)		.4	V
V_{OH}	High-level output voltage	I_{OH} = -12.0mA, V_{DD} = 4.5V (TTL)	2.4	--	V
V_{OL}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)	--	V_{SS}+0.05	V
V_{OH}	High-level output voltage	I_{OH} = -200µA, V_{DD} = 4.5V (CMOS)	V_{DD}-0.05	--	V
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-10	10	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V	-10	10	µA
I_{OS} [3,4]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	-160	160	mA
C_{IN} [5]	Input capacitance	f=1MHz @0V	--	15	pF
$C_{I/O}$ [5]	Bidirectional capacitance	f=1MHz @0V	--	15	pF
I_{CC}	Output three-state, worst-case pattern programmed, f_{MAX1}	V_{DD} = 5.5V	--	120	mA

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Duration not to exceed 1 second, one output at a time.
4. Guaranteed, but not tested.
5. Tested for initial qualification only.

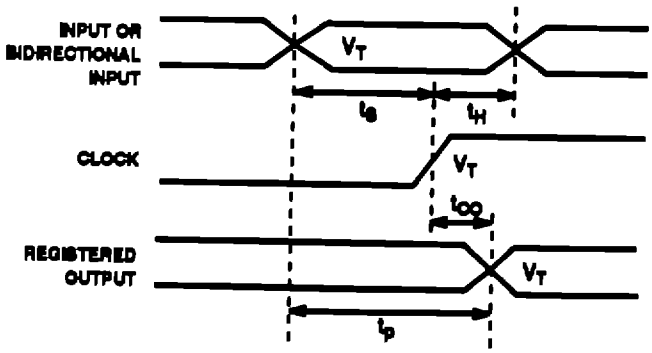
AC CHARACTERISTICS READ CYCLE (Post-Radiation) [1,2]
(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PD}	Input to output propagation delay	--	25	ns
t_{EA}	Input to output enable delay	--	25	ns
t_{ER}	Input to output disable delay	--	25	ns
t_{CO}	Clock to output delay	--	15	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback	--	28	ns
t_S	Input or feedback setup time	18	--	ns
t_H	Input or feedback hold time	0	--	ns
t_P	External clock period (t_{CO} + t_S)	33	--	ns
$t_{WH, WL}$	Clock width, clock high time, clock low time	14	--	ns
f_{MAX1}	External maximum frequency (1/(t_{CO} + t_S))	30	--	MHz
f_{MAX2}	Data path maximum frequency (1/(t_{WH} + t_{WL}))	36	--	MHz
f_{MAX3}	Internal feedback maximum frequency (1/(t_{CO} + t_{CF}))	32	--	MHz
t_{CF}	Register clock to feedback input	--	13	ns
t_{AW}	Asynchronous reset width	25	--	ns
t_{AR}	Asynchronous reset recovery time	25	--	ns
t_{AP}	Input to asynchronous reset	--	25	ns
t_{SPR}	Synchronous preset recovery time	25	--	ns
t_{PR}	Power up reset time	1.0	--	µs

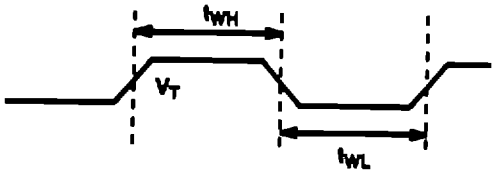
Notes:
1. Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
2. Guaranteed by characterization.



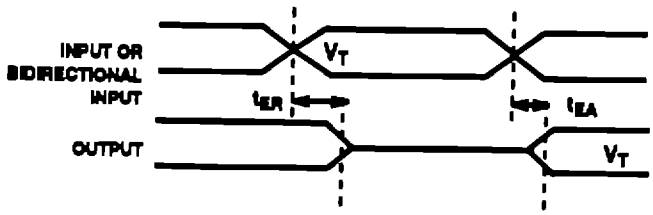
Combinatorial Output



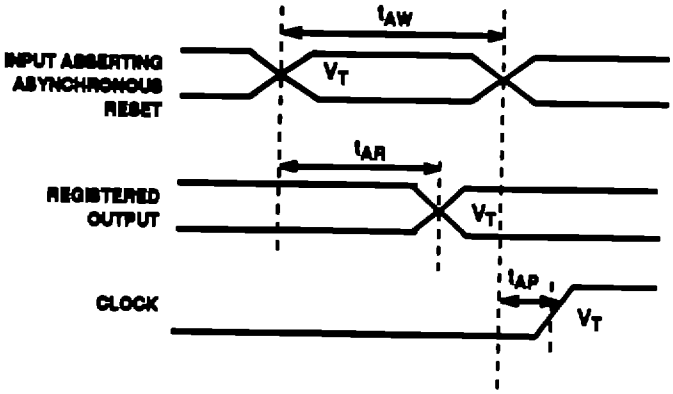
Registered Output



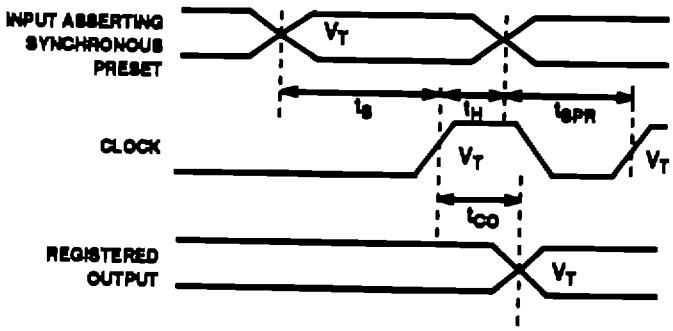
Clock Width



Combinatorial Output
(V_{OH} - 0.5V, V_{OL} + 0.5V)



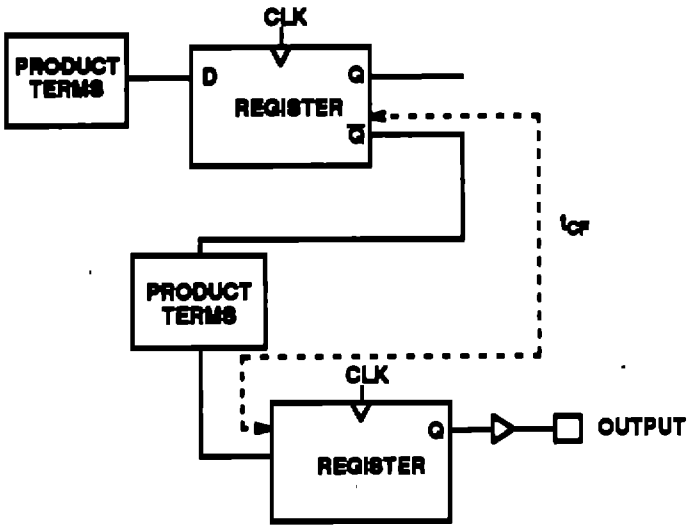
Asynchronous Reset

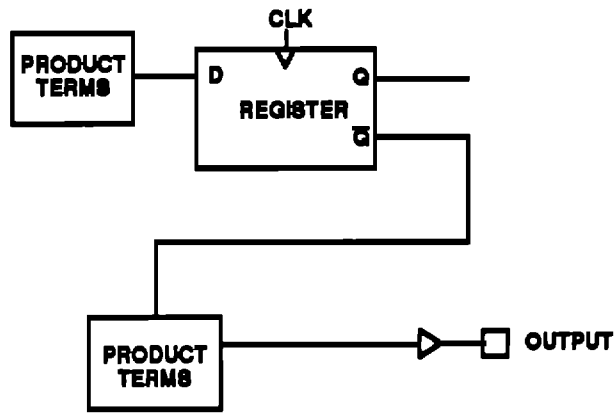


Synchronous Preset

Notes:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 3ns maximum.

Figure 4. AC Electrical





Clock to Combinatorial Output (t_{CO2})

Note:
t_{CF} defined as the propagation delay from $\overline{Q}$ to D register input.

$$f_{MAX3}\text{; Internal Feedback } \left(\frac{1}{t_{CO} + t_{CF}}\right)$$

Figure 5. Signal Paths

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. See figure 6 for a timing diagram. Due to the synchronous operation of the power-up reset and the wide range of ways V_{DD} can rise to its steady state, the following two conditions are required to ensure a valid power-up reset.

- The V_{DD} rise must be monotonic
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

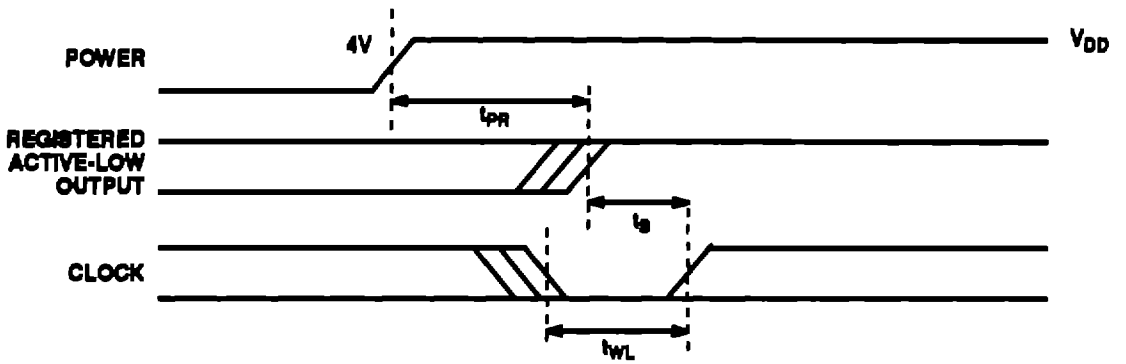


Figure 6. Power-Up Reset Waveform

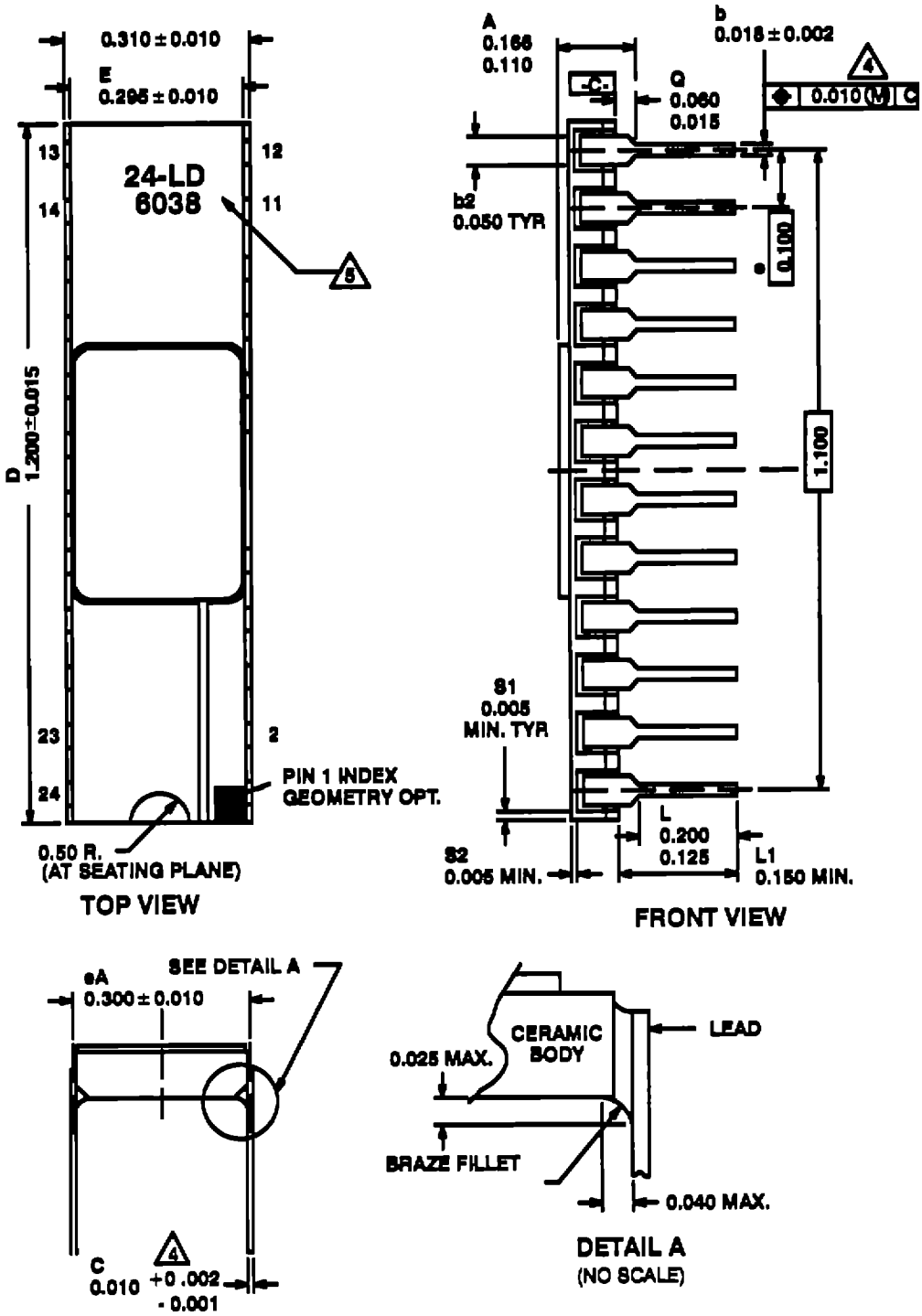
RADIATION HARDNESS

The UT22VP10 RADPAL incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

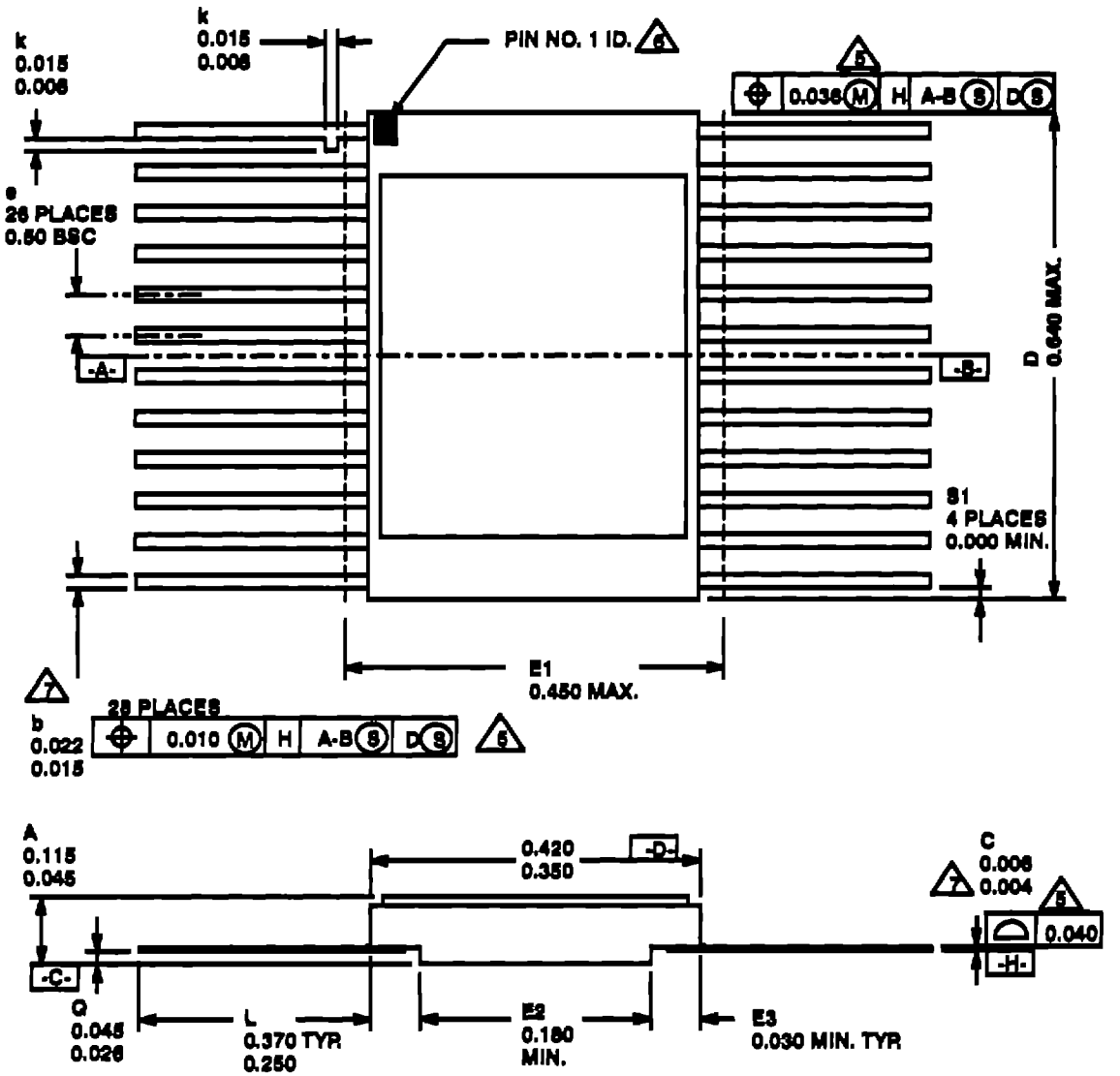
PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
LET Threshold	-55°C to +125°C	50	MeV-cm^2/mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm^2

Note:
1. The RADPAL will not latchup during radiation exposure under recommended operating conditions.



Notes:
1. Package material: Opaque ceramic.
2. All exposed metallized areas are finished per MIL-I-38535.
3. Letter designations are for cross-reference to MIL-STD-1835.
4. For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.
5. Numbering and lettering on the ceramic are not subject to visual marking criteria.

Figure 7. 24-Pin 100-mil Center DIP (0.300 x 1.2)



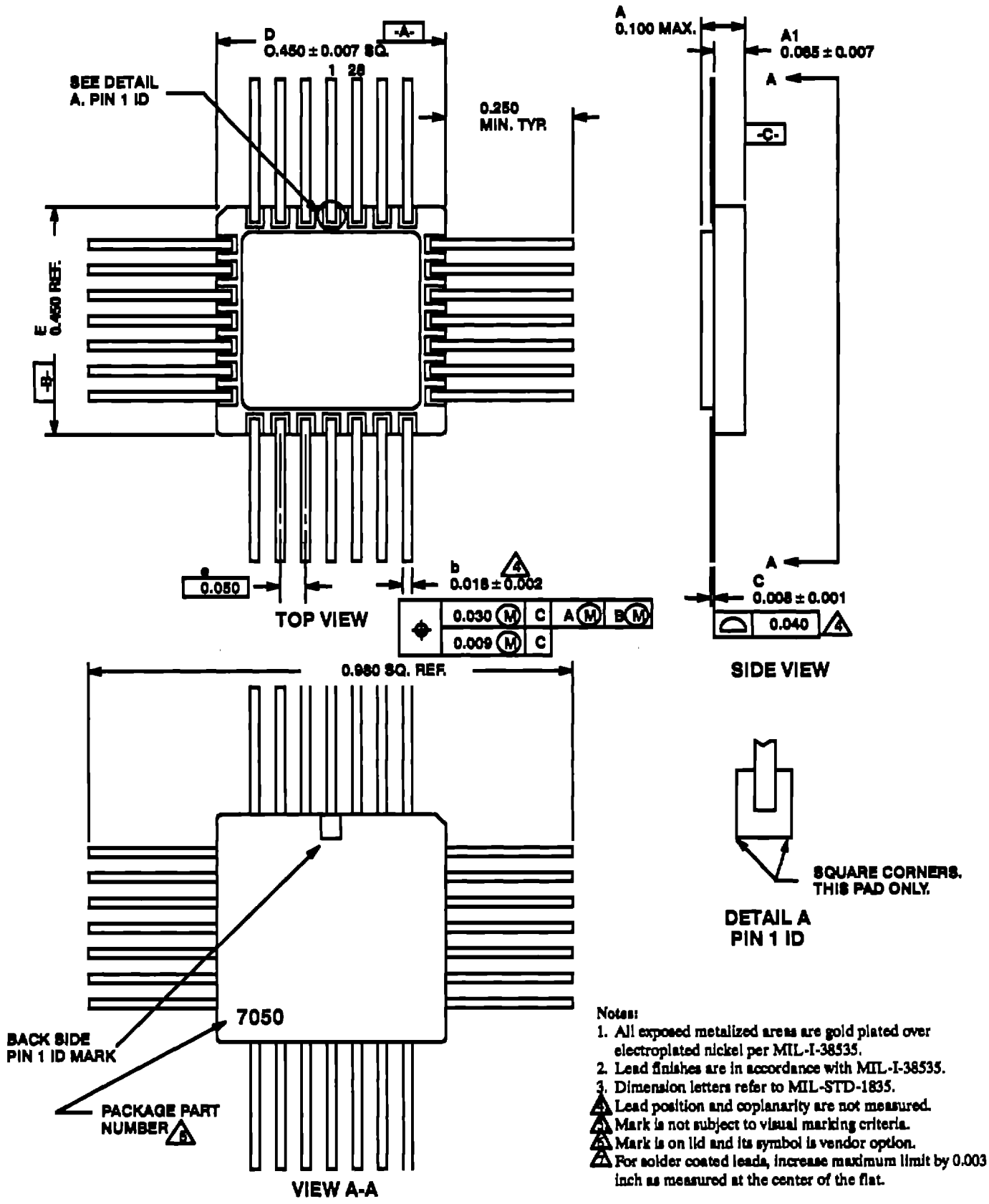
Notes:
1. All exposed metalized areas are gold plated over electroplated nickel per MIL-I-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-I-38535.
4. Dimension letters refer to MIL-STD-1835.

△ Lead position and coplanarity are not measured.

△ ID mark symbol is vendor option.

△ For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.

Figure 8. 24-Lead Flatpack (.45 x .64)



Notes:
1. All exposed metalized areas are gold plated over electroplated nickel per MIL-I-38535.
2. Lead finishes are in accordance with MIL-I-38535.
3. Dimension letters refer to MIL-STD-1835.
4. Lead position and coplanarity are not measured.
5. Mark is not subject to visual marking criteria.
6. Mark is on lid and its symbol is vendor option.
7. For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.

Figure 9. 28-Lead Quad-Flatpack (.45 x .45)

ORDERING INFORMATION

UT22VP10: Prototypes and Military Temperature Range

UT 22VP10 * _** * * *

- Lead Finish: [1]
  - (A) = Hot solder dipped
  - (C) = Gold
  - (X) = Factory option (gold or solder) [2]
- Screening:
  - (T) = Military temperature range flow [3]
  - (P) = Prototype flow [4]
- Package Type:
  - (P) = 24-lead ceramic side-brazed DIP (0.300" body)
  - (U) = 24-lead ceramic bottom-brazed dual-in-line flatpack (0.050" lead pitch)
  - (W) = 28-lead ceramic top-brazed quad-flatpack (0.050" lead pitch)
- Device Type Modifier/Speed:
  - (C-25) = CMOS I/O; 25ns propagation delay
  - (T-25) = TTL I/O; 25ns propagation delay

Notes
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military temperature range flow per *UTMC Manufacturing Flows Technical Description*. Devices have 48 hours of burn-in and are tested at -55°C, room temperature, and 125°C. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Prototype flow per *UTMC Manufacturing Flows Technical Description*. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is at UTMC's option and an "X" must be specified when ordering.

UT22VP10: QML Class Q & Class V

5962 - 94754 ** * * *

- Lead Finish: [1]
  - (A) = Hot solder dipped
  - (C) = Gold
  - (X) = Factory option (gold or solder) [2]
- Case Outline:
  - (L) = 24-lead ceramic side-brazed DIP (0.300" body)
  - (X) = 24-lead ceramic bottom-brazed dual-in-line flatpack (0.050" lead pitch)
  - (Y) = 28-lead ceramic top-brazed quad-flatpack (0.050" lead pitch)
- Class Designator:
  - (V) = Class V, QML qualified to MIL-I-38535
  - (Q) = CLASS Q, QML qualified to MIL-I-38535
- Device Type/Speed::
  - (01) = CMOS I/O: 25ns propagation delay
  - (02) = TTL I/O2; 5ns propagation delay
- Drawing Number: No options
- Total Dose:
  - (H) = 1E6 rads(Si) per 5962-94754 drawing
  - (R) = 1E5 rads(Si) per 5962-94754 drawing
- Federal Stock Class Designator: No options

Notes
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

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