Thin Film Technology Corp.

Product Family: High Power Chip Resistor

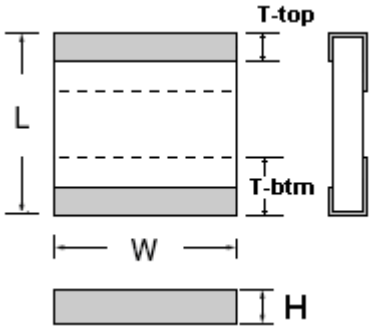
Construction:
- 99.5% BeO or 99.6% Alumina Ceramic
- Nickel alloy thin film resistive element
- Epoxy-resin overcoat
- Pre-tinned (Sn100, matte) terminations over Ni barrier

Features:
- TCR's to ± 25ppm
- Tolerances less than ± 1%
- Custom and standard sizes available
- High volume production, suitable for commercial and special applications

Description:

These power resistors are designed to tolerate high current and establish a low thermal resistance interface with the circuit board. A lower thermal resistance more efficiently sinks heat to the board, enabling a larger effective area for heat dissipation. As a result, much lower surface temperatures are achievable in comparison to standard chip resistors for the same chip size and applied power. The BP series effectively integrates the power resistor with the board, providing a thermal resistance comparable with aluminum heat-sinks.

Dimensions:

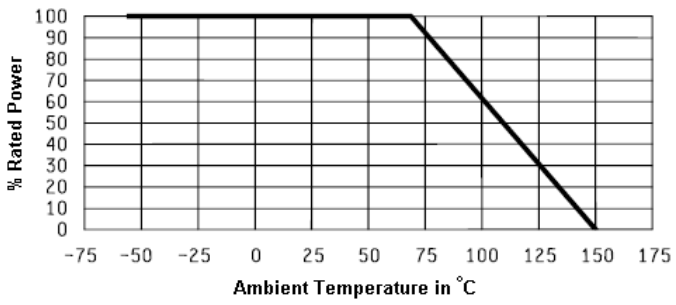


Size		Dimensions (mm)				
Inch	Metric	L	W	H	T-top	T-btm
2512	6332	6.3 ± 0.2	3.2 ± 0.2	1.1 ± 0.1 (BP) 0.7± 0.1 (CP)	0.9 ± 0.2	2.0 ± 0.2
2525	6363	6.3 ± 0.2	6.3 ± 0.2	1.1 ± 0.1 (BP) 0.7± 0.1 (CP)	0.9 ± 0.2	2.0 ± 0.2
Call for other sizes						

Electrical Specifications:

Size: Inch (Metric)	2512 (6332)	2525 (6363)
Rated Power at 70ºC [1] (BeO)	Up to 5W [1]	Up to 8W [1]
Rated Power at 70ºC [1] (Alumina)	Up to 2W [1]	Up to 3W [1]
Rated Voltage	√(PxR)	
Resistance Tolerance	± 1 to 5%	
Resistance Values	5 to 200 Ω, call for other values	
TCR (ppm/ºC) [2]	± 25 to 200	
Operating Temperature Range [3]	-55 to 150ºC	
Insulation Resistance (100V, 1min) [4]	> 1GΩ	

Derating Curve:



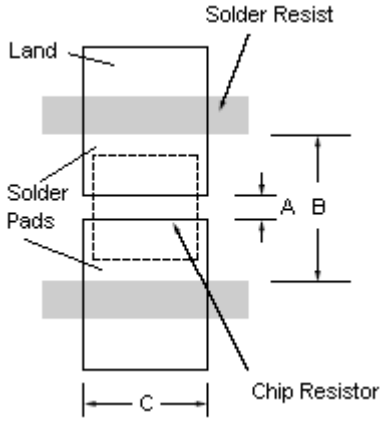
Notes:
1. Dependent on effective thermal conductivity of board construction/land design and size of board - greater power capability for board/land with lower thermal resistance. For relatively high thermal resistance mountings, the power resistors are capable of reflowing solder bonds before device damage occurs.
2. Per MIL-PRF-55342 (-55/25/125ºC).
3. Per MIL-PRF-55342, see derating curve.
4. Per IEC 60115-1.

Environmental Performance Specifications:

Test	Reference	Conditions of Test	Requirement
Life	MIL-PRF-55342, MIL-STD-202 Method 108A	70ºC, 2000h, rated power, 1.5h on, 0.5h off	± 0.5% + 0.01Ω
Thermal Shock	MIL-PRF-55342, MIL-STD-202 Method 107G	Condition F-3, -65ºC/0.25h to 150ºC/0.25h, 100 cycles	± 0.1% + 0.01Ω
High Temperature Exposure	MIL-PRF-55342	150ºC, 100h	± 0.1% + 0.01Ω
Short Time Overload	MIL-PRF-55342	6.25x rated power, 5 sec.	± 0.1% + 0.01Ω
Moisture Resistance	MIL-PRF-55342, MIL-STD-202 Method 106G	25/65/25/65/25/–10ºC, 90% to 98%RH, 10 cycles, 24h/cycle, with and without bias, bias = 1.5h on, 0.5h off @ 1/10th rated power	± 0.1% + 0.01Ω
Resistance to Soldering Heat [1]	MIL-PRF-55342, MIL-STD-202 Method 210F	260ºC for 15 sec., over 220ºC for 60 sec., 3 cycles	± 0.1% + 0.01Ω
Solderability [2]	MIL-PRF-55342, MIL-STD-202 Method 208H	Precondition E: 150ºC dry bake for 16h, Method 1 "Dip and Look Test", 245ºC, 5 sec., Pb-free (SnAgCu) Solder	Min 95% coverage of critical area
Board Flex	IEC 60115-1 / JIS C 5202	Bend amount of 3mm, measurements during and after bend	± 0.1% + 0.01Ω, No mechanical damage
Terminal Strength	MIL-PRF-55342	Force of 3kg for 30 sec.	No mechanical damage

Notes:
1. Test conditions modified to represent the high temperature Pb-free reflow conditions and an extra cycle is added.
2. JESD22-B102D adds test conditions for Pb-free and is aligned with J-STD-002B referenced in MIL-STD-202 Method 208H. JESD22-B102D procedure comes from EIA-638, "Surface Mount Solderability Test".

Recommended Solder Pad Dimensions:



	Dimensions (mm)	
Size: Metric (Inch)	2512 (6332)	2525 (6363)
A	1.6	1.6
B	7.7	7.7
C	3.5	6.7

Notes on board construction and land design:
1. A multi-layer board with several ground or power planes significantly reduces thermal resistance.
2. Plated via holes around the power resistor further reduces thermal resistance.
3. Maximize land area beyond solder pad area in both width and length to further reduce thermal resistance.
4. Optimizing the thermal resistance of the board helps dissipate heat, enabling higher power handling and lower surface temperatures.

Part Numbering: (Ex. BP2512S27R0J)

BP	2512	S	27R0	J
Product Designator	Size, Inch	TCR	Resistance Value	Tolerance
BP for BeO CP for Alumina	Refer to table above	E = ± 25 ppm/C H = ± 50 ppm/C K = ± 100 ppm/C S = ± 200 ppm/C	Ex. 27R0 = 27.0 Ω	F = ± 1% G = ± 2% J = ± 5%