SONY

CXP88800

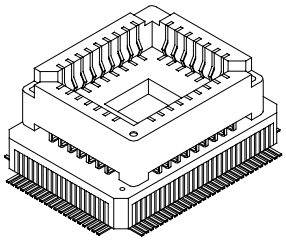
CMOS 8-bit Single Chip Microcomputer

Piggyback/ evaluator type

Description

The CXP88800 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP88616/88624, CXP88732/88740/88748 and CXP88852/88860.

100 pin QFP (Ceramic)



Features

- A wide instruction set (213 instructions) which cover various types of data.
  - 16-bit operation/multiplication and division/ boolean bit operation instructions
- Minimum instruction cycle: 250ns at 16MHz operation; 122µs at 32kHz operation
- Applicable EPROM: LCC type 27C512 (Maximum capacity : 60K bytes for option1, 32K bytes for option2)
- Incorporated RAM capacity: 1600 bytes
- Peripheral functions
  - A/D converter: 8-bit, 8-channel, successive approximation method (Conversion time of 20.0µs/16MHz)
  - Serial interface: Incorporated 8-bit and 8-stage FIFO (auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock synchronous type, 1 channel
  - Timer: 8-bit timer, 8-bit timer/counter, 2 channels; 19-bit time base timer, 32kHz timer/counter
  - High precision timing pattern generator: PPG 19-pin, 32-stage programmable, RTG 5 pins, 2 channels; 5-bit, 8-stage FIFO (RECCTL control), 1 channel
  - PWM/DA gate output: PWM output 12 bits 2 channels (Repetitive frequency 62.5kHz/16MHz); DA gate pulse output 13 bits, 2 channels
  - Analog signal input circuit: Capstan FG amplifier circuit; Drum FG amplifier circuit; Drum PG amplifer circuit; PBCTL amplifier circuit
  - CTL write/rewrite circuit: Recording current control circuit
  - Servo input control: Capstan FG, drum FG/PG, CTL input
  - VSYNC separator
  - FRC capture unit: Incorporated 26-bit and 8-stage FIFO
  - PWM output: 14 bits, 1 channel
  - VISS/VASS circuit: Pulse duty auto detection circuit
  - Remote control receiving circuit: 8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - Tri-state output: PPG output 1 pin, output 8 pins
  - Psendo HSYNC output function
  - High-speed head switching circuit
- Interruption: 20 factors, 15 vectors, multi-interruption possible
- Standby mode: SLEEP/STOP
- Package: 100-pin ceramic QFP

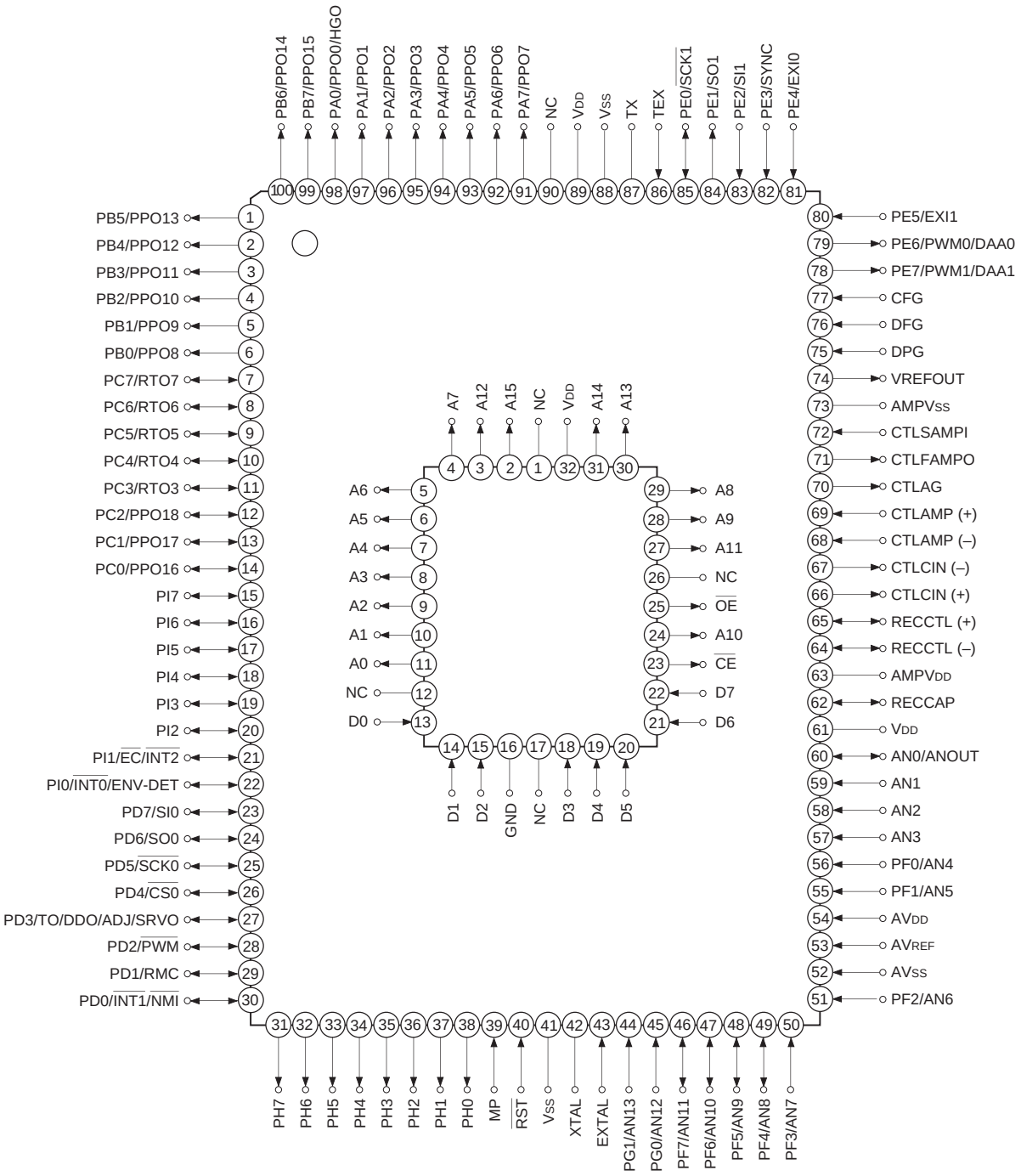
Note) Mask option depends on the type of the CXP88800. Refer to the Products List for details.

Structure

Silicon gate CMOS IC

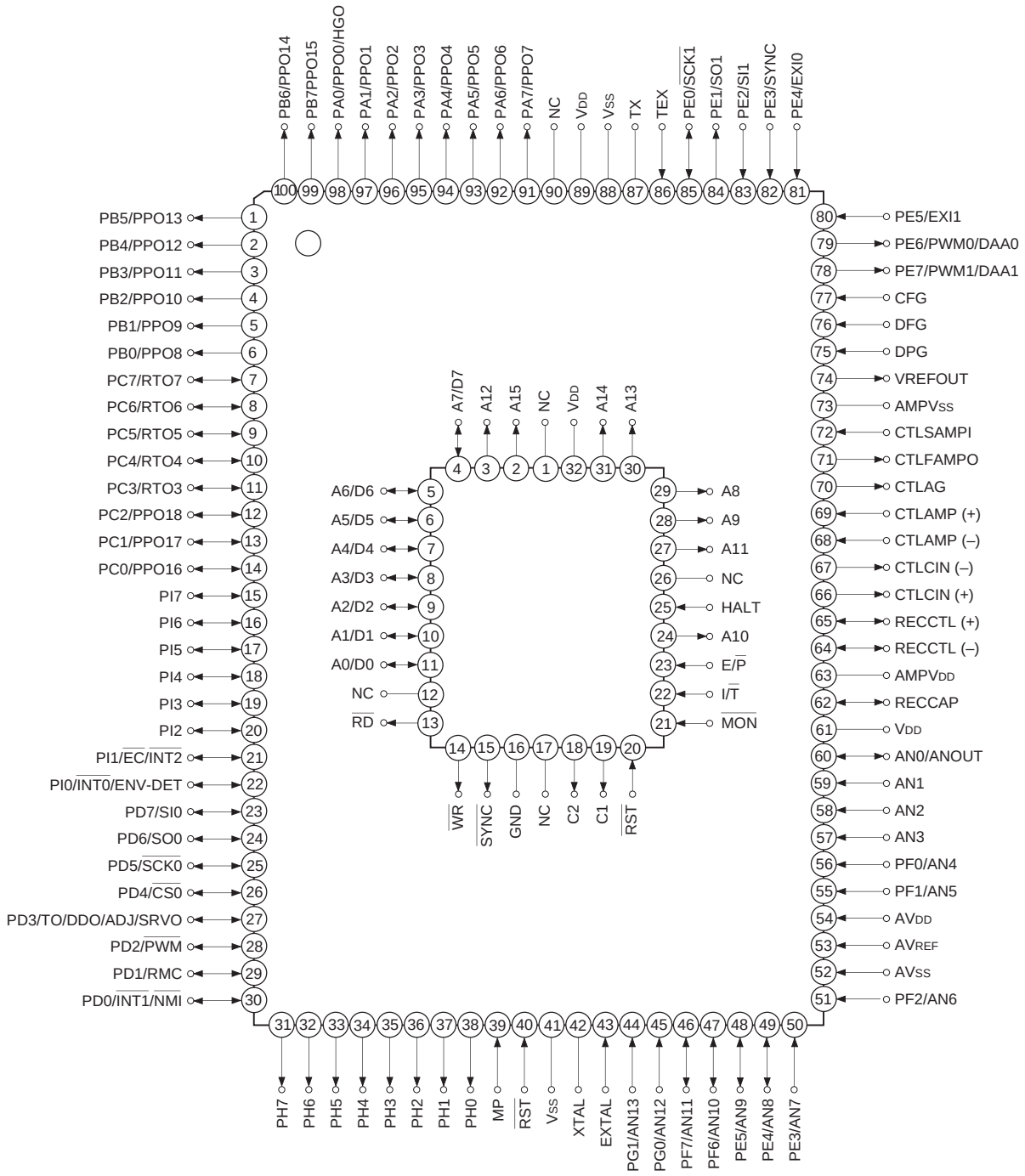
E96106-ST

Pin Assignment in Piggyback Mode



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{DD} (Pins 61 and 89) are both connected to V_{DD}.
3. V_{SS} (Pins 41 and 88) are both connected to GND.
4. MP (Pin 39) is always connected to GND.

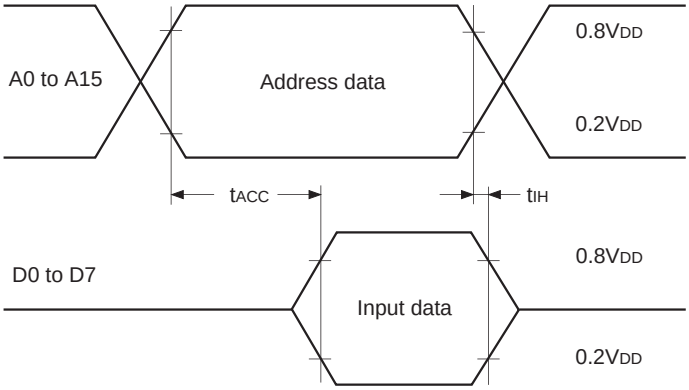
Pin Assignment in Evaluator Mode



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{DD} (Pins 61 and 89) are both connected to V_{DD}.
3. V_{SS} (Pins 41 and 88) are both connected to GND.
4. MP (Pin 39) is always connected to GND.

EPROM Read Timing (Ta=–20 to +75°C, V_{DD}=4.5 to 5.5V, V_{SS}=0V)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		75	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

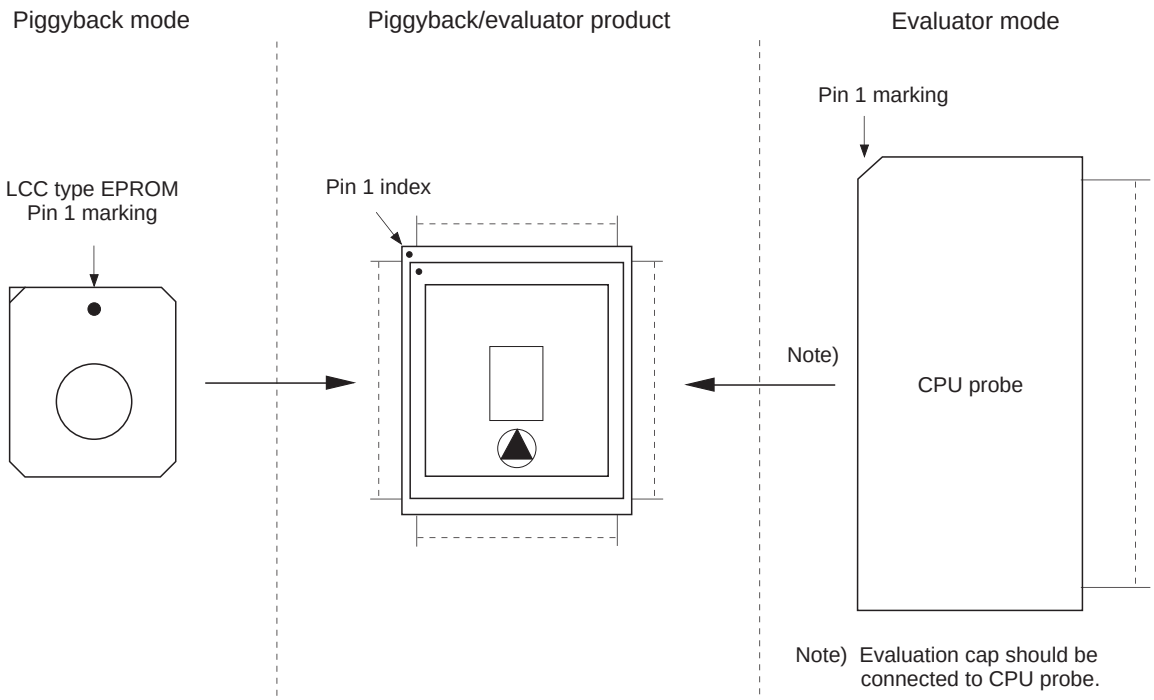


Product List

Option item	Products								
	Mask product							Piggyback/evaluator product	
	CXP 88616	CXP 88624	CXP 88732	CXP 88740	CXP 88748	CXP 88852	CXP 88860	CXP88800 -U01Q	CXP88800 -U02Q
Package	100-pin plastic QFP							100-pin ceramic QFP	
ROM capacity	16K bytes	24K bytes	32K bytes	40K bytes	48K bytes	52K bytes	60K bytes	EPROM 60K bytes	EPROM 32K bytes
								27C512 used	
Reset pin pull-up resistor	Existent/Non-existent							Existent	
Input circuit format*1	CMOS schmitt/TTL schmitt							TTL schmitt	
Power-on reset circuit	Existent/ Non-existent	Non-existent						Non-existent	Existent

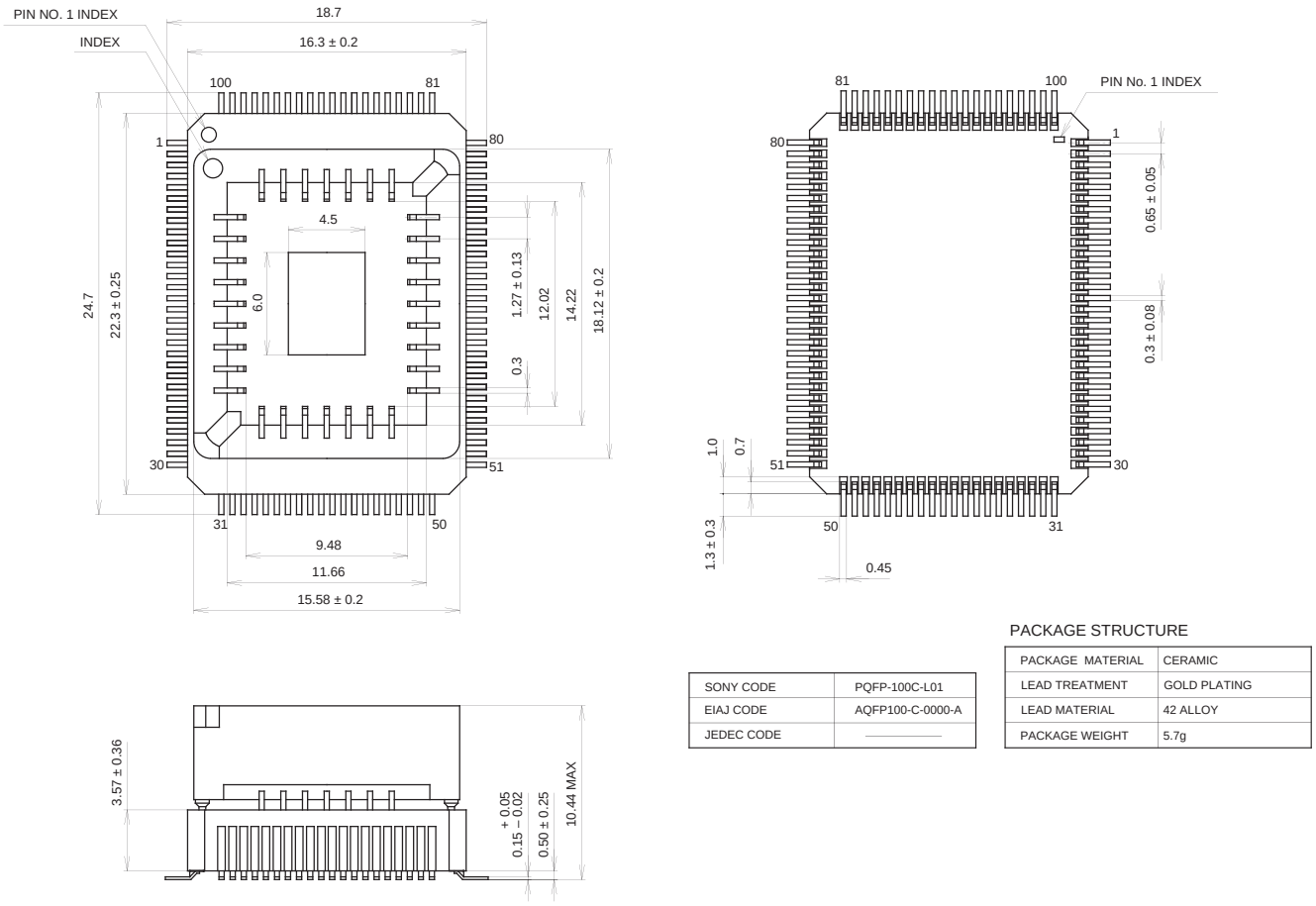
*1) The input circuit format can be selected for PE3/SYNC.

Piggyback mode/evaluator mode can be switched as shown below.



Package Outline Unit: mm

100PIN PQFP (CERAMIC)



SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g