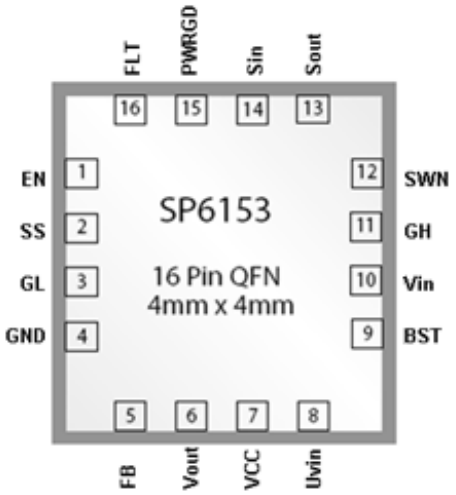
SP6153

300kHz Synchronous Buck Controller with Frequency Synchronization

FEATURES

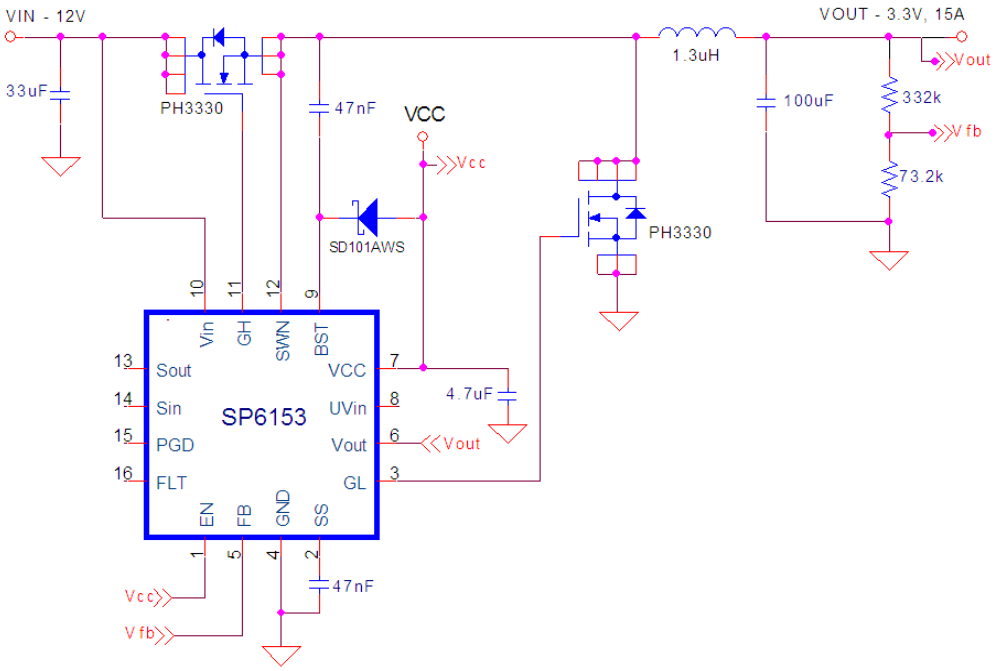
- 4.5V → 30V Input step down converter
- Built-in feedback compensation with feed forward
- Overcurrent circuit protection with auto-restart using FET RDSon sensing
- 300kHz fixed switching frequency
- External synchronization capable
- Up to 30A output capability
- Highly integrated design, minimal components
- UVLO detects both V_{CC} and V_{IN}
- Power Good and Fault Output
- On-board 1Ω sink (1.5Ω source) NFET drivers
- Programmable soft start
- Fast transient response
- High efficiency: Greater than 95% possible
- Evaluation boards available to aid in design



Description

The SP6153 has been designed to be implemented as synchronous step-down switching regulator. A complete high performance supply using Type III compensation can be created with as few as 11 external components. Compensation has been optimized based on output voltage and output capacitor selection. The SP6153 is designed to drive a pair of external N-Channel FETs using a fixed frequency, feed-forward PWM voltage mode architecture. Protection features include UVLO, thermal shutdown, current limit using FET RDSon and output short circuit protection.

TYPICAL APPLICATION SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

VCC……..……..5.5V
VIN… ……..……35V
BST……..……40V
BST-SWN……..……..……5.5V
SWN……..……..……-2V to 35V
GH…… -0.3V to BST+0.3V
GH-SWN……..……5.5V
All other pins……-0.3V to VCC+0.3V
Peak Output Current < 10us GH,GL…… ……... 2A

Storage Temperature……-65 °C to 150 °C
Power Dissipation……..1W
Lead Temperature (Soldering, 10 sec)……..……300 °C
ESD Rating…… …+/-1kV UVIN, +/-2kV All Other Pins HBM
UVIN to VIN……1kV
Thermal Resistance θ_{JC}……..……..5°C/W

ELECTRICAL SPECIFICATIONS: (Unless otherwise specified)

-40 °C< Tj< 125 °C, 4.5V<VCC<5.5V, VIN=12V, BST=LX+5V, UVIN=3.0V, CVCC=1uF, CCOMP=0.1uF, CGH=CGL=3.3nF, CSS=50nF, RPRGD=10K the ♦ denotes the specifications which apply over the full junction temperature range for 4.5<VIN<30 volts.

PARAMETER	MIN	TYP	MAX		UNITS	CONDITIONS
QUIESCENT CURRENT						
VIN Supply Current		2.6	3.5	♦	mA	VFB=1V, VIN = 12V (No switching)
BST Supply Current		0.3	0.6	♦	mA	VFB=1V (No switching)
VIN Sleep Current			50	♦	uA	EN = 0V
5V Internal Linear Regulator (Note 1)						
Vcc Output Voltage	4.6		5.4	♦	V	VIN=6V to 30V, ILOAD = 0ma-30mA

PARAMETER	MIN	TYP	MAX		UNITS	CONDITIONS
FEATURES: UVLO, Enable						
VCC UVLO Start Threshold	4.0	4.2	4.4	♦	V	
VCC UVLO Hysteresis		200		♦	mV	
UVIN Start Threshold	2.3	2.5	2.7	♦	V	Apply voltage to UVIN pin
UVIN Hysteresis		300		♦	mV	Apply voltage to UVIN pin
VIN Start Threshold	9.0	9.5	10	♦	V	UVIN Floating
			4.75	♦	V	(Vcc tied to UVin , Switching, CGL=CGH=3.3nF, BST tied to Vcc)
VIN Hysteresis		1.20		♦	V	UVIN Floating
Enable Threshold	0.8		1.6	♦	V	Applied voltage at EN pin

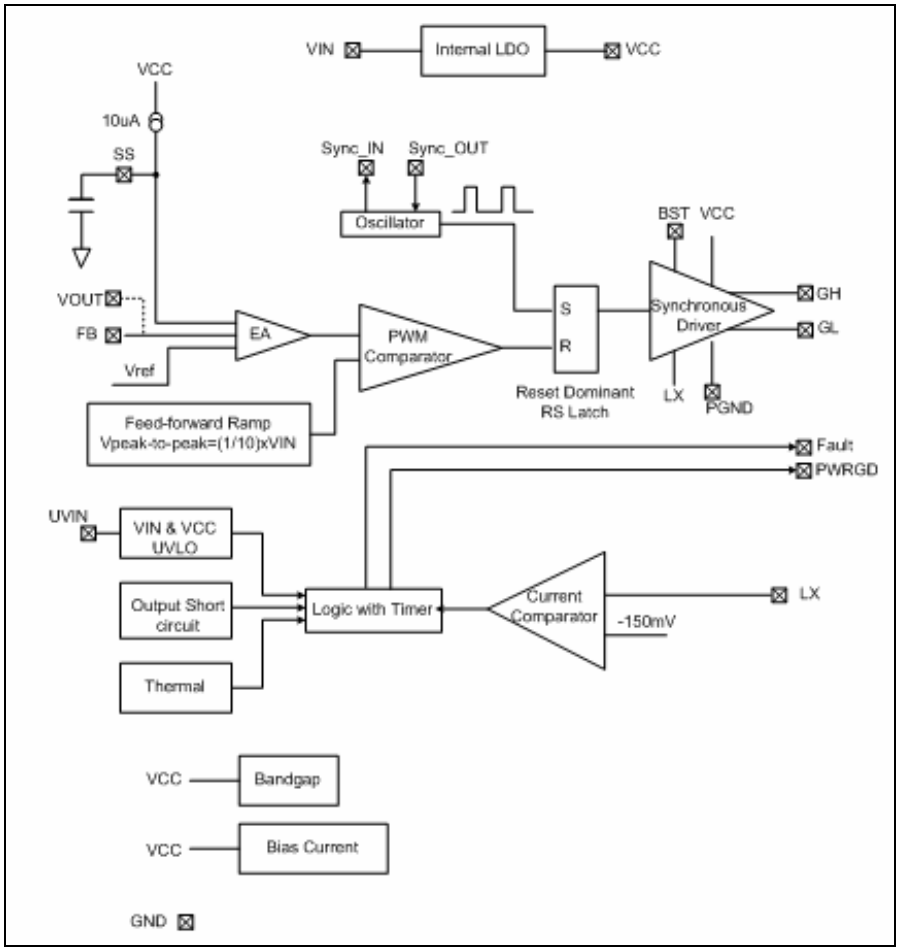
(Note 1): For 5Vin applications, it is suggested to tie Vcc to Vin to bypass internal LDO dropout and assure minimum input voltage operation.

PARAMETER	MIN	TYP	MAX		UNITS	CONDITIONS
ERROR AMPLIFIER						
Error Amplifier Reference	0.594	0.600	0.606		V	2X Gain Configuration, Measure VFB, Ta =25C
	0.588	0.606	0.612	♦	V	Over Line and Temperature
VFB Input Bias Current		150			nA	
CONTROL LOOP: PWM COMPARATOR, RAMP & LOOP DELAY PATH						
GH Minimum Pulse Width		50		♦	ns	Ramp COMP until GH starts switching
Maximum Duty Ratio	90	96			%	
Minimum Duty Ratio			0		%	
Internal Oscillator Frequency	255	300	345	♦	kHz	

PARAMETER	MIN	TYP	MAX		UNITS	CONDITIONS
SOFTSTART						
SS Charge Current:		10			uA	
SS Discharge Current:	3				mA	Fault Present; V_{SS}<0.1V
Power Good Output						
Power Good Threshold	-10	-7.5	-5		%	Measure % of VFB
Power Good Hysteresis		2			%	Measure % of VFB
Power Good Low-to-High Delay		220			ms	
PRGD, FLT Sink Current	1				mA	VFB = 0V, VPWRGD=VFLT = 0.2V, VCC $\geq$ 1V
PROTECTION: Overcurrent & Thermal Protection						
Short Circuit Threshold Voltage		0.25			V	Measured VREF (0.8V) – VFB
Overcurrent Threshold Voltage		150			mV	Measured SWN-GND
Overcurrent Threshold Voltage TC		0.4		♦	%/V	
Hiccup Timeout		220			ms	
Thermal Shutdown Temperature		145			°C	
Thermal Recovery Temperature		135			°C	
Thermal Hysteresis		10			°C	

OUTPUT: NFET GATE DRIVERS						
PARAMETER	**MIN**	**TYP**	**MAX**		**UNITS**	**CONDITIONS**
GH & GL Rise Times		35			ns	
GH & GL Fall Times		30			ns	
GL,GH Pull-down resistance		1			Ω	
GL,GH Pull-up resistance		1.5			Ω	
GL to GH Non Overlap Time		35	50	♦	ns	GH & GL Measured at 2.0V
SWN to GL Non Overlap Time		20	30	♦	ns	Measured SWN = 100mV to GL = 2.0V
GH & GL Pull Down Resistance		50			kΩ	

BLOCK DIAGRAM



PIN DESCRIPTION

PIN #	PIN NAME	DESCRIPTION
1	**EN**	Enable pin - pulling this pin below 2.5V will stop the part from switching, below 0.4V will place the IC into sleep mode. This pin is internally pulled to VCC with 1uA current source. This pin is ignored when the internal FAULT flag is set. When FAULT flag is cleared EN pin will return to normal function with 10us delay.
2	**SS**	Soft Start Pin. Connect an external capacitor between SS and GND to set the soft start rate based on the 10uA source current. The SS pin is held low via a 1mA (min) current during all fault conditions. The output rise time is dictated by the time the soft start pin takes to rise to 0.6Volts. The pin will continue to rise to 5V allowing easy implementation of Sequential, Ratiometric, and Simultaneous (Output Tracking) Power Up Protocols. See ANP6.
3	**GL**	High current driver output for the low side NFET switch. It is always low if GH is high or during a fault.
4	**GND**	'Power' ground Pin. Connect this pin as close as possible to the low-side FET source.
5	**VFB**	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever VFB drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
6	**VOUT**	Connect to converter output voltage.
7	**VCC**	Output of the internal 5V linear regulator or bias supply input. If external bias supply is used connect to the voltage between 4.5V and 5.5V.
8	**UVIN**	UVLO input for Vin voltage. Internal resistor divider connected between Vin and UVIN sets UVLO threshold at 8.5V. To adjust the threshold connect an external resistor divider – see applications section.
9	**BST**	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Typical Application Circuit on page 1.The high side driver is connected between BST pin and SWN pin and delivers the BST pin voltage to the high side gate each cycle.
10	**VIN**	Connect Input voltage supply to this pin.
11	**GH**	High current driver output for the high side NFET switch. It is always low if GL is high or during a fault.
12	**SWN**	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFET transistors. This point is also the input to the internal OCP comparator. The voltage across the low side FET(s) is measured each cycle and compared to a 150mV reference. See the applications section on how to calculate the OCP level.
13	**Sout**	Sync Output. This pin can be used to synchronize two PWM controllers. The output is a logic level pulse train at the converter switching frequency. The pulses are approximately 50% duty cycle regardless of the converters present duty cycle. The rising edge of this pulse correspond with the rising edge of the high side gate (GATEH) pulse
14	**Sin**	Sync Input. This pin serves as an input for synchronization pulses and can be used to ensure the supply will operate with a set phase in relation to another signal. The input signal should not exceed the controller VCC. It can range from 10% to 90% duty cycle and remain synchronized. The Sin signal must be within +/- 15% of the internal oscillator. The GL(high) signal will always be in phase with the connected Sin(high) signal. Example: to maintain out of phase operation a signal that corresponds with the GH of Supply 1 should be connected to Sin of supply 2. NOTE: WHEN NOT USED TIE Sin TO GND
15	**PWRGD**	Power Good Output. This open drain output is pulled low when Vout is outside of the regulation. Connect an external resistor to pull high. When the output reaches regulation this output transitions high after a pre-set 200ms delay. This pin is internally pulled to VCC with 2.5uA current source.
16	**FLT**	FAULT flag. This is an open-drain output that transitions low when the internal fault is detected. This pin is internally pulled to VCC with 2.5uA current source.
PAD	**AGND**	Analog ground pin. The controller VCC and logic are referenced to this pin.

General Overview

The SP6153 is a fixed frequency, voltage mode, synchronous PWM controller optimized for high efficiency. The part has been designed to be especially attractive for single supply input voltages ranging between 5V and 30V.
The heart of the SP6153 is a wide bandwidth transconductance amplifier designed to accommodate a Type III compensation scheme.

A precision 0.6V reference present on the positive terminal of the error amplifier permits the programming of the output voltage down to 0.6V via the VFB pin. The output of the Error Amplifier is internally compared to a feed-forward (VIN/5 pk-pk) ramp and generates the PWM control. Timing is governed by an internal oscillator that sets the PWM frequency at 300 kHz.

The SP6153 contains several unique control features that are very powerful in distributed applications. First, non-synchronous driver control is enabled during startup to prohibit the low side switch from pulling down the output until the high side switch has attempted to turn on. Programmable VIN UVLO allows the user to set the exact value at which the conversion voltage can safely begin down-conversion, and an internal VCC UVLO which ensures that the controller itself has enough voltage to properly operate. By using the softstart pin alone to control start-up ramp time or the softstart and enable pin can be used to create unique sequencing configurations.

SP6153 has Type-III internal compensation for use with Electrolytic/Tantalum or Ceramic output capacitors. The controllers internal 2A FET drivers are capable of driving FETs selected for output currents up to 30 Amps.

OCP is accomplished be measuring the voltage across the low side FET(s) each cycle. This voltage/(FET RDSon) represent the current through the device. The voltage is compared to a 130mV reference and if exceeded a complete restart of the controller is initiated repeatedly until the current level decreases ('hiccup' mode) See the applications section on how to calculate the OCP level.

Other protection features include thermal shutdown and short-circuit detection. In the event that either a thermal, short-circuit, or UVLO fault is detected, the SP6153 is forced into an idle state where the output drivers are held off for a finite period before a restart is attempted.

A thermal PAD on the bottom of the QFN package ensures the controller remains cool even when driving large FETs.

Soft Start

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the positive terminal of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor.

$$I_{Vin} = \frac{C_{out} \ \Delta V_{out}}{\Delta T_{soft-start}}$$

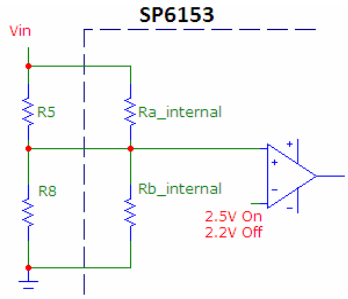
The SP6153 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10µA pull up current present at the SS pin and the 0.6V reference voltage. Therefore, the excess source can be redefined as:

$$I_{Vin} = \frac{10\mu A \ C_{out} \ \Delta V_{out}}{C_{ss} \ 0.6}$$

A typical start-up time of approximately 5ms (Vout = 0 to Vout nominal) can be achieved by using a 47nF capacitor on the soft start pin.

Under Voltage Lock Out (UVLO)

The SP6153 has two separate UVLO comparators to monitor the bias (Vcc) and Input (Vin) voltages independently. The Vcc UVLO is internally set to 4.2V. The Vin UVLO is programmable through UVIN pin. When UVIN pin is greater than 2.5V the SP6153 is permitted to start up pending the removal of all other faults. A pair of internal resistors is connected to UVIN as shown in the figure below.



Internal and external bias of UVIN

Without external biasing the Vin start threshold is 8.5V. A small capacitor may be required between UVIN and GND to filter out noise. For applications with Vin of 5V or 3.3V, connect UVIN directly to Vin. To program the Vin start threshold, use a pair of external resistors as shown. External resistors should be in the order of one to ten thousand ohms. This will ensure they are an order magnitude smaller than internal resistors. The Vin start threshold is given by:

$$V_{in_{start}} = 2.5\left(\frac{R5 + R8}{R5}\right)$$

For example, if it is required to have a Vin start threshold of 7V, then let R8 = 5kΩ and using the Vin start threshold equation we get R5= 9.09kΩ

Thermal and Short-Circuit Protection

Because the SP6153 is designed to drive large output current, there is a chance that the controller could become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures. When the IC temperature returns to 10 degrees below the shutdown temperature (typically 135°C) the IC will begin operation again with a normal soft-start.

A short-circuit detection comparator has also been included in the SP6153 to protect against an accidental short at the output of the power converter. This protection feature operates separately from the over current protection circuitry. A comparator constantly monitors the positive and negative terminals of the error amplifier, and if the VFB pin falls more than 250mV (typical) below the positive reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.6V reference during soft start, the SP6153 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

Power Good and Fault

Power Good Output: This open drain output is pulled low when Vout is outside of regulation. Connect an external resistor to pull high. When the output reaches regulation this output transitions high after a pre-set 200ms delay. This pin is internally pulled to VCC with 2.5uA current source.

The fault pin is an open-drain output that transitions low when the internal fault is detected. When multiple SP6153s are used together FAULT pins can be connected together and applied to all ENABLE inputs to ensure that under fault condition all converters turn-off and re-start with correct sequence. This pin is internally pulled to VCC with 2.5uA current source.

Over Current Protection and FET selection

Select the Power MOSFET(s) for Voltage rating $V_{(BR)}DSS$, on resistance: RDSon, and thermal resistance R_{thja}. The MOSFET voltage rating $V_{(BR)}DSS$ should be about 1.25 X Vin in order to guard against switching transients. A higher or lower rating may be concluded once MOSFET performance is characterized in circuit. RDSon should be selected such that when operating at peak current and junction temperature the overcurrent trip voltage of the SP6153 is not exceeded. Allowing 50% for temperature coefficient of RDSon and 15% for inductor current ripple, the following expression can be used as a quick selection reference:

$$RDSon \leq \frac{150mV}{1.5 * 1.15 * I_{out}}$$

More than one MOSFET may be required to meet the RDSon requirement. Within this constraint, selecting MOSFETs with lower RDSon will reduce conduction losses at the expense of increased switching losses. As a rule of thumb select the highest RDSon MOSFET that meets the above criteria

As a rough guide switching losses can be assumed to equal the conduction losses. A simplified expression for conduction losses is given by: (note Iout would be divided by number of FETs if >1)

$$P_{cond-HighSide\ FET} = I_{out}\ \ RDS_{on}\ \ \frac{V_{out}}{V_{in}}$$

or

$$P_{cond-LowSide\ FET} = I_{out}\ RDS_{on}\left[1 - \frac{V_{out}}{V_{in}}\right]$$

Then the MOSFETs junction temperature can be estimated from:

$$T_j = \left(2\ P_{cond}\ R_{th(ja)}\right) + T_{ambient}$$

Over current protection is accomplished by comparing the voltage across the low side MOSFET(s) when fully ON, to a fixed 150mV reference after a pre-set blanking time of ~120ns. The MOSFET voltage is measured at the SWN pin. This voltage represents the current through the device(s) at that point in time by Ohms Law.

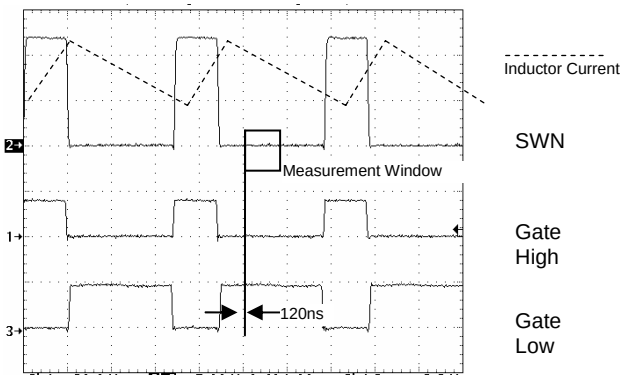
A quick estimate of the current trip point can be calculated by dividing the voltage trip level by the FET RDSon. Divide the FET resistance by the number of FETs in use.

$$OCP\ Level = \frac{150mV}{FET\ RDSon}\ (Amps)$$

However, in a DC-DC Buck Converter the inductor current is saw tooth in shape as it is charged and discharged linearly each cycle. To understand the exact trip point of your converter it is important to consider the inductor current ripple, this may be high if you are designing a wide input range converter and you are considering the entire Vin range.

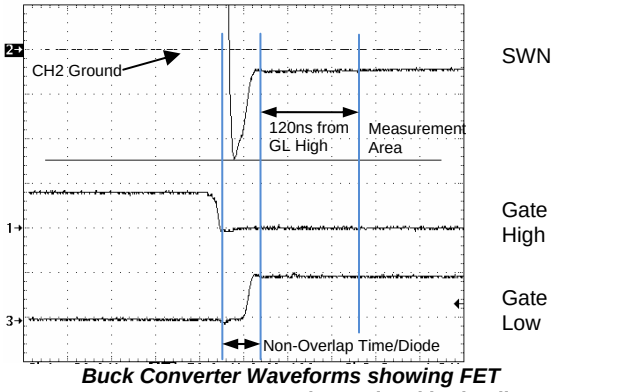
The MOSFET current is measured at a minimum of 120ns after the Gate Low signal has gone high (FET is ON) and as a result it is very close to the peak current in the inductor. The peak inductor current varies with the amount of inductance used, the input and output voltage, as well as the converter frequency; therefore it is necessary to consider these variables when calculating the converter current limit.

When the low side gate signal is high, the FET(s) is on. It is during this time the FET voltage must be sampled to measure the current.



Buck Converter Waveforms showing FET measurement area

The box shows the mesurement window (not to scale) after a 120ns minimum delay.
If we were to zoom in to the region around the mesurement window we would see the reason for the measurement delay as illustrated below. To ensure both the high and low side FET are never on at the same time there is a built in 'Non-overlap Time' to the FET driver. This is a short period (35ns typical) where neither FET is on. During this time the low side FET intrinsic or body diode will conduct briefly. The intrinsic diode has a forward voltage that is much higher than the voltage drop caused by the FET RDSon as shown below. It is not desired to measure the current during this time. Note that the voltage across the low side FET while conducting is negative. It is this negative voltage that is measured by the controller.



Buck Converter Waveforms showing FET measurement area and SWN level in detail

The inductor peak current can be calculated using the following formula:

$$I_{pk} = I_{out} + \frac{1}{2}\left[\frac{(V_{in} - V_{out})\ V_{out}}{V_{in}\ f_{sw}\ L}\right]$$

The peak FET voltage drop is then

$$Fet\ Peak\ Voltage = I_{pk}\ RDSon$$

For the FET RDSon value it is important to consider how many FETs are in use, the FET resistance at the temperature you are operating at, the FET resistance at the gate drive voltage you are using (use the 4.5V worst case level) and any trace resistance between the FETs and the meauring points that would generate any signifigant voltage drop.

The OCP trip voltage is not adjustable. However, the 150mV trip level should typically provide the user with a nominal 150% over current trip point when using FETs that have been selected to provide a good performance and size balance for the application. Users designing with maximum efficiency as their only goal and who are using FETs well below their current ratings could find the current limit higher than the 150% nominal level.

Boost Pin

Connect a 0.047µF low-ESR ceramic capacitor between the BST pin and SWN pin. The high-side MOSFET gate drive voltage is provided by this capacitor. Type X7R or X5R are recommended due to their stable values over temperature.

To obtain the Vin+Vcc voltage the high-side FET gate requires to turn on, a boost diode is required to be connected from Vcc to the BST pin. Select a part that is rated to a minimum of Vin and an average current rating of 20mA. A series resistor referred to as a 'Boost Resistor' is sometimes required to slow switching slightly and reduce circuit noise. (See application schematic for resistor placement in circuit) In particular for high current or high Vin designs, it is helpful to place this resistor in case it is required. If the design meets performance specification without it, it can be shorted or removed.

Setting the Output Voltage

The output voltage can be programmed by using a voltage divider on the output. Because the compensation is internal, an R1 of 332kΩ must be used. Set the output voltage using the following equation:

$$R_{2=}\frac{332k}{\left(\frac{V_{out}}{0.6}-1\right)}$$

Input Capacitor Selection

The input capacitance should be selected to maintain a minimum input ripple of approximately 300mV.

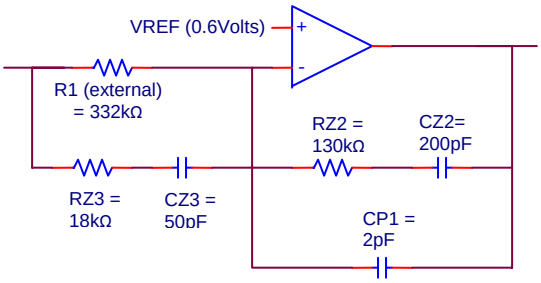
$$C_{in}=\frac{I_{out}\left[1-\frac{V_{out}}{V_{in(ave)}}\right]\frac{V_{out}}{V_{in(ave)}}}{300mV * 300kHz}$$

Check the capacitance versus operating voltage ratings for the ceramic capacitors selected. Very significant reductions in capacitance can be seen when used above 1/3 the rated voltage.

Output Inductor and Output Capacitor Selection with Example

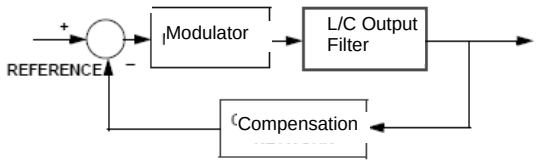
The 6153 has a built in Type III compensation. This saves valuable board space and still allows for the use of high performance - low ESR ceramic output capacitors. However, because the compensation is fixed certain guidelines must be followed to yield a stable design.

If you have experience designing a DC-DC converter with Type III compensation use the internal compensation values shown below in your design calculations and simulations.



6153 Internal Compensation Components

Alternatively the following simplified design procedure can be used. The equations are derived from the standard Buck converter model containing the Modulator, Output Filter, and Compensation Network.



Basic Buck Converter Control Model

The equations in this simplified approach account for the ramp and input voltage, the location of the LC double pole and the location of the output capacitor ESR zero. They will ensure there is adequate phase boost at the converter cross-over frequency to provide stable operation. Other assumptions that were made generating the simplified equations include:

i) The converter bandwidth will be approximately 30kHz

ii) CZ2 was selected by placing a zero from the compensation network at 50% of the output filter double pole frequency

iii) CP1 was calculated by placing the first pole at the ESR zero frequency

iv) RZ3 and CZ3 were selected so that the second pole is at ½ the switching frequency and the second zero is set at the output filter double pole

Step 1: Calculate the required output inductance:

$$L_{min} = \frac{V_{out}\ (V_{in(max)} - V_{out})}{V_{in(max)}\ f_{sw}\ I_{out}\ ripple\%}$$

where the ripple% is usually 30 to 40% of the maximum output current. For example: for 40% ripple, *ripple%* would be equal to '0.4'.
In general, a higher ripple % will mean a lower inductance, smaller inductor and a faster transient response but higher output voltage ripple.

For a 5V to 1.8Vout design at 20Amps we calculate:

$$L_{min} = \frac{1.8 * (5 - 1.8)}{5 * 300kHz * 20 * 0.3} = 0.48\mu H$$

Step 2: Output Capacitor Selection

The output capacitor contributes two parts of the control equation, the actual output capacitance and the capacitor ESR. The calculated target output capacitance will guarantee a stable solution, however, a significant amount of variation can be tolerated because of the conservative design procedure implemented. A final C_{out} total of -50% to +300% can be tolerated. When it is desired to use a C_{out} value beyond these limits the supply should first be simulated for stability.

Calculate the target output capacitance from:

$$C_{out\ target} = \frac{1 * 10^{-10}}{L}$$

From our example above we calculate:

$$C_{out\ target} = \frac{1 * 10^{-10}}{0.48\mu H} = 208uF$$

The supply also has a load transient requirement. With a 10 Amp load transient the supply output is required not exceed a 2% voltage deviation. The capacitance required to maintain the output to this level is calculated by:

$$C_{out} = \frac{\Delta I_{out}^{\ 2}\ L}{2\ \Delta V_{out}\ \left((V_{in}\ D_{max}) - V_{out}\right)}$$

Where ΔV_{out} is the voltage deviation, D_{max} is the maximum converter duty cycle, in this case 90%, use 0.9. Continuing with our example the C_{out} requirement for transient will be:

$$C_{out} = \frac{(10)^2 * 0.48\mu H}{2 * (1.8 * .02) * ((5 * 0.9) - 1.8)} = 246\mu F$$

We will select 300uF for our output capacitance. Next we calculate the target output capacitor ESR. Remember that paralleling capacitors also parallels the capacitor ESR.

$$ESR_{target} = \frac{3 * 10^{-7}}{C_{out}}$$

From out example this calculates to:

$$ESR_{target} = \frac{3 * 10^{-7}}{300\mu F} = 1m\Omega$$

The same considerations apply to this target output capacitor ESR. A final output capacitor ESR total that is -50% to +300% can be tolerated without concern. 3 X 100uF ceramic capacitors will be selected. The Murata part number GRM31CR60J107M is suitable. At 300kHz each capacitor has an ESR of approximately 5mΩ, giving a total output ESR of approximately 1.6mΩ.

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{out} = \sqrt{\left(\frac{I_{pk-pk}\,(1-D)}{f_{sw}\;C_{out}}\right)^2 + \left(I_{pk-pk}\;ESR\right)^2}$$

Where $I_{pk\text{-}pk}$ is defined by

$$I_{pk-pk} = \frac{V_{out}\;(V_{in-max} - V_{out})}{V_{in-max}\;f_{sw}\;L}$$

Layout

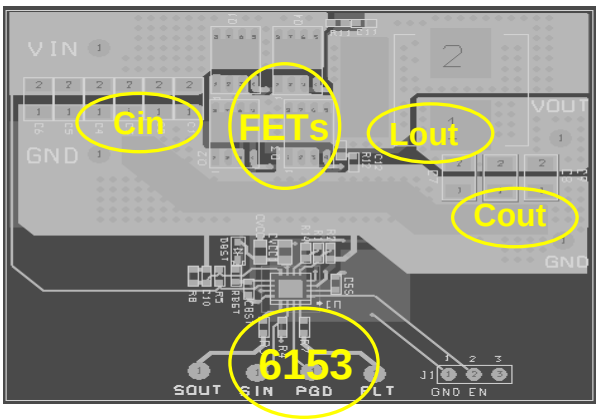
The SP6153 uses two sets of critical components: switching power components and the small signal components. The essential small signal components are those connected to susceptible nodes or those supplying critical bias currents. The switching power components are most important from a layout point of view because they switch a large amount of energy and tend to produce a large amount of electrical noise. A multi-layer printed circuit board is recommended.

Layout Considerations

A) Create a separate small analog ground plane near or under the IC. Connect the Signal Ground center pad to this plane. Small signal grounding paths including feedback resistors, soft start capacitor, should be connected to this Signal Ground plane.
B) The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistances. Connect the Vout pin as close as possible to the load.
C) Route all high speed switching nodes away from the control circuitry.
D) Place the high side FET source as close as possible to the low side FET drain.
E) Place The PWM controller IC close to lower FET. The GL connection should be short and wide. The IC can be best placed over a quiet ground area. Avoid switching ground loop current in this area.
F) The Upper FET, Lower FET, Input capacitors, Inductor and Output capacitor, should be placed first. Isolate these power components on the topside of the board with their ground terminals adjacent to one another. Place the input ceramic capacitor(s) very close to the MOSFETs.
G) Keep the loop formed by Input capacitor, the top FET and the bottom FET as small as possible.
H) Insure the current paths from the input capacitor to the MOSFET; to the output inductor and output capacitor are as short as possible with maximum allowable trace widths.
I) Place the gate drive components Boost capacitors and Boost diode together near the SP6153 IC.
J) Use wide but short traces or if possible, copper filled polygons to connect the junction of upper FET, lower FET and output inductor.
K) Do not unnecessarily oversize the copper islands for SWN/LX node. Since the SWN node is subjected to very high dv/dt voltages, the stray capacitance formed between these islands and the surrounding circuitry will tend to couple switching noise.
L) Ensure the feedback connection to output capacitor is as short and direct as possible

For more detail on the 6153 layout see the SP6153EVB (Evaluation Board) Manual available on our web site. Each layer is shown in detail as well as a complete bill of materials and performance characterization.

Starting at the top left, the areas noted are as follows: Input Capacitors, MOSFETs, Output Inductor, Output Capacitance, and Controller IC.

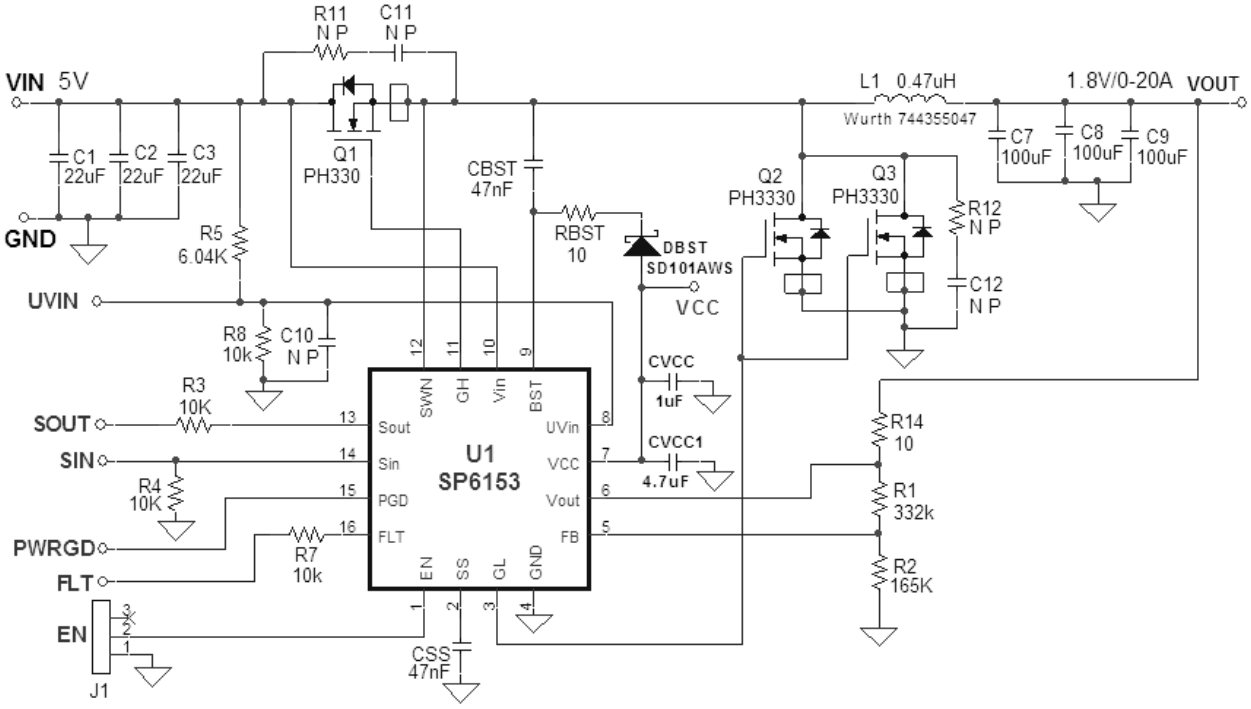


6153 Evaluation Board Screen Shot

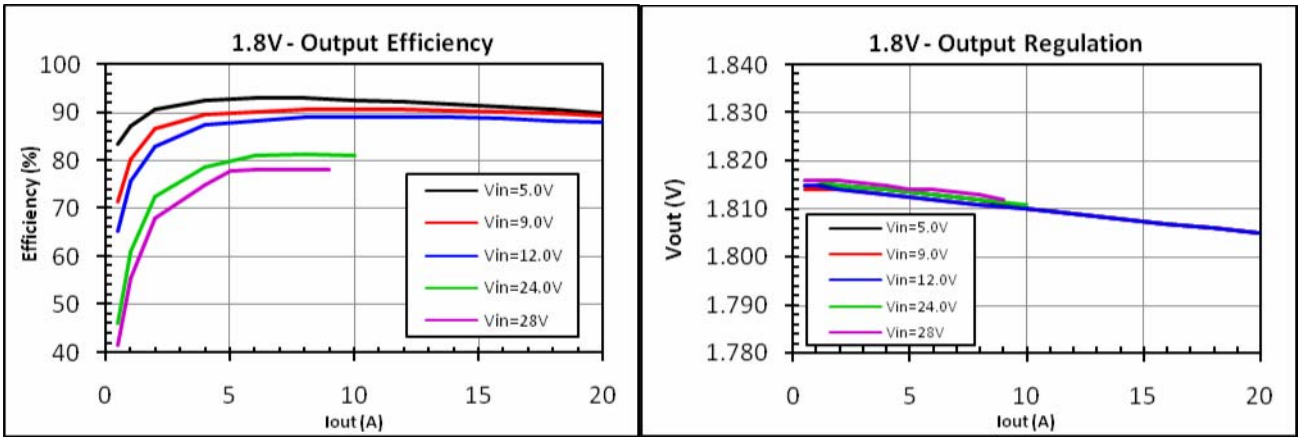
The SP6153 evaluation board was created to test and evaluate up to a 30 Amp supply. Significant copper has been used as well as multiple parallel vias to reduce copper resistance and aid in the cooling of circuit

components. This evaluation board can be ordered through our web site.

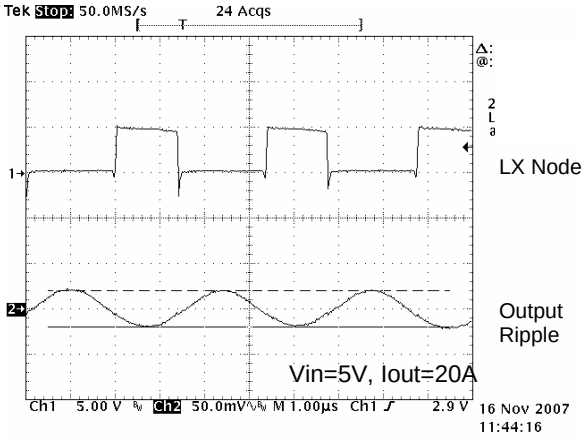
Applications Information



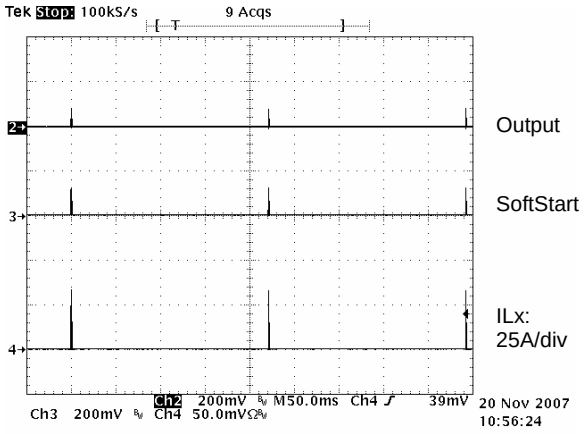
Schematic: SP6153 Configured as a 5Vin nominal to 1.8V/20 Amps DC-DC Converter.



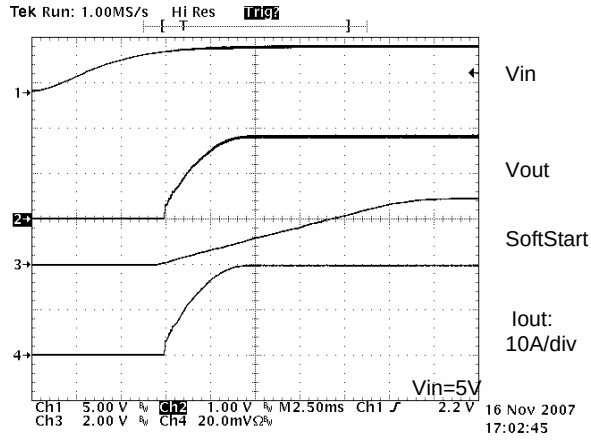
Performance Waveforms



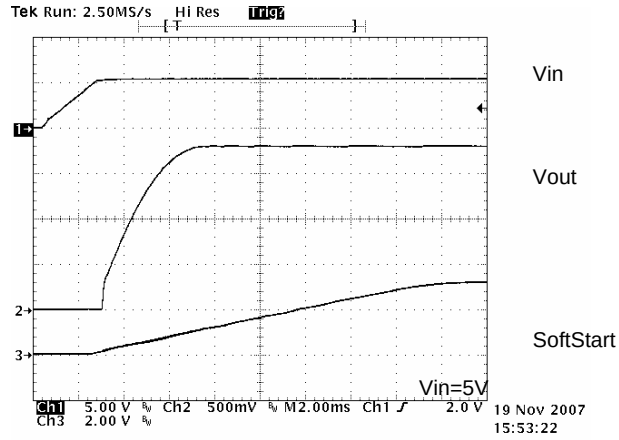
LX node & output ripple voltage



Output load Short Circuit

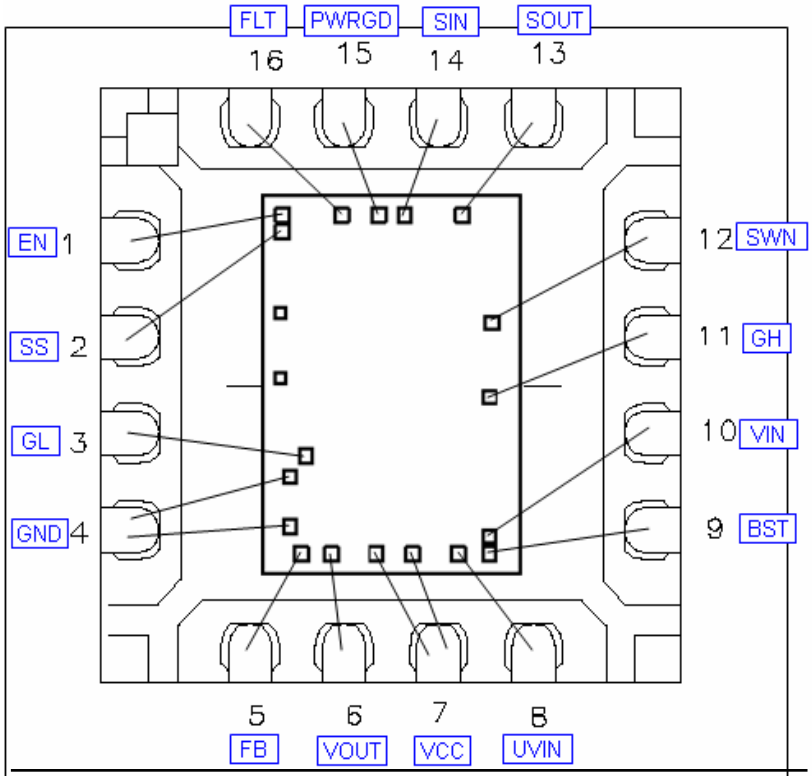


Startup into Full Load 20A



Startup into No Load

Device Bonding / Pin Out



Device information:

1. Die size: 69 X 99 MIL^2
2. On wafer step size: 70 X 100 MIL^2
3. Bond pad opening: 90 X 90 μm^2

Package: 16LD 4x4 QFN
JEDEC #: MO-220 Variation VGGC-4

BOM:

Assembly Subcon	Unisem (Option 1)	Carsem (Option 2)
DAP Size	114 X 114 MIL^2	114 X 114 MIL^2
D/A Epoxy	84-1LMISR4	QMI-519
Au Wire	1.3mil	1.3mil
Mold Comp	G770H	7730LF

Ordering Information

Part Number	Temperature Range	Package
SP6153ER1L	-40°C to +125°C	16 Pin QFN
SP6153ER1L/TR	-40°C to +125°C	16 Pin QFN

All available parts are Lead Free

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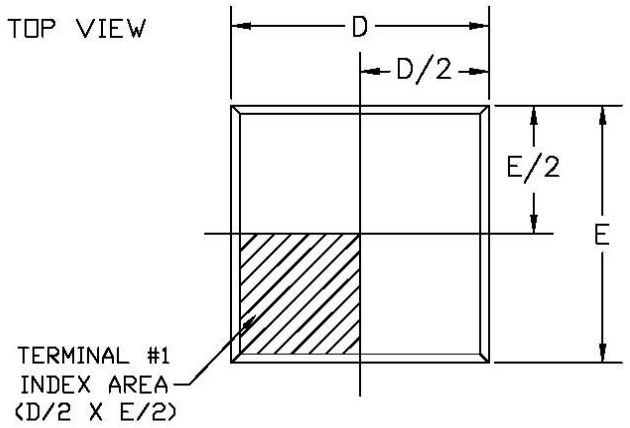
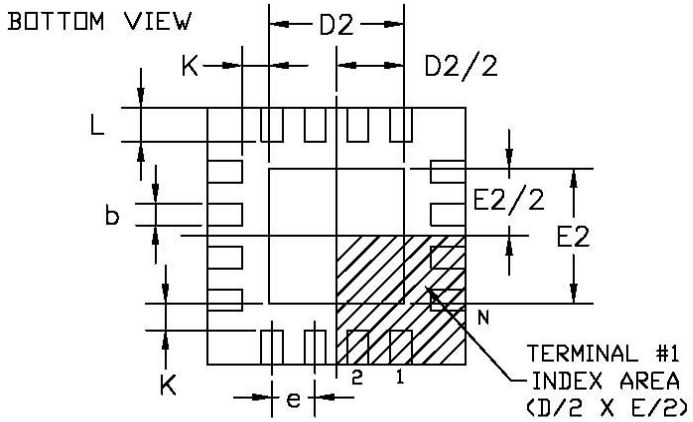
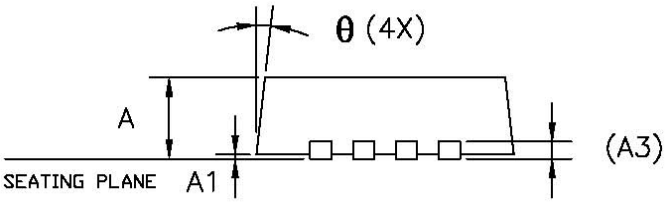
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/31/05	JL
B	MODIFY DRAWING FORMAT	07/20/06	JL







SIDE VIEW

16LD 4x4 QFN JEDEC MO-220 Variation VGGC-4

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC		
D2	2.20	2.40	2.60	0.087	0.094	0.102
E	4.00 BSC			0.157 BSC		
E2	2.20	2.40	2.60	0.087	0.094	0.102
e	0.65 BSC			0.026 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	16			16		
ND	4			4		
NE	4			4		

Solved by Sipex		SIPEX CORPORATION	
		16 PIN 4x4 QFN PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 16-PIN 4x4 QFN	
By: JL	Date: 07/20/06	Revision: B	Sheet: 1 OF 1

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