8. ELECTRICAL SPECIFICATIONS

This section contains electrical specifications and associated timing information for the TMP68010.

8.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	−0.3~+7.0	V
Input Voltage	Vin	−0.3~+7.0	V
Operating Temperature Range	T_a	0~+70	℃
Storage Temperature	Tstg	−55~+150	℃

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or Vcc).

8.2 DC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 5%, GND = 0V, Ta = 0~70℃)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	VIH	2.0	Vcc	V
Input Low Voltage	VIL	GND-0.3	0.8	V
Input Leakage Current (5.25V) $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$~$\overline{IPL2}$, $\overline{VPA}$	Iin	−	2.5	μA
Input Leakage Current (5.25V) $\overline{HALT}$, $\overline{RESET}$	Iin	−	20	μA
Three-State (Off State) Input Current (2.4V/0.4V) $\overline{AS}$, A1~A23, D0~D15, FC0~FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	ITSI	−	20	μA
Output High Voltage (IOH = −400μA) E*	VOH	Vcc-0.75	−	V
Output High Voltage (IOH = −400μA) E**, $\overline{AS}$, A1~A23, $\overline{BG}$, D0~D15, FC0~FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	VOH	2.4	−	V
Output Low Voltage (IOL = 1.6mA) $\overline{HALT}$	VOL	−	0.5	V
(IOL = 3.2mA) A1~A23, $\overline{BG}$, FC0~FC2	VOL	−	0.5	V
(IOL = 5.0mA) $\overline{RESET}$	VOL	−	0.5	V
(IOL = 5.3mA) E, $\overline{AS}$, D0~D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	VOL	−	0.5	V
Power Dissipation***	PD	−	1.50	W
Capacitance (V_{in} = 0V, T_a = 25℃ : Frequency = 1MHz)****	Cin	−	20.0	pF

8.3 AC ELECTRICAL SPECIFICATIONS-CLOCK TIMING (See Figure 8.1)

Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f	4.0	8.0	4.0	10.0	4.0	12.5	MHz
Cycle Time	tcyc	125	250	100	250	80	250	ns
Clock Pulse Width	tCL tCH	55 55	125 125	45 45	125 125	35 35	125 125	ns
Rise and Fall Times	tCr tCf	— —	10 10	— —	10 10	— —	5 5	ns

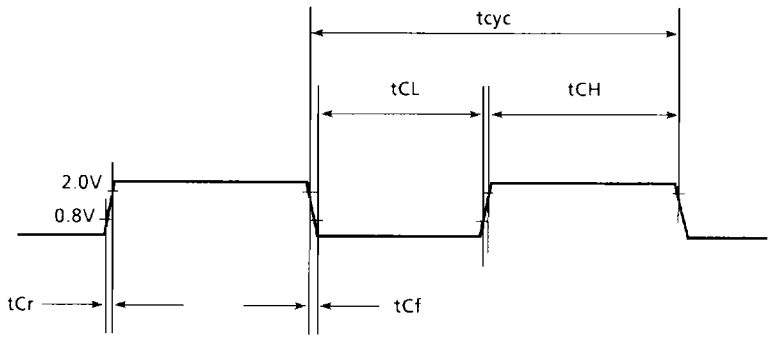


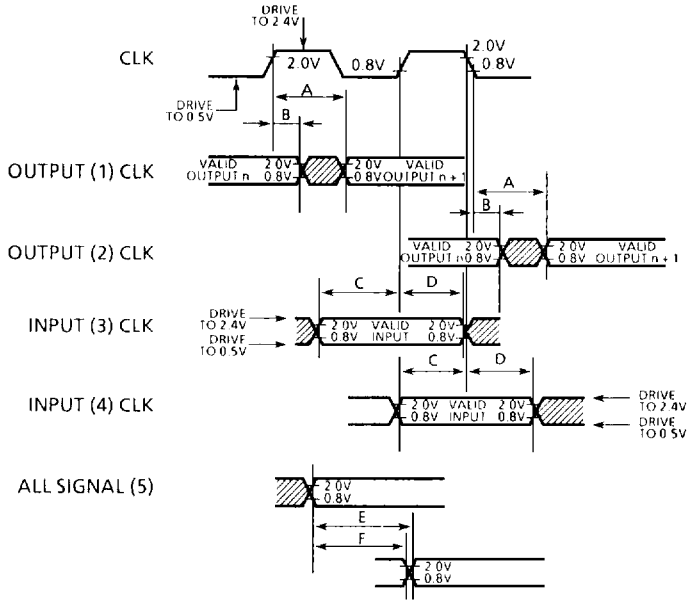
Figure 8.1 Clock Input Timing Diagram

8.4 AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clolk and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 8.2. In order to test the parameters guaranteed by TOSHIBA, inputs must be driven to the voltage levels specified in this figure. Outputs are specified with minimum and / or maximum limits, as appropriate, and are measured as shown in Figure 8.2. Inputs are specified with minimum setup and hold times, and are measured as shown. Finaly, the measurement for signal-to-signal specifications are also shown.

Note : The testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical character-istics.



Notes :

1 This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2 This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3 This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4 This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5 This timing is applicable to all parameters specified relative to the assertion / negation of another signal.

Legend :

A Maximum output delay specification.
B Minimum output hold time.
C Minimum input setup time specification.
D Minimum input hold time specification.
E Signal valid to signal valid specification (maximum or minimum).
F Signal valid to signal invalid specification (maximum to minimum).

Figure 8.2 Drive Levels and Test Points for AC Specifications

8.5 AC ELECTRICAL SPECIFICATIONS-READ AND WRITE CYCLES (1/4)

(Vcc = 5.0V ± 5%, GND = 0V, Ta = 0~70℃ ; see Figures 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	125	250	100	250	80	250	ns
2	Clock Width Low	t_{CL}	55	125	45	125	35	125	ns
3	Clock Width High	t_{CH}	55	125	45	125	35	125	ns
4	Clock Fall Time	t_{Cf}	—	10	—	10	—	5	ns
5	Clock Rise Time	t_{Cr}	—	10	—	10	—	5	ns
6	Clock Low to Address Valid	t_{CLAV}	—	62	—	50	—	50	ns
6A	Clock High to FC Valid	t_{CHFCV}	—	62	—	50	—	45	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	—	60	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low	t_{CHSL}	3	60	3	50	3	40	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Low (Read) / $\overline{AS}$ Low (Write)	t_{AVSL}	30	—	20	—	15	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Low (Read) / $\overline{AS}$ Low (Write)	t_{FCVSL}	90	—	70	—	60	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	—	62	—	50	—	40	ns
13[2]	$\overline{AS}$, $\overline{DS}$ HIGH to Address / $\overline{FC}$ Invalid	t_{SHAFI}	40	—	30	—	20	—	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (Read) / $\overline{AS}$ Low (Write)	t_{SL}	270	—	195	—	160	—	ns
14A[2]	$\overline{DS}$ Width Low (Write)	t_{DSL}	140	—	95	—	80	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	150	—	105	—	65	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	—	60	ns
17[2]	$\overline{AS}$, DS High to R / W High (Read)	t_{SHRH}	40	—	30	—	20	—	ns

8.5 AC ELECTRICAL SPECIFICATIONS - READ AND WRITE CYCLES (2/4)

(Vcc = 5.0V ± 5%, GND = 0V, Ta = 0~70°C ; see Figures 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
18[1]	Clock High to R / $\overline{W}$ High	t_{CHRH}	0	55	0	45	0	40	ns
20[1]	Clock High to R / $\overline{W}$ Low	t_{CHRL}	0	55	0	45	0	40	ns
20A[2,6]	$\overline{AS}$ Low to R / $\overline{W}$ Valid (Write)	t_{ASRV}	–	10	–	10	–	10	ns
21[2]	Address Valid to R / $\overline{W}$ Low (Write)	t_{AVRL}	20	–	0	–	0	–	ns
21A[2]	FC Valid to R / $\overline{W}$ Low (Write)	t_{FCVRL}	60	–	50	–	30	–	ns
22[2]	R / $\overline{W}$ Low to $\overline{DS}$ Low (Write)	t_{RLSL}	80	–	50	–	30	–	ns
23	Clock Low to Data Out Valid (Write)	t_{CLDO}	–	62	–	50	–	50	ns
25[2]	$\overline{AS}$, $\overline{DS}$ High to Data Out Invalid (Write)	t_{SHDOI}	40	–	30	–	20	–	ns
26[2]	Data Out Valid to DS Low (Write)	t_{DOSL}	40	–	30	–	20	–	ns
27[5]	Data in to Clock Low (Setup Time on Read)	t_{DICL}	10	–	10	–	10	–	ns
27A[5]	Late $\overline{BERR}$ Low to Clock Low (Setup Time)	t_{BELCL}	45	–	45	–	45	–	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	240	0	190	0	150	ns
29	$\overline{AS}$, $\overline{DS}$ High to Data In Invalid (Hold Time on Read)	t_{SHDII}	0	–	0	–	0	–	ns
29A	$\overline{AS}$, $\overline{DS}$ Negated to Data In High Impedance	t_{SHDZ}	–	187	–	150	–	120	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	–	0	–	0	–	ns
31[2,5]	$\overline{DTACK}$ Low to Data In (Setup Time)	t_{DALDI}	–	90	–	65	–	50	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr, f}$	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	–	62	–	50	–	40	ns
34	Clock High to BG High	t_{CHGH}	–	62	–	50	–	40	ns
35	$\overline{BR}$ Low to BG Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	Clk Per

8.5 AC ELECTRICAL SPECIFICATIONS-READ AND WRITE CYCLES (3/4)

(Vcc = 5.0V ± 5%, GND = 0V, Ta = 0~70°C ; see Figures 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
36[7]	$\overline{BR}$ High to $\overline{BG}$ High	tBRHGH	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per
37	BGACK Low to $\overline{BG}$ High	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per
37A[8]	$\overline{BGACK}$ Low to $\overline{BR}$ High	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	ns
38	$\overline{BG}$ Low to Control, Address, Data Bus High Impedance ($\overline{AS}$ High)	tGLZ	—	80	—	70	—	60	ns
39	$\overline{BG}$ Width High	tGH	1.5	—	1.5	—	1.5	—	Clk. Per
40	Clock Low to $\overline{VMA}$ Low	tCLVML	—	70	—	70	—	70	ns
41	Clock Low to E Transition	tCLET	—	55	—	45	—	35	ns
42	E Output Rise and Fall Time	tEr, f	—	15	—	15	—	15	ns
43	$\overline{VMA}$ Low to E High	tVMLEH	200	—	150	—	90	—	ns
44	$\overline{AS}$, $\overline{DS}$ High to VPA High	tSHVPH	0	120	0	90	0	70	ns
45	E Low to Control Address Bus Invalid (Address Hold Time)	tELCAI	30	—	10	—	10	—	ns
46	BGACK Width	tGAL	1.5	—	1.5	—	1.5	—	Clk. Per
47[5]	Asynchronous Input Setup Time	tASI	10	—	10	—	10	—	ns
48[2,3,5]	$\overline{DTACK}$ Low to $\overline{BERR}$ Low	tDALBEL	—	80	—	55	—	35	ns
49[9]	$\overline{AS}$, $\overline{DS}$ High to E Low	tSHEL	−70	70	−55	55	−45	45	ns
50	E Width High	tEH	450	—	350	—	280	—	ns
51	E Width Low	tEL	700	—	550	—	440	—	ns
53	Clock High to Data Out Invalid	tCHDOI	0	—	0	—	0	—	ns
54	E Low to Data Out Invalid	tELDOI	30	—	20	—	15	—	ns
55	R / W to Data Bus Driven	tRLDBD	30	—	20	—	10	—	ns
56[4]	$\overline{HALT}$ / $\overline{RESET}$ Pulse Width	tHRPW	10	—	10	—	10	—	Clk. Per

8.5 AC ELECTRICAL SPECIFICATIONS-READ AND WRITE CYCLES (4/4)

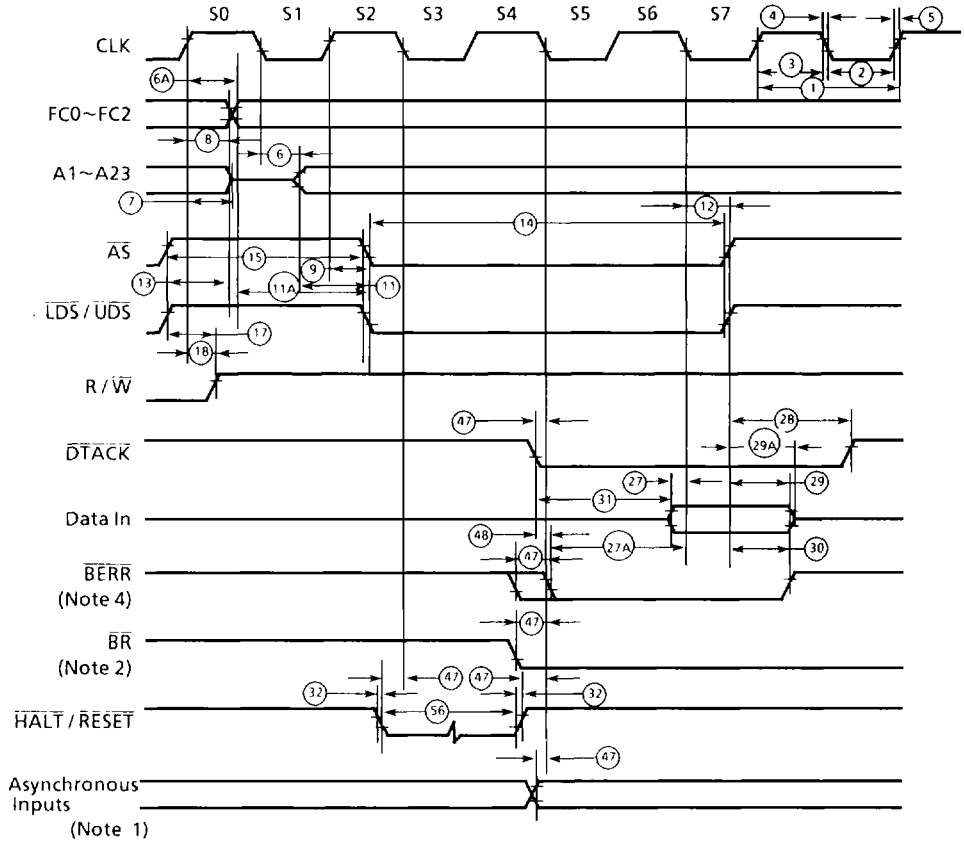
(Vcc = 5.0V ± 5%, GND = 0V, Ta = 0~70°C ; see Figures 8.3 and 8.4)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
57	$\overline{BGACK}$ High to Control Bus Driven	tGABD	1.5	–	1.5	–	1.5	–	Clk. Per
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	tGAFD	1	–	1	–	1	–	Clks
58[7]	$\overline{BG}$ High to Control Bus Driven	tGHBD	1.5	–	1.5	–	1.5	–	Clk. Per
58A[7]	BR Negated to FC, $\overline{VMA}$ Driven	tRHFD	1	–	1	–	1	–	Clks

Notes :

1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.
2. Actual value depends on clock period.
3. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47)
4. For power up, the MPU must be held in $\overline{RESET}$ state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the system.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{DTACK}$-low to data setup time (#31) and $\overline{DTACK}$-low to $\overline{BERR}$-low setup time (#48) requirements can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) for the following clock cycle, $\overline{BERR}$ must only satisfy the late-$\overline{BERR}$-low to clock-low setup time (#27A) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 10 nanoseconds from the values in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

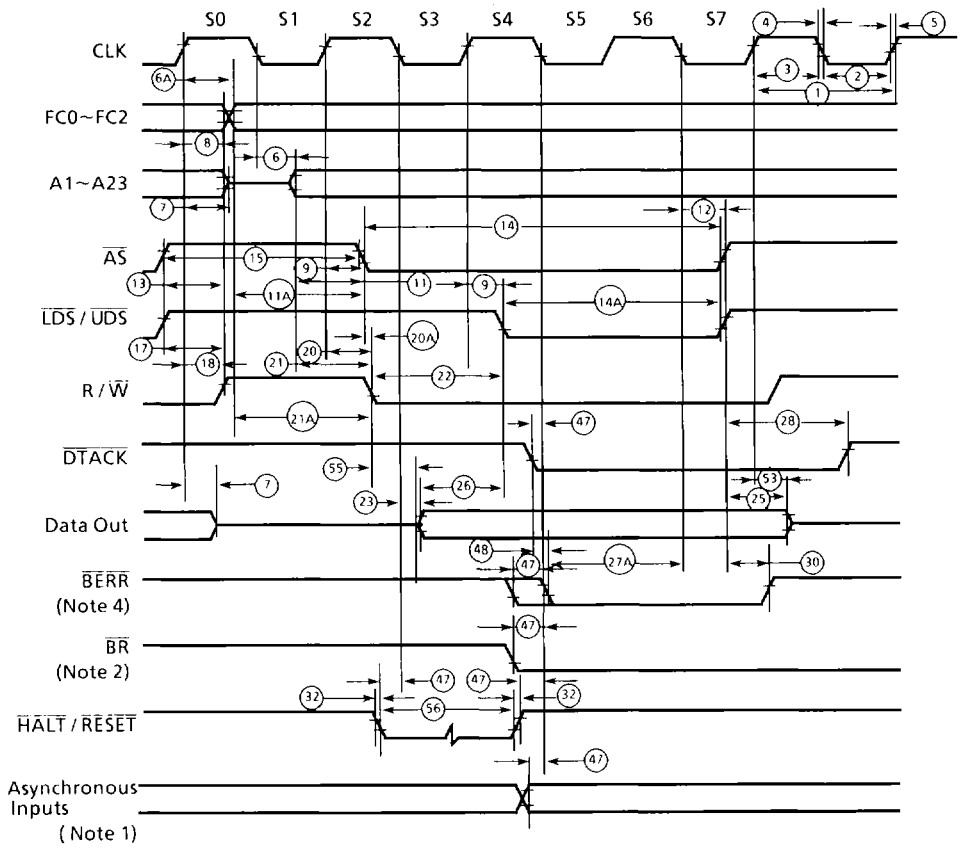


Notes:

1. Setup time for the asynchronous inputs $\overline{IPL0/2}$, $\overline{IPL1}$, and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only in order to insure being recognized at the end of this bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.
4. The timing for the first falling edge (47) of $\overline{BERR}$ are for $\overline{BERR}$ without $\overline{DTACK}$,the timings for the second falling edge (27A and 48) are for $\overline{BERR}$ with $\overline{DTACK}$.

Figure 8.3 Read Cycle Timing Diagram

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Notes :

1. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts,unless otherwise noted.
2. Because of loading variations, R / $\overline{W}$ may valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (Specification 20A).
3. The timing for the first falling edge (47) of $\overline{BERR}$ are for $\overline{BERR}$ without $\overline{DTACK}$; the timings for the second falling edge (27A and 48) are for $\overline{BERR}$ with $\overline{DTACK}$.

Figure 8.4 Write Cycle Timing Diagram

8.6 AC ELECTRICAL SPECIFICATIONS-TMP68010 TO 6800 PERIPHERAL

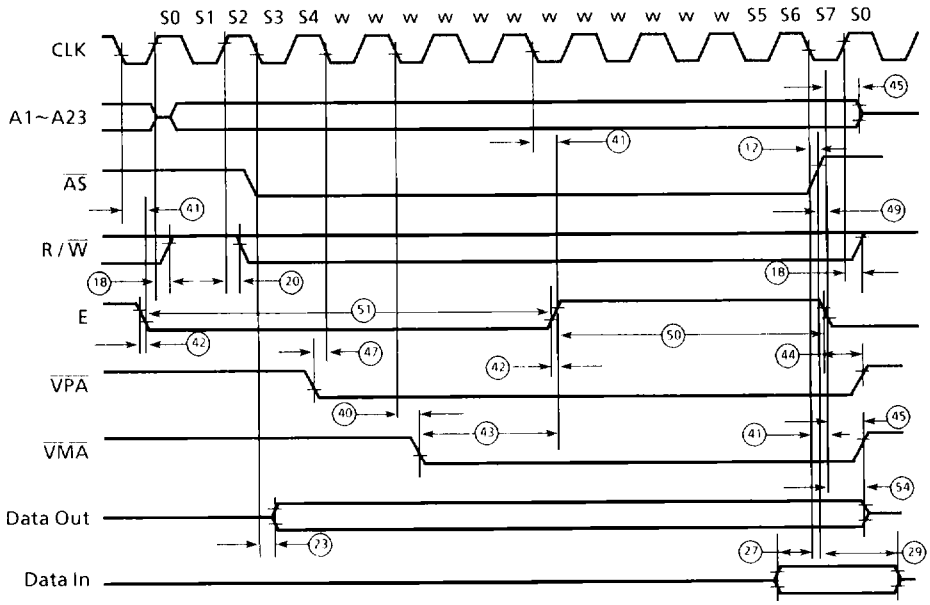
(Vcc = 5.0V ± 5% , GND = 0V , T_a = 0~70°C ; see Figures 8.5 and 8.6)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
12[1]	Clock Low to $\overline{AS}$, DS High	tCLSH	—	62	—	50	—	40	ns
18[1]	Clock High to R / W High (Read)	tCHRH	0	55	0	45	0	40	ns
20[1]	Clock High to R / W Low	tCHRL	0	55	0	45	0	40	ns
23	Clock Low to Data Out Valid (Write)	tCLDO	—	62	—	50	—	50	ns
27	Data in to Clock Low (Setup Time on Read)	tDICL	10	—	10	—	10	—	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	tSHDII	0	—	0	—	0	—	ns
40	Clock Low to $\overline{VMA}$ Low	tCLVML	—	70	—	70	—	70	ns
41	Clock Low to E Transition	tCLET	—	55	—	45	—	35	ns
42	E Output Rise and Fall Time	tEr, f	—	15	—	15	—	15	ns
43	$\overline{VMA}$ Low to E High	tVMLEH	200	—	150	—	90	—	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	tSHVPH	0	120	0	90	0	70	ns
45	E Low to Control Address Bus (Address Hold Time)	tELCAI	30	—	10	—	10	—	ns
47	Asynchronous Input Setup Time	tASI	10	—	10	—	10	—	ns
49[2]	$\overline{AS}$, DS High to E Low	tSHEL	- 70	70	- 55	55	- 45	45	ns
50	E Width High	tEH	450	—	350	—	280	—	ns
51	E Width Low	tEL	700	—	550	—	440	—	ns
54	E Low to Data Out Invalid	tELDOI	30	—	20	—	15	—	ns

Notes :

1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.
2. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.

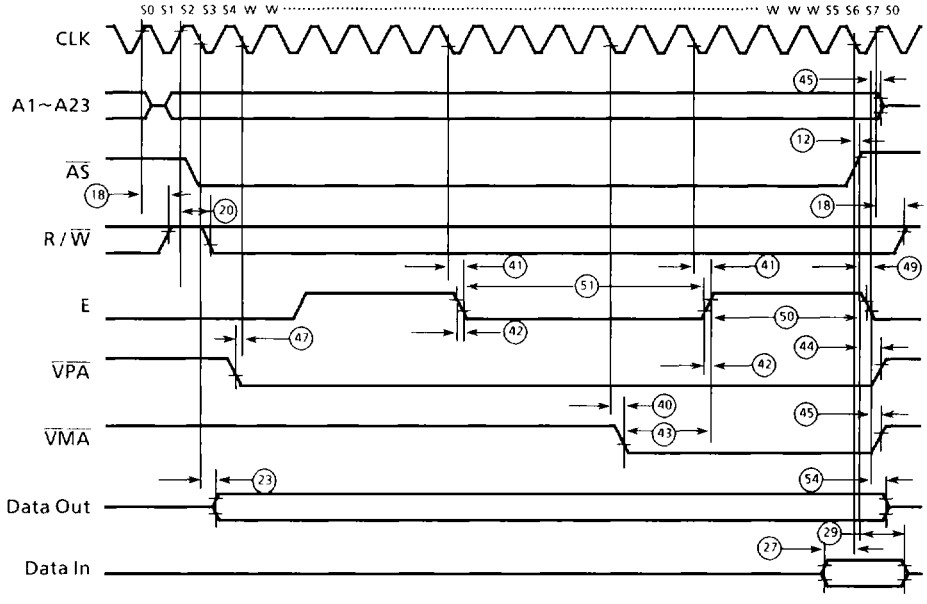
These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note : The timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$ it shows the best case possibly attainable

Figure 8.5 TMP68010 to 6800 Peripheral Timing Diagram – Best Case

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



Note : This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the worst case possibly attainable.

Figure 8.6 TMP68010 to 6800 Peripheral Timing Diagram - Worst Case

8.7 AC ELECTRICAL SPECIFICATIONS-BUS ARBITRATION

(Vcc = 5.0V ± 5% ; GND = 0V ; T_a = 0~70°C ; See Figures 8.7, 8.8 and 8.9)

Num.	Characteristic	Symbol	8MHz		10MHz		12.5MHz		Unit
			Min	Max	Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	tCHADZ	–	80	–	70	–	60	ns
16	Clock High to Control Bus High Impedance	tCHCZ	–	80	–	70	–	60	ns
33	Clock High to $\overline{BG}$ Low	tCHGL	–	62	–	50	–	40	ns
34	Clock High to $\overline{BG}$ High	tCHGH	–	62	–	50	–	40	ns
35	$\overline{BR}$ Low to BG Low	tBRLGL	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per
36[1]	$\overline{BR}$ High to $\overline{BG}$ High	tBRHGH	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	tGALGH	1.5	3.5	1.5	3.5	1.5	3.5	Clk. Per
37A[2]	$\overline{BGACK}$ Low to $\overline{BR}$ High	tGALBRH	20	1.5 Clocks	20	1.5 Clocks	20	1.5 Clocks	ns
38	$\overline{BG}$ Low to Control, Address, Data Bus High Impedance ($\overline{AS}$ High)	tGLZ	–	80	–	70	–	60	ns
39	$\overline{BG}$ Width High	tGH	1.5	–	1.5	–	1.5	–	Clk. Per
46	$\overline{BGACK}$ Width	tGAL	1.5	–	1.5	–	1.5	–	Clk. Per
47	Asynchronous Input Setup Time	tASI	10	–	10	–	10	–	ns
57[2]	$\overline{BGACK}$ High to Control Bus Driven	tGABD	1.5	–	1.5	–	1.5	–	Clk. Per
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	tGAFD	1	–	1	–	1	–	Clk. Per
58[1]	$\overline{BG}$ High to Control Bus Driven	tGHBD	1.5	–	1.5	–	1.5	–	Clk. Per
58A[1]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	tRHFD	1	–	1	–	1	–	Clk. Per

Notes :
1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
2. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

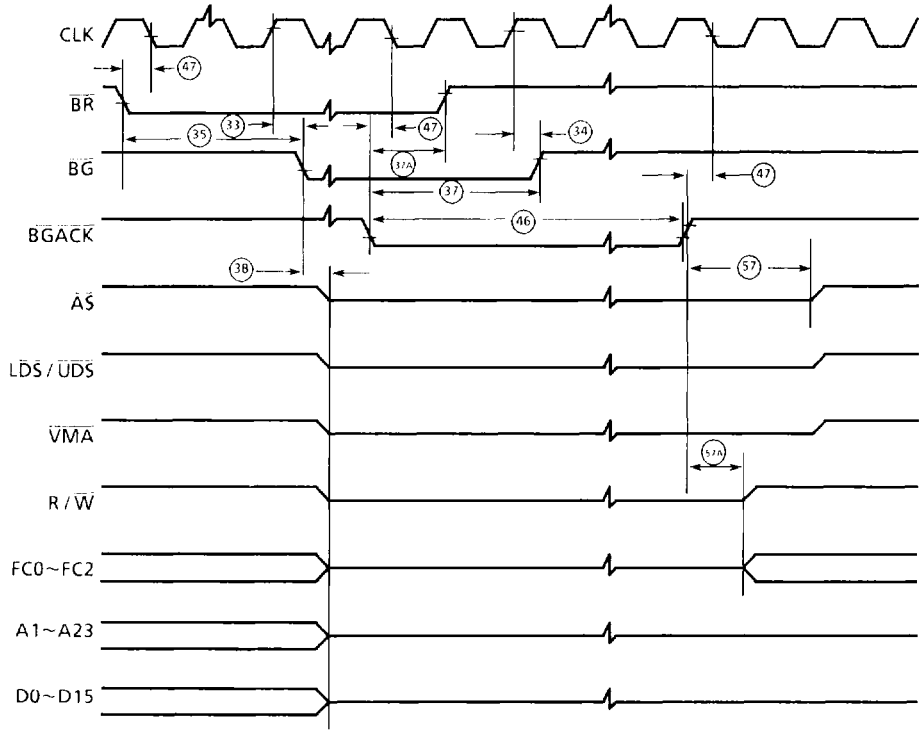


Figure 8.7 Bus Arbitration Timing – Idle Bus Case

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

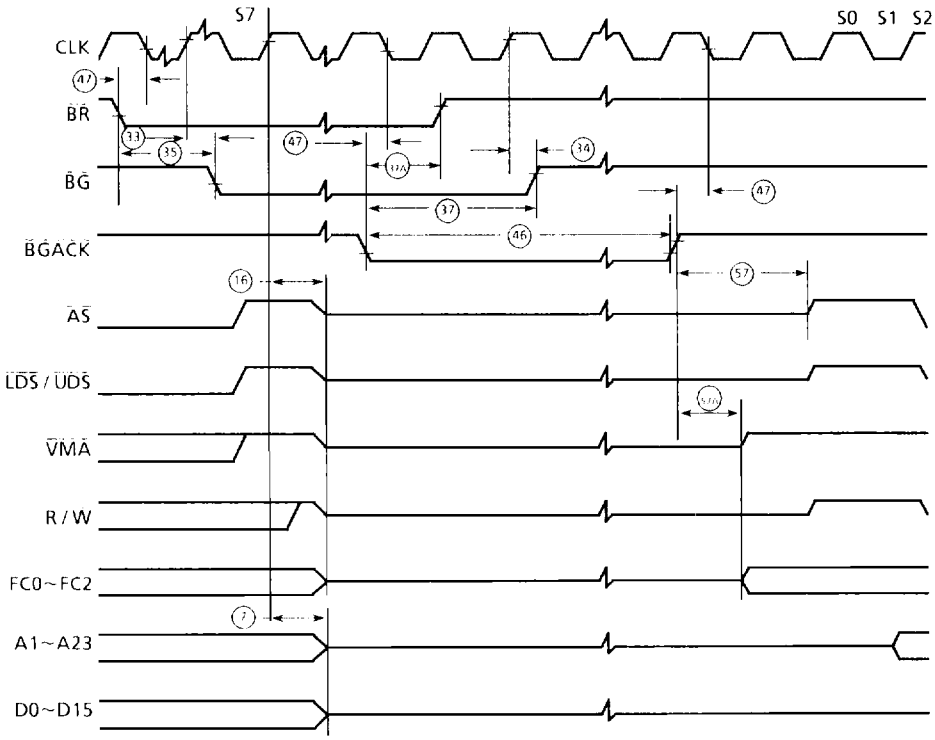


Figure 8.8 Bus Arbitration Timing - Active Bus Case

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

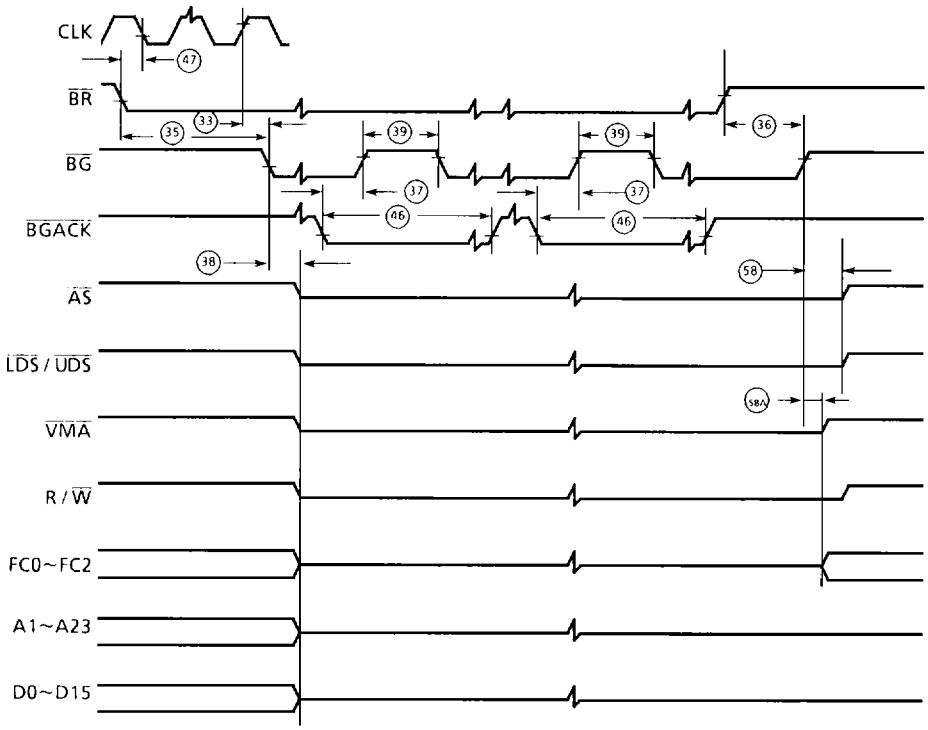


Figure 8.9 Bus Arbitration Timing - Multiple Bus Requests