Data Sheet

2.5 Gbits/sec 4-Bit Multiplexer/ Demultiplexer Chipset

Features

- Serial Data Rates up to 2.5 Gb/s
- Parallel Data Rates up to 625 Mb/s
- ECL 100K Compatible Parallel Data I/Os
- Divide-by-4 Clock for Synchronization of Parallel Data to Interfacing Chips
- SKIP Input on Demux for Realignment of Output Word Boundaries
- Differential or Single-Ended Inputs and Outputs
- Low Power Dissipation: 1.5 W (Typ. Per Chip)
- Standard ECL Power Supply: VEE = -5.2 V
- Available in Commercial (0° to +70°C) or Industrial (-40° to +85°C) Temperature Ranges
- Proven E/D Mode GaAs Technology
- 28-pin Leaded Ceramic Chip Carrier

Functional Description

The VS8004 and VS8005 are data conversion devices capable of serial data rates up to 2.5 Gb/s, transforming 4-bit wide parallel data to serial data and serial data to 4-bit wide parallel data.

The VS8004/VS8005 are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 28-pin leaded chip carrier.

VS8004

The VS8004 is a high speed 4 bit parallel to serial data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The parallel inputs [D(0:3), ND(0:3)] accept data at rates up to 625 Mb/s. The differential serial data output (SDATA, NSDATA) presents the data sequentially from the parallel data inputs at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input (CLK, NCLK). An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output (CLK4, NCLK4). This clock signal is provided so that incoming parallel signals can be synchronized to arrive at the input data registers simultaneously. An internal bias network is provided at all inputs to simplify capacitive coupling.

VS8005

The VS8005 is a high speed 4-bit serial to parallel data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The differential serial data inputs (SDATA, NSDATA) accept data at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input (CLK, NCLK). The parallel outputs [D(0:3), ND(0:3)] present the data sequentially at rates up to 625 Mb/s. An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output (CLK4, NCLK4) which is synchronous with the parallel data outputs. A control input (SKIP, NSKIP) is provided to allow realignment of the output parallel word boundaries.

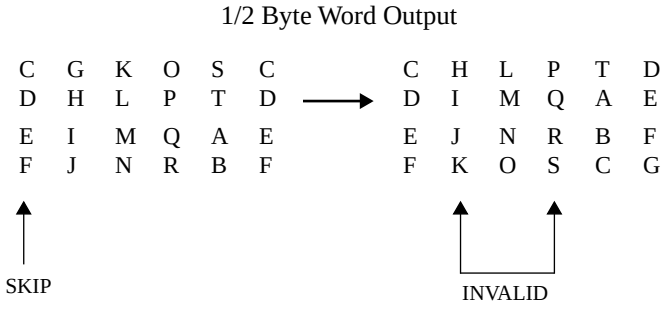
SKIP Signal

The SKIP signal is provided to allow realignment of the output parallel 4-bit word boundaries. Within the current CLK4, the rising edge of a SKIP causes an internal circuit in the VS8005 to hold the current 4-bit word output and drop the fifth output bit. The sixth output bit will become the MSB of the next 4-bit word output; and

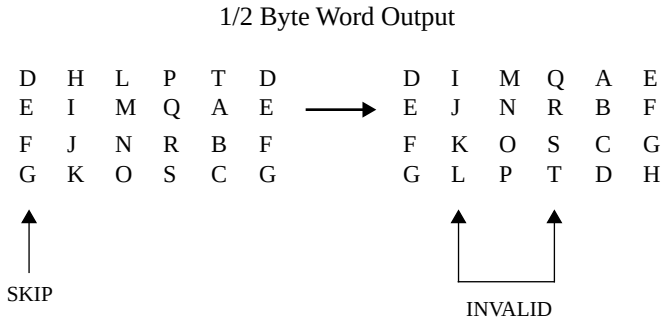
the falling edge of SKIP makes the next three parallel output words invalid (which is equal to three CLK4 or twelve CLK). After that the outputs will be valid and will have the MSB of the output realigned by one bit.

For Example, the user finds that the word boundary of the output is off by two bits, then he needs to perform two SKIPs. He needs to issue one SKIP, wait for three CLK4 cycles until the output is valid, then issue another SKIP, wait for another three CLK4 cycles. Then the outputs will have the bit positions in the right place as demonstrated in the following:

Misaligned by 2 bits:



Misaligned by 1 bit:



Realignment Done.

Applications

- High Speed Instrumentation and Test Equipment
- Fiber-optic Communication
- Local Area Networks
- Serialization of Computer Backplanes
- Computer to Computer Interfaces
- Serial Control Buses for Aerospace Environments

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Figure 1: VS8004 Block Diagram

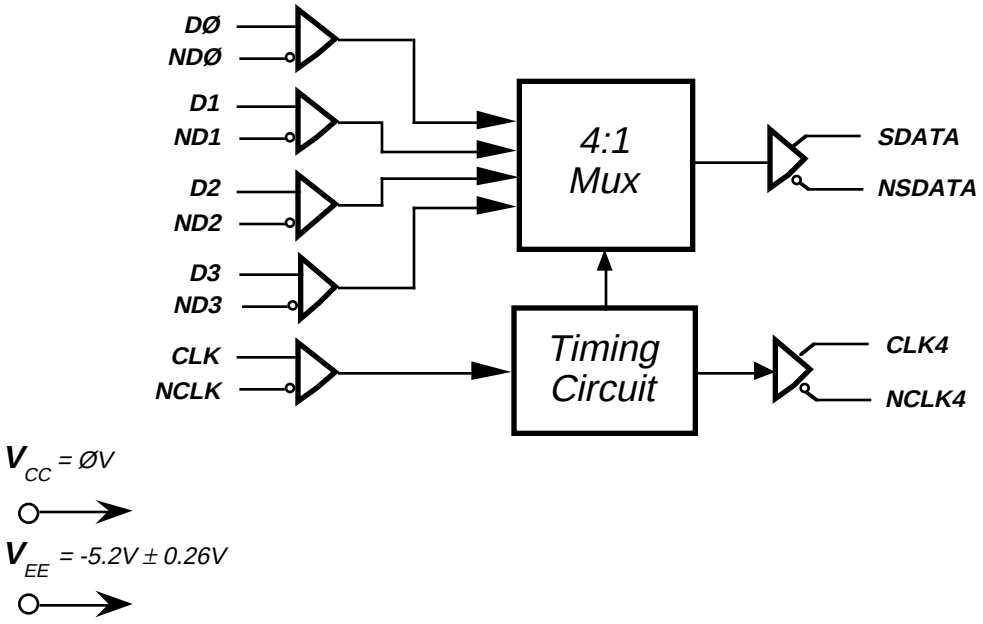
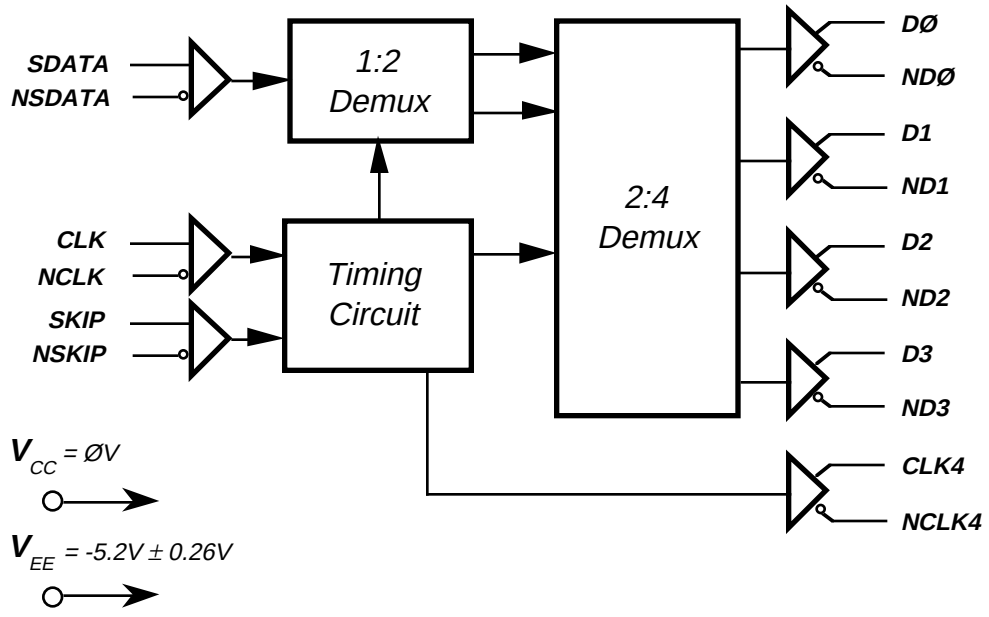


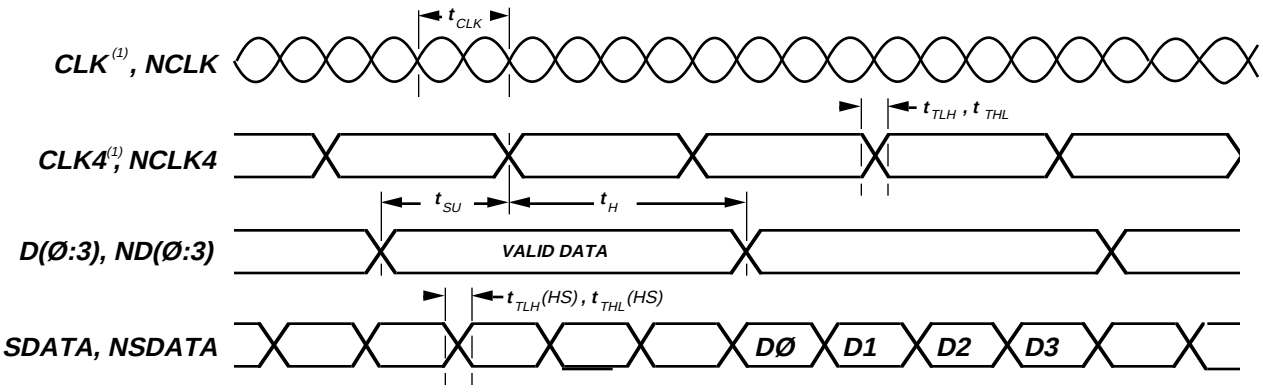
Figure 2: VS8005 Block Diagram



VS8004 AC Characteristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	High Speed clock period	400	-	-	ps
t_{SU}	D(∅:3), ND(∅:3), set-up time with respect to CLK4, NCLK4	900	-	-	ps
t_H	D(∅:3), ND(∅:3), hold time with respect to CLK4, NCLK4	-300	-	-	ps
t_{TLH}(HS), t_{THL}(HS)	SDATA, NSDATA transition time (LO to HI, HI to LO) while driving 50Ω to -2.0V	-	150	-	ps
jitter(RMS)	CLK, NCLK to SDATA, NSDATA (max-min), (HI to LO), same part, same pin at constant conditions	-	<50	-	ps
t_{TLH},t_{THL}	ECL output transition time (LO to HI, HI to LO) while driving 50Ω (CLK4, NCLK4, D(0:3), ND(0:3)) to -2.0V	-	500	-	ps

Figure 3: VS8004 Waveforms

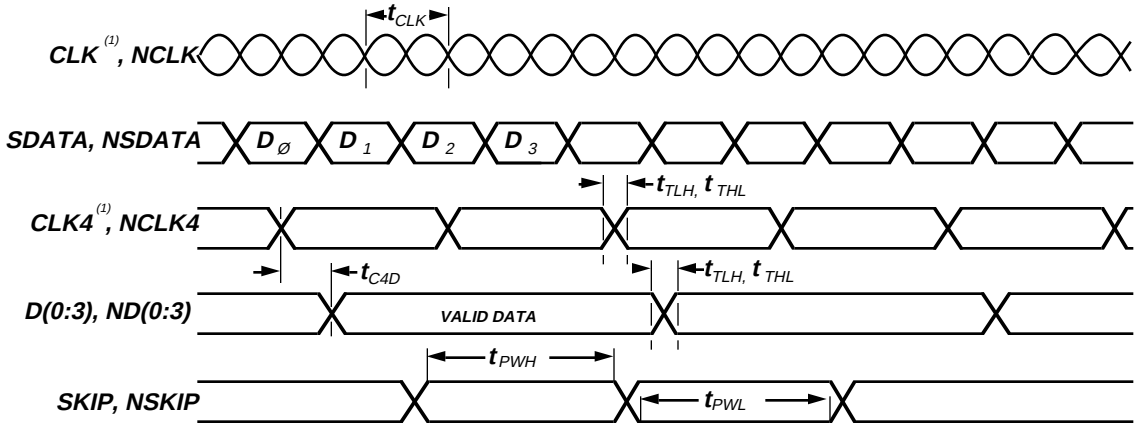


(1) Negative edge is active edge

VS8005 AC Characteristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units
t_{CLK}	High Speed clock period (CLK, NCLK)	400	-	-	ps
t_{CAD}	CLK4, NCLK4 to D(0:3), ND(0:3)	-	400	-	ps
t_{PWH}	SKIP, NSKIP pulse with (HIGH)	2	-	-	ns
t_{PWL}	SKIP, NSKIP pulse with (LOW)	2	-	-	ns
t_{TLH},t_{THL}	ECL output transition time (LOW to HIGH & HIGH to LOW) for D(0:3), ND(0:3) and CLK4, NCLK4 (Driving 50Ω)	-	500	-	ps
Phase Margin	SDATA, NSDATA phase timing margin with respect to CLK, NCLK input: *Phase Margin* = $\left(1 - \frac{t_{SU} + t_H}{t_C}\right)360°$ where t_c is minimum clock cycle.	135	-	-	degrees

Figure 4: VS8005 Waveforms



(1) Rising edge causes serial data to be latched.

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{EE}) ..... V_{CC} (GND) to -6.0V
ECL Input Voltage Applied (2) (V_{ECLIN}) .....-2.5V to + 0.5V
High Speed Input Voltage Applied (2) (V_{HSIN}).....V_{EE} -0.7V to V_{CC} + 0.7V
Output Current (output HIGH) (I_{OUT}).....-50 mA
Maximum Junction Temperature (T_J).....150°C
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage, but are stress ratings only. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{EE} must be applied before any input signal voltage (V_{ECLIN}).

Recommended Operating Conditions

Power Supply Voltage (V_{EE}) .....-5.2V ± 0.26V
Operating Temperature Range* (T).....(Commercial) 0° to 70°C, (Industrial) -40° to + 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

DC Characteristics

Table 1: ECL Inputs and Outputs

(Over recommended operating conditions with internal V_{REF}, V_{CC} = GND, Output load = 50 ohms to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	-	-1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1040	-	-600	mV	Guaranteed HIGH signal for ECL inputs
V_{IL}	Input LOW voltage	-2000	-	-1600	mV	Guaranteed LOW signal for ECL inputs
I_{IH}	Input HIGH Current	-	500	1000	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW Current	-1000	-500	-	µA	$V_{IN} = V_{IL}$ (min)

Note: 1) Differential ECL output pairs must be terminated identically.
2) Leakage currents exceed ECL specifications due to the internal bias network which is connected to all inputs

Table 2: Power Dissipation

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	Description	VS8004 (Min)	VS8004 (Typ)	VS8004 (Max)	VS8005 (Min)	VS8005 (Typ)	VS8005 (Max)	Units
I_{EE}	Power supply current from V_{EE}	-	270	350	-	310	400	mA
P_D	Power dissipation		1.5	1.9	-	1.6	2.2	W

Table 3: High Speed Inputs

(Over recommended operating conditions, V_{CC} = GND, Output load = 50 Ω to -2.0V)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal
ΔV_{IN}	Input voltage swing	0.8	1.0	1.2	V	AC Coupled

Notes: 1) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.
2) A reference generator is built in to each high speed input, and these inputs are intended to be AC coupled.
3) If a high speed input is used single-ended, a 150 pF capacitor must be connected between the unused high speed or complement input and the power supply (V_{TT}).

Table 4: High Speed Outputs

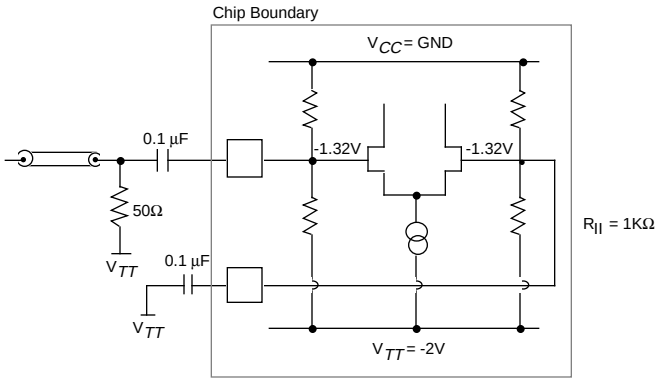
(Over recommended operating conditions, V_{CC} = GND, Output load = 50 Ω to -2.0V)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-	-0.9	-	V	Terminated to -2.0V through 50Ω
V_{OL}	Output LOW voltage	-	-1.8	-	V	Terminated to -2.0V through 50Ω
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output Load, 50Ω to -2V

Notes: 1) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling

Parallel Data, CLK, NCLK, SKIP, NSKIP Inputs

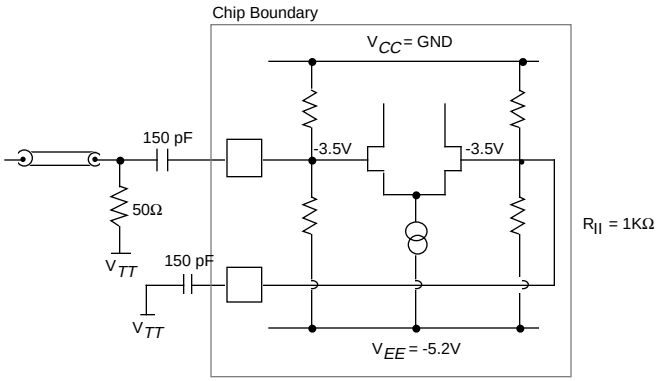
ECL inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -1.32 Volts on both the true and complement inputs.



High Speed Inputs

High speed inputs (clock or data) provide for AC coupled operation. Internal biasing will position the reference voltage of approximately -3.5 Volts on both the true and complementary inputs. Single-ended, AC coupled operation is illustrated below

.



$V_{TT} = V_{CC} - 2V$

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Figure 5: VS8004 Pin Diagram

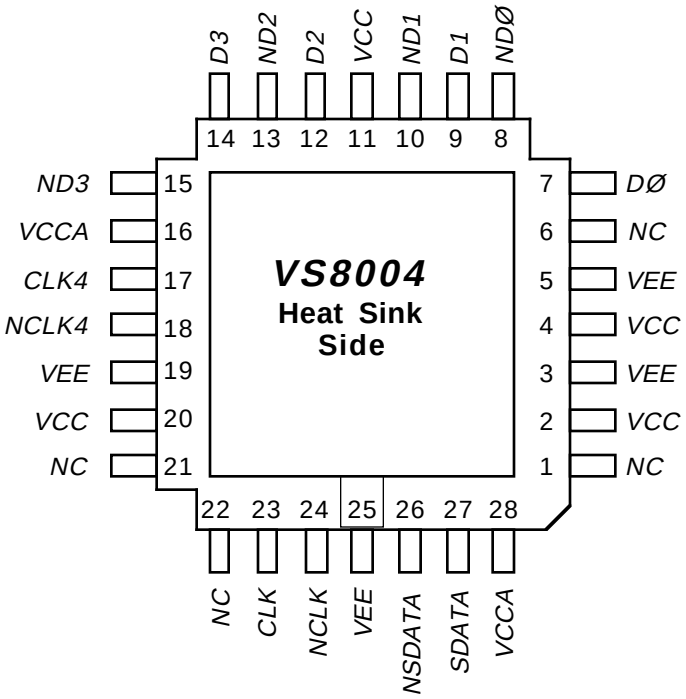


Table 5: VS8004 Pin Description

Pin #	*Name*	*I/O*	*Description*
23, 24	CLK, NCLK	I	Differential high speed clock inputs
27, 26	SDATA, NSDATA	O	Differential high speed serial data outputs
17, 18	CLK4, NCLK4	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	D(∅:3), ND(∅:3)	I	Differential parallel data inputs (ECL)
3, 5, 19, 25[(1)]	V_{EE}		-5.2V supply voltage
2, 4, 11, 20	V_{CC}		∅ V ground connection
16, 28	V_{CCA}		∅ V output ground connection (Normally connected to V_{CC})
1, 6, 21, 22	NC		No connection

Notes: 1) The heat sink is connected V_{EE} (pin 25). To prevent a short circuit between $V_{CC,}$ V_{CCA} (∅ V normally) and V_{EE} (-5.2V normally), do not connect this heat sink to ground. (∅V).

Figure 6: VS8005 Pin Diagram

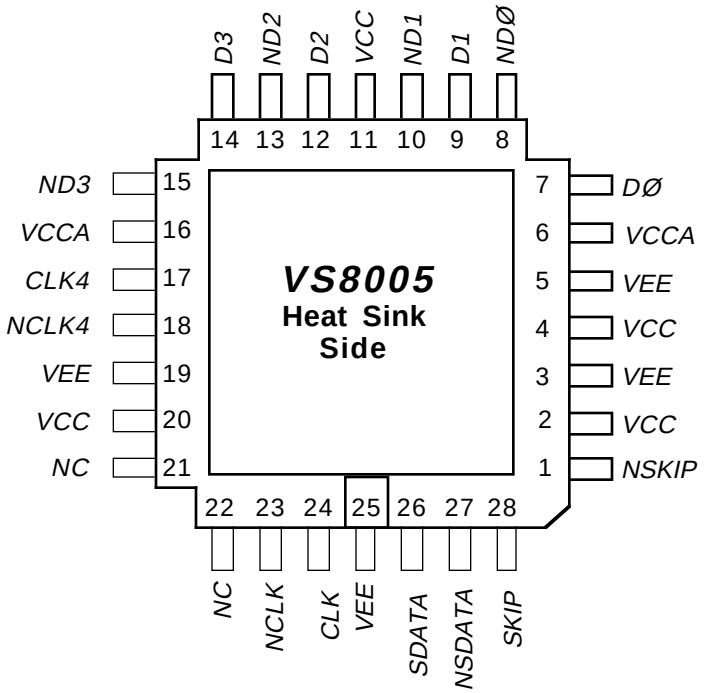


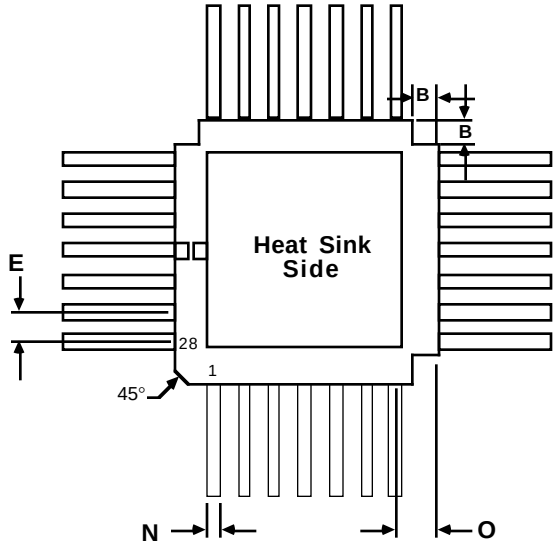
Table 6: VS8005 Pin Description

Pin #	*Name*	*I/O*	*Description*
24, 23	CLK, NCLK	I	Differential high speed clock inputs
26, 27	SDATA, NSDATA	I	Differential high speed serial data outputs
17, 18	CLK4, NCLK4	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	D(∅:3), ND(∅:3)	O	Differential parallel data outputs (ECL)
28, 1	SKIP, NSKIP	I	Differential word boundary inputs (ECL)
3, 5, 19, 25	V_{EE}		-5.2V supply voltage
2, 4, 11, 20	V_{CC}		∅ V ground connection
6, 16	V_{CCA}		∅ V output ground connection
21, 22	NC		No connection

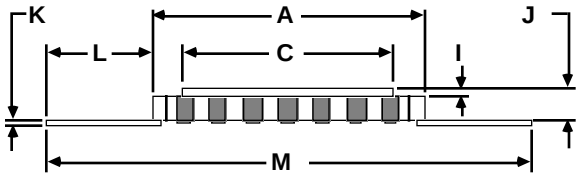
Notes: 1) The heat sink is connected to V_{EE} (pin 25). To prevent a short circuit between $V_{CC,}$ V_{CCA} (∅ V normally) and V_{EE} (-5.2V normally), do not connect this heat sink to ground.

2) The falling edge of SKIP causes realignment of the parallel word boundary making parallel data invalid for three CLK4, NCLK4 (12 CLK, NCLK) periods.

Package Information



28-Pin Leaded
Ceramic Package (LDCC)



NOTES:
Drawing not to scale.
Package: Ceramic (alumina);
Heat sink: Copper-tungsten;
Leads: Alloy 42 with gold plating.

Item	*mm (Min/Max)*	*in (Min/Max)*	*Item*	*mm (Min/Max)*	*in (Min/Max)*
A	11.176/11.682	0.440/0.460	K	0.102/0.203	0.004/0.008
B	1.016/1.524	0.040/0.060	L	5.842/6.858	0.230/0.270
C	8.128/8.636	0.33 TYP	M	22.860/25.398	0.900/1.000
E	1.143/1.397	0.050 TYP	N	0.356/0.559	0.014/0.022
I	0.406/0.610	0.016/0.024	O	1.525/2.287	0.075 TYP
J	1.829/2.235	.072/.088	—	—	—

DUT Boards

The VS8004FDUT/VS8005FDUT evaluation boards are special purpose circuit boards which provide a test bed suitable for evaluating the high performance characteristics of the VS8004 4:1 Multiplexer or the VS8005 1:4 Demultiplexer in the 28 pin leaded ceramic chip carrier.

The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 150 pF blocking capacitors. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument.

Normally, the VS8004 and VS8005 operate in an ECL environment with standard ECL power buses: ØV and -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power buses are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power bus.

The device to be tested is held in place with a pressure retaining fixture. The figure on the following page indicates the physical dimensions and the connection labels for the evaluation boards.

Figure 7: VS8004/VS8005 DUT Board Schematics

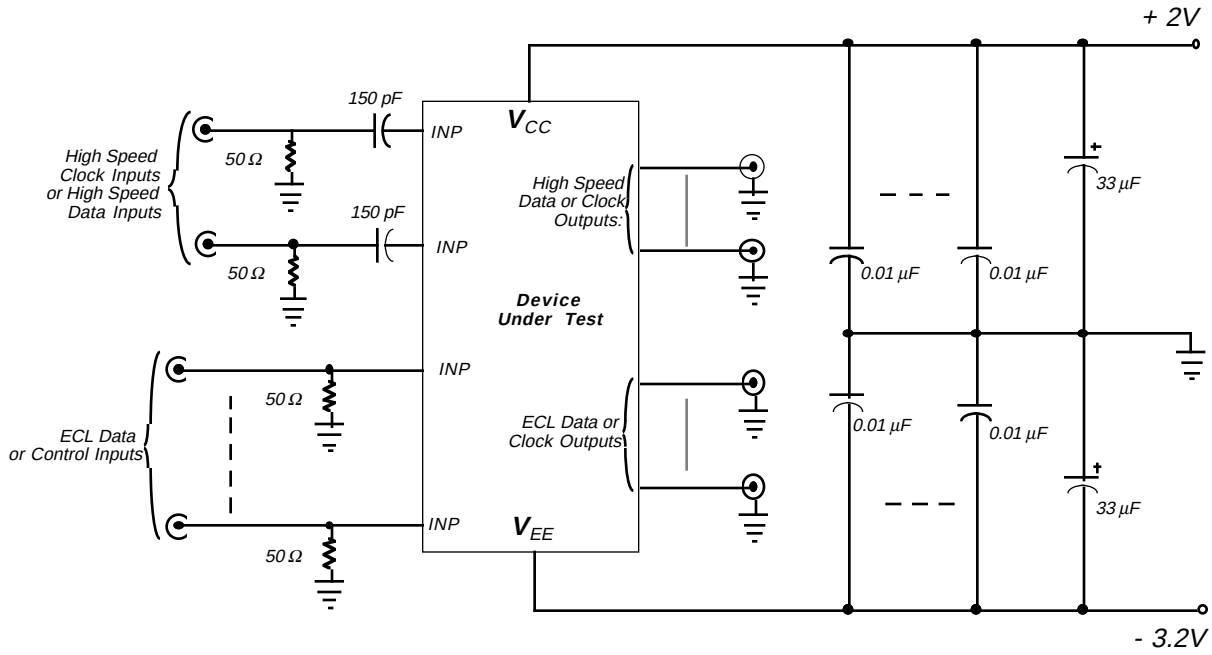
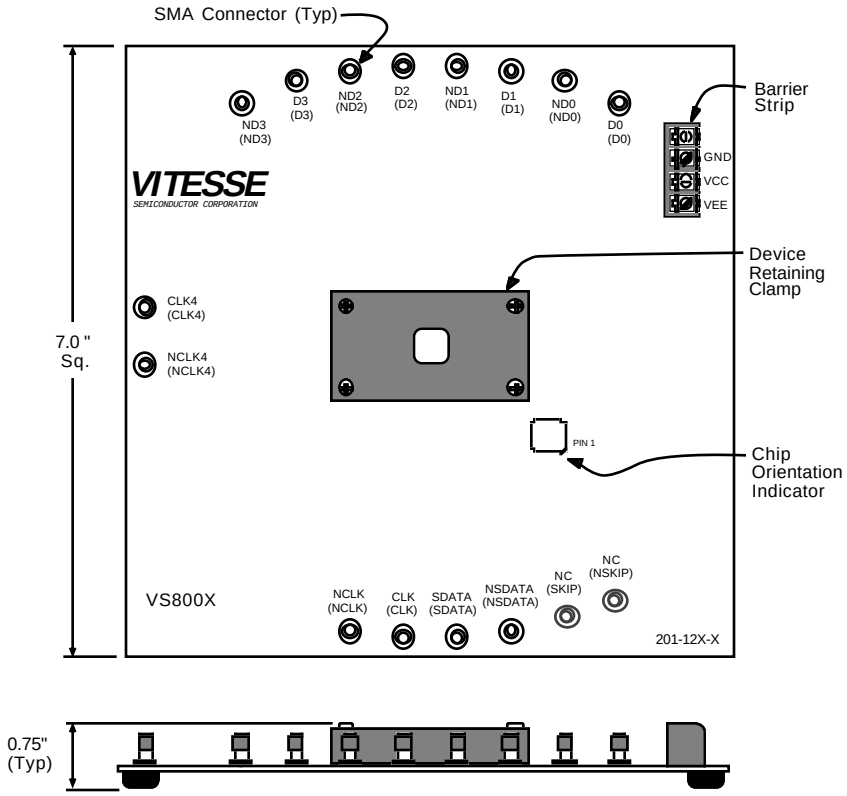


Figure 8: VS8004/VS8005 DUT Boards

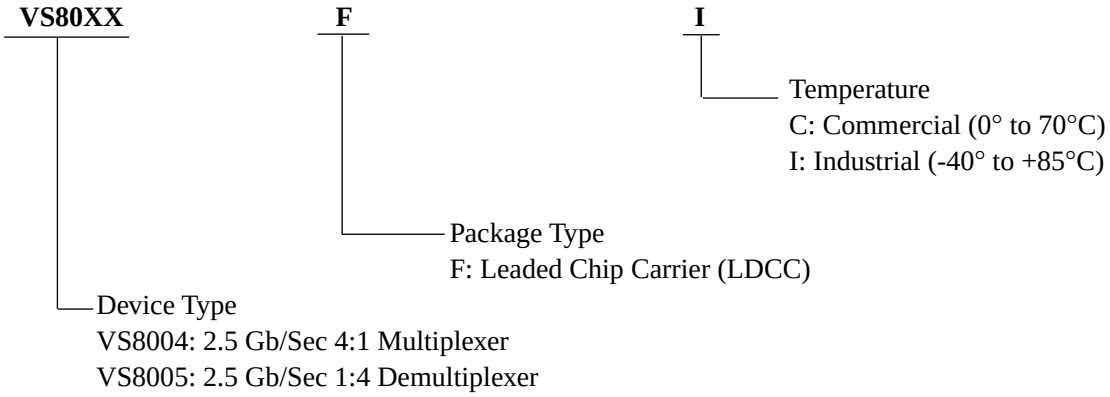


Notes: 1) This drawing represents both the VS8004FDUT and VS8005FDUT configurations. (Connection labels given in parentheses are for the VS8005.)

2) NC = No connection. Note: These connectors are omitted on the VS8004FDUT version of this evaluation board.

Ordering Information

Vitesse products are available in a variety of packages and operating ranges. The order number for this product is formed by using a combination of the following: *Device Type, Package Type, and Operating Temperature Range*.



Notice

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