



Device Overview

The 89HPES24T3G2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES24T3G2 is a 24-lane, 3-port Gen2 peripheral chip that performs PCI Express base switching with a feature set optimized for high performance applications such as servers, storage, and communications systems. It provides connectivity and switching functions between a PCI Express upstream port and two downstream ports and supports switching between downstream ports.

Features

- ◆ **High Performance PCI Express Switch**
 - Twenty-four 5 Gbps Gen2 PCI Express lanes supporting 5 Gbps and 2.5 Gbps operation
 - Up to three switch ports
 - Support for Max Payload Size up to 2048 bytes
 - Supports one virtual channel and eight traffic classes
 - Fully compliant with PCI Express base specification Revision 2.0
- ◆ **Flexible Architecture with Numerous Configuration Options**
 - Automatic per port link width negotiation to x8, x4, x2, or x1
 - Automatic lane reversal on all ports
 - Automatic polarity inversion
 - Supports in-band hot-plug presence detect capability
 - Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems

- Dynamic link width reconfiguration for power/performance optimization
- Configurable downstream port PCI-to-PCI bridge device numbering
- Crosslink support
- Supports ARI forwarding defined in the Alternative Routing-ID Interpretation (ARI) ECN for virtualized and non-virtualized environments
- Ability to load device configuration from serial EEPROM
- ◆ **Legacy Support**
 - PCI compatible INTx emulation
 - Supports bus locked transactions, allowing use of PCI Express with legacy software
- ◆ **Highly Integrated Solution**
 - Requires no external components
 - Incorporates on-chip internal memory for packet buffering and queueing
 - Integrates twenty-four 5 Gbps / 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)
- ◆ **Reliability, Availability, and Serviceability (RAS) Features**
 - Ability to disable peer-to-peer communications
 - Supports ECRC and Advanced Error Reporting
 - All internal data and control RAMs are SECDED ECC protected
 - Supports PCI Express hot-plug on all downstream ports
 - Supports upstream port hot-plug

Block Diagram

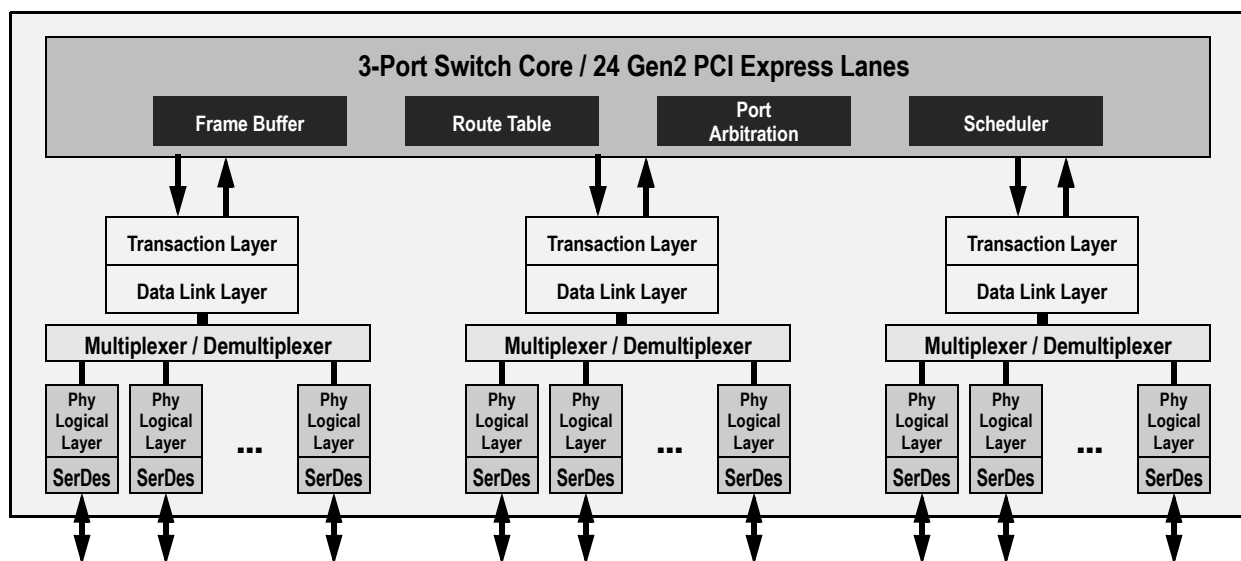


Figure 1 Internal Block Diagram

- Hot-swap capable I/O
- External Serial EEPROM contents are checksum protected
- Supports PCI Express Device Serial Number Capability
- Capability to monitor link reliability and autonomously change link speed to prevent link instability

◆ **Power Management**

- Utilizes advanced low-power design techniques to achieve low typical power consumption
- Support PCI Power Management Interface specification (PCI-PM 1.1)
 - Supports device power management states: D0, D3_{hot} and D3_{cold}
- Support for PCI Express Active State Power Management (ASPM) link state
 - Supports link power management states: L0, L0s, L1, L2/L3 Ready and L3
- Supports PCI Express Power Budgeting Capability
- Configurable SerDes power consumption
 - Supports optional PCI-Express SerDes Transmit Low-Swing Voltage Mode
 - Supports numerous SerDes Transmit Voltage Margin settings
- Unused SerDes are disabled

◆ **Testability and Debug Features**

- Per port link up and activity status outputs available on I/O expander outputs
- Built in SerDes 8-bit and 10-bit pseudo-random bit stream (PRBS) generators
- Numerous SerDes test modes, including a PRBS Master Loopback mode for in-system link testing
- Ability to read and write any internal register via SMBus and JTAG interfaces, including SerDes internal controls
- Per port statistics and performance counters, as well as proprietary link status registers

◆ **General Purpose Input/Output Pins**

- Each pin may be individually configured as an input or output
- Each pin may be individually configured as an interrupt input
- Some pins have selectable alternate functions

◆ **Option A Package: 19mm x 19mm 324-ball Flip Chip BGA with 1mm ball spacing**

◆ **Option B Package: 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES24T3G2 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 3 ports across 24 integrated serial lanes. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0, including operation in 5 Gbps, 2.5 Gbps, and mixed 5 Gbps / 2.5Gbps modes.

The PES24T3G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification

Revision 2.0. The PES24T3G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

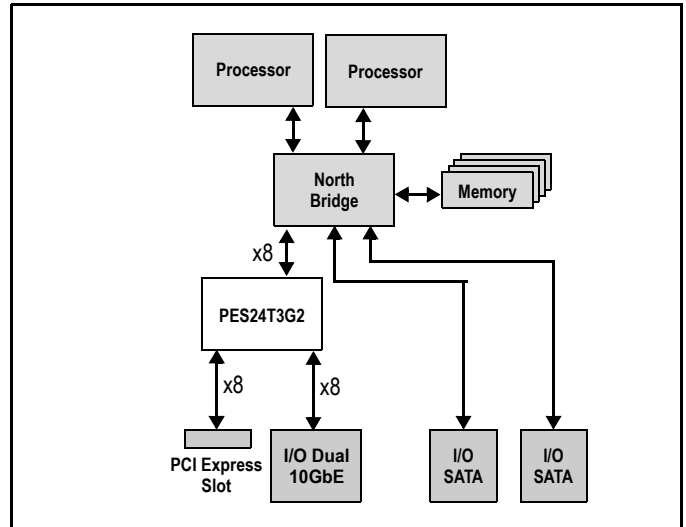


Figure 2 I/O Expansion Application

SMBus Interface

The PES24T3G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES24T3G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES24T3G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Note: MSMBADDR and SSMBADDR address pins are not available in the 19mm package. The MSMBADDR address is hardwired to 0x50, and the SSMBADDR address is hardwired to 0x77.

| Bit | Slave SMBus Address | Master SMBus Address |
|-----|---------------------|----------------------|
| 1 | SSMBADDR[1] | MSMBADDR[1] |
| 2 | SSMBADDR[2] | MSMBADDR[2] |
| 3 | SSMBADDR[3] | MSMBADDR[3] |
| 4 | 0 | MSMBADDR[4] |
| 5 | SSMBADDR[5] | 1 |
| 6 | 1 | 0 |
| 7 | 1 | 1 |

Table 1 Master and Slave SMBus Address Assignment for 27x27mm Package

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES24T3G2 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES24T3G2 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES24T3G2 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES24T3G2 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

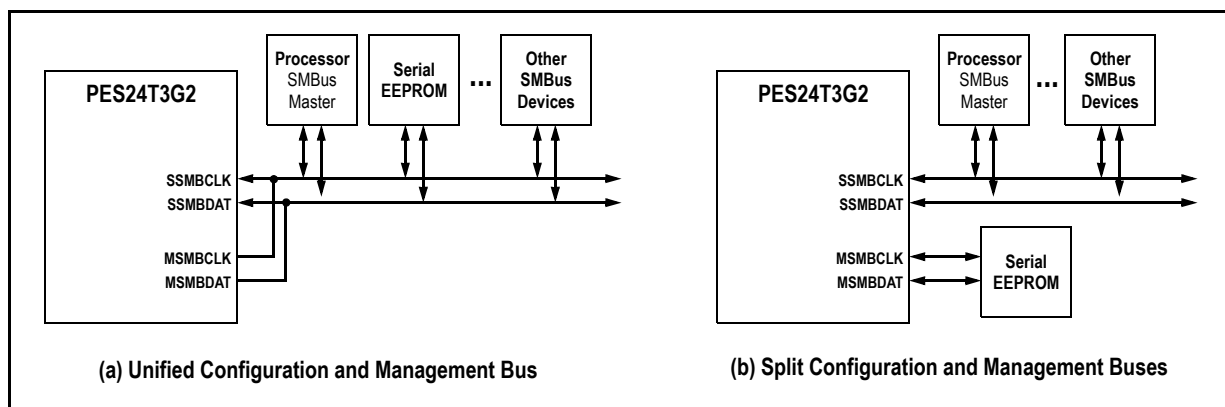


Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES24T3G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES24T3G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES24T3G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES24T3G2. In response to an I/O expander interrupt, the PES24T3G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES24T3G2 provides General Purpose Input/Output (GPIO) pins (7 pins in the 19mm package and 11 pins in the 27mm package) that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Many GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES24T3G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Note: In the PES24T3G2, the two downstream ports are labeled port 2 and port 4.

| Signal | Type | Name/Description |
|--------------------------|------|--|
| PE0RP[7:0] PE0RN[7:0] | I | PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0. Port 0 is the upstream port. |
| PE0TP[7:0] PE0TN[7:0] | O | PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port. |
| PE2RP[7:0] PE2RN[7:0] | I | PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2. |
| PE2TP[7:0] PE2TN[7:0] | O | PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2. |
| PE4RP[7:0] PE4RN[7:0] | I | PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4. |
| PE4TP[7:0] PE4TN[7:0] | O | PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4. |
| PEREFCLKP PEREFCLKN | I | PCI Express Reference Clock. Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal. |
| REFCLKM ¹ | I | PCI Express Reference Clock Mode Select. This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz This pin should be static and not change following the negation of PERSTN. |

Table 2 PCI Express Interface Pins

¹ REFCLKM is not available in the 19mm package and frequency is set at 100MHz.

| Signal | Type | Name/Description |
|------------------------------|------|--|
| MSMBADDR[4:1] ¹ | I | Master SMBus Address. These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. |
| MSMBCLK | I/O | Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus. |
| MSMBDAT | I/O | Master SMBus Data. This bidirectional signal is used for data on the master SMBus. |
| SSMBADDR[5,3:1] ² | I | Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds. |
| SSMBCLK | I/O | Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus. |

Table 3 SMBus Interface Pins (Part 1 of 2)

| Signal | Type | Name/Description |
|---------|------|---|
| SSMBDAT | I/O | Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus. |

Table 3 SMBus Interface Pins (Part 2 of 2)

¹ MSMBADDR pins are not available in the 19mm package. Address hardwired to 0x50.

² SSMBADDR pins are not available in the 19mm package. Address hardwired to 0x77.

| Signal | Type | Name/Description |
|----------------------|------|---|
| GPIO[0] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2 |
| GPIO[1] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4 |
| GPIO[2] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input |
| GPIO[3] ¹ | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input |
| GPIO[4] ¹ | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input |
| GPIO[5] ¹ | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |
| GPIO[6] ¹ | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |
| GPIO[7] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output |
| GPIO[8] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |
| GPIO[9] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |
| GPIO[10] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |

Table 4 General Purpose I/O Pins

¹ GPIO pins 3, 4, 5, 6 are not available in the 19mm package.

| Signal | Type | Name/Description |
|------------------------|------|---|
| CCLKDS | I | Common Clock Downstream. The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices. This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in each downstream port's PCIELSTS register. |
| CCLKUS | I | Common Clock Upstream. The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIEIPTS register. |
| MSMBSMODE ¹ | I | Master SMBus Slow Mode. The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden. |
| PERSTN | I | Fundamental Reset. Assertion of this signal resets all logic inside PES24T3G2 and initiates a PCI Express fundamental reset. |
| RSTHALT ² | I | Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES24T3G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. |
| SWMODE[2:0] | I | Switch Mode. These configuration pins determine the PES24T3G2 switch operating mode. 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM initialization 0x2 - through 0x7 Reserved These pins should be static and not change following the negation of PERSTN. |

Table 5 System Pins

¹ MSMBSMODE is not available in the 19mm package, resulting in the master SMBus operating only at 400 KHz.

² RSTHALT is not available in the 19mm package.

| Signal | Type | Name/Description |
|----------|------|---|
| JTAG_TCK | I | JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle. |
| JTAG_TDI | I | JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller. |
| JTAG_TDO | O | JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated. |
| JTAG_TMS | I | JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. |

Table 6 Test Pins (Part 1 of 2)

| Signal | Type | Name/Description |
|-------------|------|--|
| JTAG_TRST_N | I | JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board |

Table 6 Test Pins (Part 2 of 2)

| Signal | Type | Name/Description |
|----------------------|------|---|
| REFRES0, REFRES1 | I/O | Port 0 External Reference Resistors. Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from these pins to ground. |
| REFRES2, REFRES3 | I/O | Port 2 External Reference Resistors. Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from these pins to ground. |
| REFRES4, REFRES5 | I/O | Port 4 External Reference Resistors. Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from these pins to ground. |
| V _{DD} CORE | I | Core V_{DD}. Power supply for core logic. |
| V _{DD} I/O | I | I/O V_{DD}. LVTTTL I/O buffer power supply. |
| V _{DD} PEA | I | PCI Express Analog Power. Serdes analog power supply (1.0V). |
| V _{DD} PEHA | I | PCI Express Analog High Power. Serdes analog power supply (2.5V). |
| V _{DD} PETA | I | PCI Express Transmitter Analog Voltage. Serdes transmitter analog power supply (1.0V). |
| V _{SS} | I | Ground. |

Table 7 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the PES24T3G2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor ¹ | Notes | | |
|-----------------------|------------------------------|----------------------|--------|------------------|--------------------------------|-------------------|--|------------------|
| PCI Express Interface | PE0RN[7:0] | I | CML | Serial Link | | | | |
| | PE0RP[7:0] | I | | | | | | |
| | PE0TN[7:0] | O | | | | | | |
| | PE0TP[7:0] | O | | | | | | |
| | PE2RN[7:0] | I | | | | | | |
| | PE2RP[7:0] | I | | | | | | |
| | PE2TN[7:0] | O | | | | | | |
| | PE2TP[7:0] | O | | | | | | |
| | PE4RN[7:0] | I | | | | | | |
| | PE4RP[7:0] | I | | | | | | |
| | PE4TN[7:0] | O | | | | | | |
| | PE4TP[7:0] | O | | | | | | |
| | PEREFCLKN | I | | | | Diff. Clock Input | | Refer to Table 9 |
| | PEREFCLKP | I | | | | | | |
| | | REFCLKM ² | I | LVTTTL | Input | pull-down | | |
| SMBus | MSMBADDR[4:1] ³ | I | LVTTTL | Input | pull-down | | | |
| | MSMBCLK | I/O | | STI ⁴ | | pull-up on board | | |
| | MSMBDAT | I/O | | STI | | pull-up on board | | |
| | SSMBADDR[5,3:1] ³ | I | | Input | pull-up | | | |
| | SSMBCLK | I/O | | STI | | pull-up on board | | |
| | SSMBDAT | I/O | | STI | | pull-up on board | | |
| General Purpose I/O | GPIO[10:0] ⁵ | I/O | LVTTTL | STI, High Drive | pull-up | | | |
| System Pins | CCLKDS | I | LVTTTL | Input | pull-up | | | |
| | CCLKUS | I | | Input | pull-up | | | |
| | MSMBSMODE ⁶ | I | | Input | pull-down | | | |
| | PERSTN | I | | STI | | | | |
| | RSTHALT ⁶ | I | | Input | pull-down | | | |
| | SWMODE[2:0] | I | | Input | pull-down | | | |
| EJTAG / JTAG | JTAG_TCK | I | LVTTTL | STI | pull-up | | | |
| | JTAG_TDI | I | | STI | pull-up | | | |
| | JTAG_TDO | O | | | | | | |
| | JTAG_TMS | I | | STI | pull-up | | | |
| | JTAG_TRST_N | I | | STI | pull-up | | | |

Table 8 Pin Characteristics (Part 1 of 2)

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor ¹ | Notes |
|----------------------------|----------|------|--------|----------|--------------------------------|-------|
| SerDes Reference Resistors | REFRES0 | I/O | Analog | | | |
| | REFRES1 | I/O | | | | |
| | REFRES2 | I/O | | | | |
| | REFRES3 | I/O | | | | |
| | REFRES4 | I/O | | | | |
| | REFRES5 | I/O | | | | |

Table 8 Pin Characteristics (Part 2 of 2)

- ¹. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 90K Ω for pull-down.
- ². REFCLKM pin is not available in the 19mm package.
- ³. SMBus address pins are not available in the 19mm package.
- ⁴. Schmitt Trigger Input (STI).
- ⁵. GPIO pins 3, 4, 5, 6 are not available in the 19mm package.
- ⁶. MSMBSMODE and RSTHALT are not available in the 19mm package.

Logic Diagram — PES24T3G2

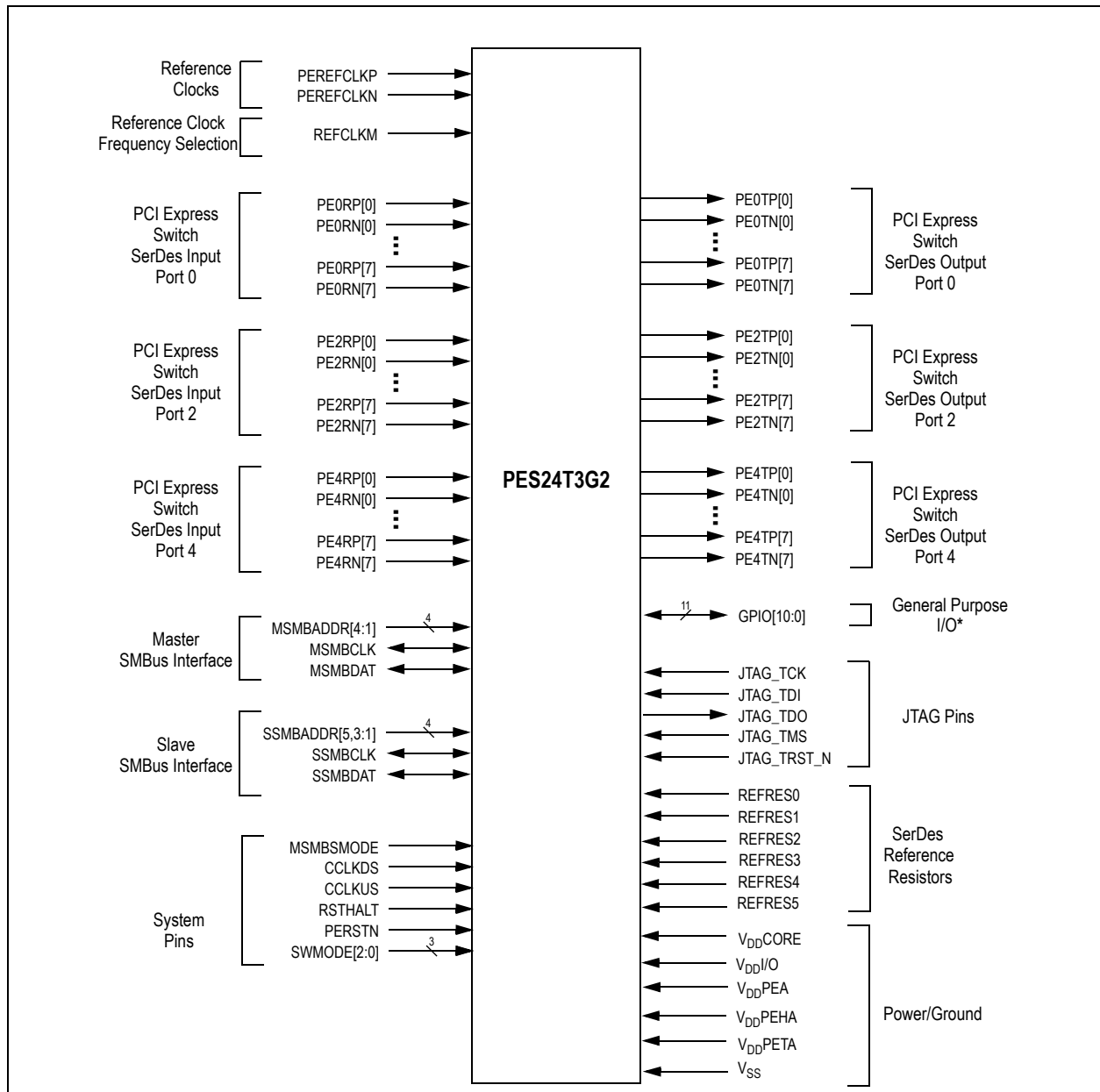


Figure 4 PES24T3G2 Logic Diagram

Note: The following pins are not available in the 19mm package: REFCLKM, MSMBADDR, SSMBADDR, MSMBSMODE, RSTHALT, GPIO[6:3].

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

| Parameter | Description | Condition | Min | Typical | Max | Unit |
|--------------------------|--|--------------|-------|---------|------------------|------|
| Refclk _{FREQ} | Input reference clock frequency range | | 100 | | 125 ¹ | MHz |
| T _{C-RISE} | Rising edge rate | Differential | 0.6 | | 4 | V/ns |
| T _{C-FALL} | Falling edge rate | Differential | 0.6 | | 4 | V/ns |
| V _{IH} | Differential input high voltage | Differential | +150 | | | mV |
| V _{IL} | Differential input low voltage | Differential | | | -150 | mV |
| V _{CROSS} | Absolute single-ended crossing point voltage | Single-ended | +250 | | +550 | mV |
| V _{CROSS-DELTA} | Variation of V _{CROSS} over all rising clock edges | Single-ended | | | +140 | mV |
| V _{RB} | Ring back voltage margin | Differential | -100 | | +100 | mV |
| T _{STABLE} | Time before V _{RB} is allowed | Differential | 500 | | | ps |
| T _{PERIOD-AVG} | Average clock period accuracy | | -300 | | 2800 | ppm |
| T _{PERIOD-ABS} | Absolute period, including spread-spectrum and jitter | | 9.847 | | 10.203 | ns |
| T _{CC-JITTER} | Cycle to cycle jitter | | | | 150 | ps |
| V _{MAX} | Absolute maximum input voltage | | | | +1.15 | V |
| V _{MIN} | Absolute minimum input voltage | | -0.3 | | | V |
| Duty Cycle | Duty cycle | | 40 | | 60 | % |
| Rise/Fall Matching | Single ended rising Refclk edge rate versus falling Refclk edge rate | | | 20 | | % |
| Z _{C-DC} | Clock source output DC impedance | | 40 | | 60 | Ω |

Table 9 Input Clock Requirements

¹ The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM. Frequency is set at 100 MHz in the 19mm package.

AC Timing Characteristics

| Parameter | Description | Gen 1 | | | Gen 2 | | | Units |
|---|--|------------------|------------------|------------------|------------------|------------------|------------------|-------|
| | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | |
| PCIe Transmit | | | | | | | | |
| UI | Unit Interval | 399.88 | 400 | 400.12 | 199.94 | 200 | 200.06 | ps |
| T _{TX-EYE} | Minimum Tx Eye Width | 0.75 | | | 0.75 | | | UI |
| T _{TX-EYE-MEDIAN-to-MAX-JITTER} | Maximum time between the jitter median and maximum deviation from the median | | | 0.125 | | | | UI |
| T _{TX-RISE} , T _{TX-FALL} | TX Rise/Fall Time: 20% - 80% | 0.125 | | | 0.15 | | | UI |
| T _{TX-IDLE-MIN} | Minimum time in idle | 20 | | | 20 | | | UI |

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

| Parameter | Description | Gen 1 | | | Gen 2 | | | Units |
|--|--|------------------|------------------|------------------|------------------|------------------|------------------|-------|
| | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | |
| T _{TX-IDLE-SET-TO-IDLE} | Maximum time to transition to a valid Idle after sending an Idle ordered set | | | 8 | | | 8 | ns |
| T _{TX-IDLE-TO-DIFF-DATA} | Maximum time to transition from valid idle to diff data | | | 8 | | | 8 | ns |
| T _{TX-SKEW} | Transmitter data skew between any 2 lanes | | | 1.3 | | | 1.3 | ns |
| T _{MIN-PULSED} | Minimum Instantaneous Lone Pulse Width | NA | | | 0.9 | | | UI |
| T _{TX-HF-DJ-DD} | Transmitter Deterministic Jitter > 1.5MHz Bandwidth | NA | | | | | 0.15 | UI |
| T _{RF-MISMATCH} | Rise/Fall Time Differential Mismatch | NA | | | | | 0.1 | UI |
| PCIe Receive | | | | | | | | |
| UI | Unit Interval | 399.88 | 400 | 400.12 | 199.94 | | 200.06 | ps |
| T _{RX-EYE (with jitter)} | Minimum Receiver Eye Width (jitter tolerance) | 0.4 | | | 0.4 | | | UI |
| T _{RX-EYE-MEDIUM TO MAX JITTER} | Max time between jitter median & max deviation | | | 0.3 | | | | UI |
| T _{RX-SKEW} | Lane to lane input skew | | | 20 | | | 8 | ns |
| T _{RX-HF-RMS} | 1.5 — 100 MHz RMS jitter (common clock) | NA | | | | | 3.4 | ps |
| T _{RX-HF-DJ-DD} | Maximum tolerable DJ by the receiver (common clock) | NA | | | | | 88 | ps |
| T _{RX-LF-RMS} | 10 KHz to 1.5 MHz RMS jitter (common clock) | NA | | | | | 4.2 | ps |
| T _{RX-MIN-PULSE} | Minimum receiver instantaneous eye width | NA | | | 0.6 | | | UI |

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

¹. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

| Signal | Symbol | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|-------------------------|------------------------------|----------------|-----|-----|------|--------------------------|
| GPIO | | | | | | |
| GPIO[10:0] ¹ | T _{pw} ² | None | 50 | — | ns | |

Table 11 GPIO AC Timing Characteristics

¹. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous. Note that GPIO{6:3} pins are not available in the 19mm package.

². The values for this symbol were determined by calculation, not by testing.

| Signal | Symbol | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|-------------------------------------|------------------------|------------------|------|------|------|--------------------------|
| JTAG | | | | | | |
| JTAG_TCK | Tper_16a | none | 50.0 | — | ns | See Figure 5. |
| | Thigh_16a, Tlow_16a | | 10.0 | 25.0 | ns | |
| JTAG_TMS ¹ , JTAG_TDI | Tsu_16b | JTAG_TCK rising | 2.4 | — | ns | |
| | Thld_16b | | 1.0 | — | ns | |
| JTAG_TDO | Tdo_16c | JTAG_TCK falling | — | 20 | ns | |
| | Tdz_16c ² | | — | 20 | ns | |
| JTAG_TRST_N | Tpw_16d ² | none | 25.0 | — | ns | |

Table 12 JTAG AC Timing Characteristics

¹ The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

² The values for this symbol were determined by calculation, not by testing.

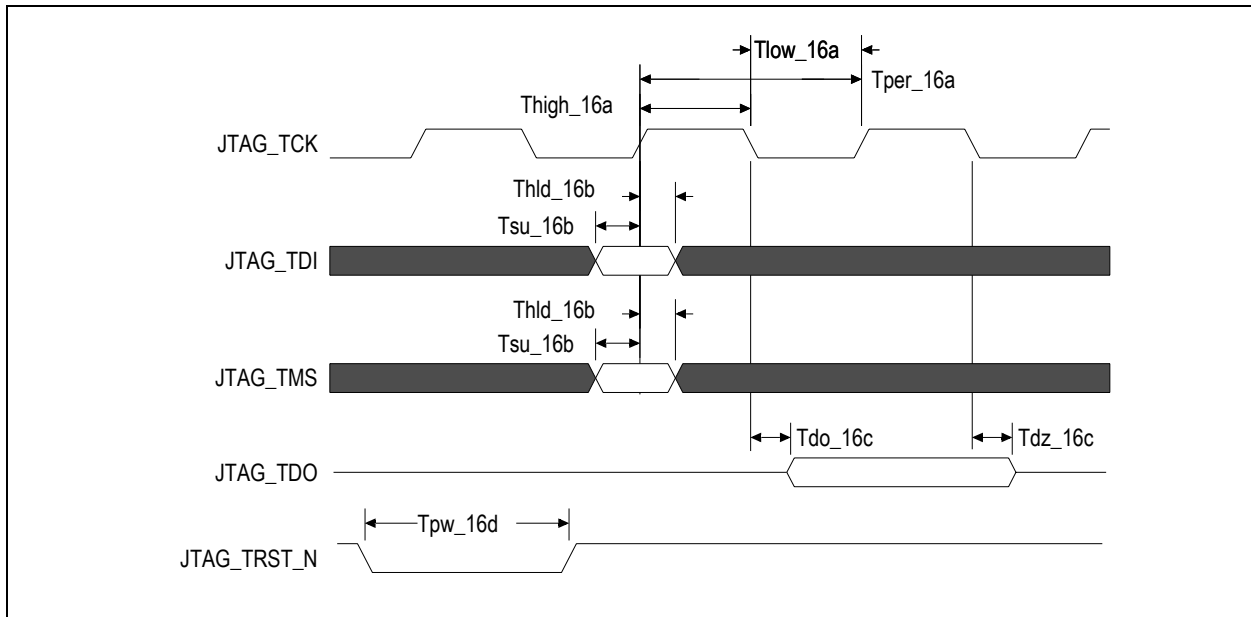


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|-----------------------------------|---|---------|---------|---------|------|
| V _{DD} CORE | Internal logic supply | 0.9 | 1.0 | 1.1 | V |
| V _{DD} I/O | I/O supply except for SerDes LVPECL/CML | 3.135 | 3.3 | 3.465 | V |
| V _{DD} PEA ¹ | PCI Express Analog Power | 0.95 | 1.0 | 1.1 | V |
| V _{DD} PEHA ² | PCI Express Analog High Power | 2.25 | 2.5 | 2.75 | V |
| V _{DD} PETA | PCI Express Transmitter Analog Voltage | 0.95 | 1.0 | 1.1 | V |
| V _{SS} | Common ground | 0 | 0 | 0 | V |

Table 13 PES24T3G2 Operating Voltages

¹ V_{DD}PEA should have no more than 25mV_{peak-peak} AC power supply noise superimposed on the 1.0V nominal DC value.

² V_{DD}PEHA should have no more than 50mV_{peak-peak} AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

| Grade | Temperature |
|------------|----------------------|
| Commercial | 0°C to +70°C Ambient |

Table 14 PES24T3G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

| Number of Active Lanes per Port | | Core Supply | | PCIe Analog Supply | | PCIe Analog High Supply | | PCIe Termination Supply | | I/O Supply | | Total | |
|---------------------------------|-------|-------------|----------|--------------------|----------|-------------------------|-----------|-------------------------|-----------|------------|------------|-----------|-----------|
| | | Typ 1.0V | Max 1.1V | Typ 1.0V | Max 1.1V | Typ 2.5V | Max 2.75V | Typ 1.0V | Max 1.15V | Typ 3.3V | Max 3.465V | Typ Power | Max Power |
| 8/8/8 (Full Swing) | mA | 1010 | 1260 | 1384 | 1600 | 161 | 176 | 541 | 600 | 3 | 5 | | |
| | Watts | 1.01 | 1.39 | 1.38 | 1.76 | 0.40 | 0.48 | 0.54 | 0.66 | 0.010 | 0.017 | 3.35 | 4.31 |
| 88/8 (Half Swing) | mA | 1010 | 1260 | 1190 | 1376 | 161 | 176 | 281 | 312 | 3 | 5 | | |
| | Watts | 1.01 | 1.39 | 1.19 | 1.51 | 0.40 | 0.48 | 0.28 | 0.34 | 0.010 | 0.017 | 2.89 | 3.74 |

Table 15 PES24T3G2 Power Consumption

Thermal Considerations — Option A Package

This section describes thermal considerations for the PES24T3G2 (19mm² FCBGA324 package). The data in Table 16 below contains information that is relevant to the thermal performance of the PES24T3G2 switch.

| Symbol | Parameter | Value | Units | Conditions |
|--------------------------|---|-------|-------|----------------|
| $T_{J(max)}$ | Junction Temperature | 125 | °C | Maximum |
| $T_{A(max)}$ | Ambient Temperature | 70 | °C | Maximum |
| $\theta_{JA(effective)}$ | Effective Thermal Resistance, Junction-to-Ambient | 16.8 | °C/W | Zero air flow |
| | | 10.1 | °C/W | 1 m/S air flow |
| | | 9.2 | °C/W | 2 m/S air flow |
| θ_{JB} | Thermal Resistance, Junction-to-Board | 4.1 | °C/W | |
| θ_{JC} | Thermal Resistance, Junction-to-Case | 0.3 | °C/W | |
| P | Power Dissipation of the Device | 4.31 | Watts | Maximum |

Table 16 Thermal Specifications for PES24T3G2, 19x19 mm FCBGA324 Package

Thermal Considerations — Option B Package

This section describes thermal considerations for the PES24T3G2 (27mm² FCBGA676 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES24T3G2 switch.

| Symbol | Parameter | Value | Units | Conditions |
|--------------------------|---|-------|-------|----------------|
| $T_{J(max)}$ | Junction Temperature | 125 | °C | Maximum |
| $T_{A(max)}$ | Ambient Temperature | 70 | °C | Maximum |
| $\theta_{JA(effective)}$ | Effective Thermal Resistance, Junction-to-Ambient | 14.6 | °C/W | Zero air flow |
| | | 8.2 | °C/W | 1 m/S air flow |
| | | 7.2 | °C/W | 2 m/S air flow |
| θ_{JB} | Thermal Resistance, Junction-to-Board | 3.1 | °C/W | |
| θ_{JC} | Thermal Resistance, Junction-to-Case | 0.3 | °C/W | |
| P | Power Dissipation of the Device | 4.31 | Watts | Maximum |

Table 17 Thermal Specifications for PES24T3G2, 27x27 mm FCBGA676 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 16. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 16), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 8 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 0.5 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

| I/O Type | Parameter | Description | Gen1 | | | Gen2 | | | Unit | Condi- tions | |
|----------------------------|--|---|------------------|------------------|------------------|------------------|------------------|------------------|------|-----------------|----------------|
| | | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | | | |
| Serial Link | PCIe Transmit | | | | | | | | | | |
| | V _{TX-DIFFp-p} | Differential peak-to-peak output voltage | 800 | | 1200 | 800 | | 1200 | mV | | |
| | V _{TX-DIFFp-p-LOW} | Low-Drive Differential Peak to Peak Output Voltage | 400 | | 1200 | 400 | | 1200 | mV | | |
| | V _{TX-DE-RATIO-3.5dB} | De-emphasized differential output voltage | -3 | | -4 | -3.0 | -3.5 | -4.0 | dB | | |
| | V _{TX-DE-RATIO-6.0dB} | De-emphasized differential output voltage | NA | | | -5.5 | -6.0 | -6.5 | dB | | |
| | V _{TX-DC-CM} | DC Common mode voltage | 0 | | 3.6 | 0 | | 3.6 | V | | |
| | V _{TX-CM-ACP} | RMS AC peak common mode output voltage | | | 20 | | | | mV | | |
| | V _{TX-CM-DC-active-idle-delta} | Abs delta of DC common mode voltage between L0 and idle | | | 100 | | | 100 | mV | | |
| | V _{TX-CM-DC-line-delta} | Abs delta of DC common mode voltage between D+ and D- | | | 25 | | | 25 | mV | | |
| | V _{TX-Idle-DiffP} | Electrical idle diff peak output | | | 20 | | | 20 | mV | | |
| | RL _{TX-DIFF} | Transmitter Differential Return loss | 10 | | | | | | 10 | dB | 0.05 - 1.25GHz |
| | | | | | | | | | 8 | dB | 1.25 - 2.5GHz |
| | RL _{TX-CM} | Transmitter Common Mode Return loss | 6 | | | | | 6 | dB | | |
| | Z _{TX-DIFF-DC} | DC Differential TX impedance | 80 | 100 | 120 | | | 120 | Ω | | |
| | V _{TX-CM-ACpp} | Peak-Peak AC Common | NA | | | | | 100 | mV | | |
| | V _{TX-DC-CM} | Transmit Driver DC Common Mode Voltage | 0 | | 3.6 | 0 | | 3.6 | V | | |
| V _{TX-RCV-DETECT} | The amount of voltage change allowed during Receiver Detection | | | 600 | | | 600 | mV | | | |
| I _{TX-SHORT} | Transmitter Short Circuit Current Limit | 0 | | 90 | | | | 90 | mA | | |

Table 18 DC Electrical Characteristics (Part 1 of 2)

| I/O Type | Parameter | Description | Gen1 | | | Gen2 | | | Unit | Condi- tions |
|-------------------------------------|--------------------------------------|--|------------------|------------------|------------------|---------------------------|------------------|------------------|-----------------|------------------|
| | | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | | |
| Serial Link (cont.) | PCIe Receive | | | | | | | | | |
| | $V_{RX-DIFFp-p}$ | Differential input voltage (peak-to-peak) | 175 | | 1200 | 120 | | 1200 | mV | |
| | $RL_{RX-DIFF}$ | Receiver Differential Return Loss | 10 | | | | | 10 | dB | 0.05 - 1.25GHz |
| | | | | | | | | 8 | | 1.25 - 2.5GHz |
| | RL_{RX-CM} | Receiver Common Mode Return Loss | 6 | | | | | 6 | dB | |
| | $Z_{RX-DIFF-DC}$ | Differential input impedance (DC) | 80 | 100 | 120 | Refer to return loss spec | | | Ω | |
| | Z_{RX--DC} | DC common mode impedance | 40 | 50 | 60 | 40 | | 60 | Ω | |
| | $Z_{RX-COMM-DC}$ | Powered down input common mode impedance (DC) | 200k | 350k | | | | 50k | Ω | |
| | $Z_{RX-HIGH-IMP-DC-POS}$ | DC input CM input impedance for $V > 0$ during reset or power down | | | 50k | | | 50k | Ω | |
| | $Z_{RX-HIGH-IMP-DC-NEG}$ | DC input CM input impedance for $V < 0$ during reset or power down | | | 1.0k | | | 1.0k | Ω | |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical idle detect threshold | 65 | | 175 | 65 | | 175 | mV | | |
| $V_{RX-CM-ACp}$ | Receiver AC common-mode peak voltage | | | 150 | | | 150 | mV | $V_{RX-CM-ACp}$ | |
| PCIe REFCLK | | | | | | | | | | |
| | C_{IN} | Input Capacitance | 1.5 | — | | 1.5 | — | | pF | |
| Other I/Os | | | | | | | | | | |
| LOW Drive Output | I_{OL} | | — | 2.5 | — | — | 2.5 | — | mA | $V_{OL} = 0.4v$ |
| | I_{OH} | | — | -5.5 | — | — | -5.5 | — | mA | $V_{OH} = 1.5V$ |
| High Drive Output | I_{OL} | | — | 12.0 | — | — | 12.0 | — | mA | $V_{OL} = 0.4v$ |
| | I_{OH} | | — | -20.0 | — | — | -20.0 | — | mA | $V_{OH} = 1.5V$ |
| Schmitt Trig- ger Input (STI) | V_{IL} | | -0.3 | — | 0.8 | -0.3 | — | 0.8 | V | — |
| | V_{IH} | | 2.0 | — | $V_{DD}/O + 0.5$ | 2.0 | — | $V_{DD}/O + 0.5$ | V | — |
| Input | V_{IL} | | -0.3 | — | 0.8 | -0.3 | — | 0.8 | V | — |
| | V_{IH} | | 2.0 | — | $V_{DD}/O + 0.5$ | 2.0 | — | $V_{DD}/O + 0.5$ | V | — |
| Capacitance | C_{IN} | | — | — | 8.5 | — | — | 8.5 | pF | — |
| Leakage | Inputs | | — | — | ± 10 | — | — | ± 10 | μA | V_{DD}/O (max) |
| | I/O_{LEAK} W/O Pull-ups/downs | | — | — | ± 10 | — | — | ± 10 | μA | V_{DD}/O (max) |
| | I/O_{LEAK} WITH Pull-ups/downs | | — | — | ± 80 | — | — | ± 80 | μA | V_{DD}/O (max) |

Table 18 DC Electrical Characteristics (Part 2 of 2)

¹ Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

Option A Package Pinout, 19x19mm 324-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES24T3G2 device.

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|---------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| A1 | V _{SS} | | B17 | PE4TN00 | | D15 | V _{DD} CORE | | F13 | V _{SS} | |
| A2 | V _{DD} I/O | | B18 | PE4TP00 | | D16 | V _{SS} | | F14 | PE4RN03 | |
| A3 | V _{SS} | | C1 | PE2TP06 | | D17 | V _{SS} | | F15 | PE4RP03 | |
| A4 | V _{SS} | | C2 | PE2TN06 | | D18 | V _{SS} | | F16 | V _{SS} | |
| A5 | V _{SS} | | C3 | V _{SS} | | E1 | PE2TP05 | | F17 | PE4TN03 | |
| A6 | V _{DD} I/O | | C4 | PE2RP06 | | E2 | PE2TN05 | | F18 | PE4TP03 | |
| A7 | V _{SS} | | C5 | PE2RN06 | | E3 | V _{SS} | | G1 | V _{SS} | |
| A8 | JTAG_TDI | | C6 | V _{SS} | | E4 | PE2RP05 | | G2 | V _{SS} | |
| A9 | MSMBDAT | | C7 | JTAG_TCK | | E5 | PE2RN05 | | G3 | V _{SS} | |
| A10 | V _{DD} I/O | | C8 | JTAG_TRST_N | | E6 | V _{DD} CORE | | G4 | V _{DD} CORE | |
| A11 | V _{SS} | | C9 | SSMBDAT | | E7 | V _{DD} CORE | | G5 | V _{DD} CORE | |
| A12 | GPIO_00 | 1 | C10 | CCLKDS | | E8 | V _{DD} CORE | | G6 | V _{DD} PEA | |
| A13 | V _{DD} I/O | | C11 | SWMODE_2 | | E9 | V _{SS} | | G7 | V _{DD} PEA | |
| A14 | V _{DD} I/O | | C12 | GPIO_02 | | E10 | V _{DD} CORE | | G8 | V _{DD} CORE | |
| A15 | V _{SS} | | C13 | GPIO_09 | | E11 | V _{DD} CORE | | G9 | V _{DD} CORE | |
| A16 | V _{SS} | | C14 | PE4RN01 | | E12 | V _{DD} CORE | | G10 | V _{DD} CORE | |
| A17 | V _{DD} I/O | | C15 | PE4RP01 | | E13 | V _{DD} CORE | | G11 | V _{SS} | |
| A18 | V _{DD} I/O | | C16 | V _{SS} | | E14 | PE4RN02 | | G12 | V _{DD} PEA | |
| B1 | PE2TP07 | | C17 | PE4TN01 | | E15 | PE4RP02 | | G13 | V _{DD} PEA | |
| B2 | PE2TN07 | | C18 | PE4TP01 | | E16 | V _{SS} | | G14 | V _{DD} CORE | |
| B3 | V _{SS} | | D1 | V _{SS} | | E17 | PE4TN02 | | G15 | V _{DD} CORE | |
| B4 | PE2RP07 | | D2 | V _{SS} | | E18 | PE4TP02 | | G16 | V _{SS} | |
| B5 | PE2RN07 | | D3 | V _{SS} | | F1 | PE2TP04 | | G17 | V _{SS} | |
| B6 | V _{DD} I/O | | D4 | V _{DD} CORE | | F2 | PE2TN04 | | G18 | V _{SS} | |
| B7 | V _{SS} | | D5 | V _{DD} CORE | | F3 | V _{SS} | | H1 | PE2TP03 | |
| B8 | JTAG_TMS | | D6 | V _{DD} I/O | | F4 | PE2RP04 | | H2 | PE2TN03 | |
| B9 | SSMBCLK | | D7 | JTAG_TDO | | F5 | PE2RN04 | | H3 | V _{SS} | |
| B10 | V _{DD} I/O | | D8 | MSMBCLK | | F6 | V _{SS} | | H4 | PE2RP03 | |
| B11 | SWMODE_1 | | D9 | CCLKUS | | F7 | V _{SS} | | H5 | PE2RN03 | |
| B12 | GPIO_01 | 1 | D10 | SWMODE_0 | | F8 | V _{DD} CORE | | H6 | V _{DD} PEA | |
| B13 | GPIO_10 | | D11 | PERSTN | | F9 | V _{SS} | | H7 | V _{DD} PEA | |
| B14 | PE4RN00 | | D12 | GPIO_07 | 1 | F10 | V _{DD} CORE | | H8 | V _{DD} CORE | |
| B15 | PE4RP00 | | D13 | GPIO_08 | | F11 | V _{SS} | | H9 | V _{DD} CORE | |
| B16 | V _{SS} | | D14 | V _{DD} CORE | | F12 | V _{SS} | | H10 | V _{DD} CORE | |

Table 19 PES24T3G2 (19x19mm 324-pin) Signal Pin-Out (Part 1 of 3)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| H11 | V _{SS} | | K13 | V _{DD} PETA | | M15 | PE4RP07 | | P17 | V _{DD} CORE | |
| H12 | V _{DD} PEA | | K14 | V _{DD} CORE | | M16 | V _{SS} | | P18 | V _{SS} | |
| H13 | V _{DD} PEA | | K15 | NC | | M17 | PE4TN07 | | R1 | V _{SS} | |
| H14 | PE4RN04 | | K16 | V _{SS} | | M18 | PE4TP07 | | R2 | V _{DD} CORE | |
| H15 | PE4RP04 | | K17 | REFRES5 | | N1 | V _{SS} | | R3 | V _{DD} CORE | |
| H16 | V _{SS} | | K18 | REFRES4 | | N2 | V _{SS} | | R4 | PE0RP07 | |
| H17 | PE4TN04 | | L1 | PE2TP01 | | N3 | V _{SS} | | R5 | PE0RP06 | |
| H18 | PE4TP04 | | L2 | PE2TN01 | | N4 | V _{DD} CORE | | R6 | NC | |
| J1 | PE2TP02 | | L3 | V _{SS} | | N5 | V _{DD} CORE | | R7 | PE0RP05 | |
| J2 | PE2TN02 | | L4 | PE2RP01 | | N6 | V _{SS} | | R8 | PE0RP04 | |
| J3 | V _{SS} | | L5 | PE2RN01 | | N7 | V _{SS} | | R9 | V _{DD} CORE | |
| J4 | PE2RP02 | | L6 | V _{DD} PETA | | N8 | V _{DD} PEA | | R10 | PE0RP03 | |
| J5 | PE2RN02 | | L7 | V _{DD} PETA | | N9 | V _{DD} PEHA | | R11 | PE0RP02 | |
| J6 | V _{DD} PEHA | | L8 | V _{DD} PEA | | N10 | V _{DD} PETA | | R12 | V _{DD} CORE | |
| J7 | V _{DD} PEHA | | L9 | V _{DD} PEHA | | N11 | V _{DD} PEA | | R13 | PE0RP01 | |
| J8 | V _{DD} CORE | | L10 | V _{DD} PETA | | N12 | V _{DD} PEHA | | R14 | PE0RP00 | |
| J9 | V _{SS} | | L11 | V _{DD} PEA | | N13 | V _{SS} | | R15 | V _{DD} CORE | |
| J10 | V _{DD} CORE | | L12 | V _{DD} PEHA | | N14 | V _{SS} | | R16 | V _{DD} CORE | |
| J11 | V _{SS} | | L13 | V _{DD} PETA | | N15 | V _{DD} CORE | | R17 | V _{DD} CORE | |
| J12 | V _{DD} PEHA | | L14 | PE4RN06 | | N16 | V _{SS} | | R18 | V _{SS} | |
| J13 | V _{DD} PEHA | | L15 | PE4RP06 | | N17 | V _{SS} | | T1 | V _{SS} | |
| J14 | PE4RN05 | | L16 | V _{SS} | | N18 | V _{SS} | | T2 | V _{SS} | |
| J15 | PE4RP05 | | L17 | PE4TN06 | | P1 | V _{SS} | | T3 | V _{SS} | |
| J16 | V _{SS} | | L18 | PE4TP06 | | P2 | V _{DD} CORE | | T4 | V _{SS} | |
| J17 | PE4TN05 | | M1 | PE2TP00 | | P3 | V _{DD} CORE | | T5 | V _{SS} | |
| J18 | PE4TP05 | | M2 | PE2TN00 | | P4 | PE0RN07 | | T6 | V _{SS} | |
| K1 | REFRES2 | | M3 | V _{SS} | | P5 | PE0RN06 | | T7 | V _{SS} | |
| K2 | REFRES3 | | M4 | PE2RP00 | | P6 | V _{DD} CORE | | T8 | V _{SS} | |
| K3 | V _{SS} | | M5 | PE2RN00 | | P7 | PE0RN05 | | T9 | V _{SS} | |
| K4 | V _{DD} CORE | | M6 | V _{DD} PETA | | P8 | PE0RN04 | | T10 | V _{SS} | |
| K5 | V _{DD} CORE | | M7 | V _{DD} PETA | | P9 | V _{DD} CORE | | T11 | V _{SS} | |
| K6 | V _{DD} PETA | | M8 | V _{DD} PEA | | P10 | PE0RN03 | | T12 | V _{SS} | |
| K7 | V _{DD} PETA | | M9 | V _{DD} PEHA | | P11 | PE0RN02 | | T13 | V _{SS} | |
| K8 | V _{DD} CORE | | M10 | V _{DD} PETA | | P12 | V _{DD} CORE | | T14 | V _{SS} | |
| K9 | V _{SS} | | M11 | V _{DD} PEA | | P13 | PE0RN01 | | T15 | V _{SS} | |
| K10 | V _{DD} CORE | | M12 | V _{DD} PEHA | | P14 | PE0RN00 | | T16 | V _{SS} | |
| K11 | V _{SS} | | M13 | V _{SS} | | P15 | V _{DD} CORE | | T17 | V _{SS} | |
| K12 | V _{DD} PETA | | M14 | PE4RN07 | | P16 | V _{DD} CORE | | T18 | V _{SS} | |

Table 19 PES24T3G2 (19x19mm 324-pin) Signal Pin-Out (Part 2 of 3)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|-----------------|-----|-----|-----------------|-----|-----|-----------------|-----|-----|-----------------|-----|
| U1 | V _{SS} | | U10 | PE0TN03 | | V1 | V _{SS} | | V10 | PE0TP03 | |
| U2 | PEREFCLKN | | U11 | PE0TN02 | | V2 | PEREFCLKP | | V11 | PE0TP02 | |
| U3 | V _{SS} | | U12 | V _{SS} | | V3 | V _{SS} | | V12 | V _{SS} | |
| U4 | PE0TN07 | | U13 | PE0TN01 | | V4 | PE0TP07 | | V13 | PE0TP01 | |
| U5 | PE0TN06 | | U14 | PE0TN00 | | V5 | PE0TP06 | | V14 | PE0TP00 | |
| U6 | REFRES1 | | U15 | V _{SS} | | V6 | REFRES0 | | V15 | V _{SS} | |
| U7 | PE0TN05 | | U16 | V _{SS} | | V7 | PE0TP05 | | V16 | V _{SS} | |
| U8 | PE0TN04 | | U17 | V _{SS} | | V8 | PE0TP04 | | V17 | V _{SS} | |
| U9 | V _{SS} | | U18 | V _{SS} | | V9 | V _{SS} | | V18 | V _{SS} | |

Table 19 PES24T3G2 (19x19mm 324-pin) Signal Pin-Out (Part 3 of 3)

Option A Package Power Pins (19x19mm 324-Pin)

| V _{DD} Core | V _{DD} Core | V _{DD} Core | V _{DD} I/O | V _{DD} PEA | V _{DD} PEHA | V _{DD} PETA |
|----------------------|----------------------|----------------------|---------------------|---------------------|----------------------|----------------------|
| D4 | G9 | N15 | A2 | G6 | J6 | K6 |
| D5 | G10 | P2 | A6 | G7 | J7 | K7 |
| D14 | G14 | P3 | A10 | G12 | J12 | K12 |
| D15 | G15 | P6 | A13 | G13 | J13 | K13 |
| E6 | H8 | P9 | A14 | H6 | L9 | L6 |
| E7 | H9 | P12 | A17 | H7 | L12 | L7 |
| E8 | H10 | P15 | A18 | H12 | M9 | L10 |
| E10 | J8 | P16 | B6 | H13 | M12 | L13 |
| E11 | J10 | P17 | B10 | L8 | N9 | M6 |
| E12 | K4 | R2 | D6 | L11 | N12 | M7 |
| E13 | K5 | R3 | | M8 | | M10 |
| F8 | K8 | R9 | | M11 | | N10 |
| F10 | K10 | R12 | | N8 | | |
| G4 | K14 | R15 | | N11 | | |
| G5 | N4 | R16 | | | | |
| G8 | N5 | R17 | | | | |

Table 20 PES24T3G2 (19x19mm 324-Pin) Power Pins

Option A Package Ground Pins (19x19mm 324-Pin)

| V_{SS} | V_{SS} | V_{SS} | V_{SS} | V_{SS} | V_{SS} |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| A1 | D16 | G11 | M3 | T1 | T18 |
| A3 | D17 | G16 | M13 | T2 | U1 |
| A4 | D18 | G17 | M16 | T3 | U3 |
| A5 | E3 | G18 | N1 | T4 | U9 |
| A7 | E9 | H3 | N2 | T5 | U12 |
| A11 | E16 | H11 | N3 | T6 | U15 |
| A15 | F3 | H16 | N6 | T7 | U16 |
| A16 | F6 | J3 | N7 | T8 | U17 |
| B3 | F7 | J9 | N13 | T9 | U18 |
| B7 | F9 | J11 | N14 | T10 | V1 |
| B16 | F11 | J16 | N16 | T11 | V3 |
| C3 | F12 | K3 | N17 | T12 | V9 |
| C6 | F13 | K9 | N18 | T13 | V12 |
| C16 | F16 | K11 | P1 | T14 | V15 |
| D1 | G1 | K16 | P18 | T15 | V16 |
| D2 | G2 | L3 | R1 | T16 | V17 |
| D3 | G3 | L16 | R18 | T17 | V18 |

Table 21 PES24T3G2 (19x19mm 324-Pin) Ground Pins

Option A Package Alternate Signal Functions (19x19mm 324-Pin)

| Pin | GPIO | Alternate |
|------------|-------------|------------------|
| A12 | GPIO_00 | P2RSTN |
| B12 | GPIO_01 | P4RSTN |
| C12 | GPIO_02 | IOEXPINTN0 |
| D12 | GPIO_07 | GPEN |

Table 22 PES24T3G2 (19x19mm 324-Pin) Alternate Signal Functions

Option A Package Signals Listed Alphabetically (19x19mm 324-Pin)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|------------------------------|
| CCLKDS | I | C10 | System |
| CCLKUS | I | D9 | |
| GPIO_00 | I/O | A12 | General Purpose Input/Output |
| GPIO_01 | I/O | B12 | |
| GPIO_02 | I/O | C12 | |
| GPIO_07 | I/O | D12 | |
| GPIO_08 | I/O | D13 | |
| GPIO_09 | I/O | C13 | |
| GPIO_10 | I/O | B13 | |
| JTAG_TCK | I | C7 | |
| JTAG_TDI | I | A8 | |
| JTAG_TDO | O | D7 | |
| JTAG_TMS | I | B8 | |
| JTAG_TRST_N | I | C8 | |
| MSMBCLK | I/O | D8 | SMBus |
| MSMBDAT | I/O | A9 | |
| NO CONNECT | | K15, R6 | |
| PE0RN00 | I | P14 | PCI Express |
| PE0RN01 | I | P13 | |
| PE0RN02 | I | P11 | |
| PE0RN03 | I | P10 | |
| PE0RN04 | I | P8 | |
| PE0RN05 | I | P7 | |
| PE0RN06 | I | P5 | |
| PE0RN07 | I | P4 | |
| PE0RP00 | I | R14 | |
| PE0RP01 | I | R13 | |
| PE0RP02 | I | R11 | |
| PE0RP03 | I | R10 | |
| PE0RP04 | I | R8 | |
| PE0RP05 | I | R7 | |
| PE0RP06 | I | R5 | |
| PE0RP07 | I | R4 | |
| PE0TN00 | O | U14 | |

Table 23 PES24T3G2 (19x19mm 324-Pin) Alphabetical Signal List (Part 1 of 4)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|---------------------|
| PE0TN01 | O | U13 | PCI Express (cont.) |
| PE0TN02 | O | U11 | |
| PE0TN03 | O | U10 | |
| PE0TN04 | O | U8 | |
| PE0TN05 | O | U7 | |
| PE0TN06 | O | U5 | |
| PE0TN07 | O | U4 | |
| PE0TP00 | O | V14 | |
| PE0TP01 | O | V13 | |
| PE0TP02 | O | V11 | |
| PE0TP03 | O | V10 | |
| PE0TP04 | O | V8 | |
| PE0TP05 | O | V7 | |
| PE0TP06 | O | V5 | |
| PE0TP07 | O | V4 | |
| PE2RN00 | I | M5 | |
| PE2RN01 | I | L5 | |
| PE2RN02 | I | J5 | |
| PE2RN03 | I | H5 | |
| PE2RN04 | I | F5 | |
| PE2RN05 | I | E5 | |
| PE2RN06 | I | C5 | |
| PE2RN07 | I | B5 | |
| PE2RP00 | I | M4 | |
| PE2RP01 | I | L4 | |
| PE2RP02 | I | J4 | |
| PE2RP03 | I | H4 | |
| PE2RP04 | I | F4 | |
| PE2RP05 | I | E4 | |
| PE2RP06 | I | C4 | |
| PE2RP07 | I | B4 | |
| PE2TN00 | O | M2 | |
| PE2TN01 | O | L2 | |
| PE2TN02 | O | J2 | |
| PE2TN03 | O | H2 | |
| PE2TN04 | O | F2 | |

Table 23 PES24T3G2 (19x19mm 324-Pin) Alphabetical Signal List (Part 2 of 4)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|---------------------|
| PE2TN05 | O | E2 | PCI Express (cont.) |
| PE2TN06 | O | C2 | |
| PE2TN07 | O | B2 | |
| PE2TP00 | O | M1 | |
| PE2TP01 | O | L1 | |
| PE2TP02 | O | J1 | |
| PE2TP03 | O | H1 | |
| PE2TP04 | O | F1 | |
| PE2TP05 | O | E1 | |
| PE2TP06 | O | C1 | |
| PE2TP07 | O | B1 | |
| PE4RN00 | I | B14 | |
| PE4RN01 | I | C14 | |
| PE4RN02 | I | E14 | |
| PE4RN03 | I | F14 | |
| PE4RN04 | I | H14 | |
| PE4RN05 | I | J14 | |
| PE4RN06 | I | L14 | |
| PE4RN07 | I | M14 | |
| PE4RP00 | I | B15 | |
| PE4RP01 | I | C15 | |
| PE4RP02 | I | E15 | |
| PE4RP03 | I | F15 | |
| PE4RP04 | I | H15 | |
| PE4RP05 | I | J15 | |
| PE4RP06 | I | L15 | |
| PE4RP07 | I | M15 | |
| PE4TN00 | O | B17 | |
| PE4TN01 | O | C17 | |
| PE4TN02 | O | E17 | |
| PE4TN03 | O | F17 | |
| PE4TN04 | O | H17 | |
| PE4TN05 | O | J17 | |
| PE4TN06 | O | L17 | |
| PE4TN07 | O | M17 | |
| PE4TP00 | O | B18 | |

Table 23 PES24T3G2 (19x19mm 324-Pin) Alphabetical Signal List (Part 3 of 4)

| Signal Name | I/O Type | Location | Signal Category |
|--|--|----------|----------------------------|
| PE4TP01 | O | C18 | PCI Express (cont.) |
| PE4TP02 | O | E18 | |
| PE4TP03 | O | F18 | |
| PE4TP04 | O | H18 | |
| PE4TP05 | O | J18 | |
| PE4TP06 | O | L18 | |
| PE4TP07 | O | M18 | |
| PEREFCLKN | I | U2 | |
| PEREFCLKP | I | V2 | |
| PERSTN | I | D11 | System |
| REFRES0 | I/O | V6 | SerDes Reference Resistors |
| REFRES1 | I/O | U6 | |
| REFRES2 | I/O | K1 | |
| REFRES3 | I/O | K2 | |
| REFRES4 | I/O | K18 | |
| REFRES5 | I/O | K17 | |
| SSMBCLK | I/O | B9 | SMBus |
| SSMBDAT | I/O | C9 | |
| SWMODE_0 | I | D10 | System |
| SWMODE_1 | I | B11 | |
| SWMODE_2 | I | C11 | |
| V _{DD} CORE, V _{DD} I/O, V _{DD} PEA, V _{DD} PEHA, V _{DD} PETA | See Table 20 for a listing of power pins. | | |
| V _{SS} | See Table 21 for a listing of ground pins. | | |

Table 23 PES24T3G2 (19x19mm 324-Pin) Alphabetical Signal List (Part 4 of 4)

Option A Package Pinout — Top View

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |
| A | | | | | | | | | | | | | | | | | | | A |
| B | | | | | | | | | | | | | | | | | | | B |
| C | | | | | | | | | | | | | | | | | | | C |
| D | | | | | | | | | | | | | | | | | | | D |
| E | | | | | | | | | | | | | | | | | | | E |
| F | | | | | | | | | | | | | | | | | | | F |
| G | | | | | | | | | | | | | | | | | | | G |
| H | | | | | | | | | | | | | | | | | | | H |
| J | | | | | | | | | | | | | | | | | | | J |
| K | | | | | | | | | | | | | | | | | | | K |
| L | | | | | | | | | | | | | | | | | | | L |
| M | | | | | | | | | | | | | | | | | | | M |
| N | | | | | | | | | | | | | | | | | | | N |
| P | | | | | | | | | | | | | | | | | | | P |
| R | | | | | | | | | | | | | | | | | | | R |
| T | | | | | | | | | | | | | | | | | | | T |
| U | | | | | | | | | | | | | | | | | | | U |
| V | | | | | | | | | | | | | | | | | | | V |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | |

| | | | | | | | |
|--|------------------------------|--|------------------------------|--|--------------------------|--|---------|
| | V _{DD} Core (Power) | | V _{DD} PETA (Power) | | V _{SS} (Ground) | | Signals |
| | V _{DD} I/O (Power) | | V _{DD} PEA (Power) | | No Connect | | |
| | | | V _{DD} PEHA (Power) | | | | |

19x19mm Package Drawing — Page Two

| REVISIONS | | DATE | APPROVED |
|-----------|-----------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/10/07 | |

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- 2 "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
- 3 "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
- 4 "N" REPRESENTS THE BALLCOUNT NUMBER

△ DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

△ SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

△ "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY

△ EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 ALL DIMENSIONS ARE IN MILLIMETERS

| SYMBOL | JEDEC VARIATION | | | NOTE |
|--------------------|-----------------|-----|------|------|
| | MIN | NOM | MAX | |
| A | — | — | 3.42 | |
| A1 | .30 | — | — | |
| A2 | 2.16 | — | 2.82 | |
| D | 19.00 BSC | | | |
| E | 19.00 BSC | | | |
| M | 18 | | | 3 |
| N | 324 | | | 4 |
| e | 1.00 BSC | | | |
| b | .50 | .60 | .70 | 5 |
| CENTER BALL MATRIX | N/A | | | |

BOTTOM VIEW
(BALL SIDE VIEW)

| | | | |
|---|-----------------------|-------------------------|---------------------------------|
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR | 2975 Skender Way | IDT™ | 2975 Skender Way |
| XXX.X | Santa Clara, CA 95054 | | Santa Clara, CA 95054 |
| XXX.X | PHONE: (408) 727-6116 | WWW.IDT.COM | PHONE: (408) 727-6116 |
| XXX.X | FAX: (408) 492-8674 | | FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | BU/BR/AL/AR 324 PACKAGE OUTLINE |
| DRAWN | 07/18/10/07 | 19.0 X 19.0 mm BODY | |
| CHECKED | | 1.00 mm BALLPITCH FCBCA | |
| | | SIZE | C |
| | | DRAWING No. | PSC-4211 |
| | | REV | 00 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

Option B Package Pinout, 27x27mm 676-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES24T3G2 device.

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|---------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| A1 | V _{SS} | | B9 | MSMBDAT | | C17 | V _{DD} I/O | | D25 | V _{SS} | |
| A2 | V _{SS} | | B10 | SSMBADDR_2 | | C18 | V _{SS} | | D26 | NC | |
| A3 | V _{SS} | | B11 | SSMBADDR_5 | | C19 | V _{DD} I/O | | E1 | V _{SS} | |
| A4 | JTAG_TDI | | B12 | SSMBDAT | | C20 | V _{SS} | | E2 | V _{SS} | |
| A5 | JTAG_TMS | | B13 | V _{SS} | | C21 | V _{DD} I/O | | E3 | V _{SS} | |
| A6 | MSMBADDR_1 | | B14 | SWMODE_0 | | C22 | GPIO_10 | | E4 | V _{SS} | |
| A7 | MSMBADDR_3 | | B15 | SWMODE_2 | | C23 | V _{DD} I/O | | E5 | V _{SS} | |
| A8 | MSMBCLK | | B16 | V _{SS} | | C24 | V _{SS} | | E6 | V _{DD} CORE | |
| A9 | SSMBADDR_1 | | B17 | V _{DD} I/O | | C25 | V _{SS} | | E7 | V _{DD} CORE | |
| A10 | SSMBADDR_3 | | B18 | GPIO_00 | 1 | C26 | NC | | E8 | V _{SS} | |
| A11 | SSMBCLK | | B19 | GPIO_02 | 1 | D1 | PEREFCLKP | | E9 | V _{DD} CORE | |
| A12 | CCLKUS | | B20 | GPIO_04 | 1 | D2 | V _{SS} | | E10 | V _{SS} | |
| A13 | CCLKDS | | B21 | GPIO_06 | | D3 | V _{SS} | | E11 | V _{DD} CORE | |
| A14 | V _{SS} | | B22 | MSMBSMODE | | D4 | V _{SS} | | E12 | V _{SS} | |
| A15 | SWMODE_1 | | B23 | REFCLKM | | D5 | V _{DD} CORE | | E13 | V _{DD} CORE | |
| A16 | NC | | B24 | V _{DD} I/O | | D6 | V _{DD} CORE | | E14 | V _{SS} | |
| A17 | PERSTN | | B25 | V _{SS} | | D7 | V _{SS} | | E15 | V _{DD} CORE | |
| A18 | RSTHALT | | B26 | V _{SS} | | D8 | V _{DD} CORE | | E16 | V _{SS} | |
| A19 | GPIO_01 | 1 | C1 | PEREFCLKN | | D9 | V _{SS} | | E17 | V _{DD} CORE | |
| A20 | GPIO_03 | 1 | C2 | V _{SS} | | D10 | V _{DD} CORE | | E18 | V _{SS} | |
| A21 | GPIO_05 | | C3 | V _{SS} | | D11 | V _{SS} | | E19 | V _{DD} CORE | |
| A22 | GPIO_07 | 1 | C4 | V _{DD} CORE | | D12 | V _{DD} CORE | | E20 | V _{DD} CORE | |
| A23 | V _{SS} | | C5 | V _{DD} I/O | | D13 | V _{DD} CORE | | E21 | V _{DD} CORE | |
| A24 | GPIO_09 | | C6 | V _{SS} | | D14 | V _{SS} | | E22 | V _{SS} | |
| A25 | V _{SS} | | C7 | V _{DD} I/O | | D15 | V _{DD} CORE | | E23 | V _{SS} | |
| A26 | V _{SS} | | C8 | V _{SS} | | D16 | V _{SS} | | E24 | V _{SS} | |
| B1 | V _{SS} | | C9 | V _{DD} I/O | | D17 | V _{DD} CORE | | E25 | V _{SS} | |
| B2 | V _{SS} | | C10 | V _{SS} | | D18 | V _{DD} CORE | | E26 | V _{SS} | |
| B3 | V _{DD} I/O | | C11 | V _{DD} I/O | | D19 | V _{DD} CORE | | F1 | V _{DD} CORE | |
| B4 | JTAG_TCK | | C12 | V _{SS} | | D20 | V _{SS} | | F2 | V _{DD} CORE | |
| B5 | JTAG-TDO | | C13 | V _{DD} I/O | | D21 | V _{DD} CORE | | F3 | V _{DD} PEA | |
| B6 | JTAG-TRST_N | | C14 | V _{DD} CORE | | D22 | V _{DD} CORE | | F4 | V _{SS} | |
| B7 | MSMBADDR_2 | | C15 | V _{DD} I/O | | D23 | GPIO_08 | | F5 | V _{SS} | |
| B8 | MSMBADDR_4 | | C16 | V _{DD} CORE | | D24 | V _{SS} | | F6 | V _{DD} I/O | |

Table 24 PES24T3G2 (27x27mm 676-Pin) Signal Pin-Out (Part 1 of 5)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| F7 | V _{SS} | | G18 | V _{SS} | | J3 | V _{DD} PETA | | K14 | V _{SS} | |
| F8 | V _{SS} | | G19 | V _{SS} | | J4 | PE2RN06 | | K15 | V _{DD} CORE | |
| F9 | V _{SS} | | G20 | V _{SS} | | J5 | PE2RP06 | | K16 | V _{DD} CORE | |
| F10 | V _{SS} | | G21 | V _{SS} | | J6 | V _{SS} | | K17 | V _{SS} | |
| F11 | V _{SS} | | G22 | PE4RP00 | | J7 | V _{DD} CORE | | K18 | V _{SS} | |
| F12 | NC | | G23 | PE4RN00 | | J8 | V _{DD} CORE | | K19 | V _{DD} CORE | |
| F13 | V _{SS} | | G24 | V _{DD} PETA | | J9 | V _{SS} | | K20 | V _{DD} CORE | |
| F14 | V _{SS} | | G25 | PE4TP00 | | J10 | V _{SS} | | K21 | V _{SS} | |
| F15 | V _{SS} | | G26 | PE4TN00 | | J11 | V _{DD} CORE | | K22 | V _{DD} PEA | |
| F16 | NC | | H1 | V _{SS} | | J12 | V _{DD} CORE | | K23 | V _{DD} PEA | |
| F17 | V _{SS} | | H2 | V _{SS} | | J13 | V _{SS} | | K24 | V _{DD} PEA | |
| F18 | V _{SS} | | H3 | V _{DD} PEHA | | J14 | V _{SS} | | K25 | V _{SS} | |
| F19 | V _{SS} | | H4 | V _{DD} PEHA | | J15 | V _{DD} CORE | | K26 | REFRES4 | |
| F20 | V _{SS} | | H5 | V _{SS} | | J16 | V _{DD} CORE | | L1 | PE2TN05 | |
| F21 | V _{SS} | | H6 | V _{SS} | | J17 | V _{SS} | | L2 | PE2TP05 | |
| F22 | V _{SS} | | H7 | V _{DD} CORE | | J18 | V _{SS} | | L3 | V _{DD} PETA | |
| F23 | V _{SS} | | H8 | V _{DD} CORE | | J19 | V _{DD} CORE | | L4 | PE2RN05 | |
| F24 | V _{DD} PEA | | H9 | V _{SS} | | J20 | V _{DD} CORE | | L5 | PE2RP05 | |
| F25 | V _{DD} CORE | | H10 | V _{SS} | | J21 | V _{SS} | | L6 | V _{SS} | |
| F26 | V _{DD} CORE | | H11 | V _{DD} CORE | | J22 | PE4RP01 | | L7 | V _{DD} CORE | |
| G1 | PE2TN07 | | H12 | V _{DD} CORE | | J23 | PE4RN01 | | L8 | V _{DD} CORE | |
| G2 | PE2TP07 | | H13 | V _{SS} | | J24 | V _{DD} PETA | | L9 | V _{SS} | |
| G3 | V _{DD} PETA | | H14 | V _{SS} | | J25 | PE4TP01 | | L10 | V _{SS} | |
| G4 | PE2RN07 | | H15 | V _{DD} CORE | | J26 | PE4TN01 | | L11 | V _{DD} CORE | |
| G5 | PE2RP07 | | H16 | V _{DD} CORE | | K1 | REFRES3 | | L12 | V _{DD} CORE | |
| G6 | V _{SS} | | H17 | V _{SS} | | K2 | V _{SS} | | L13 | V _{SS} | |
| G7 | V _{SS} | | H18 | V _{SS} | | K3 | V _{DD} PEA | | L14 | V _{SS} | |
| G8 | V _{SS} | | H19 | V _{DD} CORE | | K4 | V _{DD} PEA | | L15 | V _{DD} CORE | |
| G9 | V _{SS} | | H20 | V _{DD} CORE | | K5 | V _{DD} PEA | | L16 | V _{DD} CORE | |
| G10 | V _{SS} | | H21 | V _{SS} | | K6 | V _{SS} | | L17 | V _{SS} | |
| G11 | V _{SS} | | H22 | V _{SS} | | K7 | V _{DD} CORE | | L18 | V _{SS} | |
| G12 | V _{SS} | | H23 | V _{DD} PEHA | | K8 | V _{DD} CORE | | L19 | V _{DD} CORE | |
| G13 | V _{SS} | | H24 | V _{DD} PEHA | | K9 | V _{SS} | | L20 | V _{DD} CORE | |
| G14 | V _{SS} | | H25 | V _{SS} | | K10 | V _{SS} | | L21 | V _{SS} | |
| G15 | V _{SS} | | H26 | V _{SS} | | K11 | V _{DD} CORE | | L22 | PE4RP02 | |
| G16 | V _{SS} | | J1 | PE2TN06 | | K12 | V _{DD} CORE | | L23 | PE4RN02 | |
| G17 | V _{SS} | | J2 | PE2TP06 | | K13 | V _{SS} | | L24 | V _{DD} PETA | |

Table 24 PES24T3G2 (27x27mm 676-Pin) Signal Pin-Out (Part 2 of 5)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| L25 | PE4TP02 | | N10 | V _{SS} | | P21 | V _{SS} | | T6 | NC | |
| L26 | PE4TN02 | | N11 | V _{DD} CORE | | P22 | V _{SS} | | T7 | V _{DD} CORE | |
| M1 | V _{DD} CORE | | N12 | V _{DD} CORE | | P23 | V _{DD} PEHA | | T8 | V _{DD} CORE | |
| M2 | V _{SS} | | N13 | V _{SS} | | P24 | V _{DD} PEHA | | T9 | V _{SS} | |
| M3 | V _{DD} PEHA | | N14 | V _{SS} | | P25 | V _{SS} | | T10 | V _{SS} | |
| M4 | V _{DD} PEHA | | N15 | V _{DD} CORE | | P26 | V _{DD} CORE | | T11 | V _{DD} CORE | |
| M5 | V _{SS} | | N16 | V _{DD} CORE | | R1 | PE2TN03 | | T12 | V _{DD} CORE | |
| M6 | NC | | N17 | V _{SS} | | R2 | PE2TP03 | | T13 | V _{SS} | |
| M7 | V _{DD} CORE | | N18 | V _{SS} | | R3 | V _{DD} PETA | | T14 | V _{SS} | |
| M8 | V _{DD} CORE | | N19 | V _{DD} CORE | | R4 | PE2RN03 | | T15 | V _{DD} CORE | |
| M9 | V _{SS} | | N20 | V _{DD} CORE | | R5 | PE2RP03 | | T16 | V _{DD} CORE | |
| M10 | V _{SS} | | N21 | V _{SS} | | R6 | V _{SS} | | T17 | V _{SS} | |
| M11 | V _{DD} CORE | | N22 | PE4RP03 | | R7 | V _{DD} CORE | | T18 | V _{SS} | |
| M12 | V _{DD} CORE | | N23 | PE4RN03 | | R8 | V _{DD} CORE | | T19 | V _{DD} CORE | |
| M13 | V _{SS} | | N24 | V _{DD} PETA | | R9 | V _{SS} | | T20 | V _{DD} CORE | |
| M14 | V _{SS} | | N25 | PE4TP03 | | R10 | V _{SS} | | T21 | NC | |
| M15 | V _{DD} CORE | | N26 | PE4TN03 | | R11 | V _{DD} CORE | | T22 | V _{SS} | |
| M16 | V _{DD} CORE | | P1 | V _{DD} CORE | | R12 | V _{DD} CORE | | T23 | V _{DD} PEA | |
| M17 | V _{SS} | | P2 | V _{SS} | | R13 | V _{SS} | | T24 | V _{DD} PEA | |
| M18 | V _{SS} | | P3 | V _{DD} PEHA | | R14 | V _{SS} | | T25 | V _{SS} | |
| M19 | V _{DD} CORE | | P4 | V _{DD} PEHA | | R15 | V _{DD} CORE | | T26 | V _{DD} CORE | |
| M20 | V _{DD} CORE | | P5 | V _{SS} | | R16 | V _{DD} CORE | | U1 | PE2TN02 | |
| M21 | NC | | P6 | V _{SS} | | R17 | V _{SS} | | U2 | PE2TP02 | |
| M22 | V _{SS} | | P7 | V _{DD} CORE | | R18 | V _{SS} | | U3 | V _{DD} PETA | |
| M23 | V _{DD} PEHA | | P8 | V _{DD} CORE | | R19 | V _{DD} CORE | | U4 | PE2RN02 | |
| M24 | V _{DD} PEHA | | P9 | V _{SS} | | R20 | V _{DD} CORE | | U5 | PE2RP02 | |
| M25 | V _{SS} | | P10 | V _{SS} | | R21 | V _{SS} | | U6 | V _{SS} | |
| M26 | V _{DD} CORE | | P11 | V _{DD} CORE | | R22 | PE4RP04 | | U7 | V _{DD} CORE | |
| N1 | PE2TN04 | | P12 | V _{DD} CORE | | R23 | PE4RN04 | | U8 | V _{DD} CORE | |
| N2 | PE2TP04 | | P13 | V _{SS} | | R24 | V _{DD} PETA | | U9 | V _{SS} | |
| N3 | V _{DD} PETA | | P14 | V _{SS} | | R25 | PE4TP04 | | U10 | V _{SS} | |
| N4 | PE2RN04 | | P15 | V _{DD} CORE | | R26 | PE4TN04 | | U11 | V _{DD} CORE | |
| N5 | PE2RP04 | | P16 | V _{DD} CORE | | T1 | V _{DD} CORE | | U12 | V _{DD} CORE | |
| N6 | V _{SS} | | P17 | V _{SS} | | T2 | V _{SS} | | U13 | V _{SS} | |
| N7 | V _{DD} CORE | | P18 | V _{SS} | | T3 | V _{DD} PEA | | U14 | V _{SS} | |
| N8 | V _{DD} CORE | | P19 | V _{DD} CORE | | T4 | V _{DD} PEA | | U15 | V _{DD} CORE | |
| N9 | V _{SS} | | P20 | V _{DD} CORE | | T5 | V _{SS} | | U16 | V _{DD} CORE | |

Table 24 PES24T3G2 (27x27mm 676-Pin) Signal Pin-Out (Part 3 of 5)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|----------------------|-----|-----|----------------------|-----|------|----------------------|-----|------|----------------------|-----|
| U17 | V _{SS} | | W2 | PE2TP01 | | Y13 | V _{SS} | | AA24 | V _{DD} PETA | |
| U18 | V _{SS} | | W3 | V _{DD} PETA | | Y14 | V _{SS} | | AA25 | PE4TP07 | |
| U19 | V _{DD} CORE | | W4 | PE2RN01 | | Y15 | V _{DD} CORE | | AA26 | PE4TN07 | |
| U20 | V _{DD} CORE | | W5 | PE2RP01 | | Y16 | V _{DD} CORE | | AB1 | V _{SS} | |
| U21 | V _{SS} | | W6 | V _{SS} | | Y17 | V _{SS} | | AB2 | V _{SS} | |
| U22 | PE4RP05 | | W7 | V _{DD} CORE | | Y18 | V _{SS} | | AB3 | V _{DD} CORE | |
| U23 | PE4RN05 | | W8 | V _{DD} CORE | | Y19 | V _{DD} CORE | | AB4 | V _{DD} CORE | |
| U24 | V _{DD} PETA | | W9 | V _{SS} | | Y20 | V _{DD} CORE | | AB5 | V _{DD} CORE | |
| U25 | PE4TP05 | | W10 | V _{SS} | | Y21 | V _{SS} | | AB6 | V _{SS} | |
| U26 | PE4TN05 | | W11 | V _{DD} CORE | | Y22 | V _{SS} | | AB7 | PE0RP07 | |
| V1 | V _{DD} CORE | | W12 | V _{DD} CORE | | Y23 | V _{DD} PEHA | | AB8 | V _{SS} | |
| V2 | V _{SS} | | W13 | V _{SS} | | Y24 | V _{DD} PEHA | | AB9 | PE0RP06 | |
| V3 | V _{DD} PEA | | W14 | V _{SS} | | Y25 | V _{SS} | | AB10 | V _{DD} PEA | |
| V4 | V _{DD} PEA | | W15 | V _{DD} CORE | | Y26 | REFRES5 | | AB11 | PE0RP05 | |
| V5 | V _{DD} PEA | | W16 | V _{DD} CORE | | AA1 | PE2TN00 | | AB12 | V _{SS} | |
| V6 | V _{SS} | | W17 | V _{SS} | | AA2 | PE2TP00 | | AB13 | PE0RP04 | |
| V7 | V _{DD} CORE | | W18 | V _{SS} | | AA3 | V _{DD} PETA | | AB14 | V _{DD} PEA | |
| V8 | V _{DD} CORE | | W19 | V _{DD} CORE | | AA4 | PE2RN00 | | AB15 | PE0RP03 | |
| V9 | V _{SS} | | W20 | V _{DD} CORE | | AA5 | PE2RP00 | | AB16 | V _{SS} | |
| V10 | V _{SS} | | W21 | V _{SS} | | AA6 | V _{SS} | | AB17 | PE0RP02 | |
| V11 | V _{DD} CORE | | W22 | PE4RP06 | | AA7 | V _{SS} | | AB18 | V _{DD} PEA | |
| V12 | V _{DD} CORE | | W23 | PE4RN06 | | AA8 | V _{SS} | | AB19 | PE0RP01 | |
| V13 | V _{SS} | | W24 | V _{DD} PETA | | AA9 | V _{SS} | | AB20 | V _{SS} | |
| V14 | V _{SS} | | W25 | PE4TP06 | | AA10 | V _{SS} | | AB21 | PE0RP00 | |
| V15 | V _{DD} CORE | | W26 | PE4TN06 | | AA11 | V _{SS} | | AB22 | V _{SS} | |
| V16 | V _{DD} CORE | | Y1 | REFRES2 | | AA12 | NC | | AB23 | V _{DD} CORE | |
| V17 | V _{SS} | | Y2 | V _{SS} | | AA13 | V _{SS} | | AB24 | V _{DD} CORE | |
| V18 | V _{SS} | | Y3 | V _{DD} PEHA | | AA14 | V _{SS} | | AB25 | V _{SS} | |
| V19 | V _{DD} CORE | | Y4 | V _{DD} PEHA | | AA15 | V _{SS} | | AB26 | V _{SS} | |
| V20 | V _{DD} CORE | | Y5 | V _{SS} | | AA16 | NC | | AC1 | V _{SS} | |
| V21 | V _{SS} | | Y6 | V _{SS} | | AA17 | V _{SS} | | AC2 | V _{SS} | |
| V22 | V _{DD} PEA | | Y7 | V _{DD} CORE | | AA18 | V _{SS} | | AC3 | V _{DD} CORE | |
| V23 | V _{DD} PEA | | Y8 | V _{DD} CORE | | AA19 | V _{SS} | | AC4 | V _{DD} CORE | |
| V24 | V _{DD} PEA | | Y9 | V _{SS} | | AA20 | V _{SS} | | AC5 | V _{DD} CORE | |
| V25 | V _{SS} | | Y10 | V _{SS} | | AA21 | V _{SS} | | AC6 | V _{DD} PEHA | |
| V26 | V _{DD} CORE | | Y11 | V _{DD} CORE | | AA22 | PE4RP07 | | AC7 | PE0RN07 | |
| W1 | PE2TN01 | | Y12 | V _{DD} CORE | | AA23 | PE4RN07 | | AC8 | V _{DD} PEA | |

Table 24 PES24T3G2 (27x27mm 676-Pin) Signal Pin-Out (Part 4 of 5)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|------|----------------------|-----|------|----------------------|-----|------|----------------------|-----|------|----------------------|-----|
| AC9 | PE0RN06 | | AD7 | V _{SS} | | AE5 | V _{SS} | | AF3 | V _{DD} CORE | |
| AC10 | V _{DD} PEA | | AD8 | V _{DD} PETA | | AE6 | V _{SS} | | AF4 | V _{DD} CORE | |
| AC11 | PE0RN05 | | AD9 | V _{SS} | | AE7 | PE0TP07 | | AF5 | V _{DD} CORE | |
| AC12 | V _{DD} PEHA | | AD10 | V _{DD} PETA | | AE8 | V _{SS} | | AF6 | V _{SS} | |
| AC13 | PE0RN04 | | AD11 | V _{DD} PETA | | AE9 | PE0TP06 | | AF7 | PE0TN07 | |
| AC14 | V _{DD} PEHA | | AD12 | V _{DD} PEHA | | AE10 | V _{SS} | | AF8 | REFRES1 | |
| AC15 | PE0RN03 | | AD13 | V _{DD} PETA | | AE11 | PE0TP05 | | AF9 | PE0TN06 | |
| AC16 | V _{DD} PEA | | AD14 | V _{DD} PEHA | | AE12 | V _{SS} | | AF10 | V _{DD} CORE | |
| AC17 | PE0RN02 | | AD15 | V _{DD} PETA | | AE13 | PE0TP04 | | AF11 | PE0TN05 | |
| AC18 | V _{DD} PEA | | AD16 | V _{DD} PEA | | AE14 | V _{SS} | | AF12 | V _{DD} CORE | |
| AC19 | PE0RN01 | | AD17 | V _{SS} | | AE15 | PE0TP03 | | AF13 | PE0TN04 | |
| AC20 | V _{DD} PEHA | | AD18 | V _{DD} PETA | | AE16 | V _{SS} | | AF14 | V _{DD} CORE | |
| AC21 | PE0RN00 | | AD19 | V _{DD} PETA | | AE17 | PE0TP02 | | AF15 | PE0TN03 | |
| AC22 | V _{SS} | | AD20 | V _{DD} PEHA | | AE18 | V _{SS} | | AF16 | V _{DD} CORE | |
| AC23 | V _{DD} CORE | | AD21 | V _{DD} PETA | | AE19 | PE0TP01 | | AF17 | PE0TN02 | |
| AC24 | V _{DD} CORE | | AD22 | V _{SS} | | AE20 | V _{SS} | | AF18 | REFRES0 | |
| AC25 | V _{SS} | | AD23 | V _{DD} CORE | | AE21 | PE0TP00 | | AF19 | PE0TN01 | |
| AC26 | V _{SS} | | AD24 | V _{DD} CORE | | AE22 | V _{SS} | | AF20 | V _{SS} | |
| AD1 | V _{SS} | | AD25 | V _{SS} | | AE23 | V _{DD} CORE | | AF21 | PE0TN00 | |
| AD2 | V _{SS} | | AD26 | V _{SS} | | AE24 | V _{DD} CORE | | AF22 | V _{SS} | |
| AD3 | V _{DD} CORE | | AE1 | V _{SS} | | AE25 | V _{SS} | | AF23 | V _{DD} CORE | |
| AD4 | V _{DD} CORE | | AE2 | V _{SS} | | AE26 | V _{SS} | | AF24 | V _{DD} CORE | |
| AD5 | V _{DD} CORE | | AE3 | V _{DD} CORE | | AF1 | V _{SS} | | AF25 | V _{SS} | |
| AD6 | V _{DD} PEHA | | AE4 | V _{DD} CORE | | AF2 | V _{SS} | | AF26 | V _{SS} | |

Table 24 PES24T3G2 (27x27mm 676-Pin) Signal Pin-Out (Part 5 of 5)

Option B Package Core Power Pins (27x27mm 676-Pin Package)

| V_{DD}Core | V_{DD}Core | V_{DD}Core | V_{DD}Core | V_{DD}Core | V_{DD}Core |
|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| C4 | H7 | L16 | P20 | V7 | AB24 |
| C14 | H8 | L19 | P26 | V8 | AC3 |
| C16 | H11 | L20 | R7 | V11 | AC4 |
| D5 | H12 | M1 | R8 | V12 | AC5 |
| D6 | H15 | M7 | R11 | V15 | AC23 |
| D8 | H16 | M8 | R12 | V16 | AC24 |
| D10 | H19 | M11 | R15 | V19 | AD3 |
| D12 | H20 | M12 | R16 | V20 | AD4 |
| D13 | J7 | M15 | R19 | V26 | AD5 |
| D15 | J8 | M16 | R20 | W7 | AD23 |
| D17 | J11 | M19 | T1 | W8 | AD24 |
| D18 | J12 | M20 | T7 | W11 | AE3 |
| D19 | J15 | M26 | T8 | W12 | AE4 |
| D21 | J16 | N7 | T11 | W15 | AE23 |
| D22 | J19 | N8 | T12 | W16 | AE24 |
| E6 | J20 | N11 | T15 | W19 | AF3 |
| E7 | K7 | N12 | T16 | W20 | AF4 |
| E9 | K8 | N15 | T19 | Y7 | AF5 |
| E11 | K11 | N16 | T20 | Y8 | AF10 |
| E13 | K12 | N19 | T26 | Y11 | AF12 |
| E15 | K15 | N20 | U7 | Y12 | AF14 |
| E17 | K16 | P1 | U8 | Y15 | AF16 |
| E19 | K19 | P7 | U11 | Y16 | AF23 |
| E20 | K20 | P8 | U12 | Y19 | AF24 |
| E21 | L7 | P11 | U15 | Y20 | |
| F1 | L8 | P12 | U16 | AB3 | |
| F2 | L11 | P15 | U19 | AB4 | |
| F25 | L12 | P16 | U20 | AB5 | |
| F26 | L15 | P19 | V1 | AB23 | |

Table 25 PES24T3G2 (27x27mm 676-Pin) Core Power Pins

Option B Package I/O, PCIe, and Transmitter Power Pins (27x27mm 676-Pin)

| V_{DD}I/O | V_{DD}PEA | V_{DD}PEHA | V_{DD}PETA |
|--------------------------|--------------------------|---------------------------|---------------------------|
| B3 | F3 | H3 | G3 |
| B17 | F24 | H4 | G24 |
| B24 | K3 | H23 | J3 |
| C5 | K4 | H24 | J24 |
| C7 | K5 | M3 | L3 |
| C9 | K22 | M4 | L24 |
| C11 | K23 | M23 | N3 |
| C13 | K24 | M24 | N24 |
| C15 | T3 | P3 | R3 |
| C17 | T4 | P4 | R24 |
| C19 | T23 | P23 | U3 |
| C21 | T24 | P24 | U24 |
| C23 | V3 | Y3 | W3 |
| F6 | V4 | Y4 | W24 |
| | V5 | Y23 | AA3 |
| | V22 | Y24 | AA24 |
| | V23 | AC6 | AD8 |
| | V24 | AC12 | AD10 |
| | AB10 | AC14 | AD11 |
| | AB14 | AC20 | AD13 |
| | AB18 | AD6 | AD15 |
| | AC8 | AD12 | AD18 |
| | AC10 | AD14 | AD19 |
| | AC16 | AD20 | AD21 |
| | AC18 | | |
| | AD16 | | |

Table 26 PES24T3G2 (27x27mm 676-Pin) I/O, PCIe, Transmitter Power Pins

Option B Package Ground Pins (27x27mm 676-Pin)

| V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| A1 | E1 | G7 | J17 | N13 | T25 | Y17 | AD1 |
| A2 | E2 | G8 | J18 | N14 | U6 | Y18 | AD2 |
| A3 | E3 | G9 | J21 | N17 | U9 | Y21 | AD7 |
| A14 | E4 | G10 | K2 | N18 | U10 | Y22 | AD9 |
| A23 | E5 | G11 | K6 | N21 | U13 | Y25 | AD17 |
| A25 | E8 | G12 | K9 | P2 | U14 | AA6 | AD22 |
| A26 | E10 | G13 | K10 | P5 | U17 | AA7 | AD25 |
| B1 | E12 | G14 | K13 | P6 | U18 | AA8 | AD26 |
| B2 | E14 | G15 | K14 | P9 | U21 | AA9 | AE1 |
| B13 | E16 | G16 | K17 | P10 | V2 | AA10 | AE2 |
| B16 | E18 | G17 | K18 | P13 | V6 | AA11 | AE5 |
| B25 | E22 | G18 | K21 | P14 | V9 | AA13 | AE6 |
| B26 | E23 | G19 | K25 | P17 | V10 | AA14 | AE8 |
| C2 | E24 | G20 | L6 | P18 | V13 | AA15 | AE10 |
| C3 | E25 | G21 | L9 | P21 | V14 | AA17 | AE12 |
| C6 | E26 | H1 | L10 | P22 | V17 | AA18 | AE14 |
| C8 | F4 | H2 | L13 | P25 | V18 | AA19 | AE16 |
| C10 | F5 | H5 | L14 | R6 | V21 | AA20 | AE18 |
| C12 | F7 | H6 | L17 | R9 | V25 | AA21 | AE20 |
| C18 | F8 | H9 | L18 | R10 | W6 | AB1 | AE22 |
| C20 | F9 | H10 | L21 | R13 | W9 | AB2 | AE25 |
| C24 | F10 | H13 | M2 | R14 | W10 | AB6 | AE26 |
| C25 | F11 | H14 | M5 | R17 | W13 | AB8 | AF1 |
| D2 | F13 | H17 | M9 | R18 | W14 | AB12 | AF2 |
| D3 | F14 | H18 | M10 | R21 | W17 | AB16 | AF6 |
| D4 | F15 | H21 | M13 | T2 | W18 | AB20 | AF20 |
| D7 | F17 | H22 | M14 | T5 | W21 | AB22 | AF22 |
| D9 | F18 | H25 | M17 | T9 | Y2 | AB25 | AF25 |
| D11 | F19 | H26 | M18 | T10 | Y5 | AB26 | AF26 |
| D14 | F20 | J6 | M22 | T13 | Y6 | AC1 | |
| D16 | F21 | J9 | M25 | T14 | Y9 | AC2 | |
| D20 | F22 | J10 | N6 | T17 | Y10 | AC22 | |
| D24 | F23 | J13 | N9 | T18 | Y13 | AC25 | |
| D25 | G6 | J14 | N10 | T22 | Y14 | AC26 | |

Table 27 PES24T3G2 (27x27mm 676-Pin) Ground Pins

Option B Package Alternate Signal Functions (27x27mm 676-Pin)

| Pin | GPIO | Alternate |
|-----|---------|------------|
| B18 | GPIO[0] | P2RSTN |
| A19 | GPIO[1] | P4RSTN |
| B19 | GPIO[2] | IOEXPINTN0 |
| A20 | GPIO[3] | IOEXPINTN1 |
| B20 | GPIO[4] | IOEXPINTN2 |
| A22 | GPIO[7] | GPEN |

Table 28 PES24T3G2 (27x27mm 676-Pin) Alternate Signal Functions

Option B Package No Connect Pins (27x27mm 676-Pin)

| NC Pins |
|---------|
| A16 |
| C26 |
| D26 |
| F12 |
| F16 |
| M6 |
| M21 |
| T6 |
| T21 |
| AA12 |
| AA16 |

Table 29 PES24T3G2 (27x27mm 676-Pin) No Connect Pins

Option B Package Signals Listed Alphabetically (27x27mm 676-Pin)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|---|----------|------------------------------|
| CCLKDS | I | A13 | System |
| CCLKUS | I | A12 | |
| GPIO_00 | I/O | B18 | General Purpose Input/Output |
| GPIO_01 | I/O | A19 | |
| GPIO_02 | I/O | B19 | |
| GPIO_03 | I/O | A20 | |
| GPIO_04 | I/O | B20 | |
| GPIO_05 | I/O | A21 | |
| GPIO_06 | I/O | B21 | |
| GPIO_07 | I/O | A22 | |
| GPIO_08 | I/O | D23 | |
| GPIO_09 | I/O | A24 | |
| GPIO_10 | I/O | C22 | |
| JTAG_TCK | I | B4 | JTAG |
| JTAG_TDI | I | A4 | |
| JTAG_TDO | O | B5 | |
| JTAG_TMS | I | A5 | |
| JTAG_TRST_N | I | B6 | |
| MSMBADDR_1 | I | A6 | SMBus |
| MSMBADDR_2 | I | B7 | |
| MSMBADDR_3 | I | A7 | |
| MSMBADDR_4 | I | B8 | |
| MSMBCLK | I/O | A8 | |
| MSMBDAT | I/O | B9 | |
| MSMBSMODE | I | B22 | System |
| NO CONNECT | See Table 29 for a list of No Connect pins. | | |

Table 30 PES24T3G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 1 of 5)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|-----------------|
| PE0RN00 | I | AC21 | PCI Express |
| PE0RN01 | I | AC19 | |
| PE0RN02 | I | AC17 | |
| PE0RN03 | I | AC15 | |
| PE0RN04 | I | AC13 | |
| PE0RN05 | I | AC11 | |
| PE0RN06 | I | AC9 | |
| PE0RN07 | I | AC7 | |
| PE0RP00 | I | AB21 | |
| PE0RP01 | I | AB19 | |
| PE0RP02 | I | AB17 | |
| PE0RP03 | I | AB15 | |
| PE0RP04 | I | AB13 | |
| PE0RP05 | I | AB11 | |
| PE0RP06 | I | AB9 | |
| PE0RP07 | I | AB7 | |
| PE0TN00 | O | AF21 | |
| PE0TN01 | O | AF19 | |
| PE0TN02 | O | AF17 | |
| PE0TN03 | O | AF15 | |
| PE0TN04 | O | AF13 | |
| PE0TN05 | O | AF11 | |
| PE0TN06 | O | AF9 | |
| PE0TN07 | O | AF7 | |
| PE0TP00 | O | AE21 | |
| PE0TP01 | O | AE19 | |
| PE0TP02 | O | AE17 | |
| PE0TP03 | O | AE15 | |
| PE0TP04 | O | AE13 | |
| PE0TP05 | O | AE11 | |
| PE0TP06 | O | AE9 | |
| PE0TP07 | O | AE7 | |
| PE2RN00 | I | AA4 | |
| PE2RN01 | I | W4 | |
| PE2RN02 | I | U4 | |
| PE2RN03 | I | R4 | |

Table 30 PES24T3G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 2 of 5)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|---------------------|
| PE2RN04 | I | N4 | PCI Express (cont.) |
| PE2RN05 | I | L4 | |
| PE2RN06 | I | J4 | |
| PE2RN07 | I | G4 | |
| PE2RP00 | I | AA5 | |
| PE2RP01 | I | W5 | |
| PE2RP02 | I | U5 | |
| PE2RP03 | I | R5 | |
| PE2RP04 | I | N5 | |
| PE2RP05 | I | L5 | |
| PE2RP06 | I | J5 | |
| PE2RP07 | I | G5 | |
| PE2TN00 | O | AA1 | |
| PE2TN01 | O | W1 | |
| PE2TN02 | O | U1 | |
| PE2TN03 | O | R1 | |
| PE2TN04 | O | N1 | |
| PE2TN05 | O | L1 | |
| PE2TN06 | O | J1 | |
| PE2TN07 | O | G1 | |
| PE2TP00 | O | AA2 | |
| PE2TP01 | O | W2 | |
| PE2TP02 | O | U2 | |
| PE2TP03 | O | R2 | |
| PE2TP04 | O | N2 | |
| PE2TP05 | O | L2 | |
| PE2TP06 | O | J2 | |
| PE2TP07 | O | G2 | |
| PE4RN00 | I | G23 | |
| PE4RN01 | I | J23 | |
| PE4RN02 | I | L23 | |
| PE4RN03 | I | N23 | |
| PE4RN04 | I | R23 | |
| PE4RN05 | I | U23 | |
| PE4RN06 | I | W23 | |
| PE4RN07 | I | AA23 | |

Table 30 PES24T3G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 3 of 5)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|----------------------------|
| PE4RP00 | I | G22 | PCI Express (cont.) |
| PE4RP01 | I | J22 | |
| PE4RP02 | I | L22 | |
| PE4RP03 | I | N22 | |
| PE4RP04 | I | R22 | |
| PE4RP05 | I | U22 | |
| PE4RP06 | I | W22 | |
| PE4RP07 | I | AA22 | |
| PE4TN00 | O | G26 | |
| PE4TN01 | O | J26 | |
| PE4TN02 | O | L26 | |
| PE4TN03 | O | N26 | |
| PE4TN04 | O | R26 | |
| PE4TN05 | O | U26 | |
| PE4TN06 | O | W26 | |
| PE4TN07 | O | AA26 | |
| PE4TP00 | O | G25 | |
| PE4TP01 | O | J25 | |
| PE4TP02 | O | L25 | |
| PE4TP03 | O | N25 | |
| PE4TP04 | O | R25 | |
| PE4TP05 | O | U25 | |
| PE4TP06 | O | W25 | |
| PE4TP07 | O | AA25 | |
| PEREFCLKN | I | C1 | |
| PEREFCLKP | I | D1 | |
| PERSTN | I | A17 | System |
| REFCLKM | I | B23 | PCI Express |
| REFRES0 | I/O | AF18 | SerDes Reference Resistors |
| REFRES1 | I/O | AF8 | |
| REFRES2 | I/O | Y1 | |
| REFRES3 | I/O | K1 | |
| REFRES4 | I/O | K26 | |
| REFRES5 | I/O | Y26 | |
| RSTHALT | I | A18 | System |









Table 30 PES24T3G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 4 of 5)

| Signal Name | I/O Type | Location | Signal Category |
|--|---|----------|-----------------|
| SSMBADDR_1 | I | A9 | SMBus |
| SSMBADDR_2 | I | B10 | |
| SSMBADDR_3 | I | A10 | |
| SSMBADDR_5 | I | B11 | |
| SSMBCLK | I/O | A11 | |
| SSMBDAT | I/O | B12 | |
| SWMODE_0 | I | B14 | System |
| SWMODE_1 | I | A15 | |
| SWMODE_2 | I | B15 | |
| V _{DD} CORE, V _{DD} I/O, V _{DD} PEA, V _{DD} PEHA, V _{DD} PETA | See Tables 25 and 26 for a listing of power pins. | | |
| V _{SS} | See Table 27 for a listing of ground pins. | | |

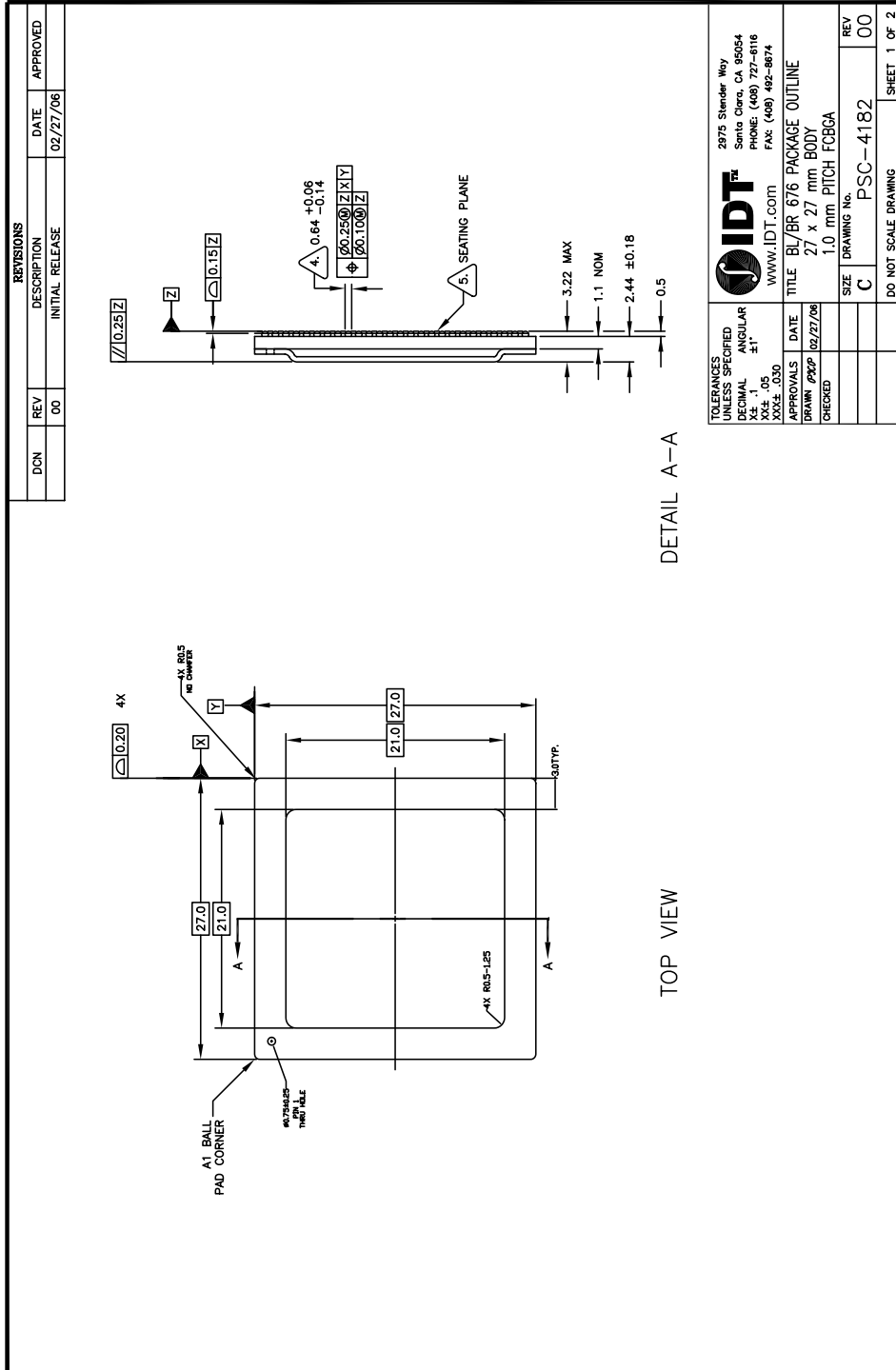
Table 30 PES24T3G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 5 of 5)

Option B Package Pinout (27x27mm) — Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | | |
|----|----------|----------|----------|----------|----------|------------|----------|----------|----------|----------|----------|------------|------------|----------|----------|------------|------------|----------|----------|----------|----------|------------|----------|----------|----------|----------|-----|----|
| A | Signal | Vss | Vss | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Vss | Signal | No Connect | Signal | Signal | Signal | Signal | Signal | Signal | Vss | Signal | Vss | Vss | A | |
| B | Vss | Vss | VDD I/O | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Vss | Signal | Signal | VDD I/O | Signal | Signal | Signal | Signal | Signal | Signal | VDD I/O | Vss | Vss | Vss | B | |
| C | Signal | Vss | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | Vss | VDD Core | VDD I/O | C | |
| D | Signal | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | D | |
| E | Vss | Vss | Vss | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | E | |
| F | VDD Core | VDD Core | VDD PEHA | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | No Connect | Vss | Vss | VDD Core | No Connect | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | F | |
| G | Signal | Signal | VDD PETA | Signal | Signal | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | G | |
| H | Vss | Vss | VDD PEHA | VDD PEHA | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD PEHA | VDD PEHA | H | |
| J | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | Signal | J | |
| K | Signal | Vss | VDD PEHA | VDD PEHA | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD PEHA | VDD PEHA | VDD PEHA | Vss | Signal | K | |
| L | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | Signal | L | |
| M | VDD Core | Vss | VDD PEHA | VDD PEHA | Vss | No Connect | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | No Connect | VDD PEHA | VDD PEHA | Vss | VDD Core | M | |
| N | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | Signal | N | |
| P | VDD Core | Vss | VDD PEHA | VDD PEHA | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | P | |
| R | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | Signal | R | |
| T | VDD Core | Vss | VDD PEHA | VDD PEHA | Vss | No Connect | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | No Connect | VDD PEHA | VDD PEHA | Vss | VDD Core | T | |
| U | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | Signal | U | |
| V | VDD Core | Vss | VDD PEHA | VDD PEHA | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD PEHA | VDD PEHA | VDD PEHA | Vss | VDD Core | V | |
| W | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | Signal | W | |
| Y | Signal | Vss | VDD PEHA | VDD PEHA | Vss | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | VDD PEHA | VDD PEHA | Vss | Signal | Signal | Y | |
| AA | Signal | Signal | VDD PETA | Signal | Signal | Vss | VDD Core | VDD Core | Vss | VDD Core | VDD Core | Vss | No Connect | Vss | Vss | VDD Core | No Connect | Vss | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PETA | Signal | AA | |
| AB | Vss | Vss | VDD Core | VDD Core | Vss | Signal | Signal | VDD PEHA | Signal | Signal | VDD PEHA | Signal | Signal | VDD PEHA | Signal | Signal | VDD PEHA | Signal | Signal | VDD PEHA | Signal | Signal | VDD Core | VDD Core | Vss | Vss | AB | |
| AC | Vss | Vss | VDD Core | VDD Core | Vss | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD PEHA | Signal | VDD Core | VDD Core | Vss | Vss | AC |
| AD | Vss | Vss | VDD Core | VDD Core | Vss | VDD PEHA | VDD PETA | VDD PETA | VDD PETA | VDD PEHA | VDD PETA | VDD PETA | VDD PEHA | VDD PETA | VDD PEHA | VDD PETA | VDD PEHA | VDD PETA | VDD PEHA | VDD PETA | VDD PEHA | VDD PETA | VDD PEHA | VDD Core | VDD Core | Vss | Vss | AD |
| AE | Vss | Vss | VDD Core | VDD Core | Vss | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | VDD Core | VDD Core | Vss | Vss | AE | |
| AF | Vss | Vss | VDD Core | VDD Core | Vss | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | Signal | VDD Core | VDD Core | Vss | Vss | AF | |

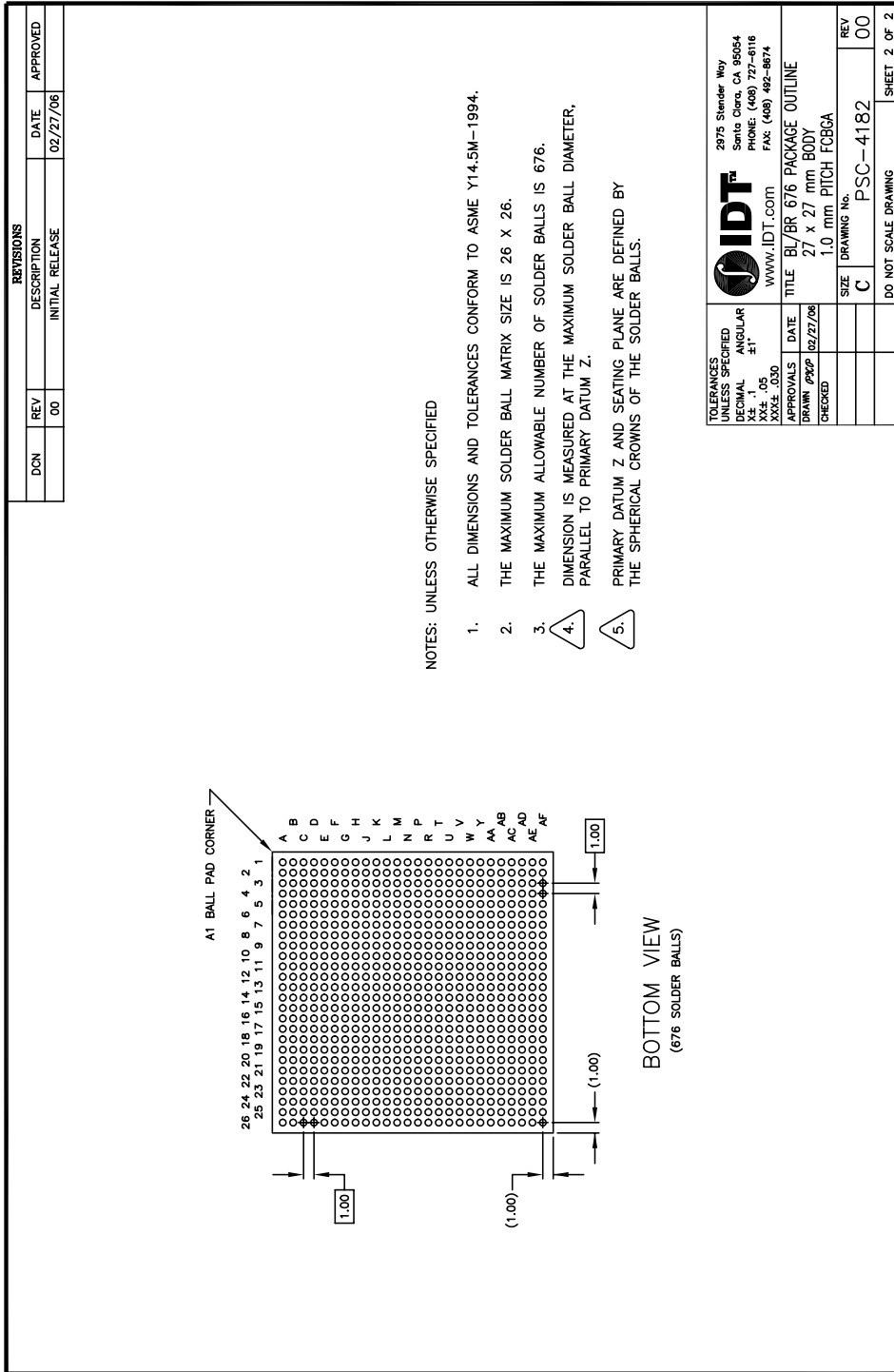
| | | | | | |
|---|------------------------------|---|--|---|------------|
|  | V _{DD} Core (Power) |  | V _{DD} PETA (Transmitter Power) |  | Signals |
|  | V _{DD} I/O (Power) |  | V _{DD} PEA (Analog Power) |  | No Connect |
|  | V _{SS} (Ground) |  | V _{DD} PEHA (High Analog Power) | | |

27x27mm Package Drawing — 676-Pin BL676/BR676



| | | | |
|--|----------------------------------|---|----------------------|
| IDT™ 2975 Slender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8874 WWW.IDT.COM | | TITLE: BL/BR 676 PACKAGE OUTLINE 27 x 27 mm BODY 1.0 mm PITCH FCBGA | |
| TOLERANCES UNLESS SPECIFIED: DECIMAL X.X ±.1 ANGULAR ±1° XXX.XXX ±.005 APPROVALS: DATE: 02/27/06 DRAWN: PXP CHECKED: | SIZE: C DRAWING No.: PSC-4182 | REV: 00 SHEET: 1 OF 2 | DO NOT SCALE DRAWING |

27x27mm Package Drawing — Page Two



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.
2. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 26 X 26.
3. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 676.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

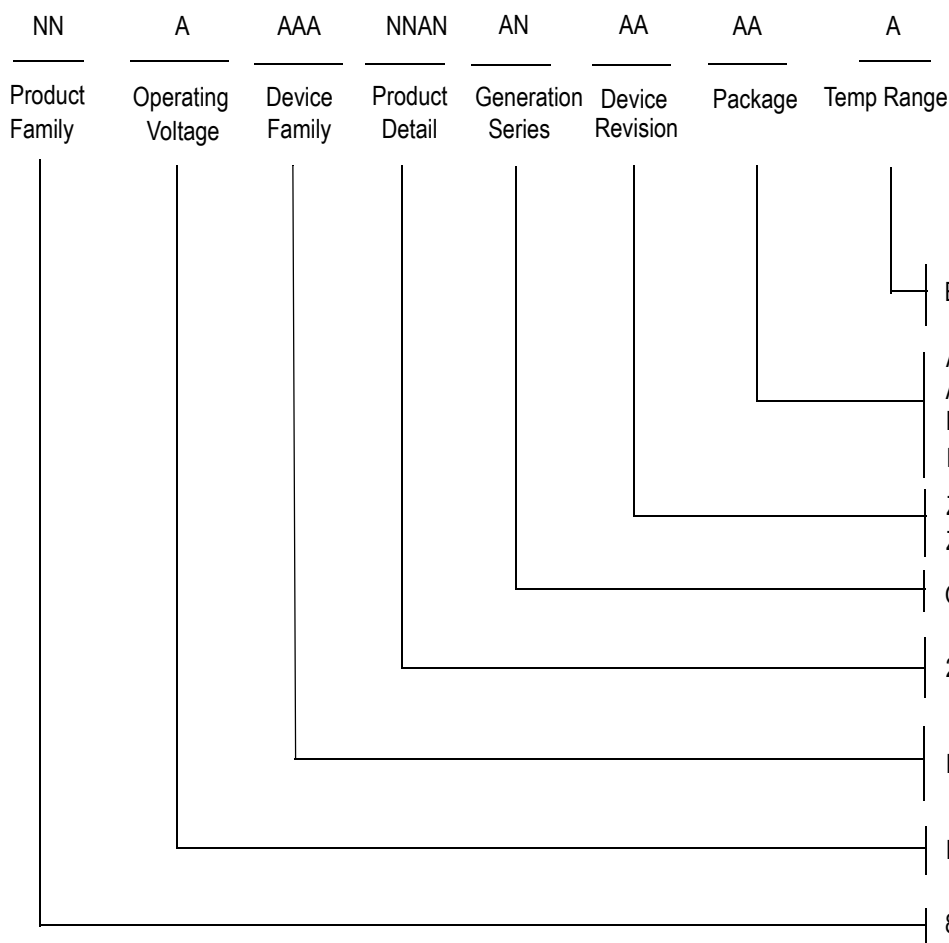
| | |
|--|--|
| 2975 Slender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8874 www.IDT.com | |
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X.X: .1 31° X.XX: .05 X.XX: .030 | TITLE BL/BR 676 PACKAGE OUTLINE 27 x 27 mm BODY 1.0 mm PITCH FCBGA |
| APPROVALS DRAWN: PMP CHECKED: | DATE: 02/27/06 DRAWING No. PSC-4182 |
| REV: 00 | REV: 00 |
| DO NOT SCALE DRAWING | |
| SHEET 2 OF 2 | |

Revision History

January 15, 2009: Publication of final data sheet.

February 11, 2009: Revised AC Timing Characteristics table and DC Electrical Characteristics table to correct typos.

Ordering Information



Legend
 A = Alpha Character
 N = Numeric Character

Blank Commercial Temperature (0°C to +70°C Ambient)
 AL 324-ball FCBGA
 ALG 324-ball FCBGA, Green
 BL 676-ball FCBGA
 BLG 676-ball FCBGA, Green
 ZB ZB revision
 ZC ZC revision
 G2 PCIe Gen 2
 24T3 24-lane, 3-port
 PES PCI Express Switch
 H 1.0V +/- 0.1V Core Voltage
 89 Serial Switching Product

Valid Combinations

Option A (19x19mm)

- 89HPES24T3G2ZBAL 324-ball FCBGA package, Commercial Temperature
- 89HPES24T3G2ZBALG 324-ball Green FCBGA package, Commercial Temperature
- 89HPES24T3G2ZCAL 324-ball FCBGA package, Commercial Temperature
- 89HPES24T3G2ZCALG 324-ball Green FCBGA package, Commercial Temperature

Option B (27x27mm)

- 89HPES24T3G2ZBBL 676-ball FCBGA package, Commercial Temperature
- 89HPES24T3G2ZBBLG 676-ball Green FCBGA package, Commercial Temperature
- 89HPES24T3G2ZCBL 676-ball FCBGA package, Commercial Temperature
- 89HPES24T3G2ZCBLG 676-ball Green FCBGA package, Commercial Temperature



CORPORATE HEADQUARTERS
 6024 Silver Creek Valley Road
 San Jose, CA 95138

for SALES:
 800-345-7015 or 408-284-8200
 fax: 408-284-2775
www.idt.com

for Tech Support:
 email: ssdhelp@idt.com
 phone: 408-284-8208