Fast Charge Battery Manager with Power Path and USB Compatibility

ADP5065

FEATURES

3 MHz Switch mode charger
1.25 A charge current from dedicated charger
Up to 680 mA charging current from 500mA USB Host
Operating input voltage from 4.0V up to 5.5V
Tolerant input voltage -0.5V to 20V (USB VBUS)
 Dead battery Isolation FET between battery and charger output
Battery Thermistor input with Automatic charger shutdown if Battery temperature exceeds limits
Compliant with the JEITA LiIon battery charging temperature specification
SYS_EN_OK flag to hold off system turn-on until battery is at minimum required level for guaranteed system start-up due to minimum battery voltage and/or minimum battery charge level requirements
EOC programming with C/20, C/10 and specific current level selection

APPLICATIONS

Digital Still Cameras
Digital Video cameras
Single cell Li-Ion Portable equipment
PDA's, Audio, GPS devices
Mobile Phones

## FUNCTIONAL BLOCK DIAGRAM
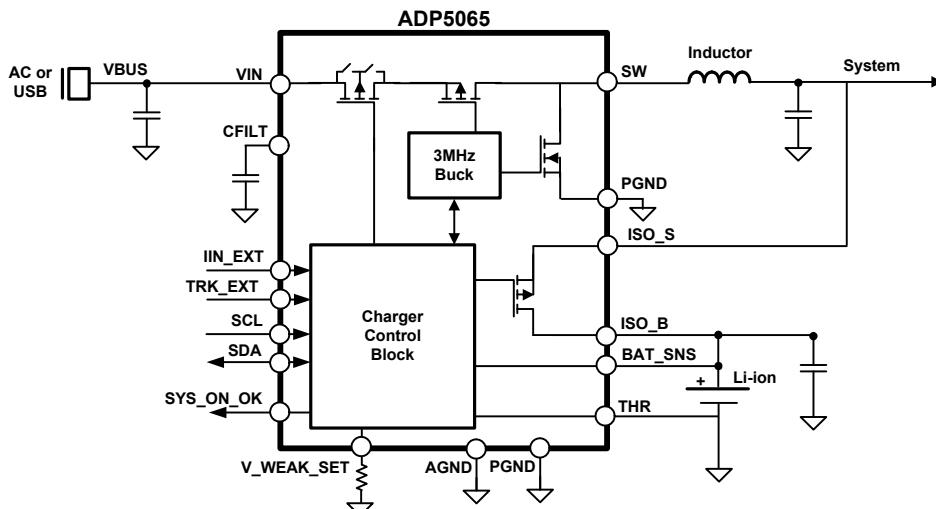
GENERAL DESCRIPTION

The ADP5065 charger is fully compliant with the USB 2.0, USB 3.0 and USB Battery Charging Specification 1.1 and enables charging via the mini-USB VBUS pin from a wall charger, car charger, or USB Host port.

The ADP5065 operates from a 4V to 5.5V input voltage range but is tolerant up to 20V. These alleviate the concerns of the USB bus spiking during disconnect or connect scenarios.

The ADP5065 also features an internal FET between the DCDC charger output and the battery. This permits Battery Isolation and hence System powering under a dead battery or no battery scenario which allows for immediate system function on connection to a USB power supply

Based on the type of USB source detected by an external the USB detection chip, the ADP5065 can be set to apply the correct current limit for optimal charging and USB compliance.

PACKAGE AND EXTERNALS

The ADP5065 comes in a very small and low profile WLCSP-20 (0.5 mm pitch spacing) package.

The overall solution requires only 5 small, low profile external components consisting of 4 ceramic capacitors (1 of which is the battery filter capacitor), 1 multi-layer inductor and 1 optional dead battery situation default setting resistor.

This enables a very small PCB area to provide an integrated and performance enhancing solution to USB battery charging and power rail provision

Figure 1. ADP5065 Block Diagram

Rev. PrA

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REVISION HISTORY

Revision PrA: Initial Revision

SPECIFICATIONS

Unless otherwise noted, -40 °C < T_J < 125 °C, V_{VIN} = 5.0 V, V_{ISO_S} > 3.0 V, V_{HOT} < V_{THR} < V_{COLD}, V_{BAT_SNS} = 3.6 V, C_{VIN} = 2.2 μF, C_{DCDC} = 22 μF, C_{BAT} = 22 μF, C_{CFILT} = 4.7 μF L_{OUT} = 1 μH, all registers at default values

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
GENERAL PARAMETERS						
Tolerable Supply voltage	V_{VIN}	-0.5		20	V	
Under-Voltage Lock-Out	V_{UVLO}	2.3	2.4	2.5	V	Rising threshold, higher of V_{CFILT} and V_{BAT_SNS}
		50	100	150	mV	Hysteresis, higher if V_{CFILT} and V_{BAT_SNS} falling
Total Input Current	I_{VIN}	86	92	100		Nominal USB initialized current level [1]
				150		USB super-speed
				300		USB enumerated current level (Chinese Spec')
		460	475	500		USB enumerated current level
				900		Dedicated charger input
				1500		Dedicated wall charger
Current consumption	I_{QVIN}		TBD			
Current consumption	I_{QISO_B}		250		nA	
SW Pin Leakage Current	$-I_{OUT}$			2	μA	V_{VIN} = 0V
CHARGING PARAMETERS						
Fast Charge Current, CC mode (Battery voltage > V_{TRK_DEAD})	I_{CHG}		1250		mA	V_{CFILT} > V_{BAT_SNS} + V_{CCDROP} [1,2]
Fast Charge Current Accuracy	$I_{CHG(TOL)}$	-5		5	%	T_J = 25°C, Battery charging only operates between 0°C and 115°C (Isothermal regulation)
Trickle Charge Current	I_{TRK_DEAD}		20		mA	[1,2]
Weak Charge Current	I_{CHG_WEAK}		I_{CHG} + 20		mA	When V_{TRK_DEAD} < V_{BAT_SNS} < V_{WEAK} but [1,3]
DEAD battery - Trickle to WEAK Charge Threshold	V_{TRK_DEAD}		2.5		V	On BAT_SNS [1]
Trickle to WEAK Charge Threshold Hysteresis	ΔV_{TRK_DEAD}		100		mV	
WEAK Battery Threshold – WEAK to FAST charge threshold	V_{WEAK}		3.0		V	On BAT_SNS, [1,3]
WEAK Battery Threshold Hysteresis	ΔV_{WEAK}		100		mV	
Battery Termination Voltage	V_{TRM}	- 0.3%	4.200	+ 0.3%	V	On BAT_SNS, T_J = 25°C, IEND = 52.5mA [1]
Battery Termination Voltage	V_{TRM}	4.158	4.200	4.242	V	On BAT_SNS, T_J = 0°C to 115°C [1]
Battery Over Voltage Threshold	V_{BATOV}		V_{CFILT} −0.15		V	Relative to CFILT voltage, BAT_SNS rising V_{BAT_SNS} = V_{TRM} [1]
Charge Complete Current	I_{END}		52.5		mA	
Charging Complete Current Threshold Accuracy		-30		30	%	IEND > 50mA
Recharge Voltage Differential	V_{RCH}		260		mV	Relative to V_{TRM}, BAT_SNS falling [1]
Battery node short threshold voltage	V_{BAT_SHR}		2.4		V	[1]
CHARGER DC-DC CONVERTER						
Switching Frequency	f_{SWCHG}		3		MHz	
Maximum Duty Cycle	D_{MAX}		91		%	
Peak Inductor Current	$I_{L(PK)}$			2000	mA	
Regulated System Voltage	V_{ISO_STRK}	3.244	3.3	3.366	V	V_{BAT_SNS} < V_{TRK_DEAD}, Trickle charging mode
Load regulation			5		mV/A	
DC-DC Power PMOS On Resistance	$R_{DS(ON)P}$		220		mΩ	
DC-DC Power NMOS On Resistance	$R_{DS(ON)N}$		150		mΩ	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
BATTERY ISOLATION FET						
Bump to Bump resistance between ISO_B and ISO_S bumps including bump resistances and Battery Isolation PMOS On Resistance	$R_{DSONISO}$		78		mΩ	On Battery supplement mode, VIN=0V V(ISO_B)=3.6V, I(ISO_B)=500mA
Regulated System Voltage	V_{ISO_SFC}	3.2	3.3	3.4	V	V_{TRK_DEAD} < Vbat_sns, Fast Charging CC mode
Maximum ISO_B Current	I_{MAX_ISO}	1.5		2.2	A	On Battery supplement mode, Vin=0V, V(ISO_B)=3.6V, Tj<85C
Battery Supplementary Threshold	V_{THISO}	0	5	10	mV	$V_{ISO\_S1:2}$ < $V_{ISO\_B1:2}$, Vsys rising
HIGH VOLTAGE BLOCKING FET						
VIN Input – High voltage blocking FET On Resistance	R_{DSONHV}		350		mΩ	VIN=5V, Iin=500mA
VIN Input Current , Suspend-Mode	$I_{SUSPEND}$		1.3	2.5	mA	EN_CHG = LOW
VIN Input Voltage Good Threshold rising	$V_{VIN\_OK\_RISE}$	3.8	3.9	4.0	V	
VIN Input Voltage Good Threshold falling	$V_{VIN\_OK\_FALL}$		3.6	3.67	V	
VIN Input Over Voltage Threshold	V_{VIN_OV}	5.35	5.42	5.5	V	
VIN Input Over Voltage Threshold Hysteresis			0.075		V	
CFILT total external capacitance		2.0	4.7	5.0	μF	
VIN transition timing - Min rise time for Vin from 5V to 20V	T_{VIN_RISE}	10			μs	
VIN transition timing - Min fall time for Vin from 4V to 0V	T_{VIN_FALL}	10			μs	
THERMAL CONTROL						
Isothermal Charging Temperature	T_{LIM}		115		°C	
Thermal Early Warning Temperature	T_{SDL}		130		°C	
Thermal Shutdown Temperature	T_{SD}		140		°C	T_J rising
Thermal Shutdown Temperature	T_{SD}		110		°C	T_J falling
THERMISTOR CONTROL						
Thermistor Current with 10k NTC	I_{NTC_10k}			400	μA	
Thermistor Current with 100k NTC	I_{NTC_100k}			40	μA	
Thermistor capacitance	C_{NTC}			100	pF	
Cold temperature limit	I_{NTC_COLD}		0		°C	No battery charging occurs
Hot temperature limit	I_{NTC_HOT}		60		°C	No battery charging occurs
JEITA SPECIFICATION [4]						
JEITA cold temperature threshold	I_{JEITA_COLD}		0		°C	No battery charging occurs
JEITA cool temperature threshold	I_{JEITA_COOL}		10		°C	Battery charging occurs at 50% of programmed level
JEITA typical temperature threshold	I_{JEITA_TYP}				°C	Normal battery charging occurs at default/programmed levels
JEITA warm temperature threshold	I_{JEITA_WARM}		45		°C	Battery termination voltage (V_{TRM}) is reduced by 100mV
JEITA hot temperature threshold	I_{JEITA_HOT}		60		°C	No battery charging occurs

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions / Comments
BATTERY DETECTION						
Battery Detection Sink Current	I_{SINK}		20		mA	
Battery Detection Source Current	I_{SOURCE}		10		mA	
Battery Low Threshold	V_{BATL}		1.9		V	
Battery High Threshold	V_{BATH}		3.4		V	
No Battery Threshold	V_{NOBAT}		3.3		V	$V_{TRM} \geq 3.7V$
			3.0			$V_{TRM} < 3.7V$
Battery detection Timer	t_{BATOK}		333		ms	
TIMERS						
Start charging delay timer	t_{START}		1		s	
Trickle Charge Timer	t_{TRK}		60		min	
Fast Charge Timer	t_{CHG}		600		min	
Charge Complete Timer	t_{END}		7.5		min	$V_{BAT\_SNS}= V_{TRM}, I_{CHG} < I_{END}$
Deglitch Timer	t_{DG}		31		ms	Applies to $V_{TRK}, V_{RCH}, I_{END}, V_{DEAD}, V_{VIN\_OK}$
Watchdog Timer	t_{WD}		32		s	[1]
Safety Timer	t_{SAFE}	36	40	44	min	
Battery node short timer	t_{BAT_SHR}		30		s	[1]
I²C COMPATIBLE INTERFACE[5]						
Capacitive load, each bus line	C_S			400	pF	
SCL clock frequency	f_{SCL}			400	kHz	
SCL high time	t_{HIGH}	0.6			µs	
SCL low time	t_{LOW}	1.3			µs	
Data setup time	t_{SUDAT}	100			ns	
Data hold time	t_{HDDAT}	0		0.9	µs	
Setup time for repeated start	t_{SUSTA}	0.6			µs	
Hold time for start/repeated start	t_{HDSTA}	0.6			µs	
Bus free time between a stop and a start condition	t_{BUF}	1.3			µs	
Setup time for stop condition	t_{SUSTO}	0.6			µs	
Rise time of SCL/SDA	t_R	20		300	ns	
Fall time of SCL/SDA	t_F	20		300	ns	
Pulse width of suppressed spike	t_{SP}	0		50	ns	
LOGIC INPUTS						
Maximum Voltage on Digital inputs	V_{DIN_MAX}			5.5	V	
Maximum Logic LOW Input Voltage	V_{IL}			0.5	V	Applies to SCL, SDA, TRK_EXT, IIN_EXT
Minimum Logic HIGH Input Voltage	V_{IH}	1.2			V	Applies to SCL, SDA, SOURCE3:1, DISABLE
LOW Level Input Current	I_{IL}	-1		1	µA	Applies to SCL, SDA, SOURCE3:1, DISABLE
HIGH Level Input Current	I_{IH}		TBD		µA	Applies to SCL, SDA, SOURCE3:1, DISABLE
HIGH Level Input Current			TBD		µA	Applies to SCL, SDA
Pulldown Resistance			350		kΩ	Applies to SOURCE3:1, DISABLE
						Applies to TRK_EXT, IIN_EXT

[1] These values are programmable via I²C. Values are given with default register values.
[2] The output current during charging may be limited by I_{BUS}, or by isothermal charging mode.
[3] Programmable via external resistor programming if required.
[4] JEITA can be enabled or disabled in I²C.
[5] A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge. The I²C timing diagram follows.

S = START CONDITION
Sr = REPEATED START CONDITION
P = STOP CONDITION
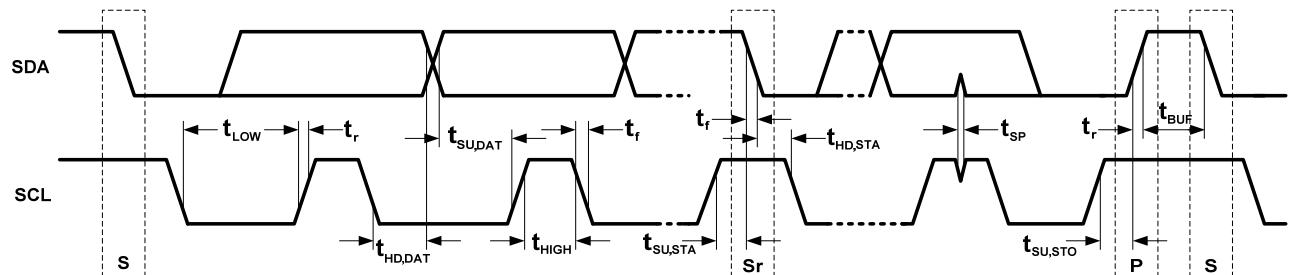
Figure 2. I²C timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Table 1. AD5065 Absolute Maximum Ratings

Parameter	Rating
VIN1:2 to PGND1:2	–0.5 V to +20V
All other pins to AGND	–0.3 V to +6 V
Ambient Temperature Range	–40℃ to +85℃
Storage Temperature Range	–65℃ to +150℃
Operating Junction Temperature Range	–40℃ to +125℃
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.

Table 2. Thermal Resistance

Package Type	θ_{JA}	Unit
5x4 Array WLCSP 0.5mm pitch (2.75mm * 2.08mm) - Based on a JEDEC, 2S2P, 4layer board with 0m/s airflow	55	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADP5065 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADP5065. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices potentially causing failure.

# PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS
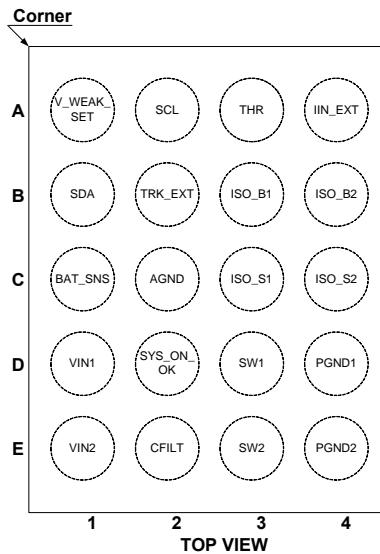
Figure 3. 20-Ball WLCSP

Table 3. Pin Function Descriptions—
20-Ball WLCSP

| Name	Type		Description
SW1:2	I/O		DC-DC converter inductor connections – high current output in charging mode
VIN1:2	I/O		Power connections to USB VBUS – high current input in charging mode
PGND1:2	G		Charger power ground pins – high current input in charging mode
AGND	G		Analog ground
CFILT	I/O		4.7uF filter capacitor connection – high current I/O in charging mode
ISO_S1:2	I/O		Charger supply side input to internal ISOLATION FET / Battery current regulation FET
ISO_B1:2	I/O		Battery supply side input to internal ISOLATION FET / Battery current regulation FET
SCL	I		I²C compatible interface serial clock
SDA	I/O		I²C compatible interface serial data
IIN_EXT	I		SetS the input current limit directly
TRK_EXT	I		Enables the trickle charge function
THR	I		Battery pack thermistor connection
BAT_SNS	I		Battery voltage sense pin
SYS_ON_OK	O		Battery ok flag output pin to enable system once battery has reached V_WEAK
V_WEAK_SET	I/O		External resistor setting pin for V_WEAK threshold (optional use)

TYPICAL PERFORMANCE CHARACTERISTICS
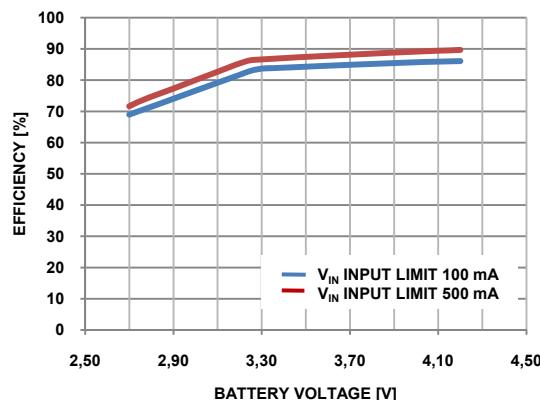
Figure 4. Battery Charger Efficiency vs. Battery Voltage,
VIN = 5.0 V

Figure 5. System Voltage Efficiency vs. Output Current,
VIN = 5.0 V

Figure 6. System Voltage Regulation vs. Output Current,
VIN = 5.0 V

Figure 7. USB Limited Battery Charge Current vs. Battery Voltage, VIN = 5.0 V, ILIM = 100 mA

Figure 8. USB Compliant Charge Current vs. Battery Voltage, VIN = 5.0 V, ILIM = 500 mA
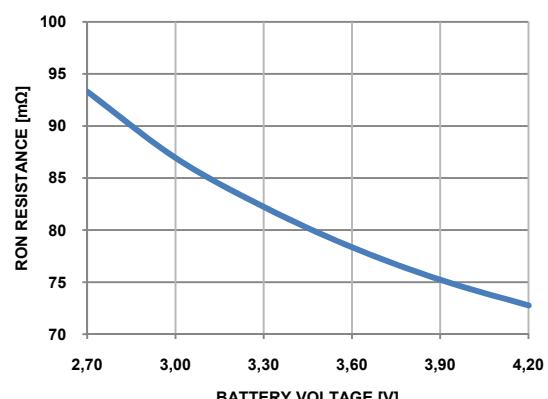

Figure 9. Battery Isolation FET Resistance vs. Battery Voltage, VIN = 5.0 V, Load Current = 1.0 A

TEMPERATURE CHARACTERISTICS
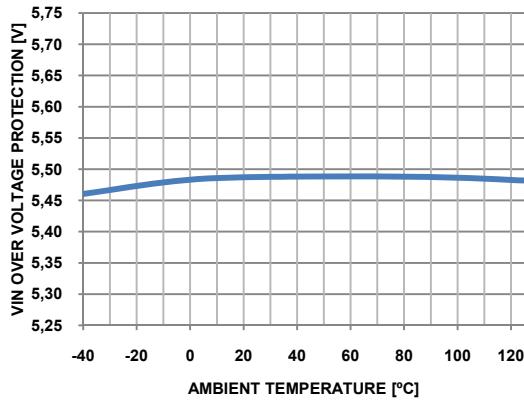
Figure 10. VIN Over Voltage Protection Rising Threshold vs. Ambient Temperature.
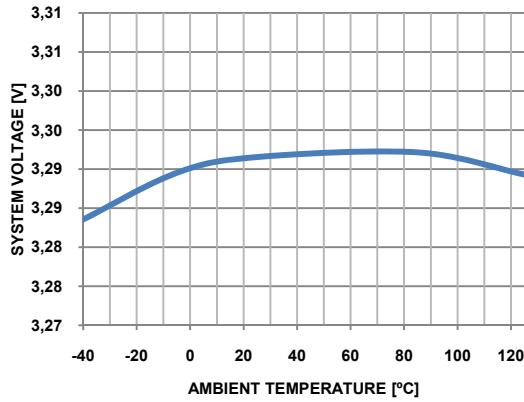
*Figure 11. System Voltage vs. Ambient Temperature, VIN = 5.0 V, R$_{load}$ = 33 Ω*
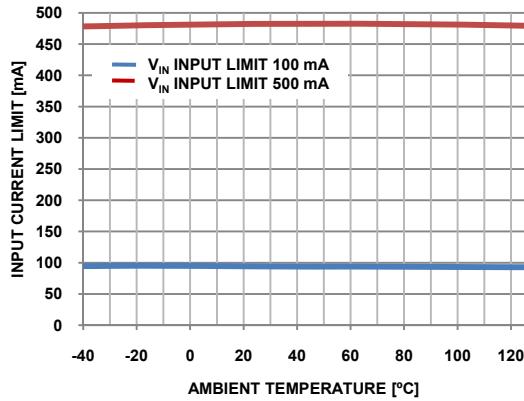
Figure 12. Input Current Limit vs. Ambient Temperature, VIN = 5.0 V
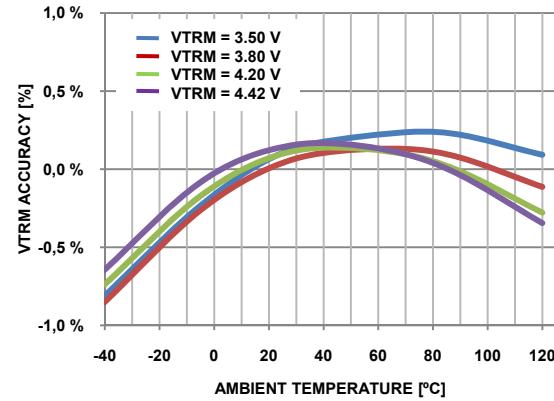
Figure 13. Termination Voltage vs. Ambient Temperature. VIN = 5.0V
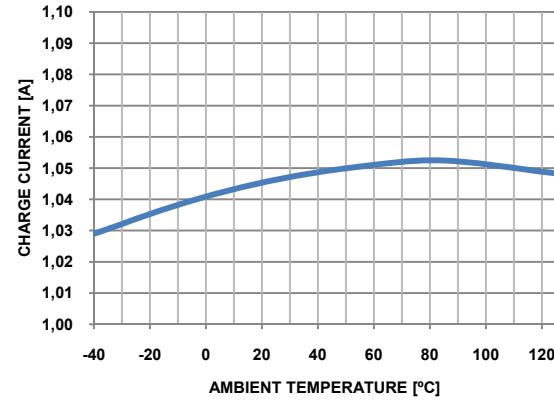
Figure 14. Fast Charge Current vs. Ambient Temperature, VIN = 5.0 V, VISO_B = 3.6 V, ICHG = 1050 mA
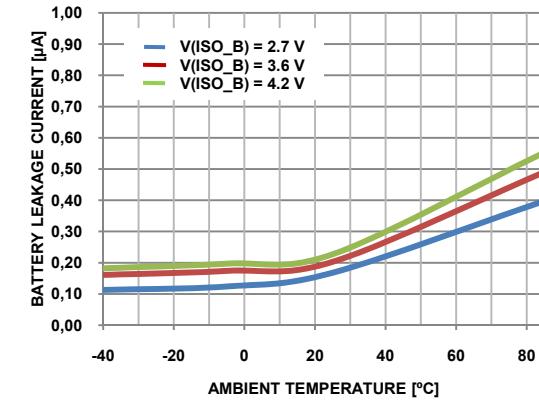
Figure 15. Battery Leakage Current vs. Ambient Temperature
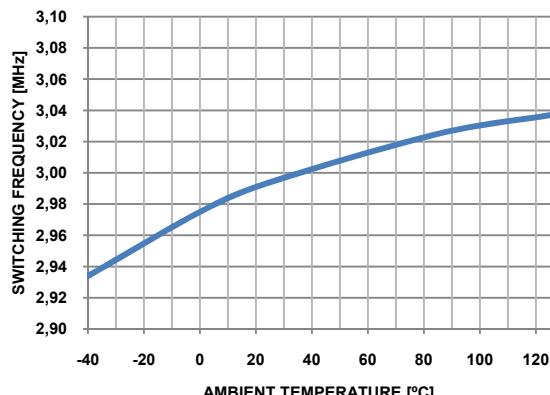
Figure 16. Switching Frequency vs. Ambient Temperature,
VIN = 5.0 V
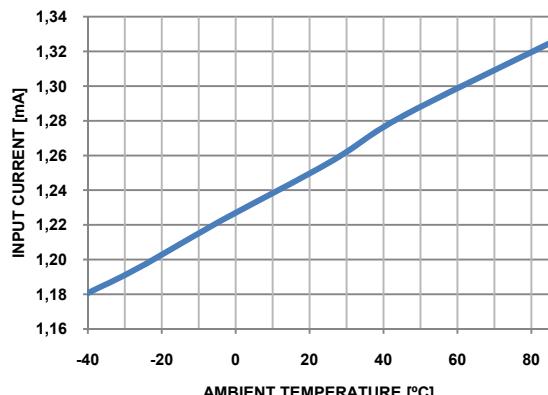
Figure 17. VIN Quiescent Current vs. Temperature, VIN = 5.0 V, Suspend-Mode
(EN_CHG = 0)

TYPICAL WAVEFORMS
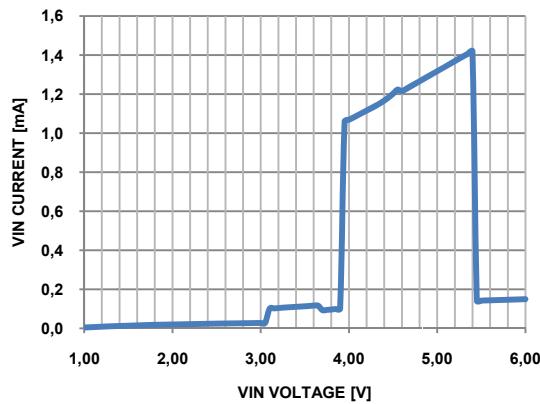
Figure 18. VIN Current vs. VIN Voltage,
Suspend-Mode (EN_CHG = 0)
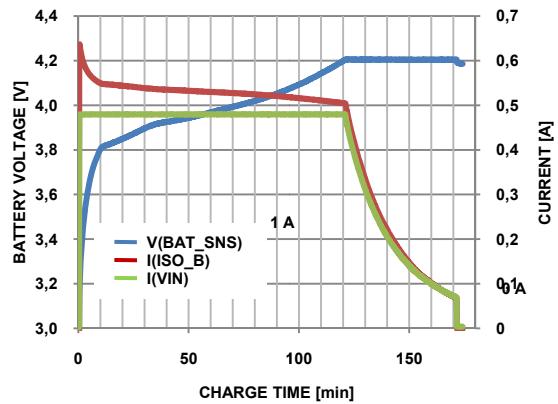
Figure 21. Charge Profile, VIN = 5.0 V, ILIM = 500 mA,
Battery Capacity = 1320 mAh
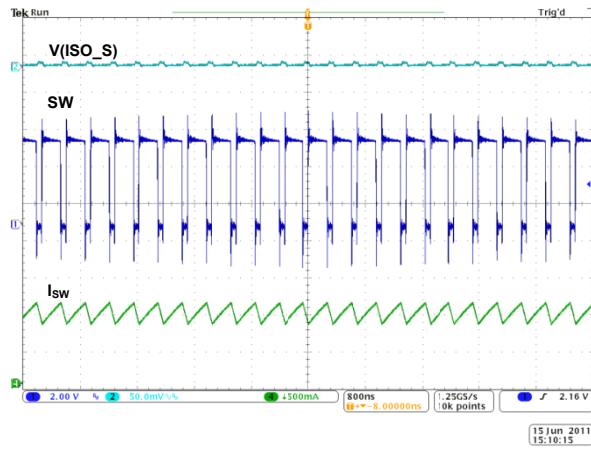
Vin 5, I(isos) 1000m

Figure 19. Typical Waveforms, VIN = 5.0 V, I_{ISO_S} = 1000 mA
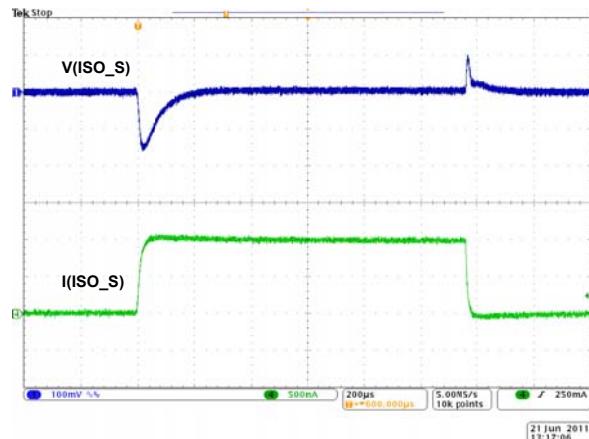
Figure 22. System Voltage Load Transient, VIN = 5.0 V, Load Transient 0 A –
1.0 A – 0 A
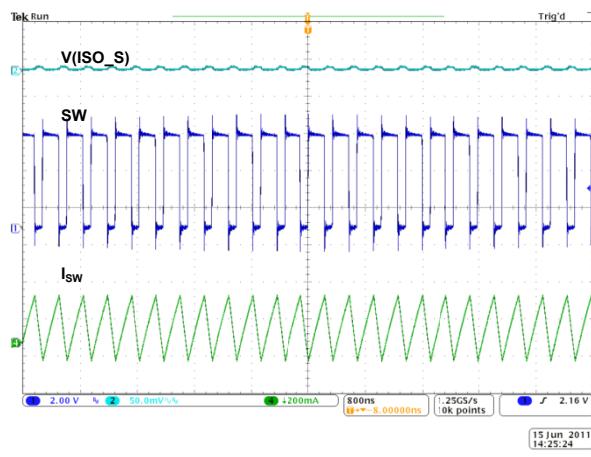
Vin 5, I(isos) 100m

Figure 20. Typical Waveforms, VIN = 5.0 V, I_{ISO_S} = 100 mA

THEORY OF OPERATION

CHARGER OPERATIONAL FLOWCHART
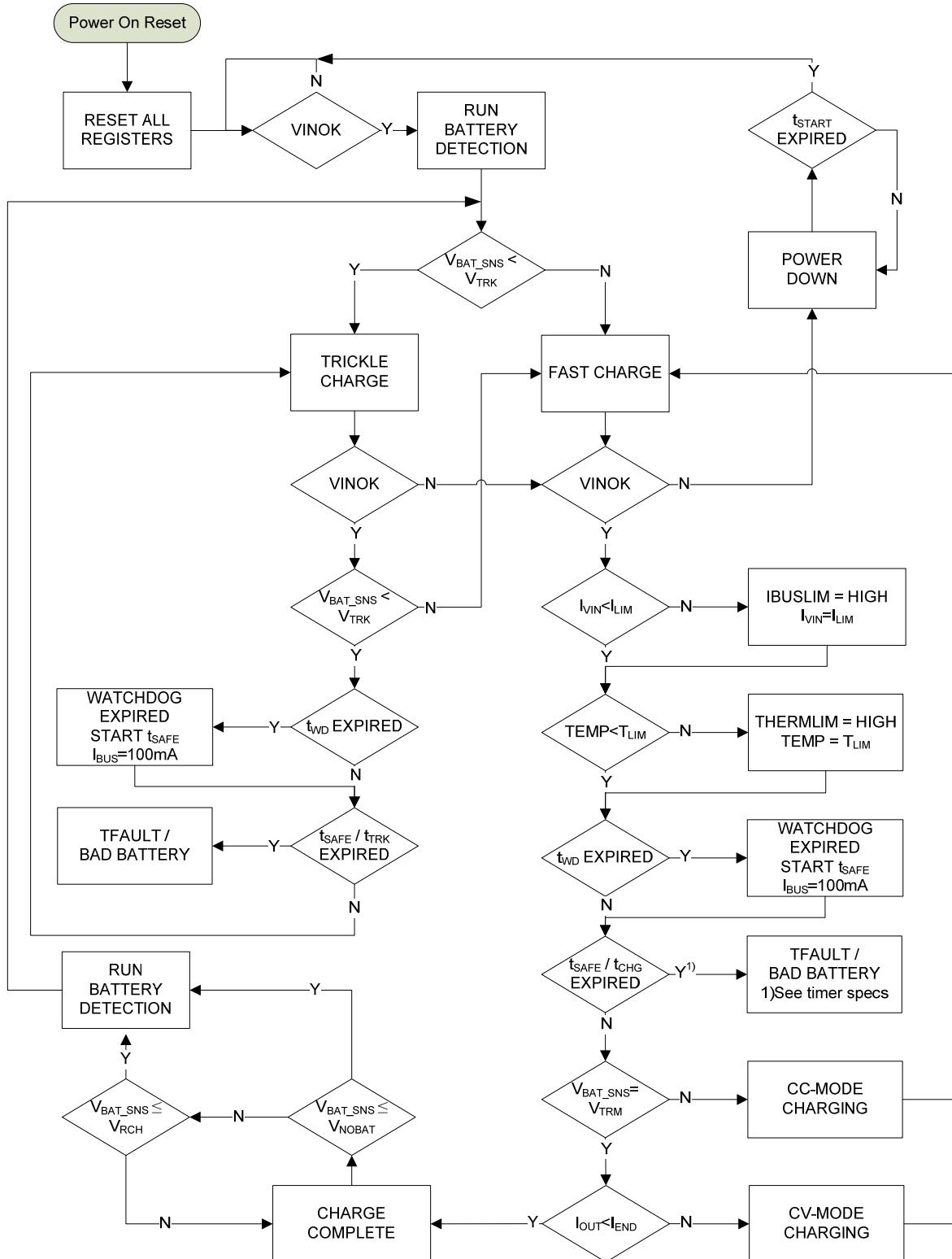
Figure 23. ADP5065 Operational Flowchart

I²C REGISTER MAP

Table 4. I²C Register Map

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x00	Manufacturer and Model ID	MANUF				MODEL			
0x01	Silicon Revision					REV			
0x02	VIN Settings				RFU	ILIM			
0x03	Termination Settings	VTRM						IEND	
0x04	Charging Current	C/20 EOC	C/10 EOC	HIGH (read only)	ICHG			ITRK_DEAD	
0x05	Voltage Threshold		VRCH		VTRK_DEAD		VWEAK		
0x06	Timer Settings			EN_ TEND	EN_ CHG_ TIMER	CHG_ TMR_ PERIOD	EN_ WD	WD PERIOD	RESET_ WD
0x07	Functional Settings1	EN_JEITA	DIS_IPK_SD	EN_ BMON	EN_THR	X	EN_EOC	EN_TRK	EN_CHG
0x08	Functional Settings2								
0x09	Interrupt Enable	EN_IND_PEAK_INT	EN_ THERM_ LIM_INT	EN_ WD_INT	EN_ TSD_INT	EN_ THR_INT	EN_ BAT_INT	EN_ CHG_INT	EN_ VIN_INT
0x0A	Interrupt Active	IND_PEAK_INT	THERM_ LIM_INT	WD_INT	TSD_INT	THR_INT	BAT_INT	CHG_INT	VIN_INT
0x0B	Charger Status 1	VIN_OV	VIN_OK	VIN_ ILIM	THERM_ LIM	CHDONE	CHARGER_STATUS		
0x0C	Charger Status 2	THR_STATUS			IPK_STAT		BATTERY_STATUS		
0x0D	Fault Register					BAT_SHR	IND_PEAK_INT	TSDL 130°C	TSD 140°C
0x10	Battery short	TBAT_SHR					VBAT_SHR		

REGISTER BIT DESCRIPTIONS

Table 5. Register Bit Descriptions

Bit(s)	Name	Access	Default	Description
0X00 MANUFACTURER AND MODEL ID REGISTER				
7:4	MANUF<3:0>	R	TBD	4-bit manufacturer identification bus
3:0	MODEL<3:0>	R	TBD	4-bit model identification bus
0X01 SILICON REVISION REGISTER				
7:4	Not Used	R		
3:0	REV<3:0>	R	TBD	4-bit silicon revision identification bus
0X02 VIN SETTINGS REGISTER				
7:5	Not Used	R		
4	RFU	R/W	0	Reserved for future use
3:0	ILIM<3:0>	R/W	0000=100mA	VIN input current limit programming bus. The current into VIN can be limited to the programmed values below 0000=100mA 1000=800mA 0001=150mA 1001=900mA 0010=200mA 1010=1000mA 0011=300mA 1011=1100mA 0100=400mA 1100=1200mA 0101=500mA 1101=1300mA 0110=600mA 1110=1400mA 0111=700mA 1111=1500mA
0X03 TERMINATION SETTINGS REGISTER				
7:2	VTRM<5:0>	R/W	100011=4.20V	Termination voltage programming bus. The values of the float voltage can be programmed as per the values below 000000=3.50V 010000=3.82V 100000=4.14V 000001=3.52V 010001=3.84V 100001=4.16V 000010=3.54V 010010=3.86V 100010=4.18V 000011=3.56V 010011=3.88V 100011=4.20V 000100=3.58V 010100=3.90V 100100=4.22V 000101=3.60V 010101=3.92V 100101=4.24V 000110=3.62V 010110=3.94V 100110=4.26V 000111=3.64V 010111=3.96V 100111=4.28V 001000=3.66V 011000=3.98V 101000=4.30V 001001=3.68V 011001=4.00V 101001=4.32V 001010=3.70V 011010=4.02V 101010=4.34V 001011=3.72V 011011=4.04V 101011=4.36V 001100=3.74V 011100=4.06V 101100=4.38V 001101=3.76V 011101=4.08V 101101=4.40V 001110=3.78V 011110=4.10V 101110 to 001111=3.80V 011111=4.12V 111111=4.42V
1:0	IEND<1:0>	R/W	01=52.5mA	Termination current programming bus. The values of the termination current can be programmed as per the values below 00=32.5mA 10=72.5mA 01=52.5mA 11=92.5mA

Bit(s)	Name	Access	Default	Description
0X04 CHARGING CURRENT SETTINGS REGISTER				
7	C/20 EOC	R/W		The C/20 bit has priority over the other settings (C/10 EOC and IEND) When bit is high c/20 programming used. 27.5mA minimum value
6	C/10 EOC	R/W		The C/10 bit has priority over the other setting (END) but not C/20 EOC When bit is high c/10 programming used unless C/20 EOC is high. 27.5mA minimum value
5	Tied high in metal	R	1	
4:2	ICHG<2:0>	R/W	111=1250mA	Fast charge current programming bus. The values of the constant current charge can be programmed as per the values below 000=550mA 001=650mA 010=750mA 011=850mA 100=950mA 101=1050mA 110=1150mA 111=1250mA
1:0	ITRK_DEAD<1:0>	R/W	10=20mA	TRICKLE and WEAK charge current programming bus. The values of the trickle nad Weak charge currents can be programmed as per the values below 00=5mA 10=20mA 01=10mA 11=20mA
0X05 VOLTAGE THRESHOLD SETTINGS REGISTER1				
7	Not Used	R		
6:5	VRCH<1:0>	R/W	11=260mV	Recharge voltage programming bus. The values of the recharge threshold can be programmed as per the values below 00=80mV 10=200mV 01=140mV 11=260mV
4:3	VTRK_DEAD<1:0>	R/W	01=2.5V	Trickle to Fast charge DEAD battery voltage programming bus. The values of the trickle to fast charge threshold can be programmed as per the values below 00=2.4V 10=2.6V 01=2.5V 11=3.3V
2:0	VWEAK<1:0>	R/W	011=3.0V	WEAK battery voltage rising threshold. Sets when the system is enabled by V_WEAK_OK signal: 000=2.7V 001=2.8V 010=2.9V 011=3.0V 100=3.1V 101=3.2V 110=3.3V 111=3.4V
0X06 TIMER SETTINGS REGISTER				
7	Not used			
6	Notused			
5	EN_TEND	R/W	1	When low disables the charge complete timer t_{END}. A 31ms deglitch timer will remain on this function.
4	EN_CHG_TIMER	R/W	1	When high the trickle / fast charge timer is enabled
3	CHG_TMR_PERIOD	R/W	1	Trickle / Fast charge timer period 0=30/300min 1=60/600min
2	EN_WD	R/W	1	When high the watchdog timer safety timer is enabled. When low the watchdog timer is disabled even if BAT_SNS exceeds V_{DEAD}

Bit(s)	Name	Access	Default	Description
1	WD PERIOD	R/W	0	Watchdog safety timer period 0=32sec/40min 1=64sec/40min
0	RESET_WD	W	0	High resets the watchdog safety timer. Bit is reset automatically.

0X07 FUNCTIONAL SETTINGS1 REGISTER

Bit(s)	Name	Access	Default	Description
7	EN_JEITA	R/W	0	When low, disables the JEITA LiIon temperature battery charging specification
6	DIS_IPK_SD	R/W	1	When high this disabled the automatic shutdown of the device if 4 peak inductor current limits are reached in succession • When high it will only flag a status bit IPK_STAT
5	EN_BMON	R/W	0	When high battery monitor is enabled even if VIN is below V_{VIN_OK}
4	EN_THR	R/W	0	When high THR current source is enabled even if VIN is below V_{VIN_OK}
3	X	R/W		
2	EN_EOC	R/W	1	When high end of charge is allowed
1	EN_TRK	R/W	1	When low Trickle charger is disabled, DC-DC Converter is enabled
0	EN_CHG	R/W	1	When low DC-DC Converter is disabled

0X08 FUNCTIONL SETTINGS2 REGISTER

Bit(s)	Name	Access	Default	Description
7:0	Not used	R/W		

0X09 INTERRUPT ENABLE REGISTER

Bit(s)	Name	Access	Default	Description
7	EN_IND_PEAK_INT	R/W	0	When high inductor peak current limit interrupt is allowed
6	EN_THERM_ LIM_INT	R/W	0	When high isothermal charging interrupt is allowed
5	EN_WD_INT	R/W	0	When high watchdog alarm interrupt is allowed
4	EN_TSD_INT	R/W	0	When high over temperature interrupt is allowed
3	EN_THR_INT	R/W	0	When high THR temperature thresholds interrupt is allowed
2	EN_BAT_INT	R/W	0	When high battery voltage thresholds interrupt is allowed
1	EN_CHG_INT	R/W	0	When high charger mode change interrupt is allowed
0	EN_VIN_INT	R/W	0	When high VIN voltage thresholds interrupt is allowed

0X0A INTERRUPT ACTIVE REGISTER, I²C READ RESET THE REGISTER BITS

Bit(s)	Name	Access	Default	Description
7	IND_PEAK_INT	R	0	When high interrupt due to inductor peak current limit
6	THERM_ LIM_INT	R	0	When high interrupt due to isothermal charging
5	WD_INT	R	0	When high interrupt due to watchdog alarm. Watchdog timer expires within 2sec / 4sec.
4	TSD_INT	R	0	When high interrupt due to over temperature fault
3	THR_INT	R	0	When high interrupt due to THR temperature thresholds
2	BAT_INT	R	0	When high interrupt due to battery voltage thresholds

Bit(s)	Name	Access	Default	Description
1	CHG_INT	R	0	When high interrupt due to charger mode change
0	VIN_INT	R	0	When high interrupt due to VIN voltage thresholds

0X0B CHARGER STATUS REGISTER 1

Bit(s)	Name	Access	Default	Description
7	VIN_OV	R	N/A	When high indicates that VIN exceeds V_{VIN_OV}
6	VIN_OK	R	N/A	When high indicates that VIN exceeds V_{VIN_OK}
5	VIN_ILIM	R	N/A	When high indicates that the current into VIN pin is limited by the high voltage blocking FET and the charger is not running at the full programmed I_{CHG}.
4	THERM_LIM	R	N/A	When high indicates that the charger is not running at the full programmed I_{CHG}, but is limited by the die temperature.
3	CHDONE	R	N/A	When high indicates the end of charge cycle has been reached. This bit will latch on, in that it will not reset to low when the V_{RCH} threshold is breached.
2:0	CHAGER_STATUS<2:0>	R	N/A	Charger status bus. 000=Off 100=Charge complete 001=Trickle charge 101=Suspend 010=Fast charge (CC-mode) 110=Trickle or Fast charge timer expired 011=Fast charge (CV-mode) 111=Battery Detection

0X0C CHARGER STATUS REGISTER 2

Bit(s)	Name	Access	Default	Description
7:5	THR_STATUS<2:0>	R	N/A	THR-pin status 000=Off 001=BatCold 010=BatCool 011=BatWarm 100=BatHot 111=Thermistor OK
4	IPK_STAT	R	N/A	Peak current limit status bit Set high if 4 or more peak inductor current limits are reached in succession
3	Not Used	R	N/A	
2:0	BATTERY_STATUS<2:0>	R		Battery status bus. 000=Battery monitor Off 001=No Battery 010=BAT_SNS < V_{TRK} 011=V_{TRK} ≤ BAT_SNS < V_{WEAK} 100=BAT_SNS ≥ V_{WEAK}

0X0D FAULT REGISTER, I^{2}C READ + I^{2}C WRITE TO RESET THE REGISTER BITS

Bit(s)	Name	Access	Default	Description
7:4	Not Used			
3	Bat_shr	R/W	0	When high battery short detection has occured
2	IND_PEAK_INT	R/W	0	When high inductor peak current limit fault has occurred
1	TSD 130˚C	R/W	0	When high the over temperature (LOWER) fault has occurred
0	TSD 140˚C	R/W	0	When high the over temperature fault has occurred

| Bit(s)	Name	Access	Default	Description
0X10 BATTERY SHORT REGISTER				
7:5	TBAT_SHR<2:0>	R/W	100 = 30seconds	Battery short time-out timer: 000= 1s 001= 2s 010= 4s 011= 10s 100= 30s 101= 60s 110= 120s 111= 180s
4:3	Not used	R/W		
2:0	VBAT_SHR<2:0>	R/W	100=2.4V	Battery short voltage threshold level: 000= 2.0V 001= 2.1V 010= 2.2V 011= 2.3V 100= 2.4V 101= 2.5V 110=2.6V 111= 2.7V

APPLICATIONS INFORMATION
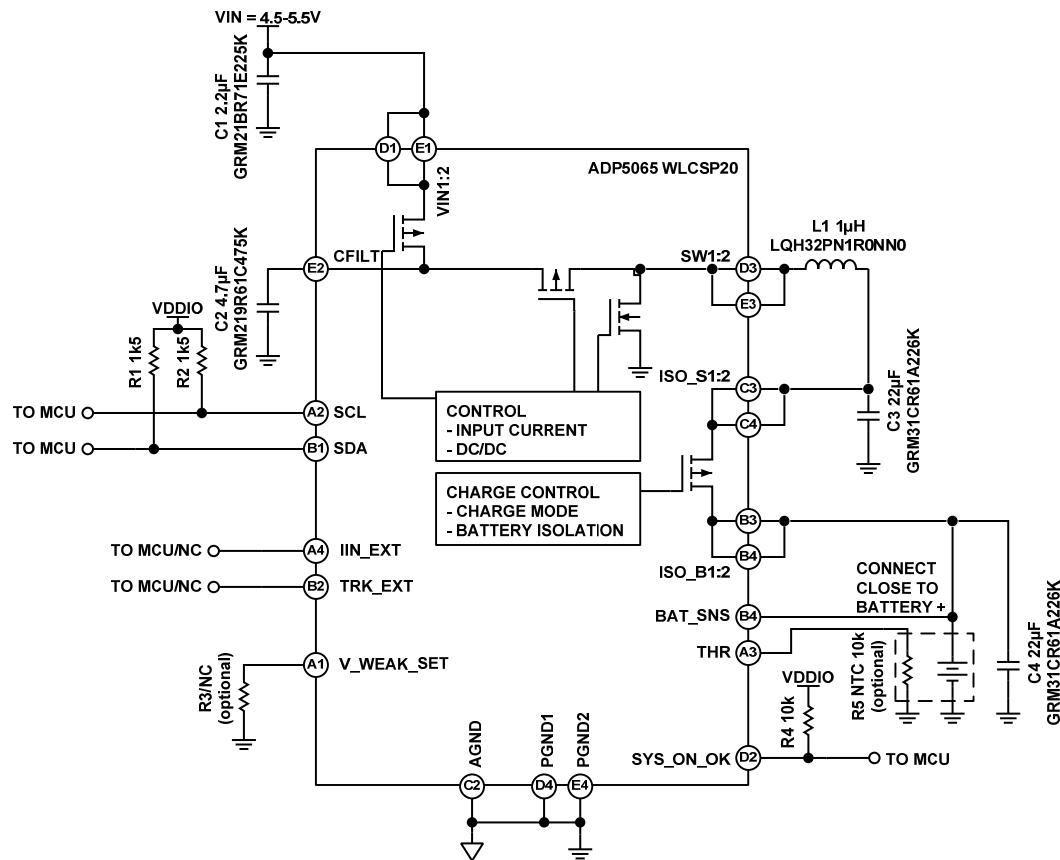


Figure 24. ADP5065 Reference Circuit Diagram.
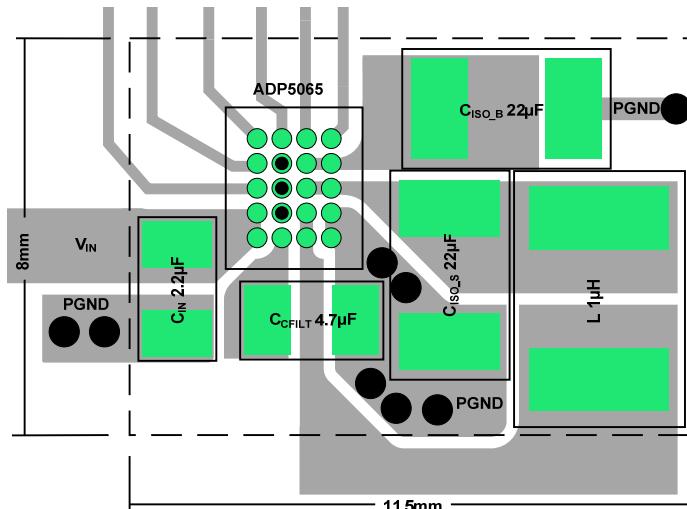
Figure 16. ADP5065 PCB Layout Suggestion.

OUTLINE DIMENSIONS
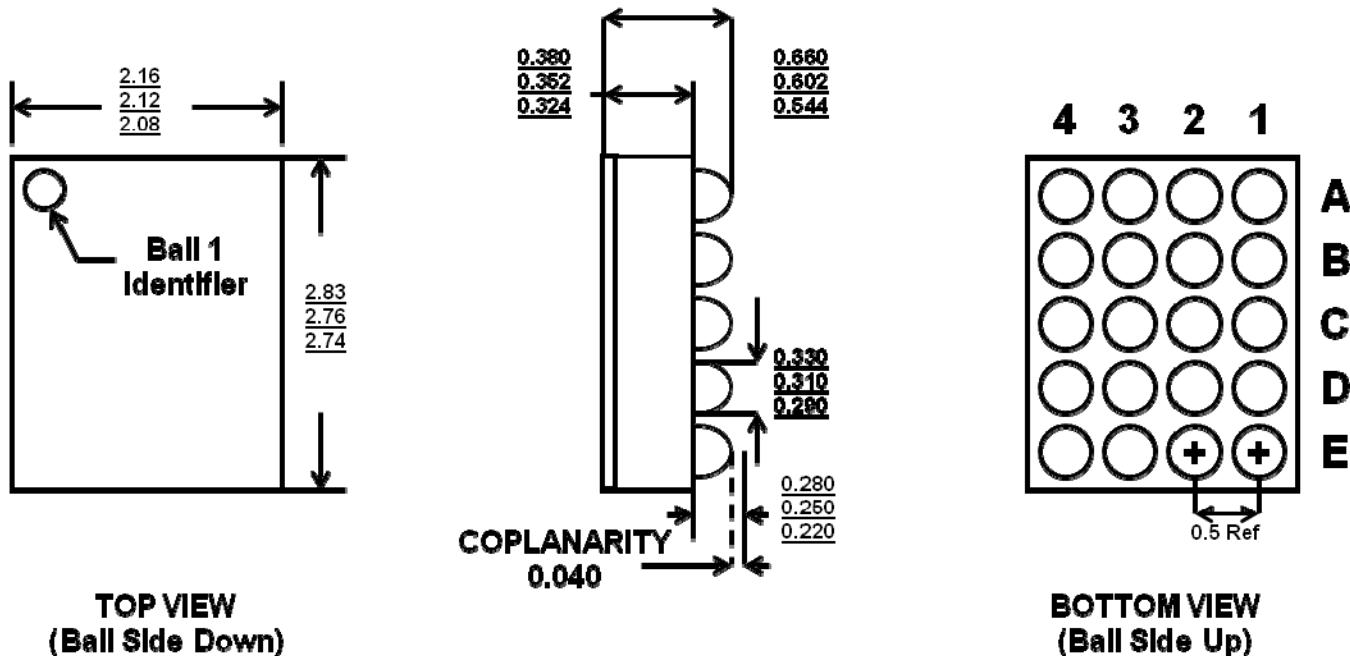
Figure 25. 20 Ball WLCSP Package. Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!
ESD SENSITIVE DEVICE

Table 6. Ordering Guide

ADP5065 Products	Temperature Package	Package Description	Package Outline
ADP5065ACBZ-1-R7	−40°C to +85°C	20 Ball WLCSP (0.5mm Pitch)	WLCSP

NOTES

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