24-Pin Enhanced AmPAL20RP10 Family

24-Pin IMOX™ Programmable Array Logic (PAL) Elements

Distinctive Characteristics

- AMD's superior IMOX technology
  - Guarantees t_{PD} = 15 ns max
- Individually programmable output polarity on each output
- Eight logical product terms per output
- Programming yields > 98% are realized via platinum-silicide fuse technology and the use of added test words
- Post Programming Functional Yield (PPFY) of 99.9%
- PRELOAD feature permits full logical verification
- Reliability assured through more than 70 billion fuse hours of life testing with no failures
- AC and DC parametric testing at the factory through on-board testing circuitry
- > 3000V ESD protection per pin
- JEDEC-Standard LCC and PLCC pinout

General Description

AMD Enhanced 24-pin PAL devices are high-speed, electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely. Typically they are a replacement for low-power Schottky SSI/MSI logic circuits, reducing chip count by more than 5 to 1 and greatly simplifying prototyping and board layout. Additional product terms, two additional outputs, and programmable output polarity are enhancements over industry-standard 24-pin PAL devices.

Five different devices are available, including both registered and combinatorial devices. All devices have user-programmable output polarity on all outputs. A variety of speed options allow the designer maximum flexibility in matching precise system requirements. The Product Selector Guide below shows the available speed options. The second table gives details about the functionality of the five available devices.

Please see the following pages for Block Diagrams.

Product Selector Guide

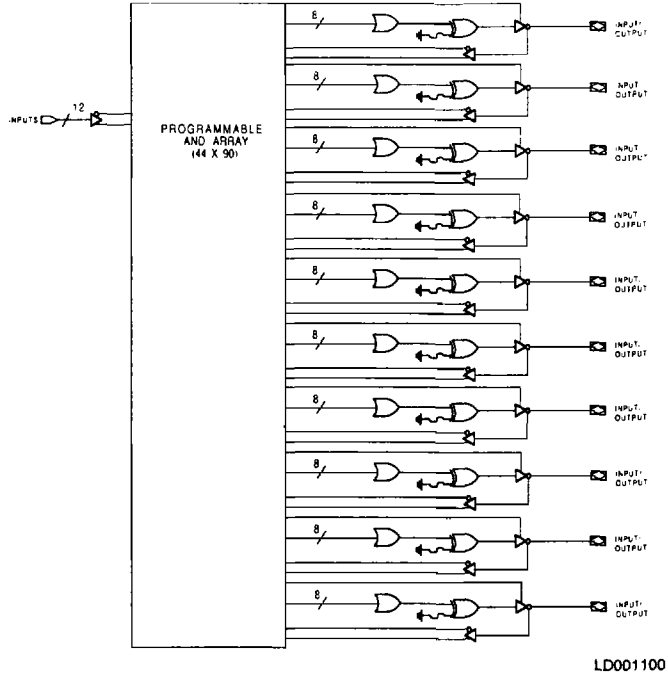
AMD PAL Speed/Power Families

Family	t_{PD} ns (Max.)		t_S ns (Min.)		t_{CO} ns (Max.)		I_{CC} mA (Max.)	I_{OL} mA (Min.)	
	C Devices	M Devices	C Devices	M Devices	C Devices	M Devices	C/M Devices	C Devices	M Devices
Very High-Speed ("B") Versions	15	20	15	20	12	15	210	24	12
High-Speed ("A") Versions	25	30	25	30	15	20	210	24	12
High-Speed, Half-Power ("AL") Versions	25	30	25	30	15	20	105	24	12
-20 & -25 Versions (AmPAL20L10 only)	20	25	N/A	N/A	N/A	N/A	165	24	12

Part Number	Array Inputs	Logic	Output Enable	Outputs/Polarity	Package Pins
22P10	12 Dedicated, 10 Bidirectional	Ten (8)-Wide AND-OR	Programmable	Bidirectional/Programmable	24
20RP4	10 Dedicated, 4 Feedback, 6 Bidirectional	Four (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
		Six 8-Wide AND-OR	Programmable	Bidirectional/Programmable	
20RP6	10 Dedicated, 6 Feedback, 4 Bidirectional	Six (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
		Four 8-Wide AND-OR	Programmable	Bidirectional/Programmable	
20RP8	10 Dedicated, 8 Feedback, 2 Bidirectional	Eight (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
		Two 8-Wide AND-OR	Programmable	Bidirectional/Programmable	
20RP10	10 Dedicated, 10 Feedback	Ten (8)-Wide AND-OR	Dedicated	Registered/Programmable	24
20L10	12 Dedicated, 8 Bidirectional	Ten (3)-Wide AND-OR	Programmable	8 Bidirectional 2 Dedicated	24

Block Diagrams

AmPAL22P10



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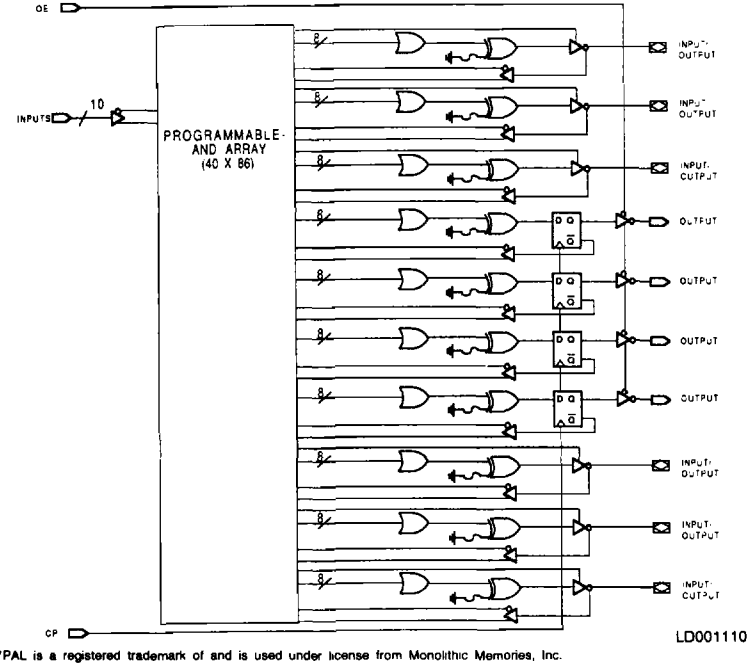
AmPAL20RP4



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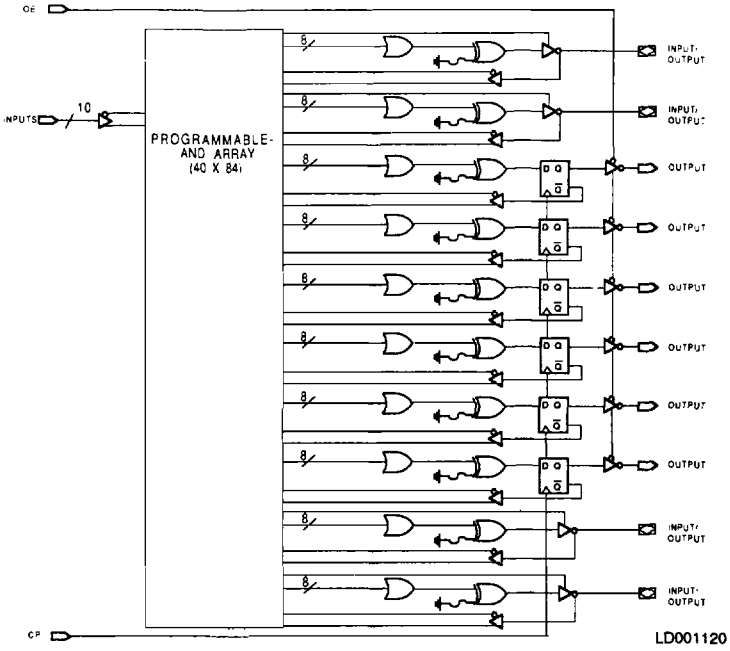
Block Diagrams (Cont'd.)

AmPAL20RP6



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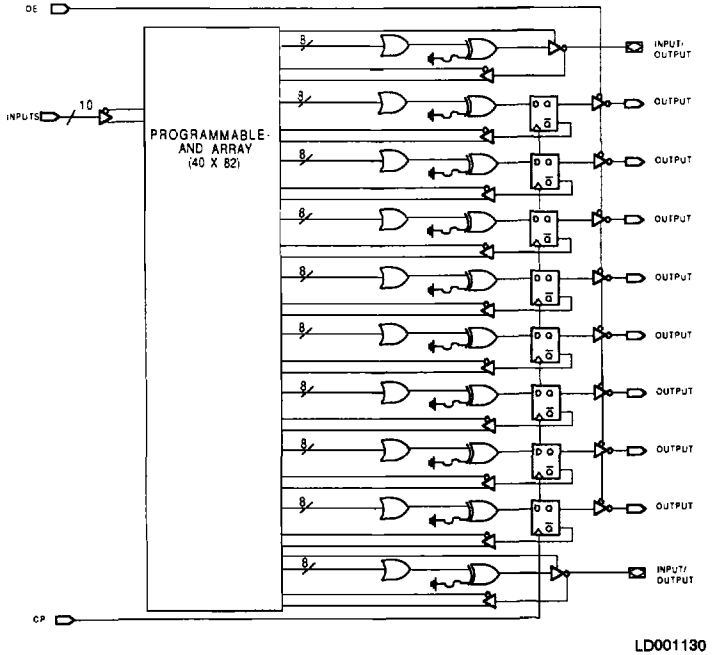
AmPAL20RP8



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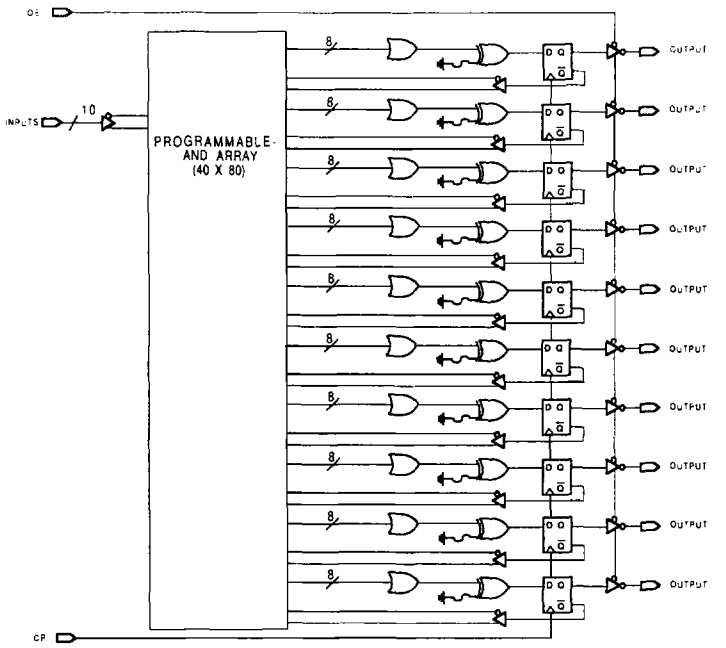
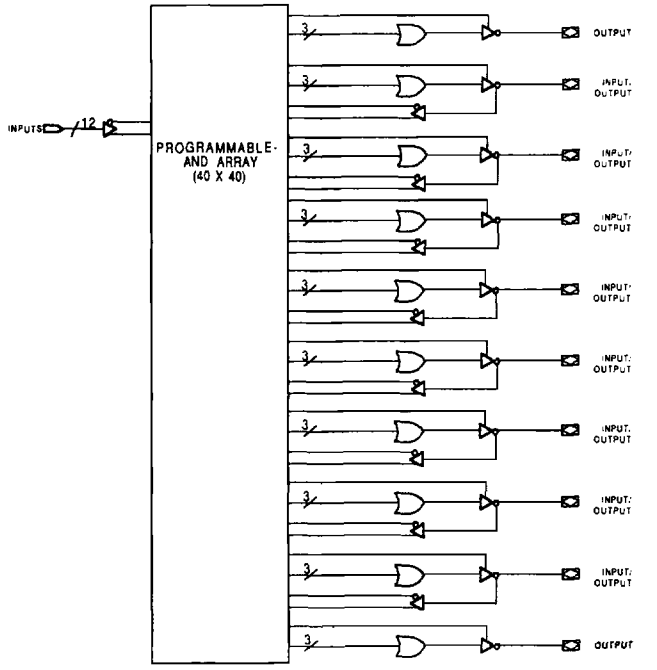
Block Diagrams (Cont'd.)

AmPAL20RP10



AmPAL20L10



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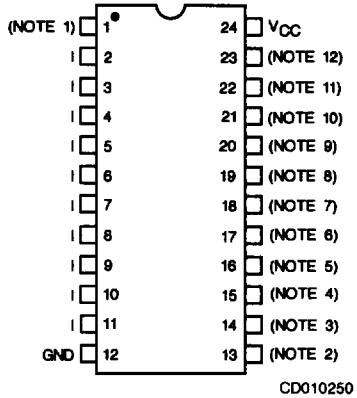
Connection Diagrams

Top View

DIPs*



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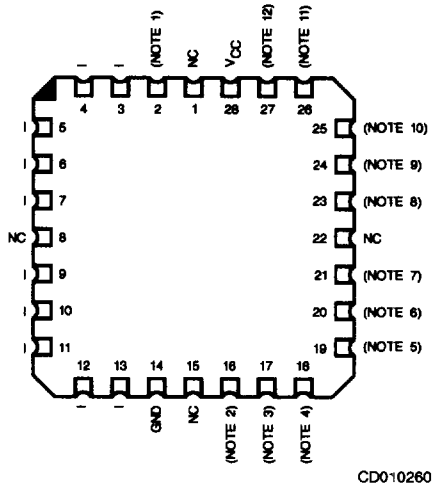
LCC**



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Note: Pin 1 is marked for orientation.

Notes:

	22P10	20RP4	20RP6	20RP8	20RP10	20L10
1	I	CLK	CLK	CLK	CLK	I
2	I	OE	OE	OE	OE	I
3	I/O	I/O	I/O	I/O	O	O
4	I/O	I/O	I/O	O	O	I/O
5	I/O	I/O	O	O	O	I/O
6	I/O	O	O	O	O	I/O
7	I/O	O	O	O	O	I/O
8	I/O	O	O	O	O	I/O
9	I/O	O	O	O	O	I/O
10	I/O	I/O	O	O	O	I/O
11	I/O	I/O	I/O	O	O	I/O
12	I/O	I/O	I/O	I/O	O	O

*Also available in 24-Pin Ceramic Flatpack. Pinouts identical to DIPs.
**Also available in 28-Pin Plastic Leaded Chip Carrier. Pinouts identical to LCC.

Pin Designations

I = Input
I/O = Input/Output
O = Output
V_{CC} = Supply Voltage
GND = Ground
CLK = Clock
OE = Output Enable
NC = No Connect

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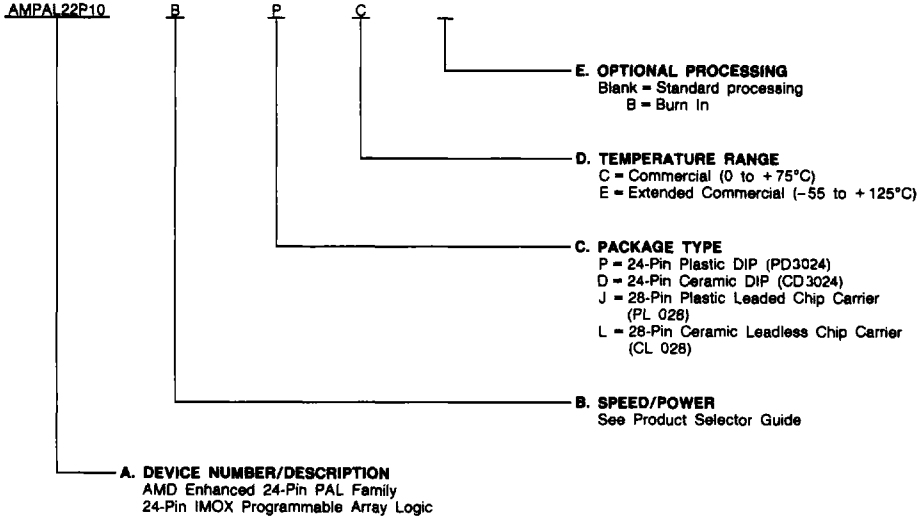
Ordering Information

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AMPAL22P10B/A/AL	PC, DC, DCB, DE, JC, LC, LE
AMPAL20RP4B/A/AL	
AMPAL20RP6B/A/AL	
AMPAL20RP8B/A/AL	
AMPAL20RP10B/A/AL	
AMPAL20L10B/-20/AL	

Valid Combinations

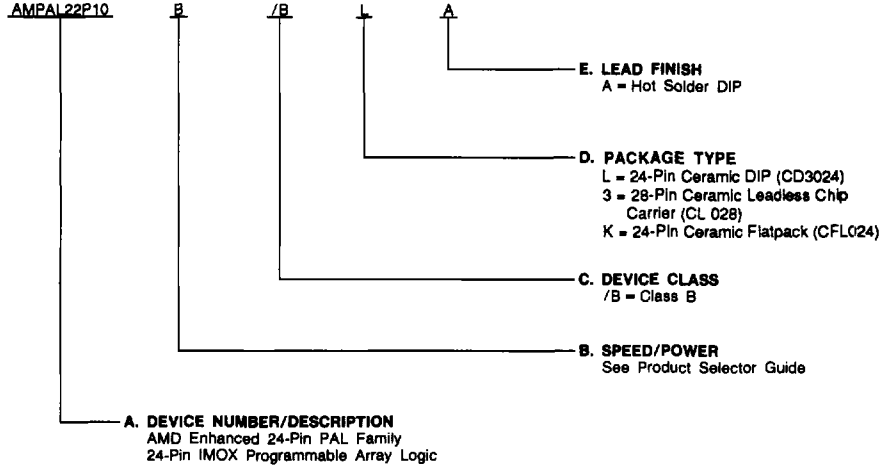
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Ordering Information (Cont'd.)

APL Products

AMD products for Aereospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AMPAL22P10B/A/AL	/BLA, /B3A, /BKA
AMPAL20RP4B/A/AL	
AMPAL20RP6B/A/AL	
AMPAL20RP8B/A/AL	
AMPAL20RP10B/A/AL	
AMPAL20L10B/-25/AL	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, & 11

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Functional Description

AMD Enhanced 24-Pin PAL Family Characteristics

All members of the AMD Enhanced 24-Pin PAL Family have common electrical characteristics and programming procedures. All parts are produced with a fusible link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit.

Initially the AND gates are connected, via fuses, to both the true and complement of each input. By selective programming of fuses the AND gates may be "connected" to only the true input (by blowing the complement fuse), to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the true and complement fuses are left intact a logical false results on the output of the AND gate, while all fuses blown results in a logical true state. For combinatorial outputs, the AND gates are connected to fixed-OR gates whose outputs become device outputs. For registered outputs, the AND gates are connected to fixed-OR gates whose outputs become output register inputs.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields (> 98%), and provide extra test paths to achieve excellent parametric correlation.

Power-Up Reset

The registered devices in the AMD PAL family have been designed to reset during system power-up. Following power-up, all registers will be initialized to zero, setting all the outputs to a logic 1. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

PRELOAD

AMD PAL devices are designed with unique PRELOAD circuitry that provides an easy method of testing registered devices for logical functionality. PRELOAD allows any arbitrary state value to be loaded into the registered output of an AMD PAL device.

A typical functional test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state or "next state." The next state is then checked to validate the transition from the present state. In this way any state transition can be checked.

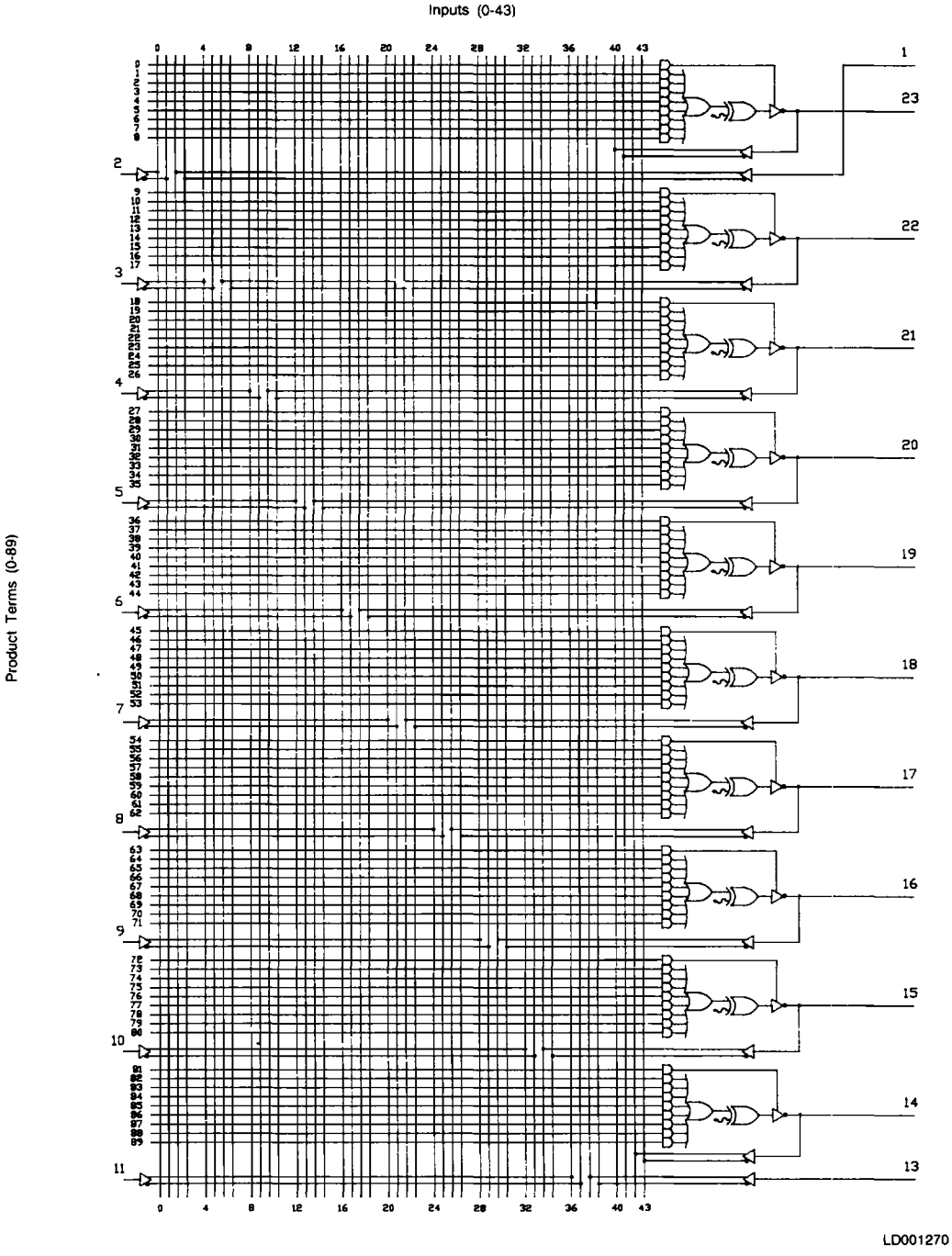


Figure 1. AmPAL22P10 Logic Diagram

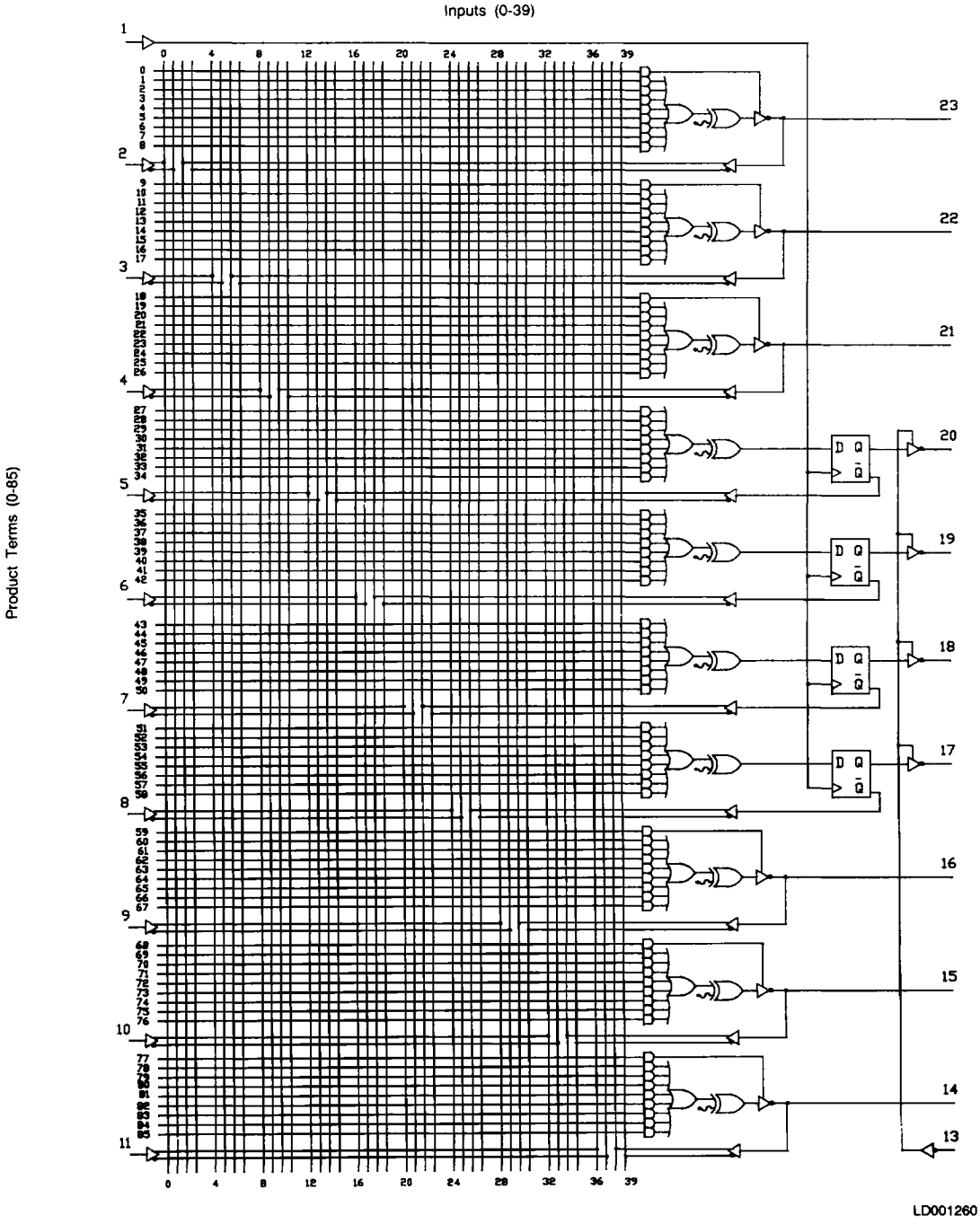


Figure 2. AmPAL20RP4 Logic Diagram

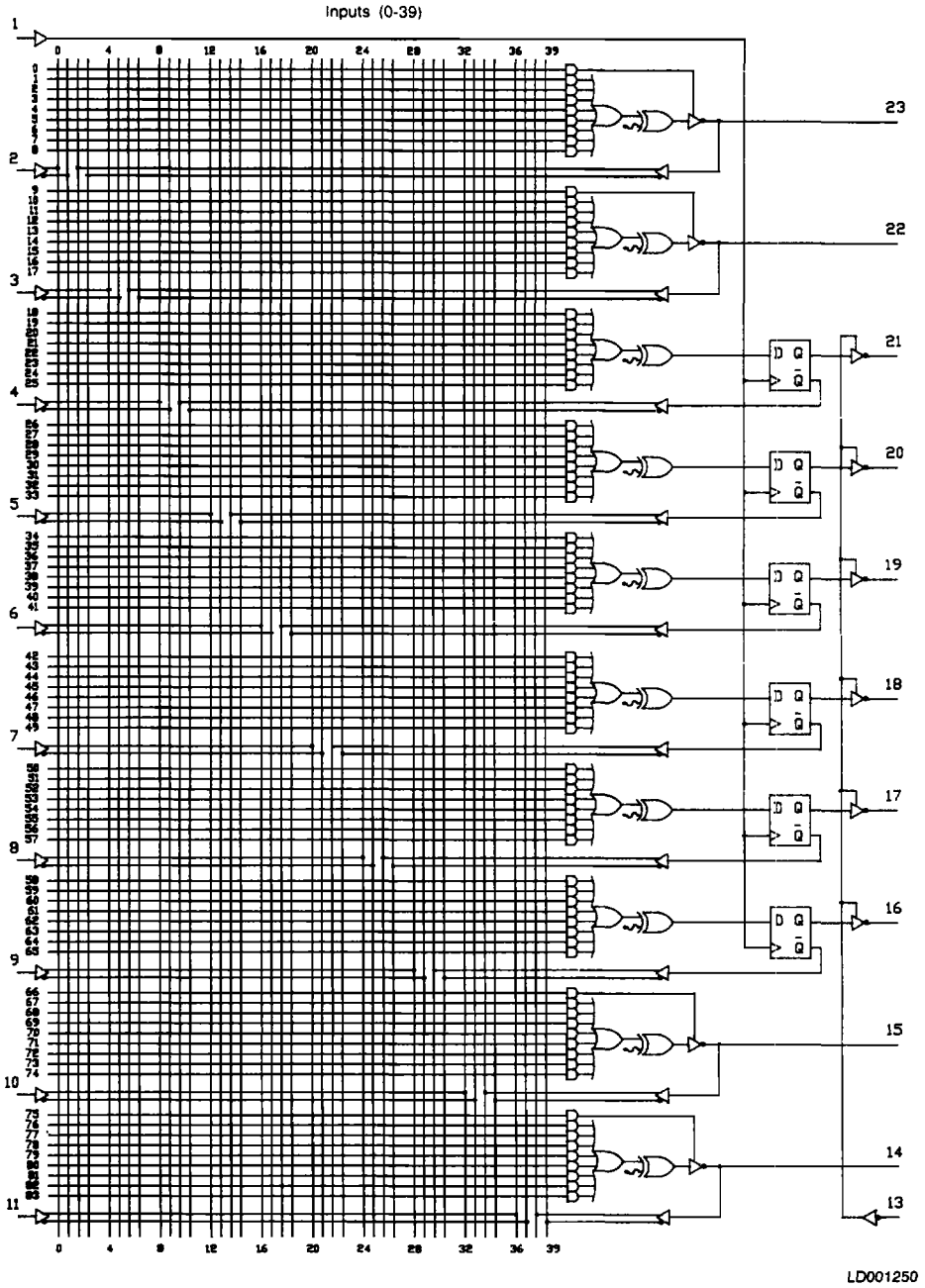


Figure 3. AmPAL20RP6 Logic Diagram

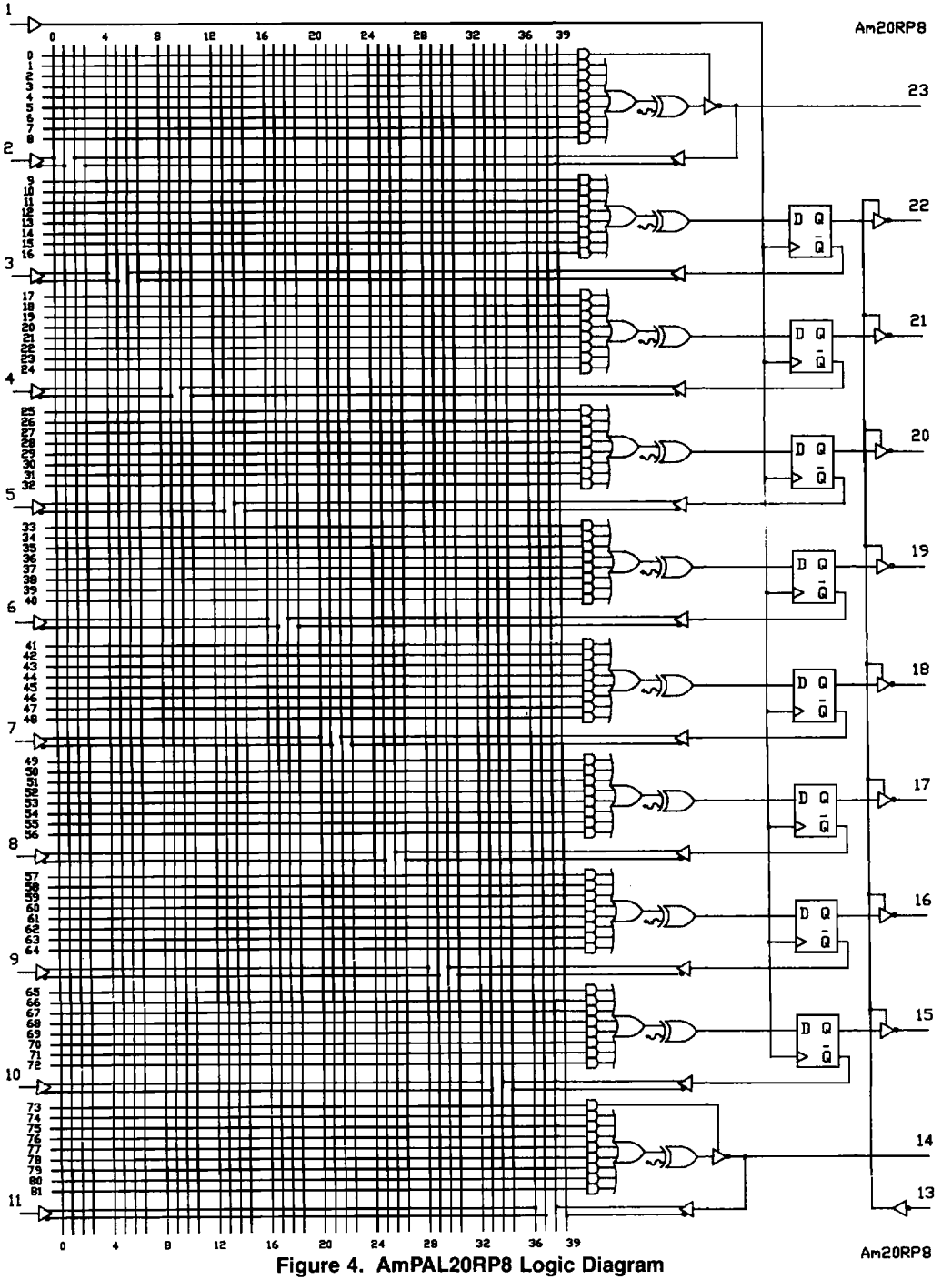


Figure 4. AmPAL20RP8 Logic Diagram

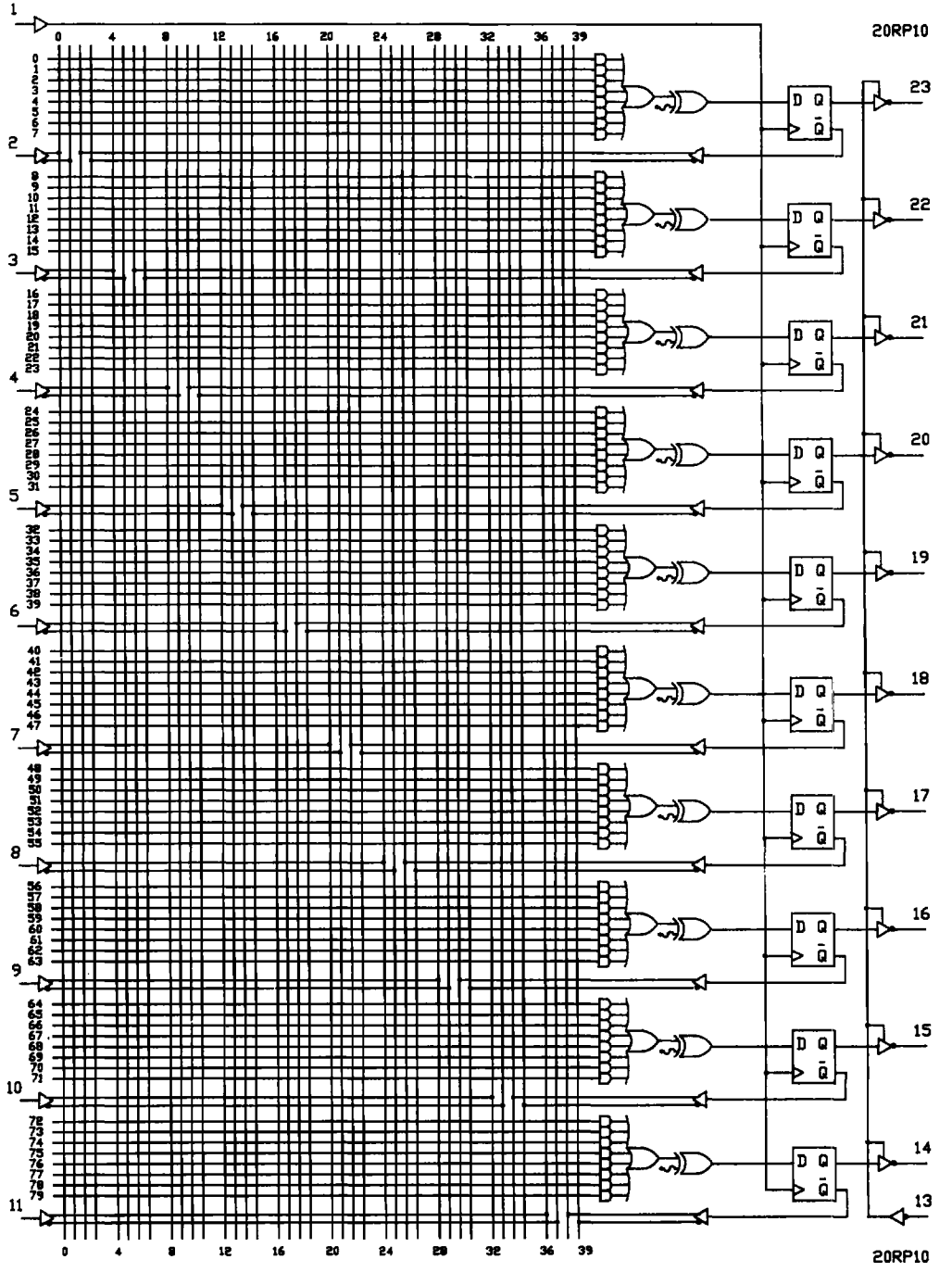


Figure 5. AmPAL20RP10 Logic Diagram

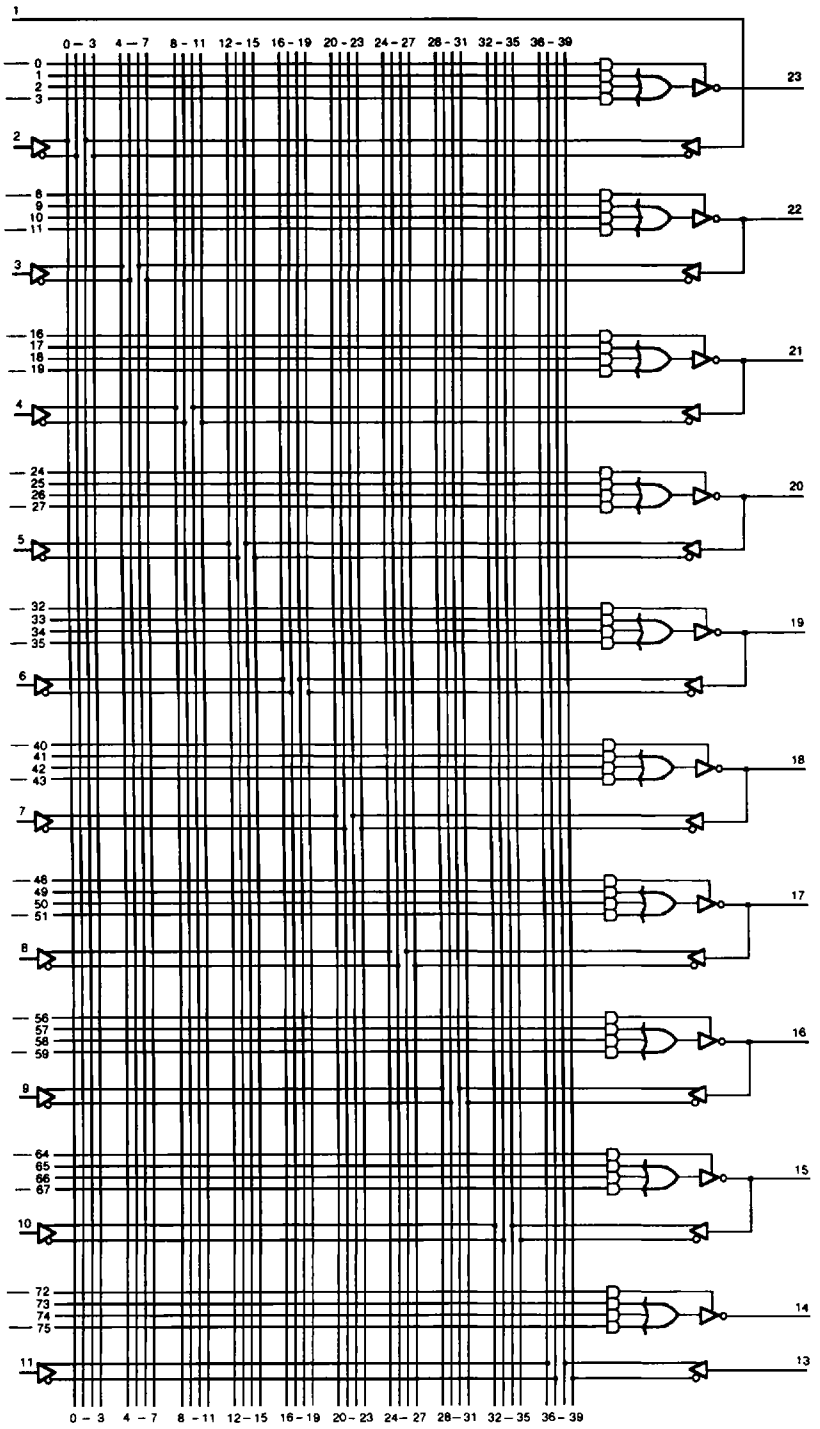
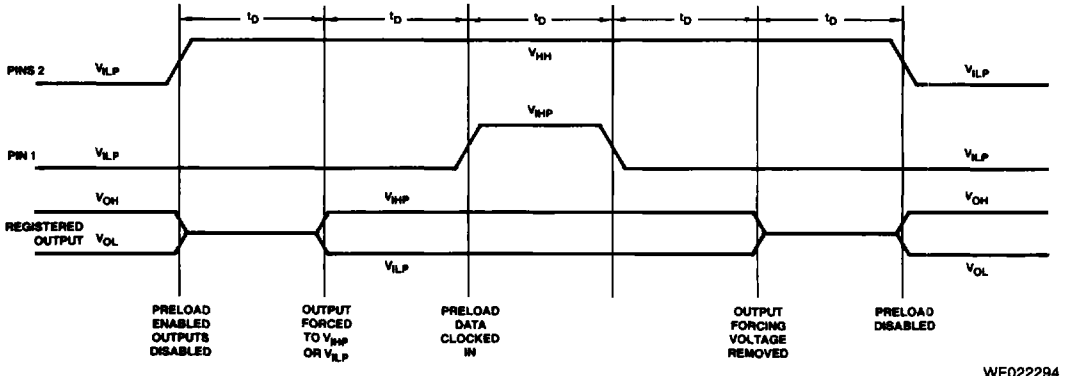


Figure 6. AmPAL20L10 Logic Diagram

PRELOAD of Registered Outputs

The AMD Enhanced 24-pin PAL devices incorporate circuitry to allow loading each register synchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



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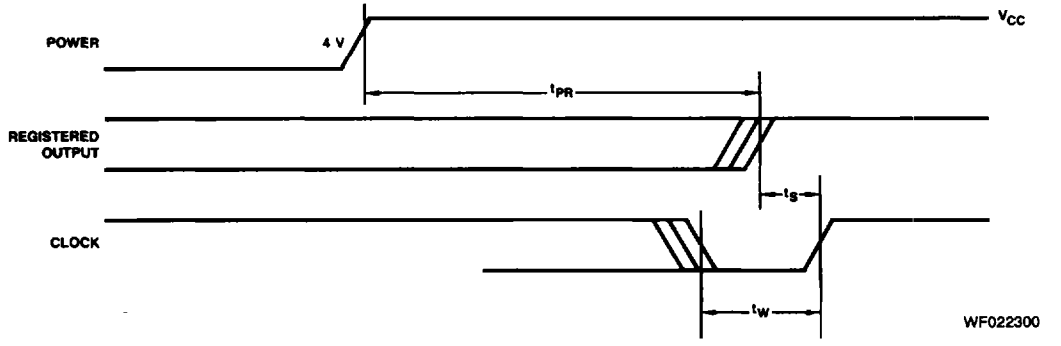
Par.	Min.	Max.
V_{HH}	10	12
V_{ILP}	0	0.5
V_{IHP}	2.4	5.5

Level forced on registered output pin during PRELOAD cycle	Register Q output state after cycle
V_{IHP}	HIGH
V_{ILP}	LOW

Power-Up Reset

The registered devices in the AMD Enhanced 24-Pin PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will be HIGH. This feature provides flexibility to the designer and is especially valuable in simplifying state-machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up RESET and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up RESET. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



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Parameters	Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up Reset Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	Clock Width				

Absolute Maximum Ratings

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5 V to +V_{CC} Max.
DC Voltage Applied to Outputs
During Programming ..... 16 V
Output Current Into Outputs During
Programming (Max Duration of 1 sec) ..... 200 mA
DC Input Voltage ..... −0.5 to +5.5 V
DC Input Current ..... −30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C) Devices
Temperature (T_A) ..... 0 to +75°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Extended Commercial (E) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Military (M) Devices*
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC Characteristics over operating range unless otherwise specified; included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted

Parameter Symbol	Parameter Description	Test Conditions				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −3.2 mA	COM'L	2.4	3.5		V
				I_{OH} = −2 mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 24 mA	COM'L			0.5	V
				I_{OL} = 12 mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs				2.0		5.5	V
V_{IL} (Note 2)	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs						0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.40 V					−20	−100	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V						25	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V						1.0	mA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 3)				−30	−60	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max.	20L10	COM'L	MIL				mA
				B	B			210	
				−20	−25			165	
				AL	AL			105	
			22P10, 20RP8, 20RP4, 20RP10 20RP6,	B	B			210	
				A	A			210	
				AL	AL			105	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA					−0.9	−1.2	V
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}		V_O = 2.7 V				100	μA
I_{OZL}				V_O = 0.4 V				−100	

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).

Capacitance*

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0 V @ f = 1 MHz	Pins 1, 13	11	pF
			Others	6	
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V @ f = 1 MHz		9	

*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Switching Characteristics

over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Commercial Range

No.	Parameter Symbol	Parameter Description	"B" Version			"A" & "AL" Versions			Units
			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 22P10, 20RP4, 20RP6, 20RP8			15			25	ns
2	t_{EA}	Input to Output Enable 22P10, 20RP4, 20RP6, 20RP8			18			25	ns
3	t_{ER}	Input to Output Disable 22P10, 20RP4, 20RP6, 20RP8			15			25	ns
4	t_{PZX}	Pin 13 to Output Enable 20RP4, 20RP6, 20RP8, 20RP10			15			20	ns
5	t_{PXZ}	Pin 13 to Output Disable 20RP4, 20RP6, 20RP8, 20RP10			12			20	ns
6	t_{CO}	Clock to Output 20RP4, 20RP6, 20RP8, 20RP10			12			15	ns
7	t_S	Input or Feedback Setup Time 20RP4, 20RP6, 20RP8, 20RP10	15			25			ns
8	t_H	Hold Time 20RP4, 20RP6, 20RP8, 20RP10	0			0			ns
9	t_P	Clock Period ($t_S + t_{CO}$)	27			40			ns
10	t_{WL}/t_{WH}	Clock Width	10/12			15/15			ns
11	$f_{MAX.}$	Maximum Frequency			37.0			25.0	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

Military Range

No.	Parameter Symbol	Parameter Description	"B" Version			"A" & "AL" Versions			Units
			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 22P10, 20RP4, 20RP6, 20RP8			20			30	ns
2	t_{EA}	Input to Output Enable 22P10, 20RP4, 20RP6, 20RP8			25			30	ns
3	t_{ER}	Input to Output Disable 22P10, 20RP4, 20RP6, 20RP8			20			30	ns
4	t_{PZX}	Pin 13 to Output Enable 20RP4, 20RP6, 20RP8, 20RP10			20			25	ns
5	t_{PXZ}	Pin 13 to Output Disable 20RP4, 20RP6, 20RP8, 20RP10			20			25	ns
6	t_{CO}	Clock to Output 20RP4, 20RP6, 20RP8, 20RP10			15			20	ns
7	t_S	Input or Feedback Setup Time 20RP4, 20RP6, 20RP8, 20RP10	20			30			ns
8	t_H	Hold Time 20RP4, 20RP6, 20RP8, 20RP10	0			0			ns
9	t_P	Clock Period ($t_S + t_{CO}$)	35			50			ns
10	t_{WL}/t_{WH}	Clock Width	12/12			20/20			ns
11	$f_{MAX.}$	Maximum Frequency			28.6			20.0	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50$ pF.
3. For three-state outputs, output enable times are tested with $C_L = 50$ pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5$ pF. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5$ V with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5$ V level with S_1 closed.

5

Switching Characteristics

over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

Commercial Range

No.	Parameter Symbol	Parameter Description	B Versions			−25 Versions (Note 4)			AL Versions			Units
			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 20L10			15			20			25	ns
2	t_{EA}	Input to Output Enable 20L10			18			20			25	ns
3	t_{ER}	Input to Output Disable 20L10			15			20			25	ns

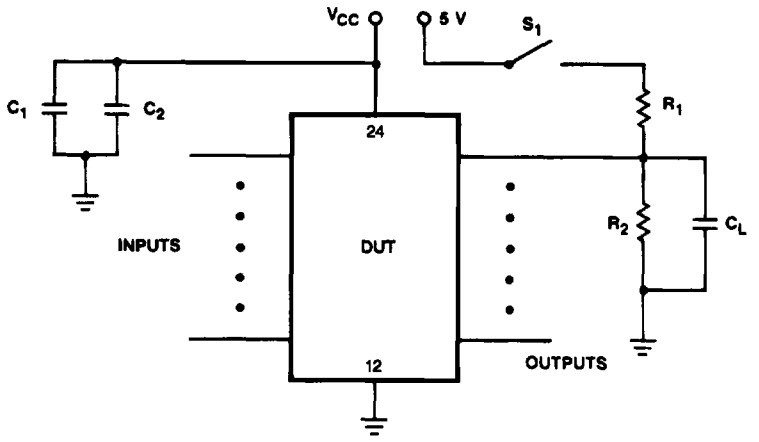
Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. t_{PD} is tested with switch S_1 closed and C_L = 50 pF.
3. For three-state outputs, output enable times are tested with C_L = 50 pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high impedance tests are made to an output voltage of V_{OH} − 0.5 V with S_1 open; LOW to high impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.
4. AmPAL20L10 only.

Military Range

No.	Parameter Symbol	Parameter Description	B Versions			−25 Versions (Note 4)			AL Versions			Units
			Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	Min.	Typ. (Note 1)	Max.	
1	t_{PD}	Input or Feedback to Non-Registered Output 20L10			20			25			30	ns
2	t_{EA}	Input to Output Enable 20L10			25			25			30	ns
3	t_{ER}	Input to Output Disable 20L10			20			25			30	ns

Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. t_{PD} is tested with switch S_1 closed and C_L = 50 pF.
3. For three-state outputs, output enable times are tested with C_L = 50 pF to the 1.5 V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5 pF. HIGH to high impedance tests are made to an output voltage of V_{OH} − 0.5 V with S_1 open; LOW to high impedance tests are made to the V_{OL} + 0.5 V level with S_1 closed.
4. AmPAL20L10 only.

Switching Test Circuit



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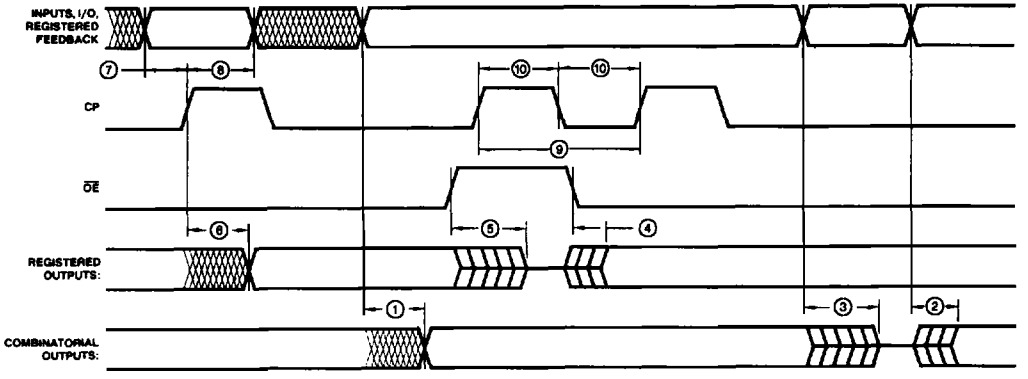
Note: C_1 and C_2 are to bypass V_{CC} to ground.

TEST OUTPUT LOADS		
Name	**Commercial**	**Military**
R_1	200 Ω	390 Ω
R_2	390 Ω	750 Ω
C_1	1 μF	1 μF
C_2	0.1 μF	0.1 μF
C_L	50 pF	50 pF

5

Switching Waveforms



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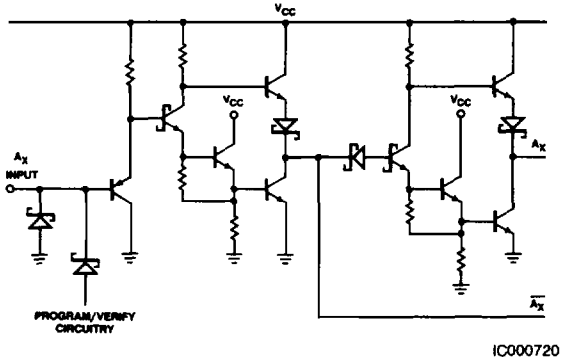
Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

Input Circuitry



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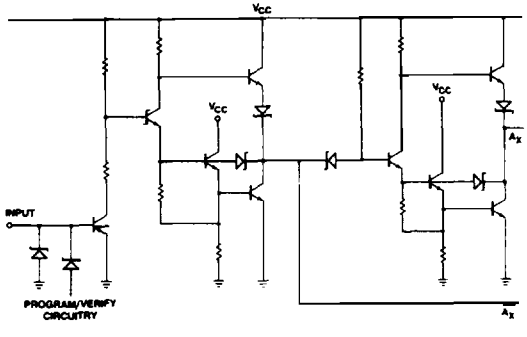
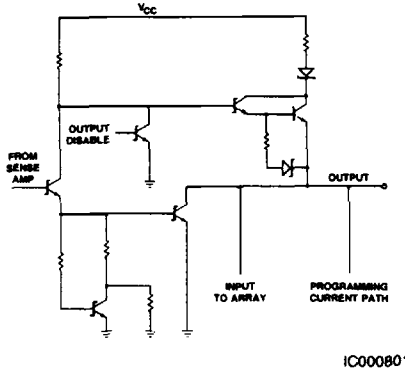
Output Circuitry





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Security Fuse Programming

A single fuse is provided on each device to prevent unauthorized copying of PAL device fuse patterns. Once blown, the circuitry enabling fuse verification and registered output PRELOAD is premanently disabled.

Programming of the security fuse is the same as an array fuse. Verification of a blown security fuse is accomplished by verifying the whole fuse array as if every fuse is blown.

Programmers/Development Systems

(refer to Programmer Reference Guide, page 3-81)