PowerPC 405CR Embedded Controller Data Sheet

Features

- IBM PowerPC™ 405 32-bit RISC processor core operating up to 266 MHz
  - Memory Management Unit
  - 16 KB instruction and 8 KB data caches
  - Multiply-Accumulate (MAC) function, including fast multiply unit
  - Programmable Timers
  - Supports JTAG for board level testing
- PC-100 Synchronous DRAM (SDRAM) interface operating up to 133 MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External Peripheral Bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, 16-, or 32-bit SRAM and external peripherals
  - Up to eight devices
  - External Mastering supported
- DMA support for external peripherals, internal UART and memory
  - Scatter-gather chaining supported
  - Four channels
- Programmable Interrupt Controller supports interrupts from a variety of sources
  - Supports 7 external and 10 internal interrupts
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to processor core
  - Programmable critical interrupt priority ordering
  - Programmable critical interrupt vector for faster vector processing
- Two serial ports (16550 compatible UART)
- One IIC (I^2C) interface
- General Purpose I/O (GPIO) available
- Internal Processor Local Bus (PLB) runs at SDRAM interface frequency

Description

The IBM PowerPC 405CR™ is a 32-bit RISC embedded controller. High performance, peripheral integration, and low cost make the device ideal for wired communications, network printers, and other computing applications.

This device is an easy upgrade for systems based on PowerPC 403xx embedded processors, while providing a base for custom chip designs.

The controller is powered by a PPC405 embedded core. This core tightly couples a 266-MHz CPU, MMU, I- and D-cache, and debug logic. Fine-tuning of the core reduces data transfer overhead, minimizes pipeline stalls, and greatly improves performance.

The PPC405CR employs the IBM CoreConnect™ bus architecture. This architecture, as implemented on the PPC405CR, consists of a 64-bit, 100-MHz Processor Local Bus (PLB) and a 32-bit, 50-MHz On-Chip Peripheral Bus (OPB).High-performance peripherals attach to the PLB; and less performance-critical peripherals attach to the OPB.

Technology: IBM CMOS SA12E 0.25 µm (0.18 µm L_{eff})

Package: 27 mm, 316-ball enhanced plastic ball grid array (E-PBGA)

Power (estimated): Typical 0.9 W, Maximum 2.0 W

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Ordering and PVR Information

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC405CR	IBM25PPC405CR-3BB200C	200MHz	27mm, 316 E-PBGA	B	0x40110041	0x22051049
PPC405CR	IBM25PPC405CR-3BB200CZ	200MHz	27mm, 316 E-PBGA	B	0x40110041	0x22051049
PPC405CR	IBM25PPC405CR-3BB266C	266MHz	27mm, 316 E-PBGA	B	0x40110041	0x22051049
PPC405CR	IBM25PPC405CR-3BB266CZ	266MHz	27mm, 316 E-PBGA	B	0x40110041	0x22051049
Note 1: Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.						

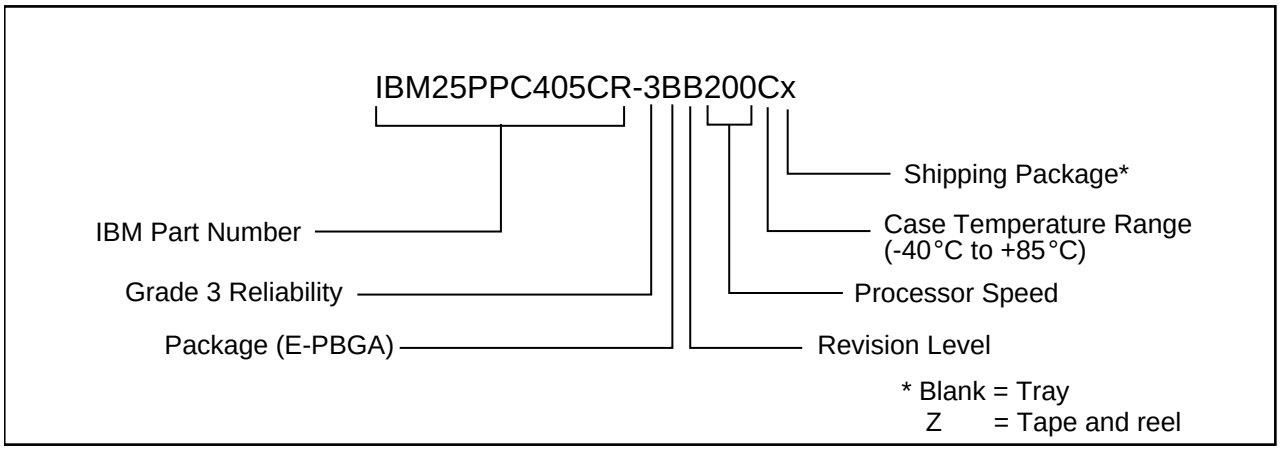
This section provides the part numbering nomenclature for the PPC405CR. For availability, contact your local IBM sales office.

The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

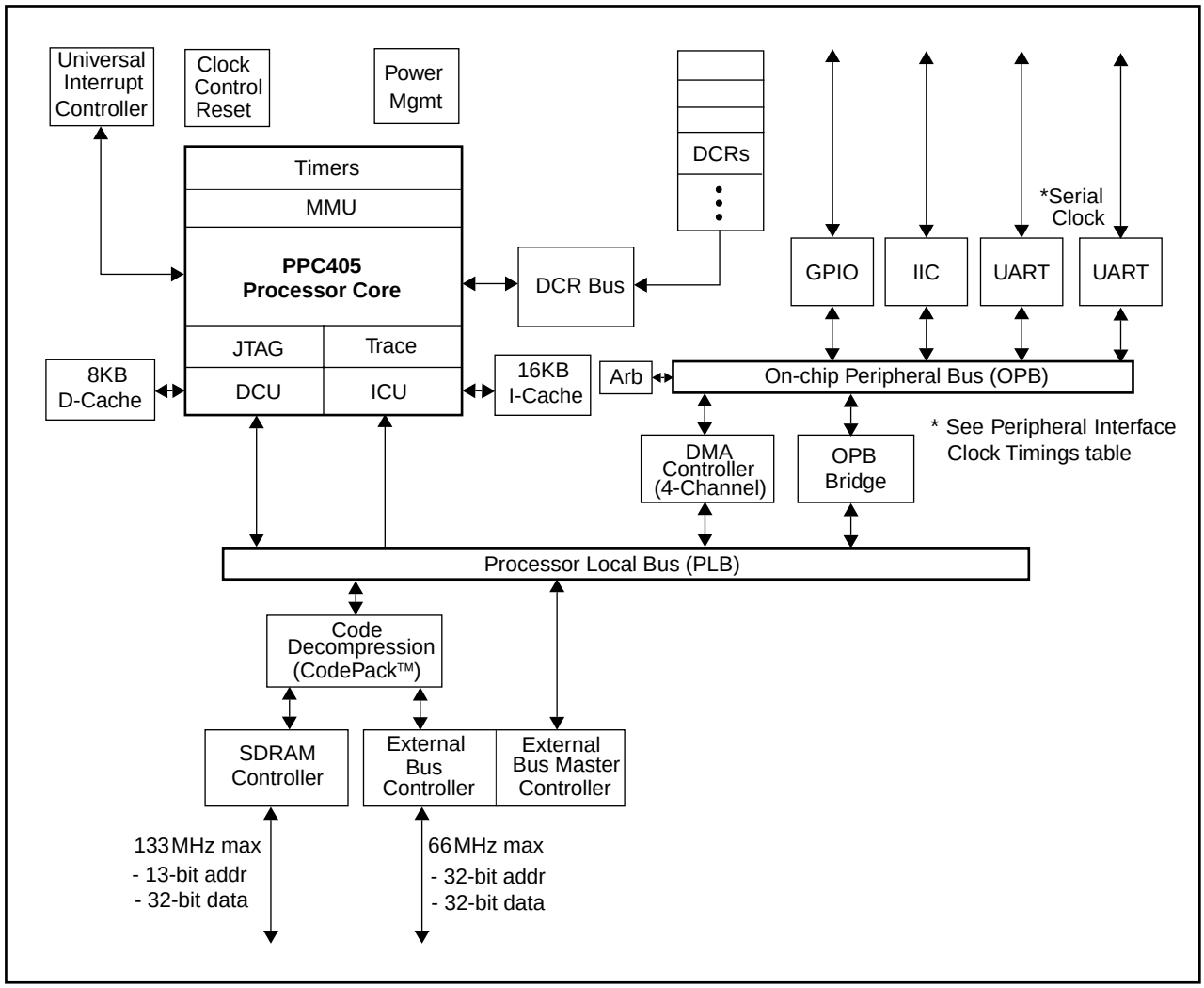
Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the PPC405CR User's Manual for details on the register content.

IBM Part Number Key



PPC405CR Embedded Controller Functional Block Diagram



The PPC405CR is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Note: IBM CoreConnect busses provide:

- 64-bit PLB interfaces up to 133MHz
- 32-bit OPB interfaces up to 66MHz

Address Map Support

The PPC405CR incorporates two simple and separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCR). This address map is accessed by software running on the PPC405CR processor through the use of MTDCR and MFDCR commands.

SysMem Memory Address Map 4GB System Memory

Function	Sub Function	Start Address	End Address	Size
Local Memory/Peripherals[1]		00000000	7FFFFFFF	2GB
Reserved		80000000	EF5FFFFF	
Internal Peripherals	Total	EF600000	EFFFFFFF	10MB
	UART0	EF600300	EF600307	8B
	Reserved	EF600308	EF6003FF	
	UART1	EF600400	EF600407	8B
	Reserved	EF600408	EF6004FF	
	IIC0	EF600500	EF60051F	32B
	Reserved	EF600520	EF6005FF	
	OPB Arbiter	EF600600	EF60063F	64B
	Reserved	EF600640	EF6006FF	
	GPIO Controller Registers	EF600700	EF60077F	128B
	Reserved	EF600780	EFFFFFFF	
Expansion ROM[2]		F0000000	FFDFFFFF	254MB
Boot ROM[2]		FFE00000	FFFFFFFF	2MB

Notes:

1. The Local Memory/Peripheral area of the memory map can be configured for SDRAM, ROM or Peripherals.
2. The Boot ROM and Expansion ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile SDRAM and SRAM in this region is supported by the controller it is not recommended that these regions be used for this purpose.

DCR Address Map 4KB Device Configuration Register

Function	Base Address Strap/Parameter	Start Address(0:9)	End Address(0:9)	Size
DCR Address Space[1]		000	3FF	1KW (4KB)[1]
Reserved		000	00F	16W
Memory Controller Registers	[0:8] = 000001000	010	011	2W
External Bus Controller Registers	[0:8] = 000001001	012	013	2W
Decompression Controller Registers	[0:8] = 000001010	014	015	2W
Reserved		016	07F	106W
PLB Registers	[0:5] = 000100	080	08F	16W
Reserved		090	09F	16W
OPB Bridge Out Registers	[0:6] = 000110 0	0A0	0A7	8W
Reserved		0A8	0AF	8W
Clock, Control and Reset	parm=0x0B0	0B0	0B7	8W
Power Management	parm=0x0B8	0B8	0BF	8W
Interrupt Controller	parm=0x0C0	0C0	0CF	16W
Reserved		0D0	0FF	48W
DMA Controller Registers	[0:3] = 0100	100	13F	64W
Reserved		140	3FF	704W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

SDRAM Memory Controller

The PPC405CR Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four logical banks. Up to 256MB per bank are supported, up to a maximum of 1GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address compare for each bank of memory
  - 4GB of address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- Up to 133MHz Memory, includes PC133 support
- 4MB to 256MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Sync DRAM configuration via mode set command
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard SEC/DED coverage
  - Aligned nibble error detect
  - Address error logging
  - Mixed ECC/non-ECC banks
  - Bypass mode

External Peripheral Bus Controller (EBC)

- Up to eight ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported
- Up to 50MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous

- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

UART

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses.
- All GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. Twenty-three GPIOs are multiplexed with:
  - 7 of 8 chip selects
  - All seven external interrupts
  - All nine instruction trace pins
- Each GPIO output is separately programmable to emulate an open drain driver (i.e., drives to zero, three-stated if output bit is 1).

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

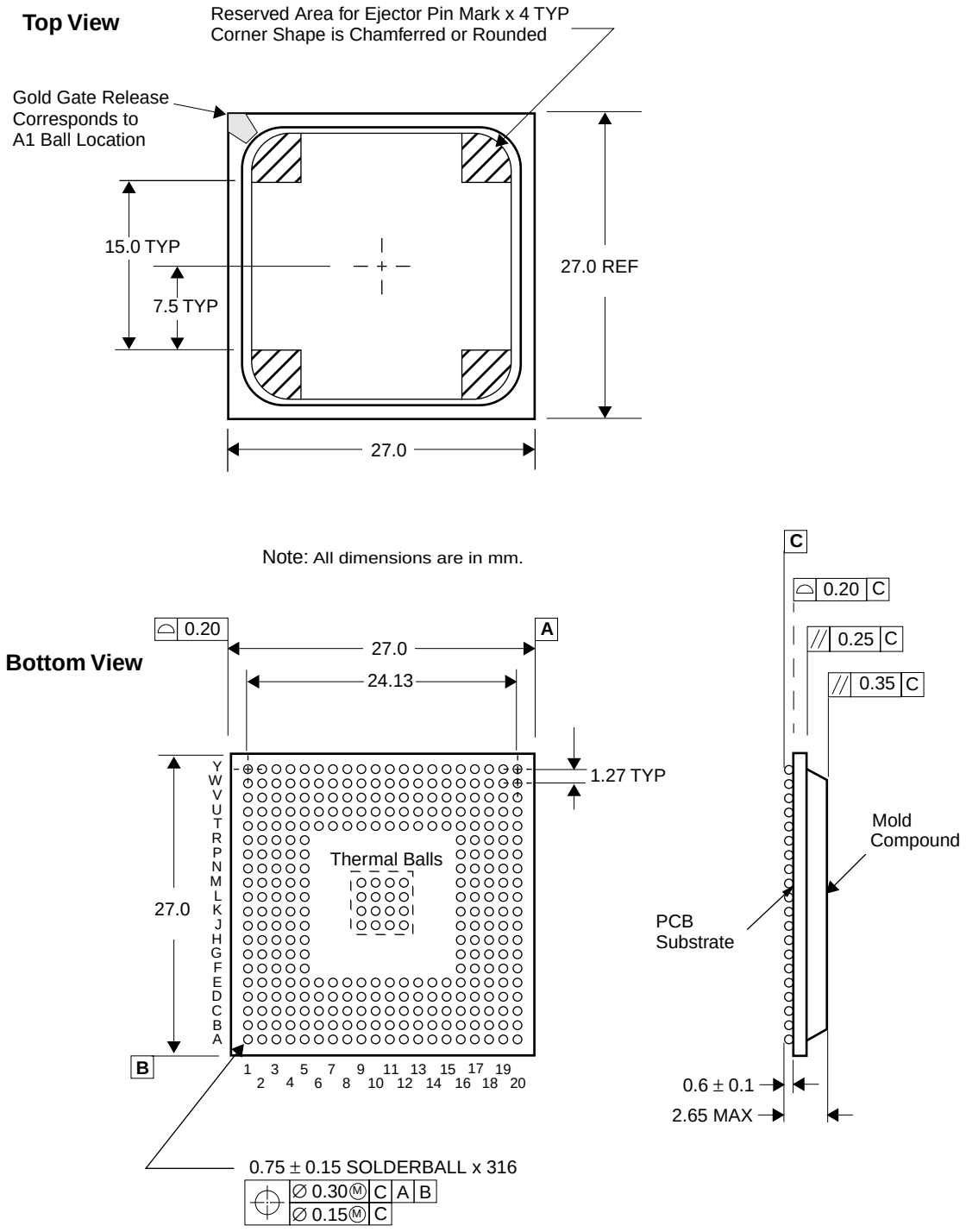
Features include:

- Supports 7 external and 10 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

JTAG

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

27mm, 316-Ball E-PBGA Package



Signals Listed Alphabetically

Signal Name	Ball	Interface Group	Page
AV_{DD}	E20	Power	29
BA0 BA1	J17 H18	SDRAM Interface	24
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	L19 N17 P17 U19	SDRAM Interface	24
BusReq	P2	External MASTER Peripheral Interface	26
$\overline{\text{CAS}}$	K17	SDRAM Interface	24
ClkEn0 ClkEn1	J19 G20	SDRAM Interface	24
DMAAck0 DMAAck1 DMAAck2 DMAAck3	C16 B17 B16 A14	External SLAVE Peripheral Interface	24
DMAReq0 DMAReq1 DMAReq2 DMAReq3	A19 C15 B15 A8	External SLAVE Peripheral Interface	24
DQM0 DQM1 DQM2 DQM3	U18 W14 Y10 U8	SDRAM Interface	24
DQMCB	V19	SDRAM Interface	24
DrvrInh1 DrvrInh2	F17 C19	System Interface	28
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	V17 Y18 U14 V13 Y13 V12 W11 V11	SDRAM Interface	24
EOT0[TC0] EOT1[TC1] EOT2[TC2] EOT3[TC3]	G4 F2 W1 Y2	External SLAVE Peripheral Interface	24
$\overline{\text{ExtAck}}$ $\overline{\text{ExtReq}}$ $\overline{\text{ExtReset}}$	U5 Y3 P4	External MASTER Peripheral Interface	26

Signals Listed Alphabetically (Continued)

Signal Name	Ball	Interface Group	Page
GND	A1 A6 A10 A15 A20 B2 B19 C3 C18 D4 D17 E5 E10 E11 E16 F1 F20 J9 J10 J11 J12 K5 K9 K10 K11 K12 K16 K20 L1 L5 L9 L10 L11 L12 L16 M9 M10 M11 M12 R1 R20	Power	29

Signals Listed Alphabetically (Continued)

Signal Name	Ball	Interface Group	Page
GND (cont)	T5 T10 T11 T16 U4 U17 V3 V18 W2 W19 Y1 Y6 Y11 Y15 Y20	Power	29
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]	B18 D16 C17 P18 T17 W18 Y19 W13 V6	System Interface	28
$\overline{\text{Halt}}$	E19	System Interface	28
HoldAck HoldPri HoldReq	T4 T3 V2	External MASTER Peripheral Interface	26
IICSCL	U15	Internal Peripheral Interface	26
IICSDA	W17	Internal Peripheral Interface	26
IRQ0[GPIO17] IRQ1[GPIO18] IRQ2[GPIO19] IRQ3[GPIO20] IRQ4[GPIO21] IRQ5[GPIO22] IRQ6[GPIO23]	D18 C20 E18 D20 G17 F18 W20	Interrupts Interface	27
MemAddr0 MemAddr1 MemAddr2 MemAddr3 MemAddr4 MemAddr5 MemAddr6 MemAddr7 MemAddr8 MemAddr9 MemAddr10 MemAddr11 MemAddr12	Y7 W7 V8 U7 Y4 U6 W4 V5 W3 V4 U3 V1 T2	SDRAM Interface	24

Signals Listed Alphabetically (Continued)

Signal Name	Ball	Interface Group	Page
MemClkOut0 MemClkOut1	H20 G18	SDRAM Interface	24
MemData0 MemData1 MemData2 MemData3 MemData4 MemData5 MemData6 MemData7 MemData8 MemData9 MemData10 MemData11 MemData12 MemData13 MemData14 MemData15 MemData16 MemData17 MemData18 MemData19 MemData20 MemData21 MemData22 MemData23 MemData24 MemData25 MemData26 MemData27 MemData28 MemData29 MemData30 MemData31	J18 K19 L20 M20 M19 L18 L17 N20 N19 M18 M17 P20 P19 N18 U20 T18 W16 Y17 Y16 V14 Y14 U12 W12 Y12 Y9 W9 V10 U10 Y8 W8 V9 U9	SDRAM Interface **Notes:** 1. MemData0 is the most significant bit (msb) 2. MemData31 is the least significant bit (lsb)	24
OV_{DD}	F5 G5 P5 R5 T6 T7 T14 T15 F16 G16 P16 R16 E6 E7 E14 E15	Power	29

Signals Listed Alphabetically (Continued)

Signal Name	Ball	Interface Group	Page
PerAddr0	A3	External SLAVE Peripheral Interface **Note:** PerAddr0 is the most significant bit (msb) on this bus.	24
PerAddr1	A4		
PerAddr2	B6		
PerAddr3	D7		
PerAddr4	C6		
PerAddr5	B7		
PerAddr6	D8		
PerAddr7	C7		
PerAddr8	B8		
PerAddr9	A7		
PerAddr10	D9		
PerAddr11	C8		
PerAddr12	B9		
PerAddr13	D10		
PerAddr14	C9		
PerAddr15	A9		
PerAddr16	B11		
PerAddr17	A11		
PerAddr18	B12		
PerAddr19	D11		
PerAddr20	A13		
PerAddr21	B13		
PerAddr22	C12		
PerAddr23	D12		
PerAddr24	B14		
PerAddr25	C13		
PerAddr26	D13		
PerAddr27	A16		
PerAddr28	C14		
PerAddr29	D14		
PerAddr30	A17		
PerAddr31	D15		
$\overline{\text{PerBLast}}$	E2	External SLAVE Peripheral Interface	24
PerClk	D3	External MASTER Peripheral Interface	26
$\overline{\text{PerCS0}}$	D6	External SLAVE Peripheral Interface	24
$\overline{\text{PerCS1}}$[GPIO10]	B5		
$\overline{\text{PerCS2}}$[GPIO11]	C5		
$\overline{\text{PerCS3}}$[GPIO12]	A5		
$\overline{\text{PerCS4}}$[GPIO13]	B10		
$\overline{\text{PerCS5}}$[GPIO14]	C10		
$\overline{\text{PerCS6}}$[GPIO15]	A12		
$\overline{\text{PerCS7}}$[GPIO16]	C11		

Signals Listed Alphabetically (Continued)

Signal Name	Ball	Interface Group	Page
PerData0	U2	External SLAVE Peripheral Interface **Note:** PerData0 is the most significant bit (msb) on this bus.	24
PerData1	R4		
PerData2	U1		
PerData3	R2		
PerData4	R3		
PerData5	T1		
PerData6	N4		
PerData7	P3		
PerData8	N2		
PerData9	P1		
PerData10	M4		
PerData11	N3		
PerData12	M2		
PerData13	N1		
PerData14	L4		
PerData15	M3		
PerData16	L2		
PerData17	M1		
PerData18	K2		
PerData19	L3		
PerData20	K1		
PerData21	J1		
PerData22	J2		
PerData23	K3		
PerData24	K4		
PerData25	H1		
PerData26	H2		
PerData27	J3		
PerData28	J4		
PerData29	G1		
PerData30	G2		
PerData31	H3		
PerErr	B1	External MASTER Peripheral Interface	26
$\overline{\text{PerOE}}$	E4	External SLAVE Peripheral Interface	24
PerPar0	C2	External SLAVE Peripheral Interface	24
PerPar1	G3		
PerPar2	E1		
PerPar3	H4		
PerReady	E3	External SLAVE Peripheral Interface	24
PerR/$\overline{\text{W}}$	C1	External SLAVE Peripheral Interface	24
$\overline{\text{PerWBE0}}$	D2	External SLAVE Peripheral Interface	24
$\overline{\text{PerWBE1}}$	F4		
$\overline{\text{PerWBE2}}$	F3		
$\overline{\text{PerWBE3}}$	D1		
$\overline{\text{PerWE}}$	C4		
$\overline{\text{RAS}}$	K18	SDRAM Interface	24
RcvrInh	E17	System Interface	28

Signals Listed Alphabetically (Continued)

Signal Name	Ball	Interface Group	Page
Reserved	G19 J20 R17 T20 V16	Other pins **Note:** G19 must be tied to OV_{DD} or GND. All other reserved pins should be left unconnected.	29
SysClk SysErr $\overline{\text{SysReset}}$	H17 A18 D19	System Interface	28
TCK TDI TDO	B4 A2 D5	JTAG Interface	27
TestEn	F19	System Interface	28
TmrClk	B20	System Interface	28
TMS	B3	JTAG Interface	27
$\overline{\text{TRST}}$	H19	JTAG Interface	27
$\overline{\text{UART0\_CTS}}$ $\overline{\text{UART0\_DCD}}$ $\overline{\text{UART0\_DSR}}$ $\overline{\text{UART0\_DTR}}$ $\overline{\text{UART0\_RI}}$ $\overline{\text{UART0\_RTS}}$ UART0_Rx UART0_Tx	W10 R18 U16 U13 V15 V20 T19 W15	Internal Peripheral Interface	26
$\overline{\text{UART1\_DSR}}$[$\overline{\text{UART1\_CTS}}$] $\overline{\text{UART1\_RTS}}$[$\overline{\text{UART1\_DTR}}$] UART1_Rx UART1_Tx	V7 W6 W5 Y5	Internal Peripheral Interface	26
UARTSerClk	R19	Internal Peripheral Interface	26
V_{DD}	E8 E9 E12 E13 H5 H16 J5 J16 M5 M16 N5 N16 T8 T9 T12 T13	Power	29
$\overline{\text{WE}}$	U11	SDRAM Interface	24

Signals Listed by Ball Assignment

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	GND	B10	$\overline{\text{PerCS4}}$[GPIO13]	C19	$\overline{\text{DrvrInh2}}$	E8	V_{DD}
A2	TDI	B11	PerAddr16	C20	IRQ1[GPIO18]	E9	V_{DD}
A3	PerAddr0	B12	PerAddr18	D1	$\overline{\text{PerWBE3}}$	E10	GND
A4	PerAddr1	B13	PerAddr21	D2	$\overline{\text{PerWBE0}}$	E11	GND
A5	$\overline{\text{PerCS3}}$[GPIO12]	B14	PerAddr24	D3	PerClk	E12	V_{DD}
A6	Gnd	B15	DMAReq2	D4	GND	E13	V_{DD}
A7	PerAddr9	B16	DMAAck2	D5	TDO	E14	OV_{DD}
A8	DMAReq3	B17	DMAAck1	D6	$\overline{\text{PerCS0}}$	E15	OV_{DD}
A9	PerAddr15	B18	GPIO1[TS1E]	D7	PerAddr3	E16	GND
A10	GND	B19	GND	D8	PerAddr6	E17	Rcrvinh
A11	PerAddr17	B20	TmrClk	D9	PerAddr10	E18	IRQ2[GPIO19]
A12	$\overline{\text{PerCS6}}$[GPIO15]	C1	PerR/W	D10	PerAddr13	E19	SysHalt
A13	PerAddr20	C2	PerPar0	D11	PerAddr19	E20	AV_{DD}
A14	DMAAck3	C3	GND	D12	PerAddr23	F1	GND
A15	GND	C4	$\overline{\text{PerWE}}$	D13	PerAdd26	F2	EOT1(TC1)
A16	PerAddr27	C5	$\overline{\text{PerCS2}}$[GPIO11]	D14	PerAddr29	F3	$\overline{\text{PerWBE2}}$
A17	PerAddr30	C6	PerAddr4	D15	PerAddr31	F4	$\overline{\text{PerWBE1}}$
A18	SysErr	C7	$\overline{\text{PerAddr7}}$	D16	GPIO2[TS2E]	F5	OV_{DD}
A19	DMAReq0	C8	PerAddr11	D17	GND	F16	OV_{DD}
A20	GND	C9	PerAddr14	D18	IRQ0[GPIO17]	F17	DrvrInh1
B1	PerErr	C10	$\overline{\text{PerCS5}}$[GPIO14]	D19	$\overline{\text{SysReset}}$	F18	IRQ5[GPIO22]
B2	GND	C11	$\overline{\text{PerCS7}}$[GPIO16]	D20	IRQ3[GPIO20]	F19	TestEn
B3	TMS	C12	PerAddr22	E1	PerPar2	F20	GND
B4	$\overline{\text{TCK}}$	C13	PerAddr25	E2	$\overline{\text{PerBLast}}$	G1	PerData29
B5	$\overline{\text{PerCS1}}$[GPIO10]	C14	PerAddr28	E3	PerReady	G2	PerData30
B6	PerAddr2	C15	DMAReq1	E4	$\overline{\text{PerOE}}$	G3	PerPar1
B7	PerAddr5	C16	$\overline{\text{DMAAck0}}$	E5	GND	G4	EOT0[TC0]
B8	PerAddr8	C17	GPIO3[TS1O]	E6	OV_{DD}	G5	OV_{DD}
B9	$\overline{\text{PerAddr12}}$	C18	GND	E7	OV_{DD}	G16	OV_{DD}

Signals Listed by Ball Assignment (Continued)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
G17	IRQ4[GPIO21]	K2	PerData18	M3	PerData15	P18	GPIO4[TS2O]
G18	MemClkout1	K3	PerData23	M4	PerData10	P19	MemData12
G19	Reserved	K4	PerData24	M5	V_{DD}	P20	MemData11
G20	ClkEn1	K5	GND	M9	Thermal Ball	R1	GND
H1	PerData25	K9	Thermal Ball	M10	Thermal Ball	R2	PerData3
H2	PerData26	K10	Thermal Ball	M11	Thermal Ball	R3	PerData4
H3	PerData31	K11	Thermal Ball	M12	Thermal Ball	R4	PerData1
H4	PerPar3	K12	Thermal Ball	M16	V_{DD}	R5	OV_{DD}
H5	V_{DD}	K16	$\overline{GND}$	M17	MemData10	R16	OV_{DD}
H16	V_{DD}	K17	$\overline{CAS}$	M18	MemData9	R17	Reserved
H17	SysClk	K18	$\overline{RAS}$	M19	MemData4	R18	$\overline{UART0\_DCD}$
H18	BA1	K19	MemData1	M20	MemData3	R19	UARTSerClk
H19	$\overline{TRST}$	K20	GND	N1	PerData13	R20	GND
H20	MemClkout0	L1	GND	N2	PerData8	T1	PerData5
J1	PerData21	L2	PerData16	N3	PerData11	T2	MemAddr12
J2	PerData22	L3	PerData19	N4	PerData6	T3	HoldPri
J3	PerData27	L4	PerData14	N5	V_{DD}	T4	HoldAck
J4	PerData28	L5	GND	N16	V_{DD}	T5	GND
J5	V_{DD}	L9	Thermal Ball	N17	$\overline{BankSel1}$	T6	OV_{DD}
J9	Thermal Ball	L10	Thermal Ball	N18	MemData13	T7	OV_{DD}
J10	Thermal Ball	L11	Thermal Ball	N19	MemData8	T8	V_{DD}
J11	Thermal Ball	L12	Thermal Ball	N20	MemData7	T9	V_{DD}
J12	Thermal Ball	L16	GND	P1	PerData9	T10	GND
J16	V_{DD}	L17	MemData6	P2	BusReq	T11	GND
J17	BA0	L18	MemData5	P3	PerData7	T12	V_{DD}
J18	MemData0	L19	$\overline{BankSel0}$	P4	$\overline{ExtReset}$	T13	V_{DD}
J19	$\overline{ClkEn0}$	L20	MemData2	P5	OV_{DD}	T14	OV_{DD}
J20	Reserved	M1	PerData17	P16	OV_{DD}	T15	OV_{DD}
K1	PerData20	M2	PerData12	P17	$\overline{BankSel2}$	T16	$\overline{GND}$

Signals Listed by Ball Assignment (Continued)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
T17	GPIO5 (TS3)	U18	DQM0	V19	DQMfsCB	W20	IRQ6[GPIO23]
T18	MemData15	U19	$\overline{\text{BankSel3}}$	V20	$\overline{\text{UART0\_RTS}}$	Y1	GND
T19	UART0_RX	U20	MemData14	W1	EOT2[TC2]	Y2	EOT3[TC3]
T20	Reserved	V1	MemAddr11	W2	$\overline{\text{GND}}$	Y3	$\overline{\text{ExtReq}}$
U1	PerData2	V2	HoldReq	W3	$\overline{\text{MemAdd8}}$	Y4	MemAddr4
U2	PerData0	V3	GND	W4	MemAdd6	Y5	UART1_TX
U3	MemAddr10	V4	MemAddr9	W5	UART1_RX	Y6	GND
U4	GND	V5	MemAddr7	W6	$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]	Y7	MemAddr0
U5	$\overline{\text{ExtAck}}$	V6	GPIO9[TrcClk]	W7	MemAddr1	Y8	MemData28
U6	MemAddr5	V7	$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]	W8	MemData29	Y9	MemData24
U7	MemAddr3	V8	MemAddr2	W9	MemData25	Y10	DQM2
U8	$\overline{\text{DQM3}}$	V9	MemData30	W10	$\overline{\text{UART0\_CTS}}$	Y11	GND
U9	MemData31	V10	MemData26	W11	ECC6	Y12	MemData23
U10	MemData27	V11	ECC7	W12	MemData22	Y13	ECC4
U11	$\overline{\text{WE}}$	V12	ECC5	W13	GPIO8[TS6]	Y14	MemData20
U12	MemData21	V13	ECC3	W14	DQM1	Y15	GND
U13	$\overline{\text{UART0\_DTR}}$	V14	MemData19	W15	UART0_TX	Y16	MemData14
U14	ECC2	V15	$\overline{\text{UART0\_RI}}$	W16	MemData1	Y17	MemData17
U15	IIC_SCL	V16	Reserved	W17	IIC_SDA	Y18	ECC1
U16	$\overline{\text{UART0\_DSR}}$	V17	ECC0	W18	GPIO6[TS4]	Y19	GPIO7[TS5]
U17	GND	V18	GND	W19	GND	Y20	GND

Pin Lists

The PPC405CR embedded controller is packaged in a 456-ball enhanced plastic ball grid array (E-PBGA). The following tables describe the package level pinout.

Pin Summary

Group	No. of Pins
SDRAM	71
External Peripheral	97
External Master	9
Internal Peripheral	15
Interrupts	7
JTAG	5
System	18
Total Signal Pins	**222**
AV_{DD}	1
OV_{DD}	16
V_{DD}	16
Gnd	40
Thermal (and Gnd)	16
Reserved	5
Total Pins	**316**

In the table “Signal Functional Description” on page 24, each I/O signal is listed along with a short description of the signal function. Some signals are multiplexed onto the same pin (ball) so that the pin is usable for different functions. Multiplexed signals are shown in square brackets following the default signal (for example, C0:3[$\overline{BE0:3}$]) and described consecutively within each pin functional description. Active-low signals such as $\overline{BE0:3}$ are marked with an overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. These pins are described in the table using a single row with a text description that indicates the different functional uses of the pin. For example, the EBC peripheral controller address pins are used as outputs by the PPC405CR to broadcast an address to external slave devices when the PPC405CR has control of the external bus. When during the course of normal chip operation an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC405CR.

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 39). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

The following table lists all of the I/O signals provided by the PPC405CR. Please refer to “Signals Listed Alphabetically” on page 13 for the pin number to which each signal is assigned.

Signal Functional Description (Part 1 of 6)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
SDRAM Interface				
MemData0:31	Memory Data bus **Notes:** 1. MemData0 is the most significant bit (msb) 2. MemData31 is the least significant bit (lsb)	I/O	3.3V LVTTL	4
MemAddr12:0	Memory Address bus	O	3.3V LVTTL	
BA0:1	Bank Address supporting up to four internal banks	O	3.3V LVTTL	
$\overline{\text{RAS}}$	Row Address Strobe	O	3.3V LVTTL	
$\overline{\text{CAS}}$	Column Address Strobe	O	3.3V LVTTL	
DQM0:3	DQM for byte lanes 0 (MemData0:7), 1 (MemData8:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
DQMCB	DQM for ECC check bits	O	3.3V LVTTL	
ECC0:7	ECC check bits 0:7	I/O	3.3V LVTTL	4
$\overline{\text{BankSel0:3}}$	Select up to four external SDRAM banks	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable	O	3.3V LVTTL	
ClkEn0:1	SDRAM Clock Enable	O	3.3V LVTTL	
MemClkOut0:1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attach without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
External SLAVE Peripheral Interface				
PerData0:31	Peripheral data bus used by PPC405CR when not in external master mode, otherwise used by external master **Note:** PerData0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerAddr0:31	Peripheral address bus used by PPC405CR when not in external master mode, otherwise used by external master. **Note:** PerAddr0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerPar0:3	Peripheral byte parity signals	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:3}}$ $\overline{\text{PerWE}}$	As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either peripheral controller or DMA controller depending upon the type of transfer involved. Used as inputs when external bus master owns the external interface	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerCS0}}$	Peripheral chip select bank 0	O	5V tolerant 3.3V LVTTL	2

Signal Functional Description (Part 2 of 6)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PerCS1:7}}$[GPIO10:16]	Seven additional peripheral chip selects or General Purpose I/O - To access this function, software must toggle a DCR register bit.	O[I/O]	5V tolerant 3.3V LVTTL	1,2
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC405CR is the bus master, it enables the selected SDRAMs to drive the bus.	O	5V tolerant 3.3V LVTTL	2
PerR/$\overline{\text{W}}$	Used by the PPC405CR when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise it used by the external master as an input to indicate the direction of transfer.	I/O	5V tolerant	1, 2
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant Rcvr	1, 2
$\overline{\text{PerBLast}}$	Used by the PPC405CR when not in external master mode, otherwise used by external master. Indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 4
DMAReq0:3	DMAReq0:3 are used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant Rcvr	1, 5
DMAAck0:3	DMAAck0:3 are used by the PPC405CR to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	6
EOT0:3[TC0:3]	End Of Transfer/Terminal Count	I/O	5V tolerant 3.3V LVTTL	1, 5

Signal Functional Description (Part 3 of 6)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External MASTER Peripheral Interface				
PerClk	Peripheral clock to be used by an external master and by synchronous peripheral slaves	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReset}}$	Peripheral reset to be used by an external master and by synchronous peripheral slaves	O	5V tolerant 3.3V LVTTL	
HoldReq	Hold Request, used by an external master to request ownership of the peripheral bus	I	5V tolerant Rcvr	1, 5
HoldAck	Hold Acknowledge, used by the PPC405CR to transfer ownership of peripheral bus to an external master	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{ExtReq}}$	$\overline{\text{ExtReq}}$ is used by an external master to indicate it is prepared to transfer data	I	5V tolerant Rcvr	1, 4
$\overline{\text{ExtAck}}$	$\overline{\text{ExtAck}}$ is used by the PPC405CR to indicate that a data transfer occurred.	O	5V tolerant 3.3V LVTTL	6
HoldPri	Used by an external master to indicate the priority of a given transfer (0 = high, 1 = low)	I	5V tolerant Rcvr	1, 4
BusReq	Used when the PPC405CR needs to regain control of peripheral interface from an external Master	O	5V tolerant 3.3V LVTTL	
PerErr	Used as an input used to record external Master errors and external slave peripheral errors	I	5V tolerant Rcvr	1, 5
Internal Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either UART.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Rx	UART0 Serial Data In	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Tx	UART0 Serial Data Out	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator	I	5V tolerant 3.3V LVTTL Rcvr	1, 4

Signal Functional Description (Part 4 of 6)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
UART1_Rx	UART1 Serial In data	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
UART1_Tx	UART1 Serial Out data.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]	UART1 Data Set Ready or UART1 Clear To Send. To access this function, software must toggle a DCR register bit.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]	UART1 Request To Send or UART1 Data Terminal Ready. To access this function, software must toggle a DCR register bit.	O	5V tolerant 3.3V LVTTL	6
IICSCL	IIC Serial Clock	I/O	5V tolerant 3.3V LVTTL	1, 2
IICSDA	IIC Serial Data	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
IRQ0:6[GPIO17:23]	Interrupt requests or General Purpose I/O. To access this function, software must toggle a DCR register bit.]	I[I/O]	5V tolerant 3.3V LVTTL	1, 5
JTAG Interface				
TDI	Test data in	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
TMS	JTAG test mode select	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
TDO	Test data out	O	5V tolerant 3.3V LVTTL	
TCK	JTAG test clock	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
$\overline{\text{TRST}}$	JTAG reset	I	5V tolerant Rcvr	5

Signal Functional Description (Part 5 of 6)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main system clock input	I	5V tolerant 3.3V LVTTL Rcvr	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to start a system reset. The PPC405CR then holds the output low for 8192 cycles to reset all internal and external logic connected to $\overline{\text{SysReset}}$. A system reset can also be initiated by software.	I/O	5V tolerant 3.3V LVTTL Rcvr	1, 2
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
GPIO1[TS1E] GPIO2[TS2E]	General Purpose I/O or Even Trace execution status.To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO3[TS1O] GPIO4[TS2O]	General Purpose I/O or Odd Trace execution status. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1 (A22, AF18), 6 (AF18 only)
GPIO5:8[TS3:6]	General Purpose I/O Trace status. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 4
GPIO9[TrcClk]]	General Purpose I/O or Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 4
TestEn	Test Enable	I	5V tolerant Rcvr w/ PD	3
RcvrInh	Receiver Inhibit. Set to 1 for normal operation. Setting to 0 disables all inputs for test purposes.	I	5V tolerant Rcvr	2
DrvrInh1:2	Driver Inhibit 1 and 2. Set to 1 for normal operation. Setting to 0 disables all outputs for test purposes.	I	5V tolerant Rcvr	2
TmrClk	This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). In most cases this input toggles much slower (in the 1MHz to 10MHz range).	I	5V tolerant 3.3V LVTTL Rcvr	1, 4

Signal Functional Description (Part 6 of 6)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Power				
GND	Ground **Note:** Pins J9–J12, K9–K12, L9–L12, and M9–M12 are also thermal balls.	I		
AV_{DD}	Filtered voltage input for PLL (analog) circuits	I		
OV_{DD}	Output driver voltage—3.3V	I		
V_{DD}	Logic voltage—2.5V	I		
Other pins				
Reserved	Ex cept for G19, do not connect signals, voltage, or ground to these pins. G19 must be tied to OV_{DD} or GND.			

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to 2.7[1]	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to 3.6[1]	V
PLL Supply Voltage	AV_{DD}	0 to 2.7	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to 3.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to 5.5	V
Storage Temperature Range	T_{STG}	-55 to 150	°C
Case temperature under bias	T_C	-40 to +120	°C

Notes:

1. If $OV_{DD} \geq 0.4$V it is required that $V_{DD} \geq 0.4$V. Supply excursions not meeting this criteria must be limited to less than 25ms duration during each power up or power down event.

Package Thermal Specifications

The PPC405CR is designed to operate within a case temperature range of -40˚C to 120˚C. Thermal resistance values for the E-PBGA package in a convection environment are as follows:

Parameter	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
Junction-to-case thermal resistance	θ_{JC}	2	2	2	°C/W
Case-to-ambient thermal resistance (without heat sink)	θ_{CA}	18	16	15	°C/W

Notes:

1. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
2. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
3. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.
4. The above assumes that the chip is mounted on a card with at least one signal and two power planes.

Recommended DC Operating Conditions

Note: Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	
PLL Supply Voltage	AV_{DD}	2.3	2.5	2.7	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	2.0		OV_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	2.0		5.5	V	
Input Logic Low	V_{IL}	0		0.8	V	
Output Logic High	V_{OH}	2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		400 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	–250 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V or 5.0V receivers)	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot (3.3V and 5.0V receivers)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		85	°C	

Capacitance

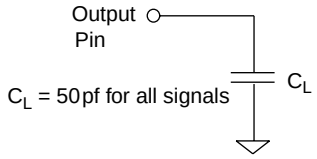
Parameter	Symbol	Maximum	Unit	Notes
Input Capacitance Group 1 (3.3V LVTTL //O)	C_{IN1}	2.5	pF	
Input Capacitance Group 2 (5V tolerant LVTTL I/O)	C_{IN2}	3.5	pF	
Input Capacitance Group 3	C_{IN3}	5.0	pF	
Input Capacitance Group 1 (RX only pins)	C_{IN4}	0.75	pF	

DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current (V_{DD})	I_{DD}		TBD		mA
Active Operating Current (OV_{DD})	I_{ODD}		TBD		mA
PLL Voltage	V_{PLL}	2.3	2.5	2.7	V
PLL V_{DD} Input current	I_{PLL}		16	23	mA

Test Conditions

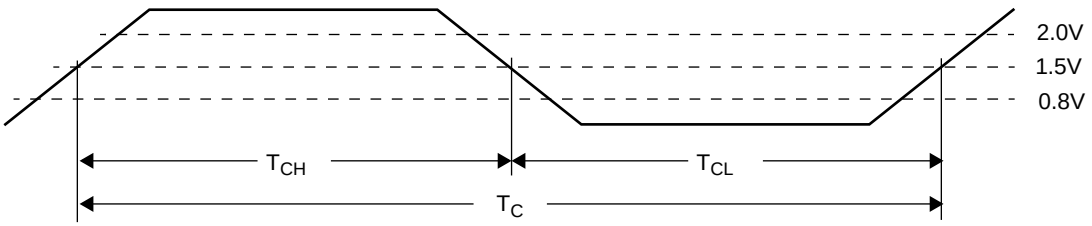
Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at V_{DD} = 3.14V and T_J = 100˚C with the 50pF test load (C_L) shown in the figure at right.



SysClk and MemClk Timing

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	25	66.6	MHz
T_C	SysClk clock period	15	40	ns
T_{CS}	Clock edge stability	–	0.15	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClk Output				
F_C	MemClk clock output frequency—200MHz		100	MHz
T_C	MemClk clock period—200MHz	10		ns
F_C	MemClk clock output frequency—266MHz		133	MHz
T_C	MemClk clock period—266MHz	7.5		ns
T_{CH}	Clock output high time	35% of nominal period	65% of nominal period	ns
T_{CL}	Clock output low time	35% of nominal period	65% of nominal period	ns

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC405CR. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC405CR the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405CR with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC405CR peripherals impose more stringent requirements (see Note 1).
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClk since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates.

2. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the PPC405CR meets the above requirements and does not adversely affect other aspects of the system.

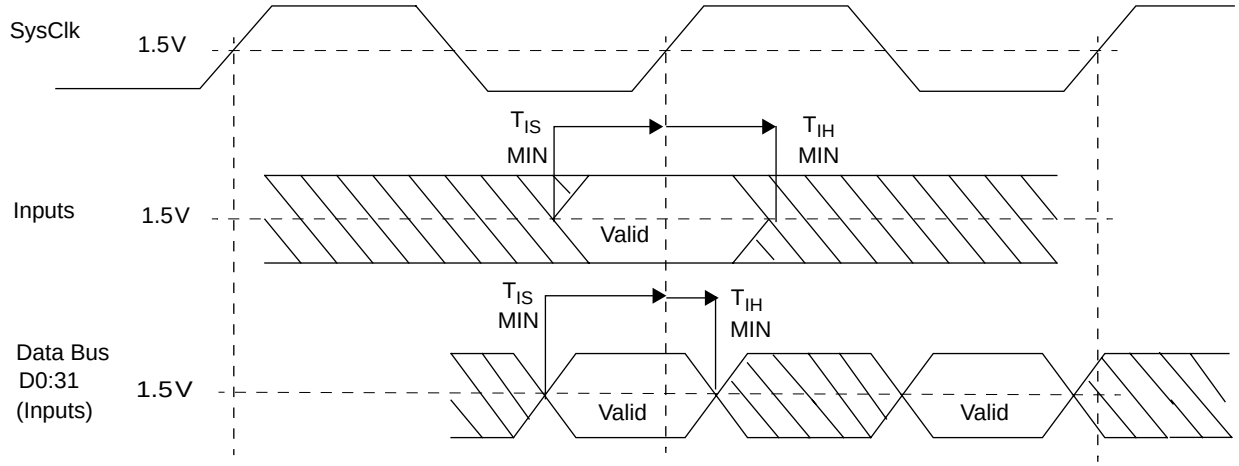
Peripheral Interface Clock Timings

Parameter	Min	Max	Units
PerClk output frequency—200 MHz (for external master or synchronous slaves)	–	50	MHz
PerClk period—200 MHz	20	–	ns
PerClk output frequency—266 MHz (for external master or synchronous slaves)	–	66	MHz
PerClk period—266 MHz	15	–	ns
PerClk output high time	50% of nominal period	66% of nominal period	ns
PerClk output low time	33% of nominal period	50% of nominal period	ns
UARTSerClk input frequency (Note 1)	–	$1000/(2T_{OPB}+2ns)$	MHz
UARTSerClk period	$2T_{OPB}+2$	–	ns
UARTSerClk input high time	$T_{OPB}+1$	–	ns
UARTSerClk input low time	$T_{OPB}+1$	–	ns
TmrClk input frequency—200 MHz	–	50	MHz
TmrClk period—200 MHz	20	–	ns
TmrClk input frequency—266 MHz	–	66	MHz
TmrClk period—266 MHz	15	–	ns
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns

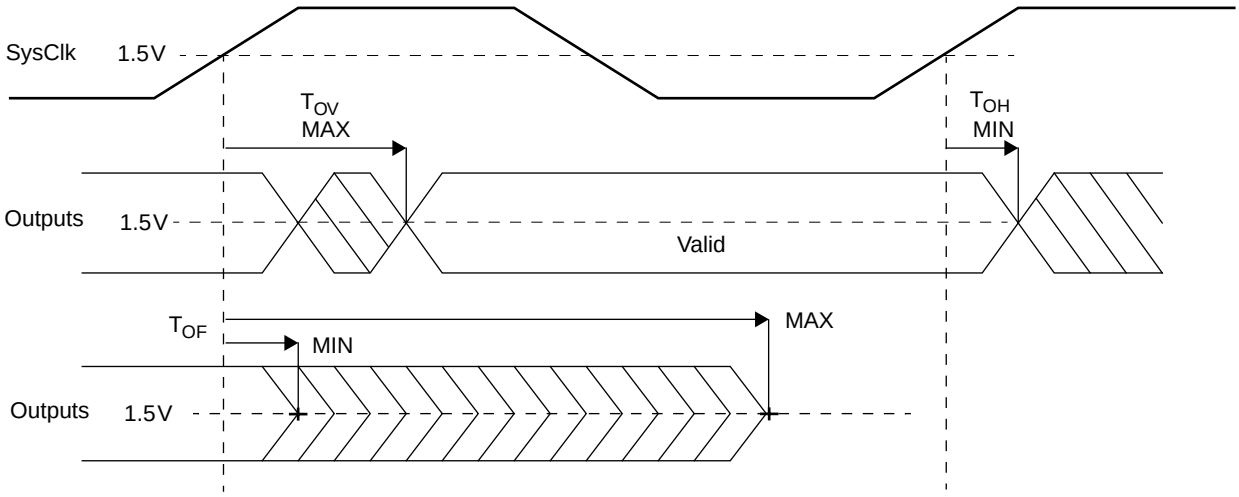
Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 50 MHz for 200 MHz parts and 66 MHz.for 266 MHz parts.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—All

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
Internal Peripheral Interface								
IICSCL	na	na	na	na	19	12		
IICSDA	na	na	na	na	19	12		
UART0_CTS	na	na			12	8		
UART0_DCD	na	na			12	8		
UART0_DSR	na	na			12	8		
UART0_DTR					12	8		
UART0_RI	na	na			12	8		
UART0_RTS			na	na	12	8		
UART0_Rx	na	na			12	8		
UART0_Tx			na	na	12	8		
UART1_RTS [UART1_DTR]			na	na	12	8		
UART1_DSR [UART1_CTS]	na	na			n/a	n/a		
UART1_Rx	na	na			n/a	n/a		
UART1_Tx			na	na	12	8		
UARTSerClk	na	na			n/a	n/a		
Interrupts Interface								
IRQ0:6[GPIO17:23]					12	8		
JTAG Interface								
TCK					n/a	n/a		async
TDI					n/a	n/a		async
TDO					12	8		async
TMS					n/a	n/a		async
TRST					n/a	n/a		async
System Interface								
DrvrInh1:2	dc	dc	n/a	n/a	n/a	n/a		
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]					12	8		
Halt	dc	dc	n/a	n/a	n/a	n/a		async
RcvrInh	dc	dc	n/a	n/a	n/a	n/a		
SysClk			n/a	n/a	n/a	n/a		
SysErr			n/a	n/a	12	8		async
SysReset					12	8		async
TestEn	dc	dc	n/a	n/a	n/a	n/a		async
TmrClk	dc	dc	n/a	n/a	n/a	n/a		async

I/O Specifications—200MHz

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
SDRAM Interface								
BA0:1	n/a	n/a	7.3	1	19	12	SysClk	1, 2
$\overline{\text{BankSel0:3}}$	n/a	n/a	5.8	1	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	7.3	1	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	4.7	1	40	25	SysClk	2
DQM0:3	n/a	n/a	6.2	1	19	12	SysClk	2
DQMCB	n/a	n/a	6	1	19	12	SysClk	2
ECC0:7	2	1	6	1	19	12	SysClk	2
MemAddr12:0	n/a	n/a	7.8	1	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0	-1	19	12	SysClk	2, 3
MemData0:31	2	1	6.2	1	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	7.4	1	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	7.4	1	19	12	SysClk	1, 2
External SLAVE Peripheral Interface								
DMAAck0:3	n/a	n/a	8	0	12	8	PerClk	
DMAReq0:3	dc	dc	n/a	n/a	n/a	n/a	PerClk	
EOT0:3[TC0:3]	dc	dc	9	0	12	8	PerClk	
PerAddr0:31	4	1	10	0	19	12	PerClk	
$\overline{\text{PerBLast}}$	4	1	8	0	12	8	PerClk	
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1:7}}$[GPIO10:16]	n/a	n/a	9	0	12	8	PerClk	
PerData0:31	6	1	10	0	19	12	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	8	0	12	8	PerClk	
PerPar0:3	4	1	10.5	0	19	12	PerClk	
PerR/$\overline{\text{W}}$	5	1	8	0	12	8	PerClk	
PerReady	9	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	4	1	8	0	12	8	PerClk	
External MASTER Peripheral Interface								
BusReq	n/a	n/a	8	0	12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	8	0	12	8	PerClk	
$\overline{\text{ExtReq}}$	6	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	8	0	19	12	PerClk	
HoldAck	n/a	n/a	8	0	12	8	PerClk	
HoldPri	4	1	n/a	n/a	n/a	n/a	PerClk	
HoldReq	6	1	n/a	n/a	n/a	n/a	PerClk	
PerClk	n/a	n/a	0.9	0.9	19	12	PLB Clk	4
PerErr	4	1	n/a	n/a	n/a	n/a	PerClk	

I/O Specifications—266 MHz (Preliminary)

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
SDRAM Interface								
BA0:1	n/a	n/a	5.5	1	19	12	SysClk	1, 2
$\overline{\text{BankSel0:3}}$	n/a	n/a	4.5	1	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	5.5	1	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	3.9	1	40	25	SysClk	2
DQM0:3	n/a	n/a	4.9	1	19	12	SysClk	2
DQMCB	n/a	n/a	4.7	1	19	12	SysClk	2
ECC0:7	1.5	1	4.7	1	19	12	SysClk	2
MemAddr12:0	n/a	n/a	5.9	1	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0	1	19	12	SysClk	2, 3
MemData0:31	1.5	1	4.8	1	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	5.6	1	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	5.6	1	19	12	SysClk	1, 2
External SLAVE Peripheral Interface								
DMAAck0:3	n/a	n/a	6	0	12	8	PerClk	
DMAReq0:3	dc	dc	n/a	n/a	n/a	n/a	PerClk	
EOT0:3[TC0:3]	dc	dc	8	0	12	8	PerClk	
PerAddr0:31	3	1	8	0	19	12	PerClk	
$\overline{\text{PerBLast}}$	3.5	1	6	0	12	8	PerClk	
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1:7}}$[GPIO10:16]	n/a	n/a	6	0	12	8	PerClk	
PerData0:31	5	1	8	0	19	12	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	6	0	12	8	PerClk	
PerPar0:3	3.5	1	8	0	19	12	PerClk	
PerR/$\overline{\text{W}}$	4	1	6	0	12	8	PerClk	
PerReady	6.5	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	3	1	6	0	12	8	PerClk	
External MASTER Peripheral Interface								
BusReq	n/a	n/a	6	0	12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	6	0	12	8	PerClk	
$\overline{\text{ExtReq}}$	5	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	6	0	19	12	PerClk	
HoldAck	n/a	n/a	6	0	12	8	PerClk	
HoldPri	3	1	n/a	n/a	n/a	n/a	PerClk	
HoldReq	5	1	n/a	n/a	n/a	n/a	PerClk	
PerClk	n/a	n/a	0.9	0.9	12	12	PLB Clk	4
PerErr	3	1	n/a	n/a	n/a	n/a	PerClk	

Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC405CR start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options:

Strapping Pin Assignments

Function	Option	Ball Strapping		
PLL Tuning for $6 \le M \le 7$ use choice 3 for $7 < M \le 12$ use choice 5 for $12 < M \le 32$ use choice 6 See Note.		**W15**	**U13**	**V20**
	Choice 1; TUNE[5:0] = 010001	0	0	0
	Choice 2; TUNE[5:0] = 010010	0	0	1
	Choice 3; TUNE[5:0] = 010011	0	1	0
	Choice 4; TUNE[5:0] = 010100	0	1	1
	Choice 5; TUNE[5:0] = 010101	1	0	0
	Choice 6; TUNE[5:0] = 010110	1	0	1
	Choice 7; TUNE[5:0] = 010111	1	1	0
	Choice 8; TUNE[5:0] = 100100	1	1	1
PLL Forward Divider		**C16**	**B17**	
	Bypass mode	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 6	1	1	
PLL Feedback Divider		**B16**	**A14**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
PLB Divider from CPU		**B18**	**D16**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
OPB Divider from PLB		**T4**	**U5**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
External Bus Divider from PLB		**C17**	**P18**	
	Divide by 2	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 5	1	1	

Strapping Pin Assignments (Continued)

Function	Option	Ball Strapping		
ROM Width		**Y5**	**W6**	
	8-bit ROM	0	0	
	16-bit ROM	0	1	
	32-bit ROM	1	0	
	Reserved	1	1	

Note: The tune bits adjust parameters that control PLL jitter. The recommended values minimize jitter for the PLL implemented in the PPC405CR. These bits are shown for information only; and do not require modification except in special clocking circumstances such as spread spectrum clocking. For details on the use of Spread Spectrum Clock Generators (SSCGs) with the PPC405CR, visit the technical documents area of the IBM PowerPC web site.

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