CMOS Static RAM for Automotive Applications 256K (32K x 8-Bit)

IDT71256SA

Features

- **32K x 8 advanced high-speed CMOS static RAM**
- **Automotive temperature options**
- **Equal access and cycle times**
  - *Automotive: 12/15/20/25/35/55ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional data inputs and outputs directly TTL-compatible**
- **Low power consumption via chip deselect**
- **Automotive product available in 28-pin, 300 mil (SOIC) package**

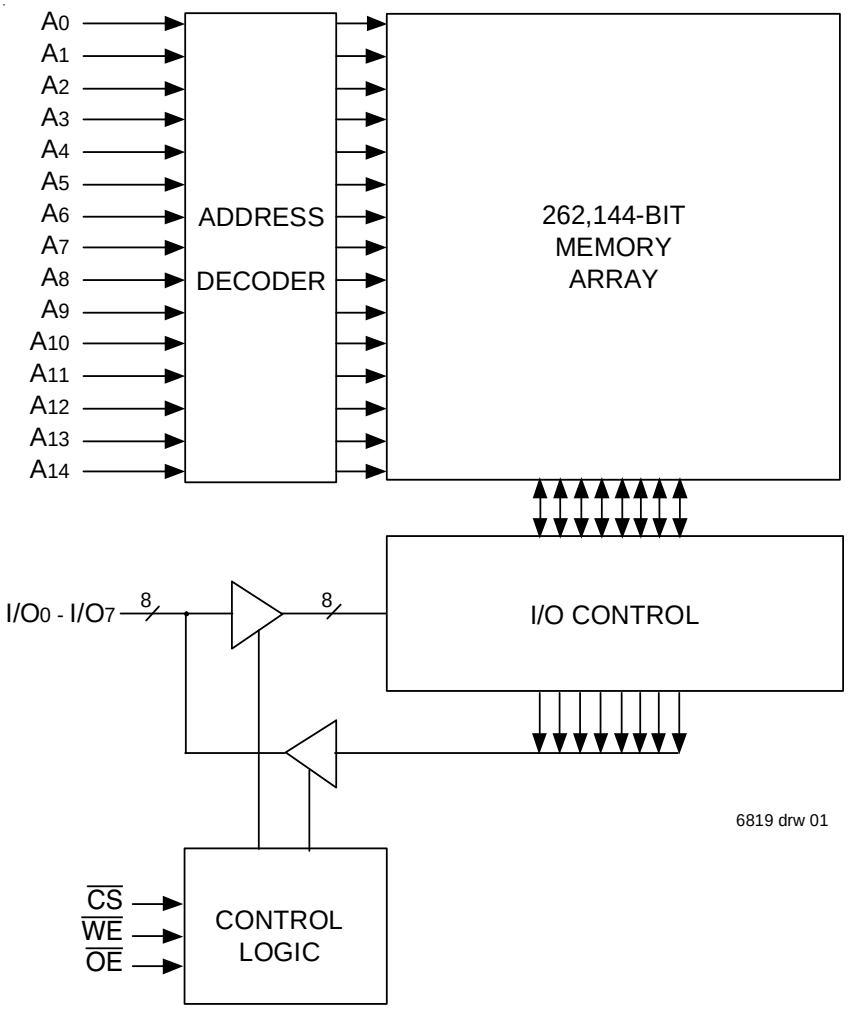
Description

The IDT71256SA is a 262,144-bit high-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs for automotive applications.

The IDT71256SA has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

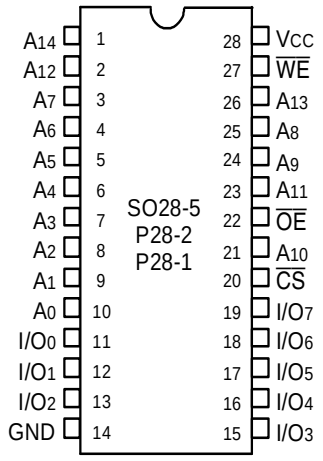
The IDT71256SA is packaged in 28-pin, 300 mil (SOIC).

Functional Block Diagram



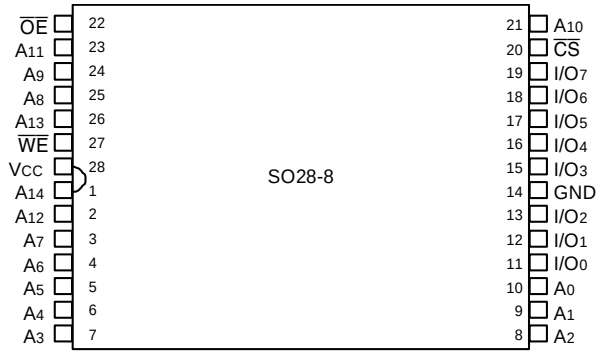
FEBRUARY 2006

Pin Configurations



6819 drw 02

DIP/SOJ
Top View



6819 drw 02a

TSOP
Top View

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage Relative to GND	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage Relative to GND	-0.5 to V_{CC}+0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_J	Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

6819 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

6819 tbl 03

NOTES:
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	Vss	V_{DD}
Automotive Grade 1	-40°C to +125°C	0V	See Below
Automotive Grade 2	-40°C to +105°C	0V	See Below
Automotive Grade 3	-40°C to +85°C	0V	See Below
Automotive Grade 4	0°C to +70°C	0V	See Below

6819 tbl 01

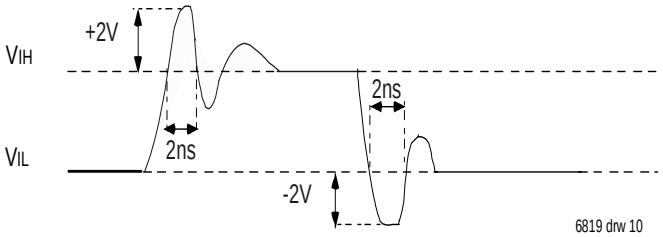
Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} +0.5 (1)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

6819 tbl 04

NOTE:
1. Refer to maximum overshoot/undershoot diagram below. The measured voltage at device pin should not exceed half sinusoidal wave with 2V peak and half period of 2ns.

Maximum Overshoot/Undershoot



6819 drw 10

DC Electrical Characteristics
(Vcc = 5.0V ± 10%, Automotive Temperature Ranges)

Symbol	Parameter	Test Conditions	IDT71256SA		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

6819 tbl 05

DC Electrical Characteristics(1)
(Vcc = 5.0V ± 10%, VLC = 0.2V, VHC = Vcc–0.2V, Automotive Temperature Ranges)

Symbol	Parameter	71256SA12	71256SA15	71256SA20	71256SA25	71256SA35	71256SA55	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	90	80	70	70	70	70	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	50	30	20	20	20	20	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2), $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	15	15	15	15	15	mA

6819 tbl 10

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

6819 tbl 07

Capacitance
(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

6819 tbl 08

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

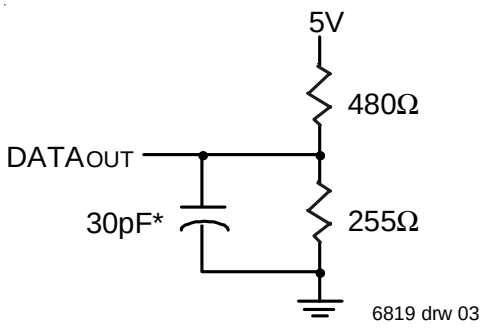


Figure 1. AC Test Load

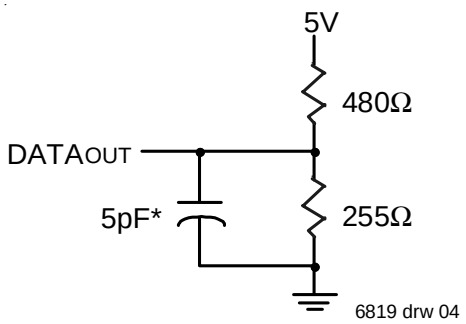


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Including jig and scope capacitance.

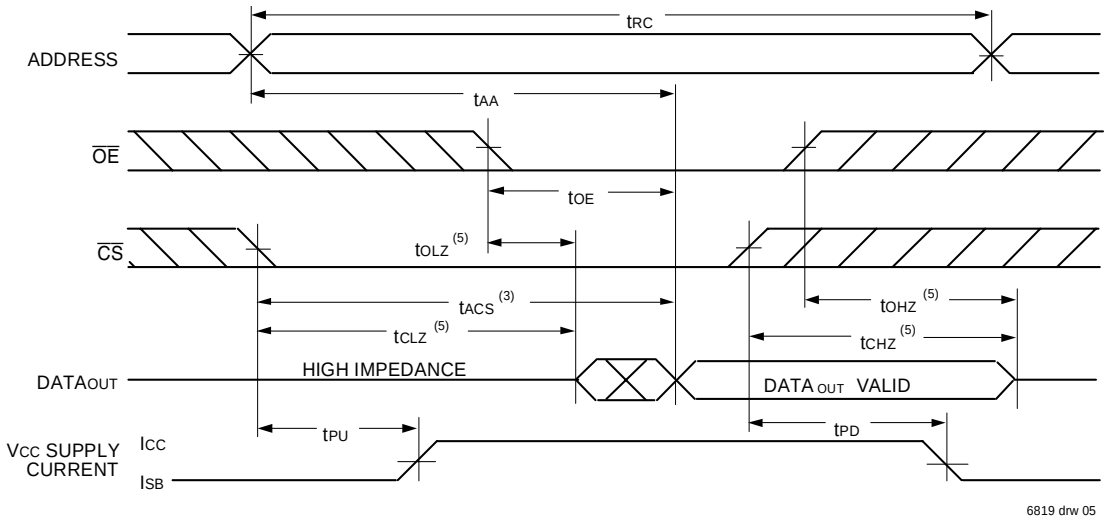
AC Electrical Characteristics (Vcc = 5.0V ± 10%, Automotive Temperature Ranges)

Symbol	Parameter	71256SA12		71256SA15		71256SA20		71256SA25		71256SA35		71256SA55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	35	—	55	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	—	35	—	55	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	—	25	—	35	—	55	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	4	—	4	—	ns
t_{CHZ}(1)	Chip Select to Output in High-Z	0	6	0	7	0	10	0	11	0	12	0	15	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	10	—	11	—	12	—	25	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	0	6	0	6	0	8	0	10	0	12	0	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	12	—	15	—	20	—	25	—	35	—	55	ns
Write Cycle														
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	35	—	55	—	ns
t_{AW}	Address Valid to End-of-Write	9	—	10	—	15	—	20	—	25	—	40	—	ns
t_{CW}	Chip Select to End-of-Write	9	—	10	—	15	—	20	—	25	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	15	—	20	—	20	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	7	—	11	—	13	—	13	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	4	—	4	—	4	—	4	—	4	—	4	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	0	6	0	6	0	10	0	11	0	12	0	15	ns

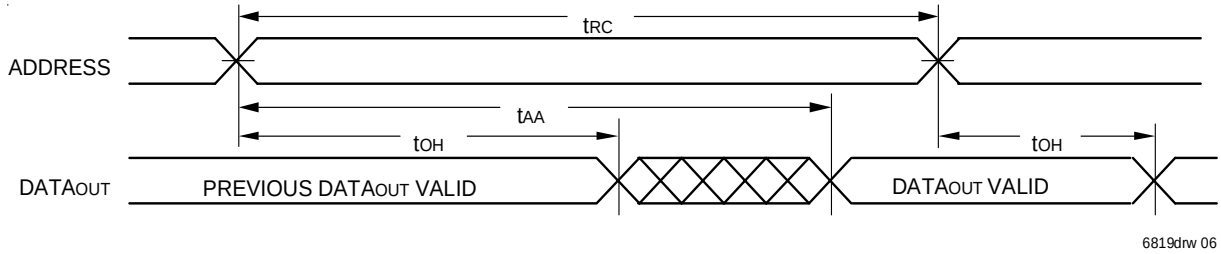
6819 tbl 09

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1(1)

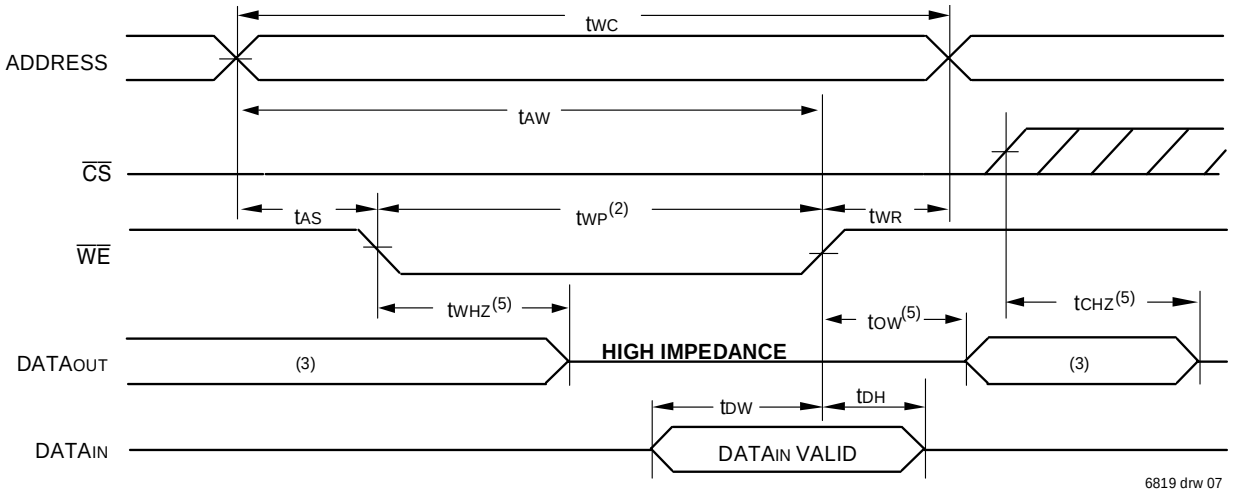


Timing Waveform of Read Cycle No. 2(1,2,4)

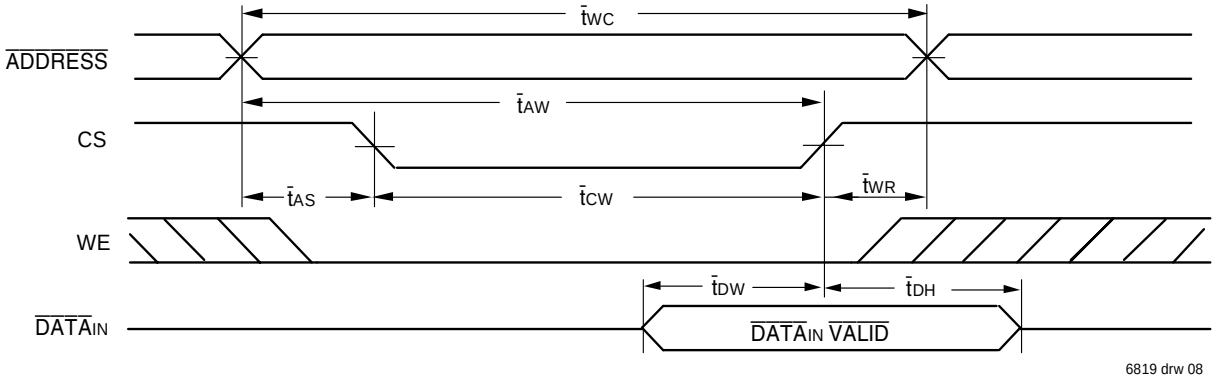


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4)



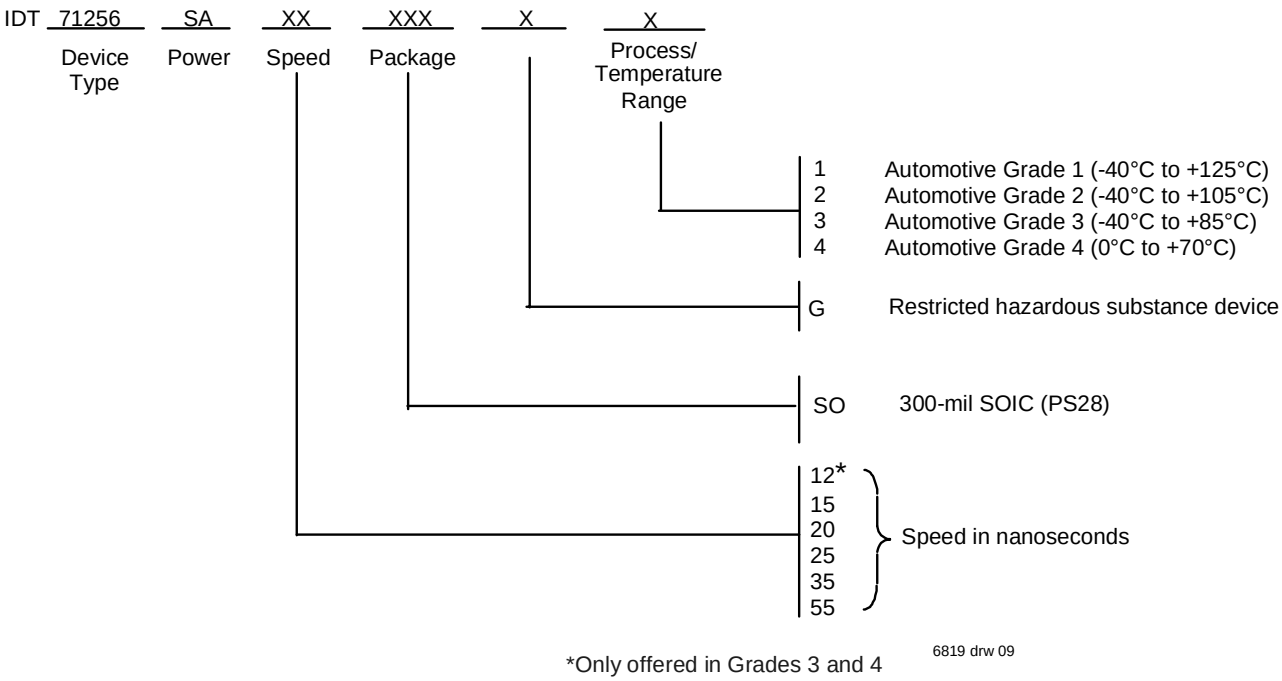
Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Ordering Information — Automotive



*Only offered in Grades 3 and 4

Datasheet Document History

Rev	Date	Page	Description
0	01/31/05	p. 1-7	Released Automotive datasheet
A	05/06/05	p. 7	Updated ordering information.
B	02/28/06	p. 1,3,4,7	Added 35ns speed grade.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or
408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
sramhelp@idt.com
800-345-7015