

FLASH MEMORY

CMOS

8M (1M × 8/512K × 16) BIT

MBM29LV800TA-90-X-12-X / MBM29LV800BA-90-X-12-X

■ FEATURES

- **Single 3.0 V read, program, and erase**
Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
48-pin TSOP(I) (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
44-pin SOP (Package suffix: PF)
46-pin SON (Package suffix: PN)
48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
90 ns maximum access time
- **Sector erase architecture**
One 16K byte, two 8K bytes, one 32K byte, and fifteen 64K bytes.
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
T = Top sector
B = Bottom sector
- **Embedded Erase™ Algorithms**
Automatically pre-program and erases the chip or any sector
- **Embedded Program™ Algorithms**
Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/BY)**
Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{cc} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
Suspends the erase operation to allow a read data in another sector within the same device

(Continued)

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

(Continued)

- **Sector protection**

Hardware method disables any combination of sectors from program or erase operations

- **Sector Protection Set function by Extended sector protection command**
- **Temporary sector unprotection**

Hardware method temporarily enables any combination of sectors from program or erase operations.

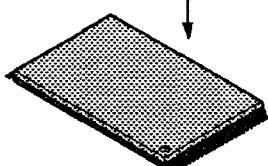
- **Extended operating temperature range : -40°C to +85°C**

Please refer to "MBM29LV800TA/MBM29LV800BA" in detailed specifications.

■ PACKAGE

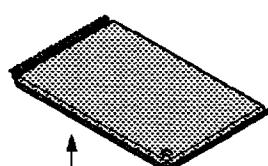
48pin-Plastic TSOP(I)

Marking Side



(FPT-48P-M19)

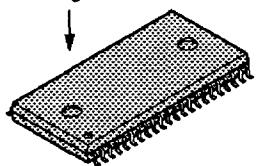
Marking Side



(FPT-48P-M20)

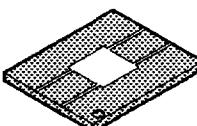
44-pin Plastic SOP

Marking Side



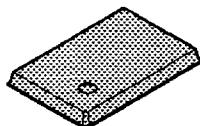
(FPT-44P-M16)

46-pin Plastic SON



(LCC-46P-M02)

48-pin Plastic FBGA



(BGA-48P-M02)

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ GENERAL DESCRIPTION

The MBM29LV800TA-X/BA-X are a 8M-bit, 3.0 V-only Flash memory organized as 1M bytes of 8 bits each or 512K words of 16 bits each. The MBM29LV800TA-X/BA-X are offered in a 48-pin TSOP(I), 44-pin SOP, 46-pin SON, and 48-ball FBGA package. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

The standard MBM29LV800TA-X/BA-X offer access times 90ns, and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable (CE), write enable (WE), and output enable (OE) controls.

The MBM29LV800TA-X/BA-X are pin and command set compatible with JEDEC standard E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV800TA-X/BA-X are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

Any sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV800TA-X/BA-X are erased when shipped from the factory.

The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by Data Polling of DQ₇, by the Toggle Bit feature on DQ₆, or the RY/BY output pin. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.

Fujitsu's Flash technology combines years of EPROM and E2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29LV800TA-X/BA-X memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16K byte, two 8K bytes, one 32K byte, and fifteen 64K bytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable.

(x8)	(x16)	(x8)	(x16)
16K byte	FFFFFH 7FFFFH	64K byte	FFFFFH 7FFFFH
8K byte	FBFFFH 7DFFFH	64K byte	EFFFFH 77FFFFH
8K byte	F9FFFH 7CFFFFH	64K byte	DFFFFH 6FFFFH
32K byte	F7FFFH 7BFFFFH	64K byte	CFFFFH 67FFFFH
64K byte	EFFFFH 77FFFFH	64K byte	BFFFFH 5FFFFH
64K byte	DFFFFH 6FFFFH	64K byte	AFFFFH 57FFFFH
64K byte	CFFFFH 67FFFFH	64K byte	9FFFFH 4FFFFH
64K byte	BFFFFH 5FFFFH	64K byte	8FFFFH 47FFFFH
64K byte	AFFFFH 57FFFFH	64K byte	7FFFFH 3FFFFH
64K byte	9FFFFH 4FFFFH	64K byte	6FFFFH 37FFFFH
64K byte	8FFFFH 47FFFFH	64K byte	5FFFFH 2FFFFH
64K byte	7FFFFH 3FFFFH	64K byte	4FFFFH 27FFFFH
64K byte	6FFFFH 37FFFFH	64K byte	3FFFFH 1FFFFH
64K byte	5FFFFH 2FFFFH	64K byte	2FFFFH 17FFFFH
64K byte	4FFFFH 27FFFFH	64K byte	1FFFFH 0FFFFH
64K byte	3FFFFH 1FFFFH	32K byte	0FFFFH 07FFFFH
64K byte	2FFFFH 17FFFFH	8K byte	07FFFH 03FFFFH
64K byte	1FFFFH 0FFFFH	8K byte	05FFFH 02FFFFH
64K byte	0FFFFH 07FFFFH	16K byte	03FFFH 01FFFFH
	00000H 00000H		00000H 00000H

MBM29LV800TA-X Sector Architecture

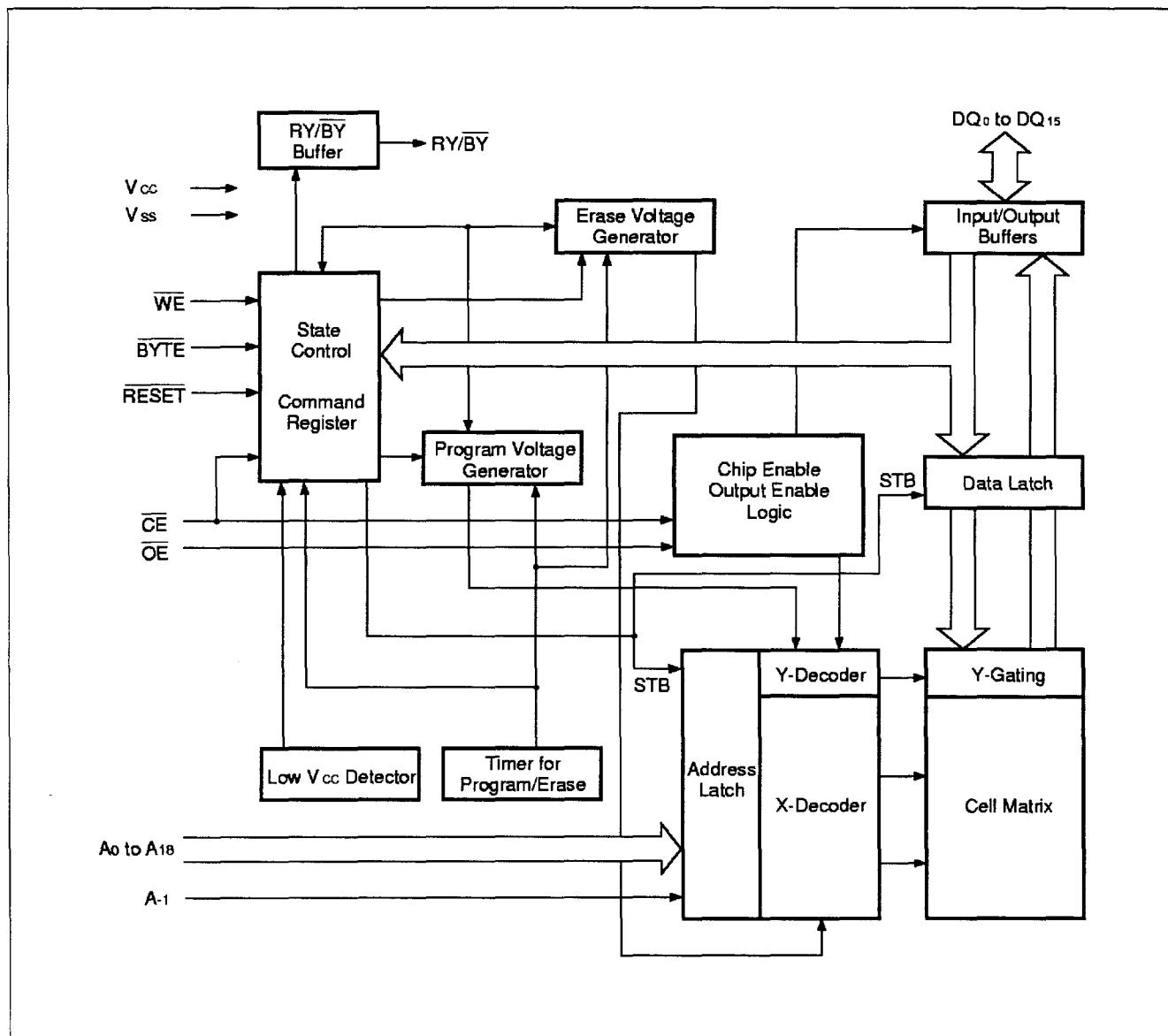
MBM29LV800BA-X Sector Architecture

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ PRODUCT LINE UP

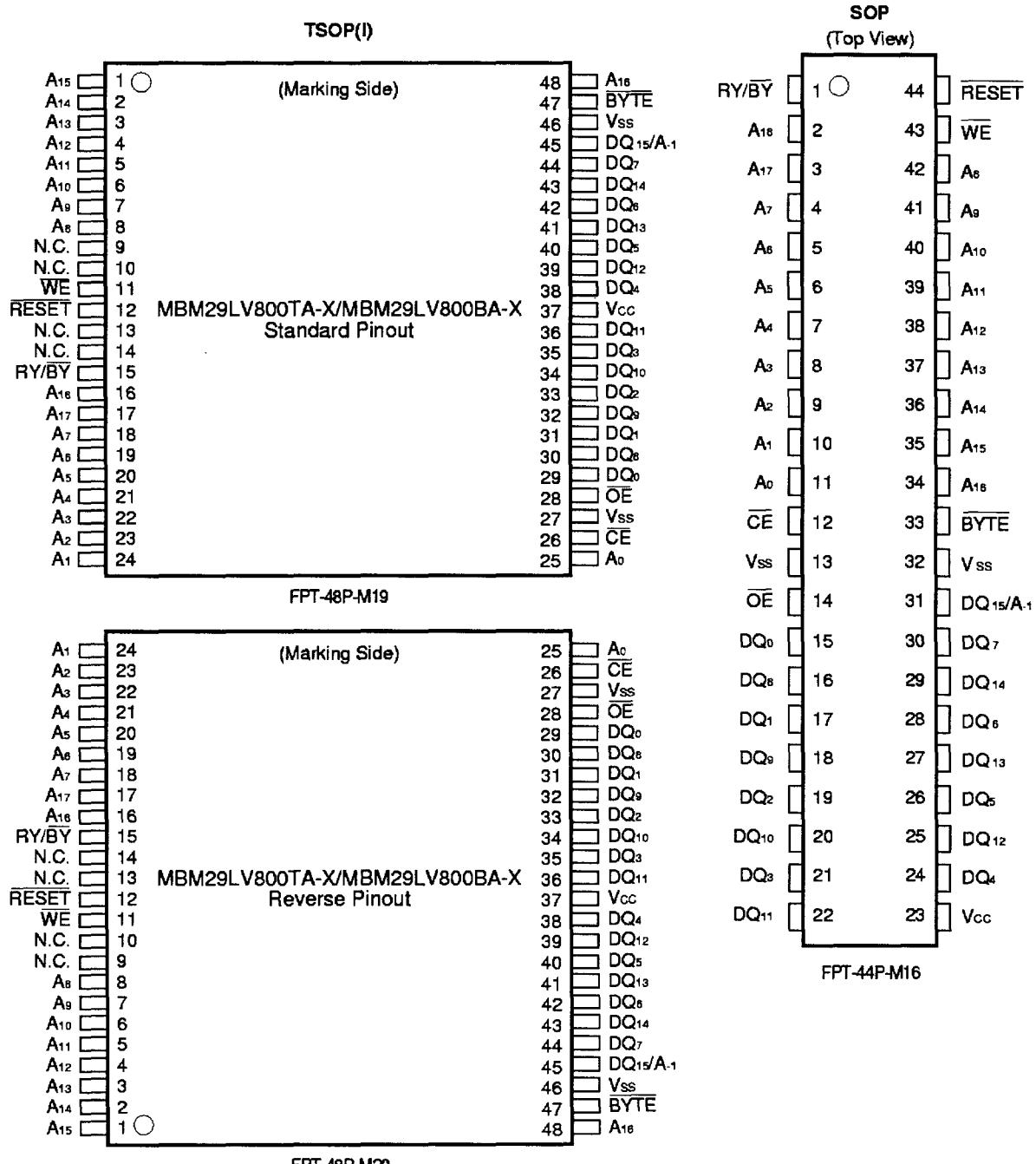
Part No.	MBM29LV800TA-X/MBM29LV800BA-X		
Ordering Part No.	V _{CC} = 3.3 V ±0.3 V	-90	—
	V _{CC} = 3.0 V +0.6 V -0.3 V	—	-12
Max. Address Access Time (ns)	90	120	
Max. CE Access Time (ns)	90	120	
Max. OE Access Time (ns)	35	50	

■ BLOCK DIAGRAM



MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ CONNECTION DIAGRAMS



(Continued)

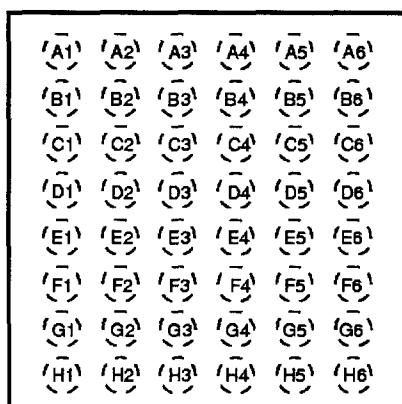
MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

(Continued)

SON (Top View)		
A ₁₃	1	O
A ₁₄	2	(Marking Side)
A ₁₅	3	46
A ₁₂	4	45
A ₁₁	5	44
A ₁₀	6	43
A ₉	7	42
A ₈	8	41
N.C.	9	40
WE	10	39
RESET	11	38
V _{cc}	12	37
DQ ₄	13	36
DQ ₁₂	14	35
DQ ₅	15	34
DQ ₁₃	16	33
DQ ₆	17	32
DQ ₁₄	18	31
DQ ₇	19	30
A ₁₆	20	29
BYTE	21	28
V _{ss}	22	27
DQ ₈ /A ₋₁	23	26
		25
		24

LCC-46P-M02

FBGA
(Top View)
Marking side



BGA-48P-M02

A1	A3	A2	A7	A3	RY/BY	A4	WE	A5	A9	A6	A13
B1	A4	B2	A ₁₇	B3	N.C.	B4	RESET	B5	A ₈	B6	A ₁₂
C1	A ₂	C2	A ₆	C3	A ₁₈	C4	N.C.	C5	A ₁₀	C6	A ₁₄
D1	A ₁	D2	A ₅	D3	N.C.	D4	N.C.	D5	A ₁₁	D6	A ₁₅
E1	A ₀	E2	DQ ₀	E3	DQ ₂	E4	DQ ₅	E5	DQ ₇	E6	A ₁₆
F1	CE	F2	DQ ₈	F3	DQ ₁₀	F4	DQ ₁₂	F5	DQ ₁₄	F6	BYTE
G1	OE	G2	DQ ₉	G3	DQ ₁₁	G4	V _{cc}	G5	DQ ₁₃	G6	DQ ₁₅ /A ₋₁
H1	V _{ss}	H2	DQ ₁	H3	DQ ₃	H4	DQ ₄	H5	DQ ₆	H6	V _{ss}

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ LOGIC SYMBOL

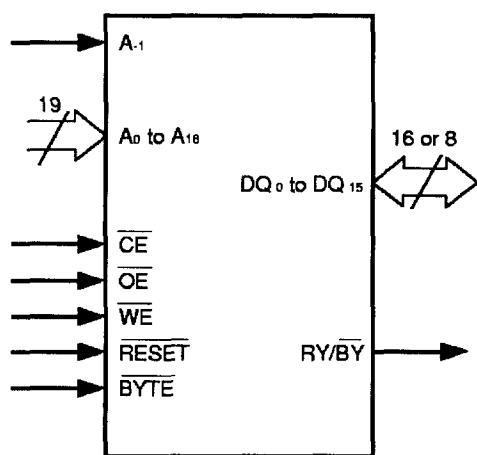


Table 1 MBM29LV800TA-X/800BA-X Pin Configuration

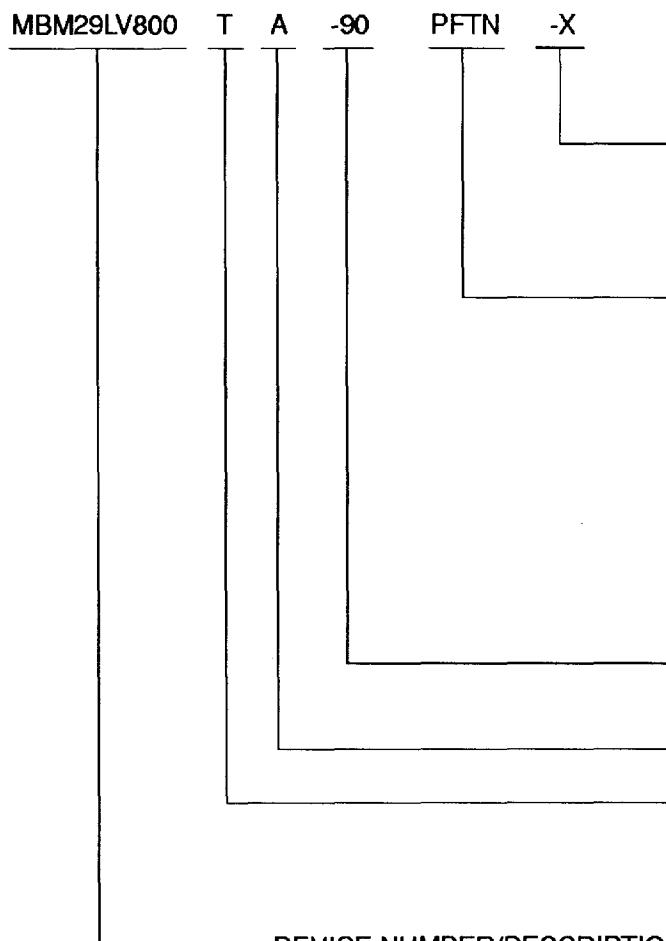
Pin	Function
A-1, A0 to A18	Address Inputs
DQ ₀ to DQ ₁₅	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
RY/BY	Ready/Busy Output
RESET	Hardware Reset Pin/Temporary Sector Unprotection
BYTE	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
V _{ss}	Device Ground
V _{cc}	Device Power Supply

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ ORDERING INFORMATION

Industrial Devices

Fujitsu industrial devices are available in several packages. The order number is formed by a combination of:



OPERATING RANGE

Industrial Products

Ambient Temperature (T_A) = -40°C to $+85^{\circ}\text{C}$

PACKAGE TYPE

PFTN = 48-Pin Thin Small Outline Package
(TSOP) Standard Pinout

PFTR = 48-Pin Thin Small Outline Package
(TSOP) Reverse Pinout

PF = 44-Pin Small Outline Package

PN = 46-Pin Small Outline Non-leaded
Package (SON)

PBT = 48-Ball Fine Pitch Ball Grid Array
Package (FBGA)

SPEED OPTION

See Product Selector Guide

Device Revision

BOOT CODE SECTOR ARCHITECTURE

TA = Top sector

BA = Bottom sector

DEVICE NUMBER/DESCRIPTION

MBM29LV800

8Mega-bit (1M x 8-Bit or 512K x 16-Bit) CMOS Flash Memory

3.0 V-only Read, Program, and Erase

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Voltage with respect to Ground All pins except A ₉ , OE, RESET (Note 1)	-0.5 V to V _{cc} + 0.5 V
V _{cc} (Note 1)	-0.5 V to +5.5 V
A ₉ , OE, and RESET (Note 2)	-0.5 V to +13.0 V

- Notes:**
1. Minimum DC voltage on input or I/O pins are -0.5 V. During voltage transitions, inputs may negative overshoot V_{ss} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{cc} + 0.5 V. During voltage transitions, outputs may positive overshoot to V_{cc} +2.0 V for periods of up to 20 ns.
 2. Minimum DC input voltage on A₉, OE and RESET pins are -0.5 V. During voltage transitions, A₉, OE and RESET pins may negative overshoot V_{ss} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on A₉, OE and RESET pins are +13.0 V which may positive overshoot to 14.0 V for periods of up to 20 ns. Voltage difference between input voltage and supply voltage (V_{IN} - V_{cc}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Industrial Devices

Ambient Temperature (T_A)

-40°C to +85°C

V_{cc} Supply Voltages

V_{cc} Supply Voltages for MBM29LV800TA/BA-90-X.....

+3.0 V to +3.6 V

V_{cc} Supply Voltages for MBM29LV800TA/BA-12-X.....

+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the devices are guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ MAXIMUM OVERSHOOT

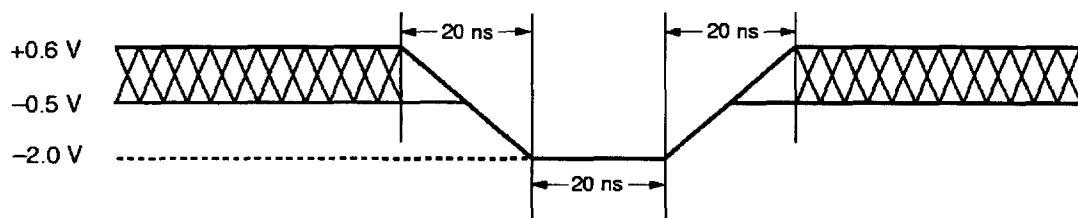


Figure 1 Maximum Negative Overshoot Waveform

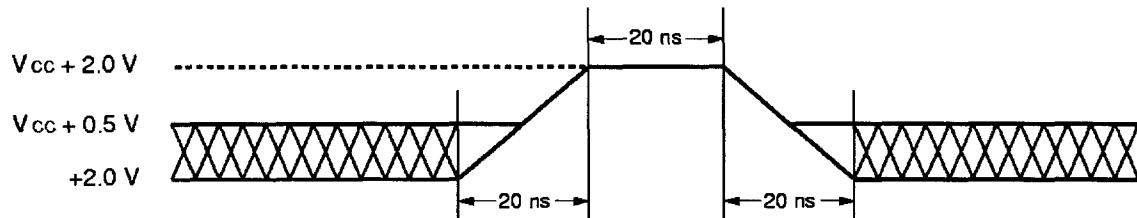
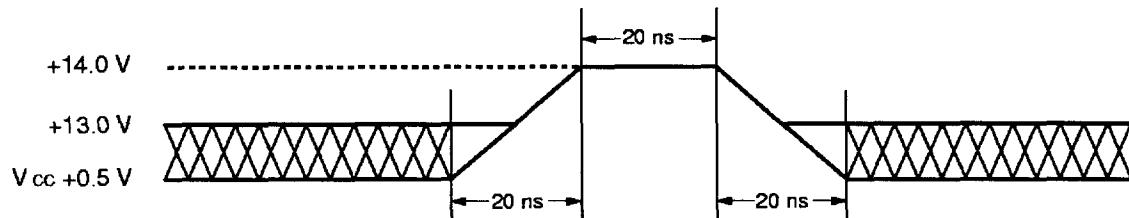


Figure 2 Maximum Positive Overshoot Waveform



*: This waveform is applied for A_9 , \overline{OE} , and \overline{RESET} .

Figure 3 Maximum Positive Overshoot Waveform

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I _{LU}	Input Leakage Current	V _{IN} = V _{SS} to V _{CC} , V _{CC} = V _{CC} Max.		-1.0	+1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = V _{SS} to V _{CC} , V _{CC} = V _{CC} Max.		-1.0	+1.0	μA
I _{LUT}	A ₉ , OE, RESET Inputs Leakage Current	V _{CC} = V _{CC} Max. A ₉ , OE, RESET = 12.5 V		—	80	μA
I _{CC1}	V _{CC} Active Current (Note 1)	CE = V _{IL} , OE = V _{IH} , f=10 MHz	Byte	—	22	mA
			Word	—	25	
		CE = V _{IL} , OE = V _{IH} , f=5 MHz	Byte	—	12	mA
			Word	—	15	
I _{CC2}	V _{CC} Active Current (Note 2)	CE = V _{IL} , OE = V _{IH}		—	35	mA
I _{CC3}	V _{CC} Current (Standby)	V _{CC} = V _{CC} Max., CE = V _{CC} ± 0.3 V, RESET = V _{CC} ± 0.3 V		—	5	μA
I _{CC4}	V _{CC} Current (Standby, Reset)	V _{CC} = V _{CC} Max., RESET = V _{SS} ± 0.3 V		—	5	μA
I _{CC5}	V _{CC} Current (Automatic Sleep Mode) (Note 3)	V _{CC} = V _{CC} Max., CE = V _{SS} ± 0.3 V, RESET = V _{CC} ± 0.3 V V _{IN} = V _{CC} ± 0.3 V or V _{SS} ± 0.3 V		—	5	μA
V _{IL}	Input Low Level	—		-0.5	0.6	V
V _{IH}	Input High Level	—		2.0	V _{CC} +0.3	V
V _{ID}	Voltage for Autoselect, Sector Protection, and Temporary Sector Unprotection (A ₉ , OE, RESET) (Note 4)	—		11.5	12.5	V
V _{OL}	Output Low Voltage Level	I _{OL} = 4.0 mA, V _{CC} = V _{CC} Min.		—	0.45	V
V _{OHI}	Output High Voltage Level	I _{OH} = -2.0 mA, V _{CC} = V _{CC} Min.		2.4	—	V
V _{OHZ}		I _{OH} = -100 μA, V _{CC} = V _{CC} Min.		V _{CC} -0.4	—	V
V _{LKO}	Low V _{CC} Lock-Out Voltage	—		2.3	2.5	V

- Notes:**
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 10 MHz).
 2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
 3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
 4. (V_{ID} - V_{CC}) do not exceed 9 V.

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ AC CHARACTERISTICS

- Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		-90-X (Note)	-12-X (Note)	Unit
JEDEC	Standard						
tAVAV	tRC	Read Cycle Time	—	Min.	90	120	ns
tAVOV	tACC	Address to Output Delay $\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	$\overline{OE} = V_{IL}$	Max.	90	120	ns
tELOV	tCE	Chip Enable to Output Delay $\overline{OE} = V_{IL}$	$\overline{OE} = V_{IL}$	Max.	90	120	ns
tGLOV	tOE	Output Enable to Output Delay	—	Max.	35	50	ns
tEHQZ	tDF	Chip Enable to Output High-Z	—	Max.	30	30	ns
tGHQZ	tDF	Output Enable to Output High-Z	—	Max.	30	30	ns
tAXOX	tOH	Output Hold Time From Addresses, \overline{CE} or \overline{OE} , Whichever Occurs First	—	Min.	0	0	ns
—	tREADY	RESET Pin Low to Read Mode	—	Max.	20	20	μs
—	tELFL tELFH	\overline{CE} or BYTE Switching Low or High	—	Max.	5	5	ns

Note: Test Conditions:

Output Load: 1 TTL gate and 30 pF (MBM29LV800TA/BA-90-X)
1 TTL gate and 100 pF (MBM29LV800TA/BA-12-X)

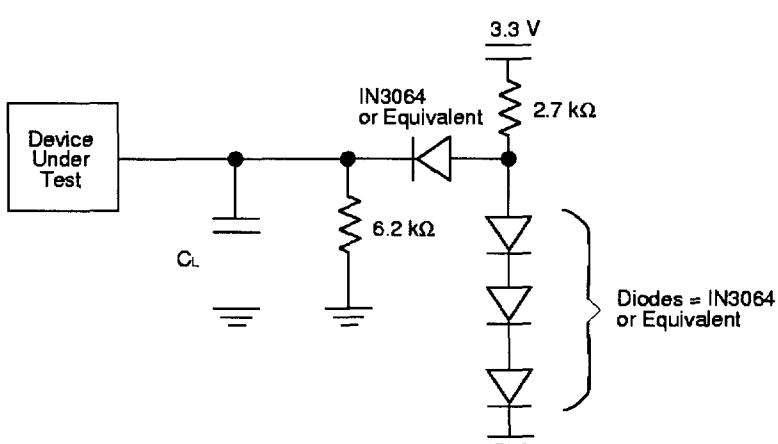
Input rise and fall times: 5 ns

Input pulse levels: 0.0 V to 3.0 V

Timing measurement reference level

Input: 1.5 V

Output: 1.5 V



Notes: $C_L = 30 \text{ pF}$ including jig capacitance (MBM29LV800TA/BA-90-X)
 $C_L = 100 \text{ pF}$ including jig capacitance (MBM29LV800TA/BA-10-X/-12-X)

Figure 4 Test Conditions

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

- Write/Erase/Program Operations

Parameter Symbols		Description		-90-X	-12-X	Unit
JEDEC	Standard					
tAVAV	t _{WC}	Write Cycle Time		Min.	90	120
tAWL	t _{AS}	Address Setup Time		Min.	0	0
tWLAX	t _{AH}	Address Hold Time		Min.	45	50
tDWWH	t _{DS}	Data Setup Time		Min.	45	50
tWHDX	t _{DH}	Data Hold Time		Min.	0	0
—	t _{OES}	Output Enable Setup Time		Min.	0	0
—	t _{OEH}	Output Enable Hold Time	Read	Min.	0	0
—			Toggle and Data Polling	Min.	10	10
tGHWL	t _{GHWL}	Read Recover Time Before Write		Min.	0	0
tGHEL	t _{GHEL}	Read Recover Time Before Write		Min.	0	0
tELWL	t _{CS}	CE Setup Time		Min.	0	0
tWEL	t _{WS}	WE Setup Time		Min.	0	0
tWHEH	t _{CH}	CE Hold Time		Min.	0	0
tEHWH	t _{WH}	WE Hold Time		Min.	0	0
tWLWH	t _{WP}	Write Pulse Width		Min.	45	50
tELEH	t _{CP}	CE Pulse Width		Min.	45	50
tWHLW	t _{WPH}	Write Pulse Width High		Min.	25	30
tEHEL	t _{CPh}	CE Pulse Width High		Min.	25	30
tWHWH1	t _{WHWH1}	Byte Programming Operation		Typ.	8	8
tWHWH2	t _{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1	1
—	t _{VCS}	V _{CC} Setup Time		Min.	50	50
—	t _{VIDR}	Rise Time to V _{ID} (Note 2)		Min.	500	500
—	t _{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4
—	t _{WPW}	Write Pulse Width (Note 2)		Min.	100	100
—	t _{OESP}	OE Setup Time to WE Active (Note 2)		Min.	4	4
—	t _{CSP}	CE Setup Time to WE Active (Note 2)		Min.	4	4
—	t _{RB}	Recover Time From RY/BY		Min.	0	0
—	t _{RP}	RESET Pulse Width		Min.	500	500
—	t _{RH}	RESET Hold Time Before Read		Min.	50	50

(Continued)

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

(Continued)

Parameter Symbols		Description	-90-X	-12-X	Unit
JEDEC	Standard				
—	t _{FLQZ}	BYTE Switching Low to Output High-Z	Max.	30	40
—	t _{FHOV}	BYTE Switching High to Output Active	Min.	30	40
—	t _{busy}	Program/Erase Valid to RY/BY Delay	Max.	90	90
—	t _{EOE}	Delay Time from Embedded Output Enable	Max.	90	120

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Protection operation.

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Word Programming Time	—	16	5200	μs	Excludes system-level overhead
Byte Programming Time	—	8	3600	μs	
Chip Programming Time	—	8.4	50	sec	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycles	—

■ TSOP(I) PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	7.5	9.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8	10	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	10	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	7.5	9.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8	10	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	10	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SON PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0	7.5	9.5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0	8	10	pF
C _{IN2}	Control Pin Capacitance	V _{IN} = 0	10	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ FBGA PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	T.B.D.	T.B.D.	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	T.B.D.	T.B.D.	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	T.B.D.	T.B.D.	pF

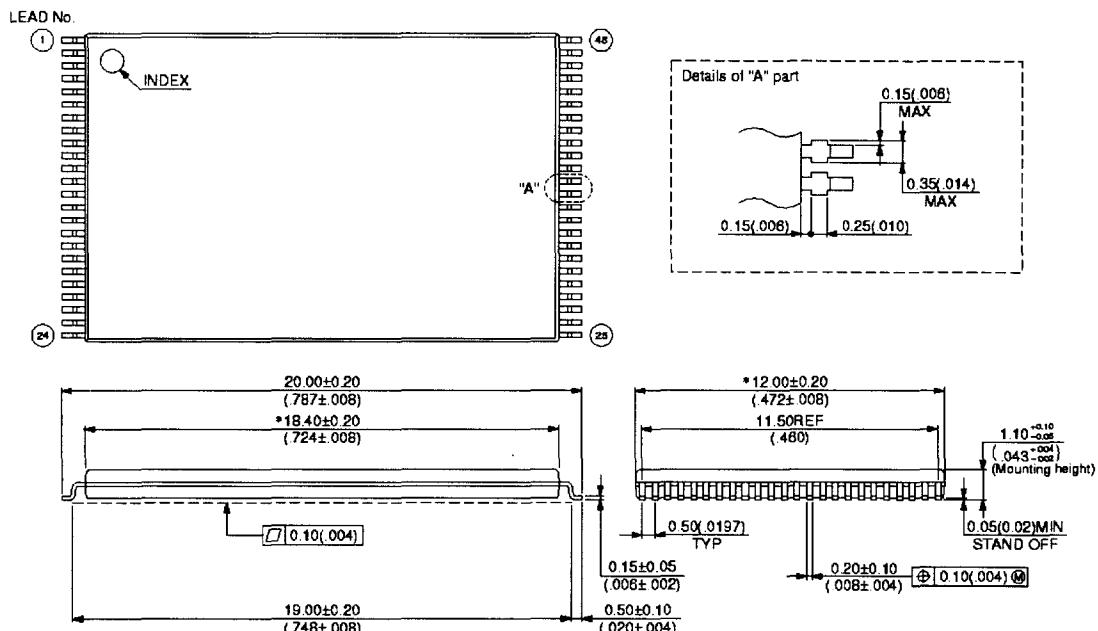
Note: Test conditions $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(I)
(FPT-48P-M19)

* Resin Protrusion. (Each Side: 0.15 (.006)Max)

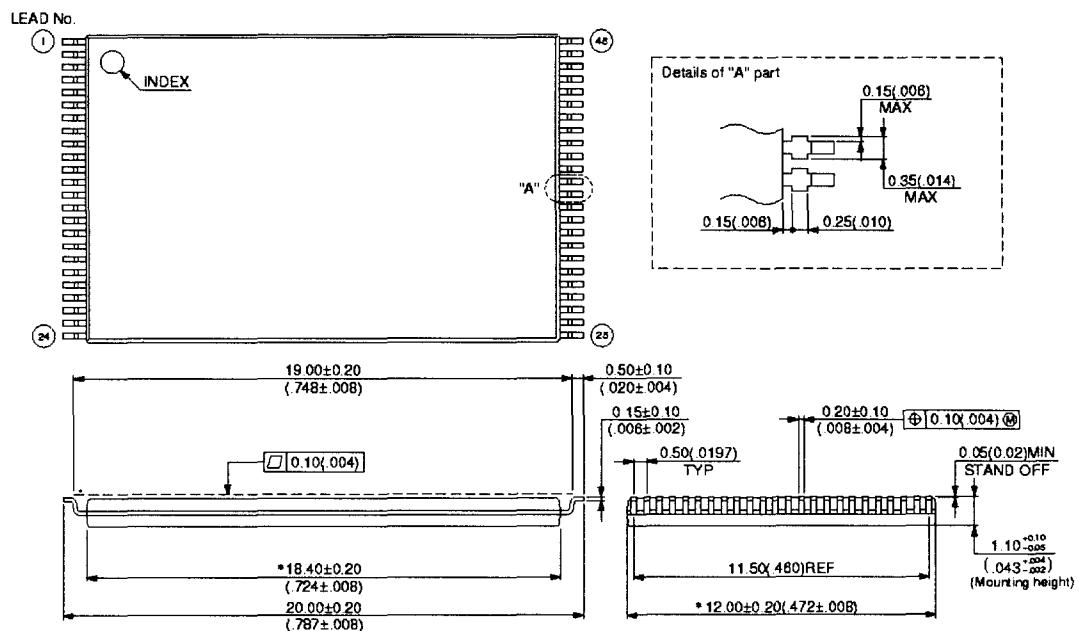


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Dimensions in mm (inches)

48-pin plastic TSOP(I)
(FPT-48P-M20)

* Resin Protrusion. (Each Side: 0.15 (.006)Max)

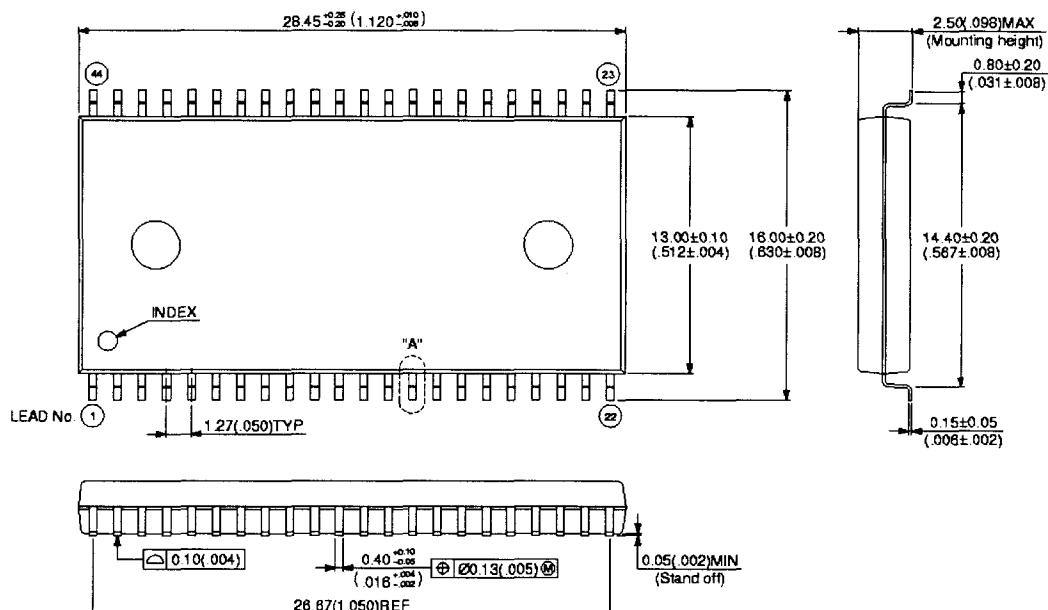


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Dimensions in mm (inches)

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

44-pin plastic SOP
(FPT-44P-M16)

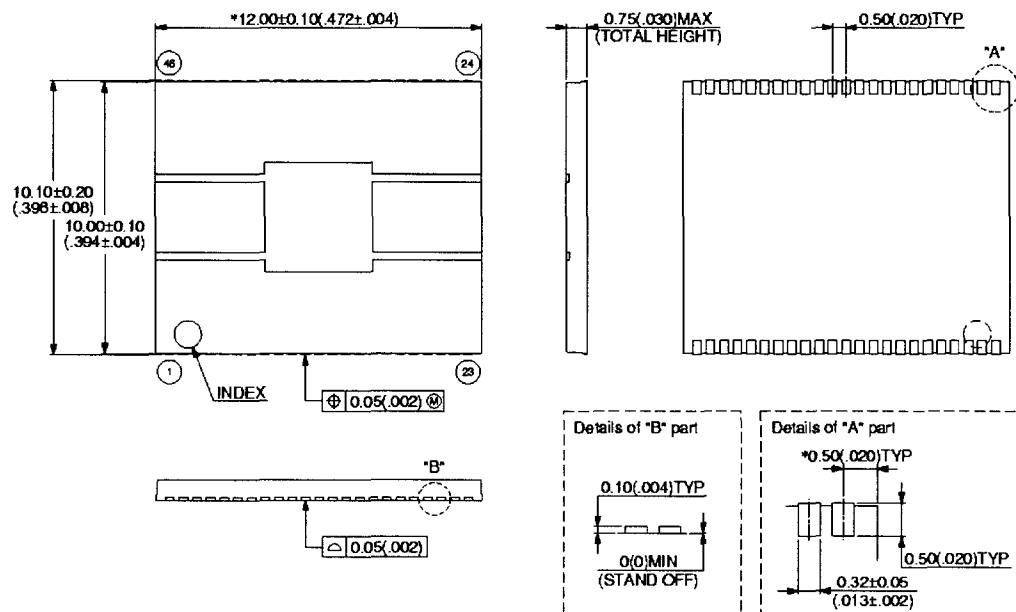


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Dimensions in mm (inches)

46-pin plastic SON
(LCC-46P-M02)

Note 1) Resin residue for * marked dimensions is 0.15 max on a single side.
Note 2) Die pad geometry may change with the models.



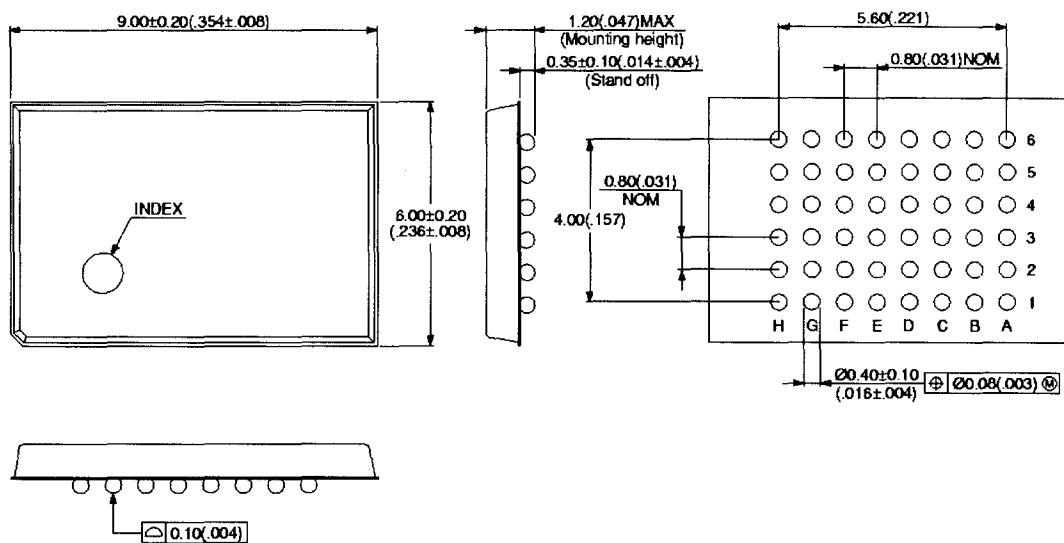
© 1997 FUJITSU LIMITED C46002S4C-3

Dimensions in mm (inches)

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

48-pin plastic FBGA
(BGA-48P-M02)

Note: The actual shape of corners may differ from the dimension.



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Dimensions in mm (inches)

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

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