CYPRESS SEMICONDUCTOR

PAL22V10C
PRELIMINARY **PAL22VP10C**

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— 7.5-ns t_{PD}, 111-MHz, f_{MAX}**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10C)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
  - **— > 2001V input protection**
- **Standard 300-mil PDIP and CDIP packages**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for improved performance**
- **Security Fuse**

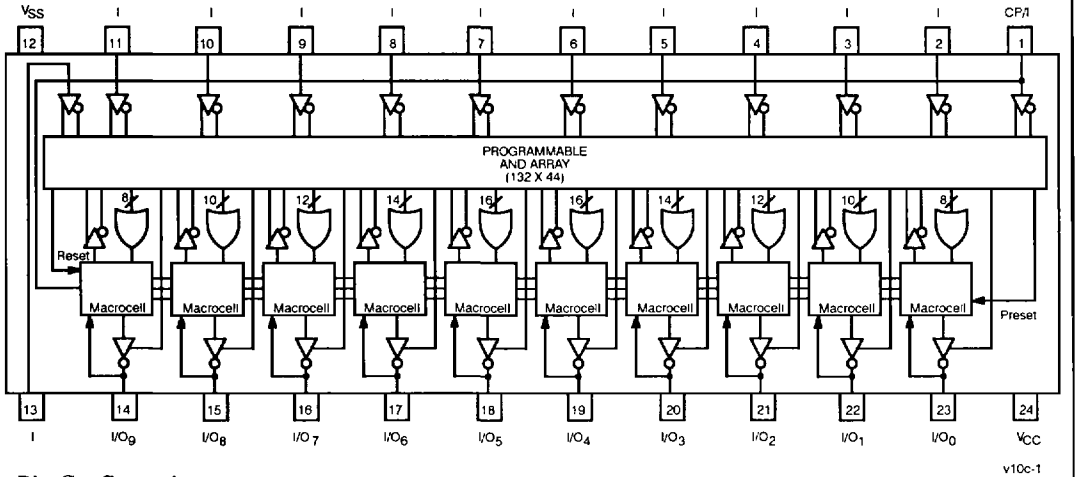
Functional Description

The Cypress PAL22V10C and PAL22VP10C are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10C and PAL22VP10C use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10C and PAL22VP10C provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The "OUTPUT ENABLE" product term available on each I/O allows this selection.

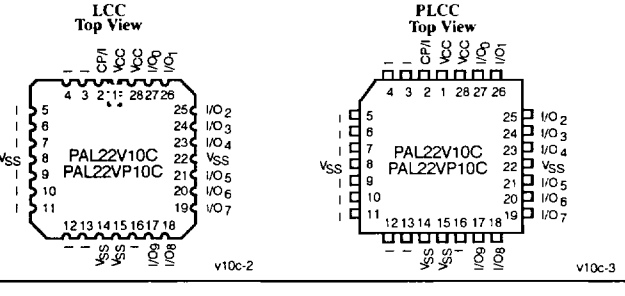
The PAL22V10C and PAL22VP10C feature variable product term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

Logic Block Diagram (PDIP/CDIP)



v10c-1

Pin Configurations



v10c-2 v10c-3

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Functional Description (cont.)

Additional features include common synchronous PRESET and asynchronous RESET product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10C and PAL22VP10C automatically reset on power-up. In addition, the PRELOAD capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10C and PAL22VP10C can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

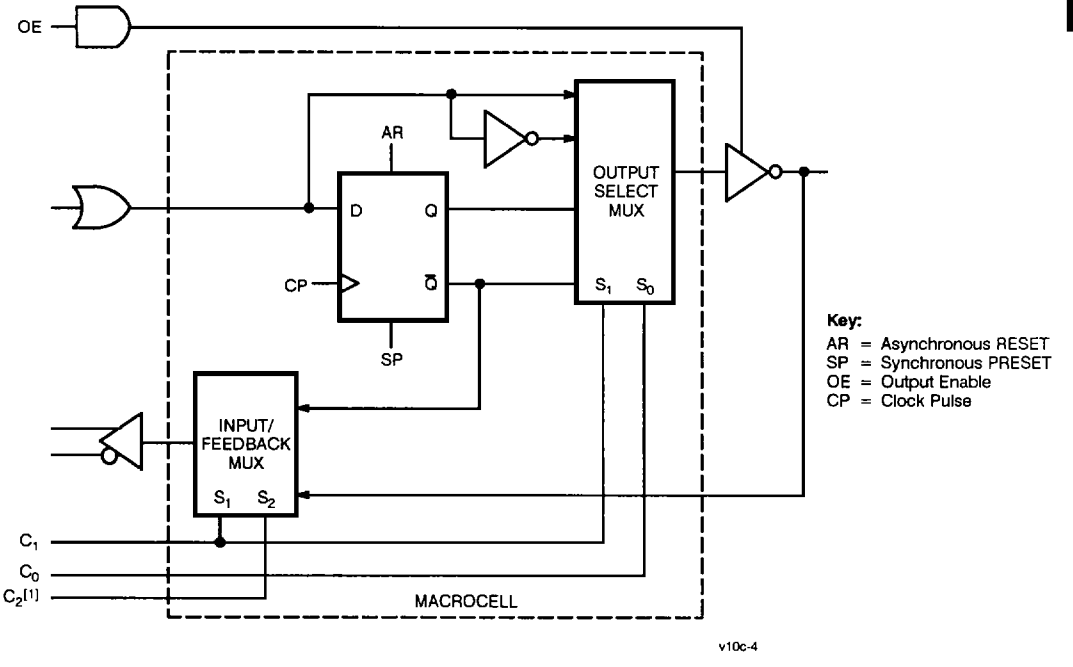
Programmable Macrocell

The PAL22V10C and PAL22VP10C each has 10 programmable output macro cells (see Macrocell). On the PAL22V10C two fuses (C1 and C0) can be programmed to configure output in one of four ways. Accordingly, each output can be "REGISTERED" or "COMBINATORIAL" with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C2) in the PAL22VP10C provides for two additional feedback paths (see *Figure 2*).

Programming

The PAL22V10C and PAL22VP10C can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

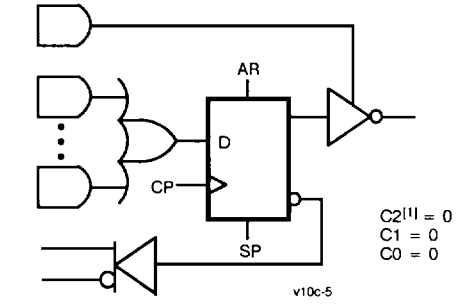
Macrocell



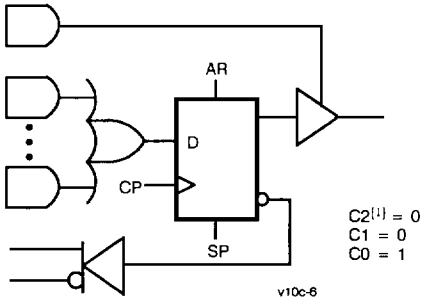
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

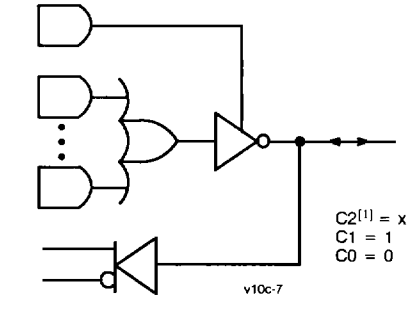
Notes:
1. PAL22VP10C only.



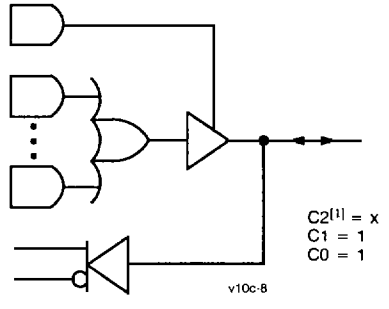
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

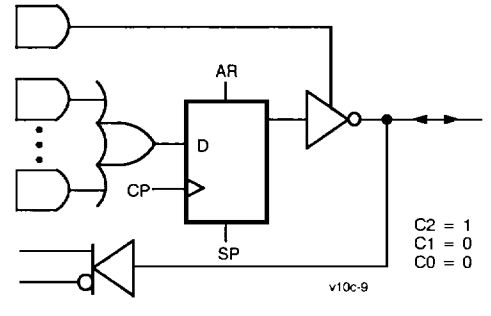


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

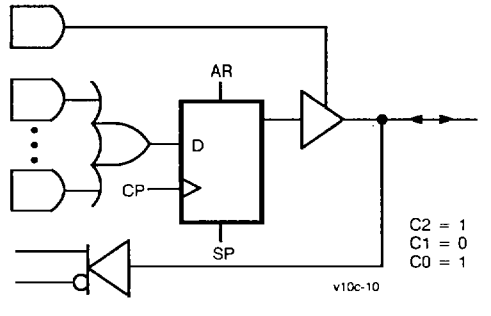


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10C and PAL22VP10C Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10C

Selection Guide

		22V10C-7 22VP10C-7	22V10C-10 22VP10C-10	22V10C-12 22VP10C-12	22V10C-15 22VP10C-15
I_{CC} (mA)	Commercial	190	190	190	
	Military			190	190
t_{PD} (ns)	Commercial	7.5	10	12	
	Military			12	15
t_s (ns)	Commercial	3.0	3.6	4.5	
	Military			4.5	7.5
t_{CO} (ns)	Commercial	6.0	7.5	9.5	
	Military			9.5	10
f_{MAX} (MHz)	Commercial	111	90	71	
	Military			71	57

4

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC} Max.

DC Input Voltage ..... −0.5V to + 5.5V

DC Input Current ..... −30 mA to + 5 mA (except during programming)

DC Program Voltage 10V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 5%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−250	50	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IH} = GND Outputs Open		Com'l		190	mA
				Mil		190	

Notes:

2. t_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Switching Characteristics PAL22V10C/PAL22VP10C[5]

Parameters	Description	Commercial						Military				Units
		-7		-10		-12		-12		-15		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[6]		7.5		10		12		12		15	ns
t_{EA}	Input to Output Enable Delay		7.5		10		12		12		15	ns
t_{ER}	Input to Output Disable Delay[7]		7.5		10		12		12		15	ns
t_{CO}	Clock to Output Delay[6]		6		7.5		9.5		9.5		10	ns
t_S	Input or Feedback Set-Up Time	3		3.6		4.5		4.5		7.5		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	9		11.1		14		14		17.5		ns
t_{WH}	Clock Width HIGH[8]	3		3		3		3		6		ns
t_{WL}	Clock Width LOW[8]	3		3		3		3		6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[9]	111		90		71		71		57		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[8, 10]	166		166		166		166		83		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11]	133		100		83		83		66		MHz
t_{CF}	Register Clock to Feedback Input[12]		4.5		6.4		7.5		7.5		7.5	ns
t_{AW}	Asynchronous Reset Width	8.5		10		12		12		15		ns
t_{AR}	Asynchronous Reset Recovery Time	5		6		7		7		10		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		12		12		14		14		20	ns
t_{SPR}	Synchronous Preset Recovery Time	5		6		7		7		10		ns
t_{PR}	Power-Up Reset Time[13]	1		1		1		1		1		µs

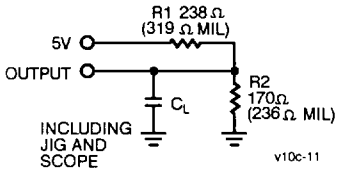
Notes:

5. AC test load used for all parameters except where noted.
6. This specification is guaranteed for all device outputs changing state in a given access cycle.
7. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
8. Tested initially and after any design or process changes that may affect these parameters.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11) minus t_S.
13. The registers in the PAL22V10C/PAL22VP10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

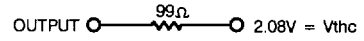
Capacitance[8]

Parameters	Description	Typical	Max.	Units
C_{IN}	Input Capacitance	11		pF
C_{OUT}	Output Capacitance	9		pF

AC Test Loads and Waveforms

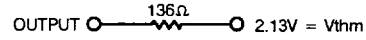


Equivalent to: THÉVENIN EQUIVALENT



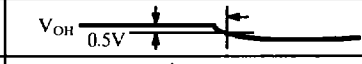
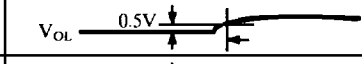
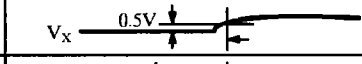
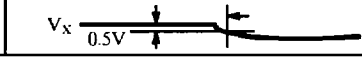
Commercial

Equivalent to: THÉVENIN EQUIVALENT

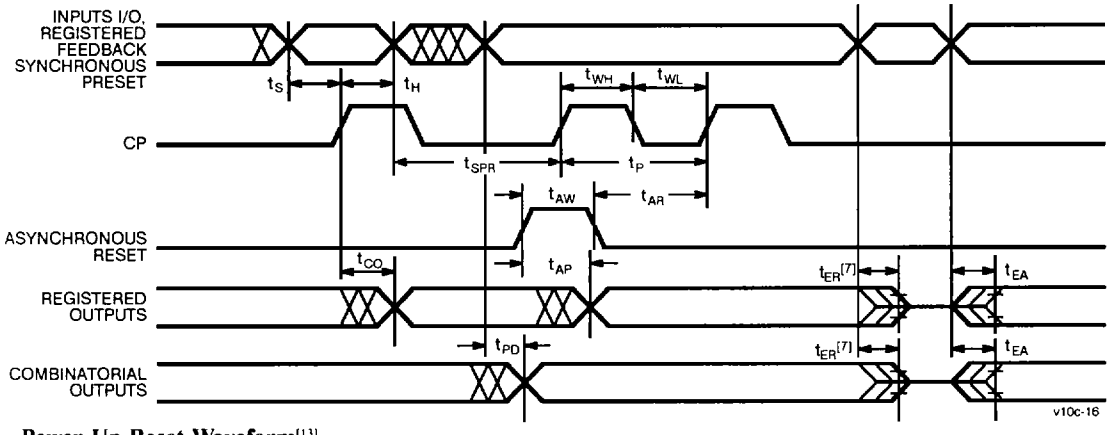


Military

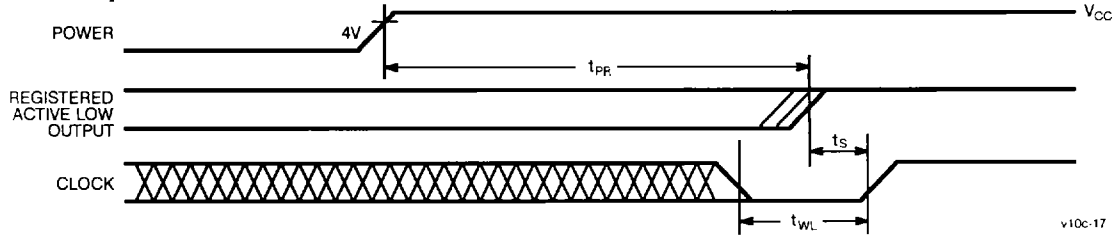
Specification	C_L	Package	Measurement Level
t_{PD}, t_{CO}, t_{CF}	15 pF	PDIP, CDIP	1.5V
	50 pF	PLCC, LCC	
t_{EA}	15 pF	PDIP, CDIP	See t_{EA} Waveform
	50 pF	PLCC, LCC	
t_{ER}	5 pF	All	See t_{ER} Waveform

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 v10c-12
$t_{ER(+)}$	2.6V	 v10c-13
$t_{EA(+)}$	V_{thc}	 v10c-14
$t_{EA(-)}$	V_{thc}	 v10c-15

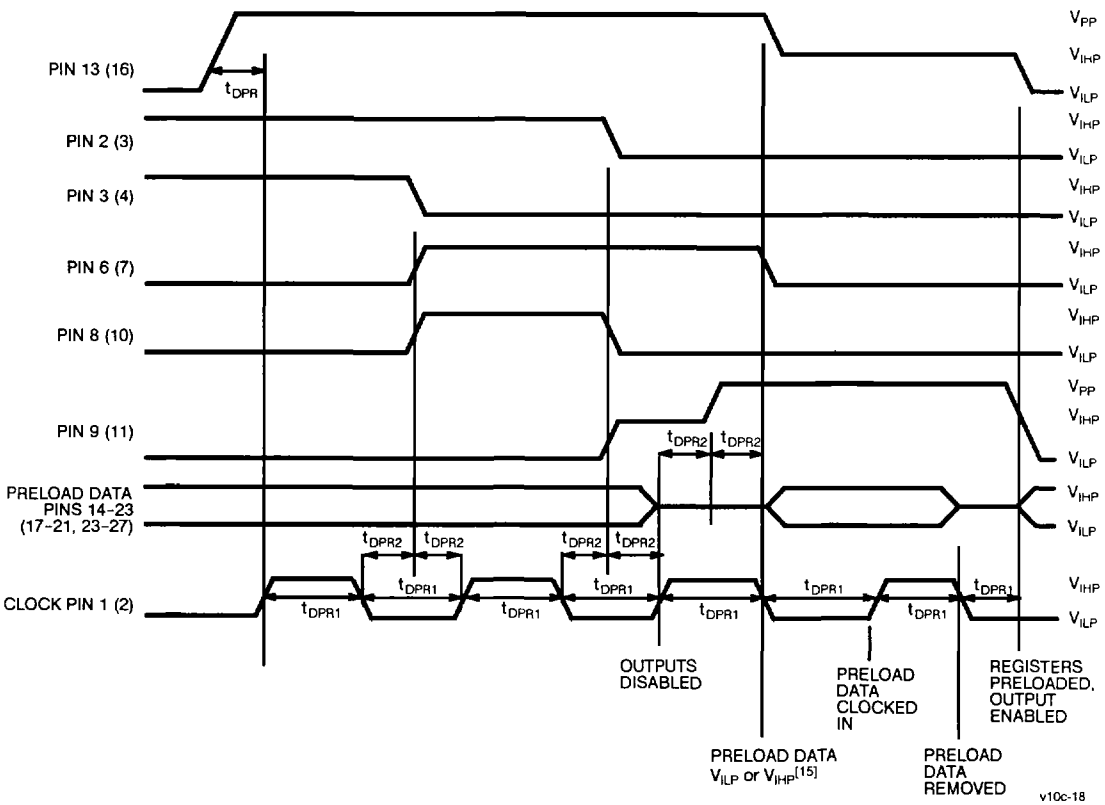
Switching Waveform



Power-Up Reset Waveform[13]



Preload Waveform[14]



Notes:

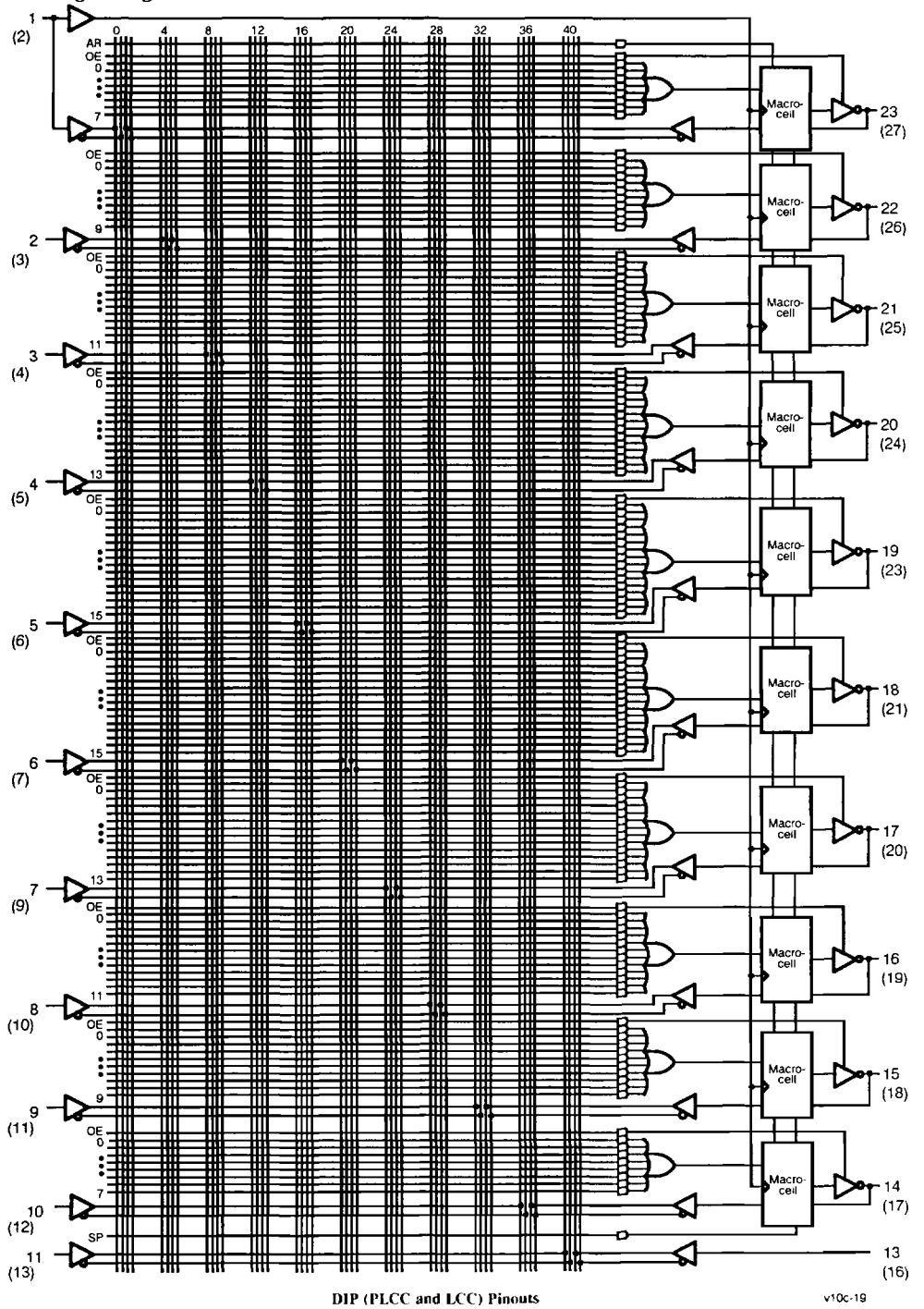
14. Pins 4 (5), 5 (6), 7 (9) at V_{ILP} ; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
15. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

DIP (PLCC, LCC) Pinouts

Forced level on register pin during preload	Register Q output state after preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V

Functional Logic Diagram for PAL22V10C/PAL22VP10C



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Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Operating Range
190	7.5	111	PAL22V10C-7PC	P13	Commercial
			PAL22V10C-7DC	D14	
			PAL22V10C-7JC	J64	
			PAL22VP10C-7PC	P13	
			PAL22VP10C-7DC	D14	
			PAL22VP10C-7JC	J64	
	10	90	PAL22V10C-10PC	P13	Commercial
			PAL22V10C-10DC	D14	
			PAL22V10C-10JC	J64	
			PAL22VP10C-10PC	P13	
			PAL22VP10C-10DC	D14	
			PAL22VP10C-10JC	J64	
	12	71	PAL22V10C-12PC	P13	Commercial
			PAL22V10C-12DC	D14	
			PAL22V10C-12JC	J64	
			PAL22VP10C-12PC	P13	
			PAL22VP10C-12DC	D14	
			PAL22VP10C-12JC	J64	
			PAL22V10C-12DMB	D14	Military
			PAL22V10C-12LMB	L64	
			PAL22VP10C-12DMB	D14	
			PAL22VP10C-12LMB	L64	
	15	57	PAL22V10C-15DMB	D14	Military
			PAL22V10C-15LMB	L64	
			PAL22VP10C-15DMB	D14	
			PAL22VP10C-15LMB	L64	

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