NATEL

DSC6206
SPA 6200

Reference Powered, 25 VA Output 16-bit, 4 Arc-minute Accuracy Digital-to-Synchro Converter

Features

- **Fully Protected 25 VA Output**
  (current limiting)
  (short circuit proof)
  (thermal cut-off)
  (over-voltage transient protected)
- ✓ **No DC Power Supplies Needed**
  (reference powered)
- **Microprocessor Compatible**
  (8- and 16-Bit)
- **Double-Buffered Digital Inputs**
- ✓ **4 Arc-minute Accuracy**
- ✓ **Low power Dissipation**
  (1.25 watts per VA delivered to load)
- **Built-in "KICK" Circuit**
  (prevents synchro "hang-ups")
- **Fully Isolated Operation**
  (inputs/outputs/reference)
- **BIT** (built-in-test) **Output**
- **Compact Bulkhead Mounting**
  (7.4 X 5.1 X 1.8 inches – 400 Hz model)

DSC6206
SPA6200

Applications

Training Simulators
Remote Indicators
Gun Fire Control
Navy Re-transmission Systems
Test Equipment

NATES008

Description

The Model **DSC6206** is the first 4 arc-minute 25 VA synchro driver with Built-in 16-bit Digital-to-Synchro capability. The 25 VA output power is delivered efficiently through a reference-powered design that develops an internal "dynamic power supply" which reduces power dissipation by a factor of 2 over conventional designs. The **6206** has an extremely low (0.05%) scale factor variation which further helps reduce power when driving TR loads. Being reference powered, it also eliminates the need for all external dc power supplies. Packaged in a single, bulkhead-mount chassis with 1/8 inch thick solid base plate, the **6206** offers excellent thermal transfer and high reliability.

The high output drive power of 25 VA makes the **6206** the ideal choice when driving single and multiple active Torque Receiver (TR) Synchro loads, Control Differential Transmitters (CDX's) and Control Transformers (CT's). Included also is a built-in "KICK" circuit which senses when a TR load may be "hung-up" and automatically shifts the output angle by 120° to free-up the synchro. In addition, the output stage is fully protected and includes fast-acting active current limiting, thermal cutoff, and output stage transient suppression to make the **6206** virtually indestructible.

Logic interface to the **6206** includes a built-in test (BIT) output signal, which continuously monitors internal operation and a disable input to control power-up sequencing in large systems.Model **6206** is packaged in the same size as just the booster amplifier available until now.

For existing designs, a pin and size compatible model SPA6200 without the built-in Digital-to-Synchro converter is made available that offers superior performance features - - - - - high accuracy of 3 arc-minutes, Remote sensing, does not require any dc power supplies (not even +5 V-dc) and offers more options for Reference, Input and Output voltages.

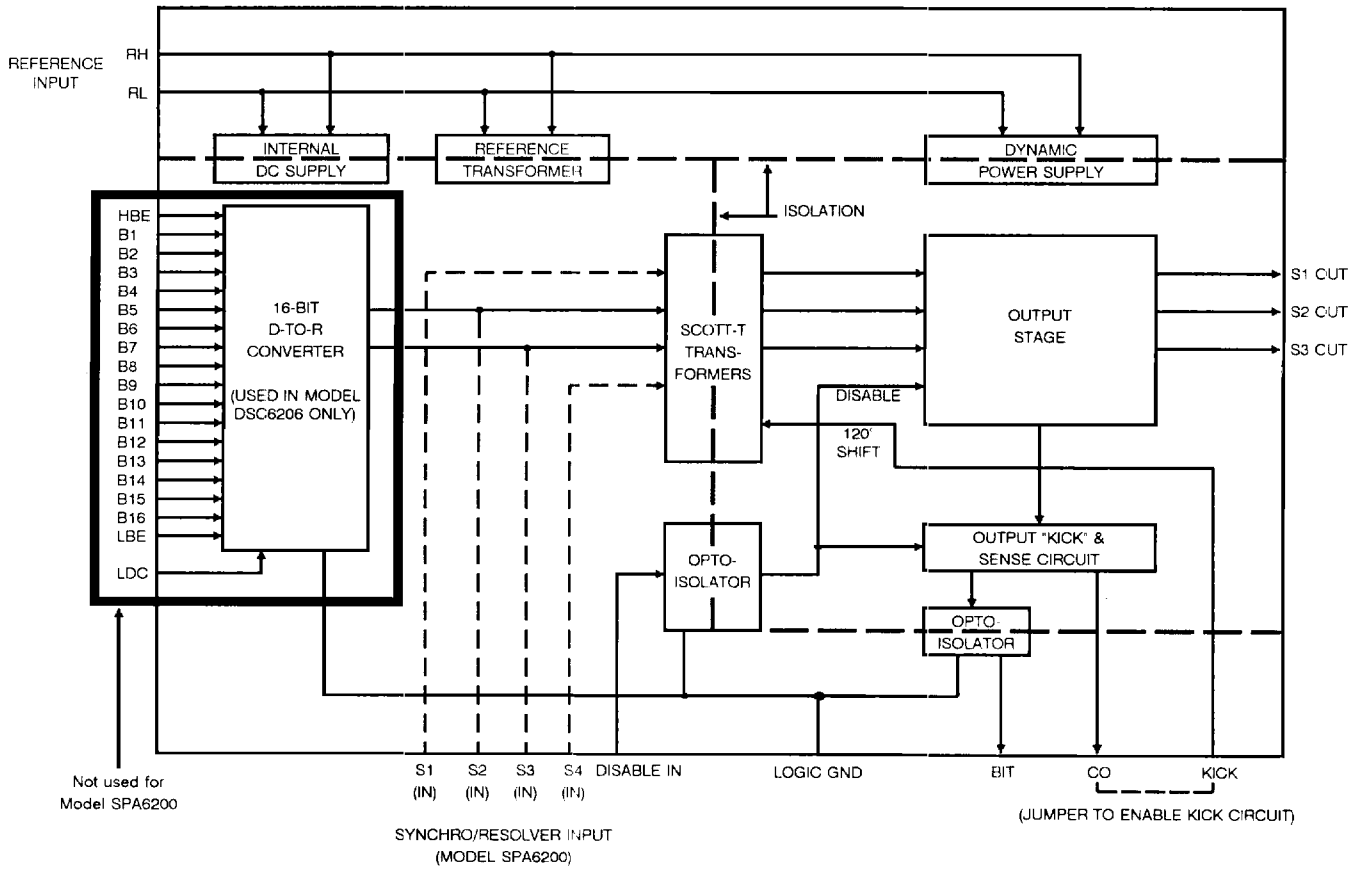


FIGURE 1 DSC6206 FUNCTIONAL BLOCK DIAGRAM

The operation of **Model 6206** is illustrated in the functional block diagram of Figure 1. The reference voltage (RH-RL) is received by both power and reference isolation transformers. One power transformer provides bias and dynamic power supply voltages to the output stage; while another acts as the "internal dc supply" to provide power to the input circuitry, and is therefore referenced to the incoming "logic ground" line. The reference isolation transformer provides a scaled-down representation of the input reference to the 16-bit D-to-R converter (not required for Model 6200).

The digital word representing the input angle is applied to the "16-bit D-to-R converter," which is configured to accept independently-enabled bytes of 8 bits each. These bytes are controlled by the HBE (high byte enable) and LBE (low byte enable) input logic controls. When interfacing the DSC6206 to an 8-bit microprocessor, these registers are normally addressed sequentially over common data lines. When interfacing to a 16-bit data bus, both input registers are enabled simultaneously to accept a single 16-bit word. The "LDC" input then loads the 16-bit word into the converter. This double-buffering is especially important in 8-bit microcomputer-based systems where false codes and servo "hunting" would otherwise occur. HBE, LBE and LDC input enables are "level sensitive" type inputs. The output of the D-to-R is changed from sine/cosine to synchro format through an isolation scott-tee type transformer. The resultant 3 signals are then applied to the output stages. For the analog input versions (SPA6200), an external signal is applied to the scott-tee input transformers, which are configured to accept either low-level (6.81 V-rms) resolver format input, (11.8 V-rms) synchro-format input, or high-level synchro input (90 V-rms). In these versions, the D-to-R converter is omitted from the unit.

The output stage consists of three precision power amplifiers in push-pull class AB configurations, powered from a dynamic power supply. This dynamic supply reduces the dissipation in the output section by allowing the output transistors to operate with less average voltage across them as compared to operation from a fixed dc power source. To assure stable operation over temperature and load variations, precision operational amplifiers are used as the primary amplifier gain element. In addition to providing short circuit protection, current limiting, and voltage-transient protection; the power amplifiers are designed to shut down in a high impedance output state when the amplifier temperature reaches 125°C, thereby making them virtually indestructible.

An internal "KICK" circuit is used in the **6206** to prevent the possibility that the torque receiver may become locked at 180° from the true angle. It does this by shifting the electrical angle by 120° if the output is in current limit for more than four seconds.

Additional logic signals include a "disable" input and a "BIT" (Built-In-Test) output. The disable input allows the output stage of the **6206** to be forced into a high impedance mode for fault isolation or in controlling power-up in systems using many **Model 6206's**.

The internal BIT circuit provides a fault indication if there is an output short circuit or overload, internal thermal shutdown, or internal circuit failure.

Specifications

PARAMETER	VALUE	REMARKS	TEST LEVEL
Accuracy			
SPA6200 DSC6206	±3.0 arc-minutes ±4.0 arc-minutes (Option S) ±8.0 arc-minutes (Option P)	Accuracy applies over the full operating temperature, frequency, power supply, and load ranges.	Note 1
Reference/Signal Input			
Reference Voltage	115 V-rms, ±10% option 9(5) 26 V-rms, ±10% option 1	For 90 (11.8) V-rms output For 11.8 V-rms output	Note 2
Frequency	360 to 440 Hz, (option 4) 54 to 440 Hz, (option 6)		Note 3
Reference Input Current 115 V-rms input [option 9 (5)]	 85 mA-rms maximum 500 (700) mA-rms maximum 1.0 (1.5) A-rms maximum	 V_{ref} = 115 V-rms, no load V_{ref} = 115 V-rms, 25 VA load V_{out} = 90 (11.8) V_{ref} = 115 V-rms, short circuit V_{out} = 90 (11.8)	Note 1
26 V-rms input (option 1)	500 mA-rms maximum 3.0 A-rms maximum 6.0 A-rms maximum	V_{ref} = 26 V-rms, no load V_{ref} = 26 V-rms, 25 VA load V_{ref} = 26 V-rms, short circuit	
Breakdown Voltage	500 V-dc minimum	To logic ground or any output	Note 3
Harmonic Distortion	Up to 10%	Without degradation in accuracy	Note 3
Signal Input Voltage (SPA6200 only)	90 V-rms ±10% (option 9) 11.8 V-rms ±10% (option 1) 6.8 V-rms ±10% (option 6)	Synchro-format Synchro-format Resolver-format	
Digital Inputs		Transient-protected CMOS	
Data Bit Coding	Positive logic, natural binary angle	Bit 1 is MSB, Bit 16 is LSB	Note 3
Logic "0" level Logic "1" level	-0.3 to 0.8 V-dc 2.4 to 5.5 V-dc		Note 2
Input Current Data bits 1-16	15 μA typical (30 μA max.), active pull down to ground	Unused pins may be left unconnected	Note 3
Input Current HBE, LBE, LDC	-15 μA typical (-30 μA max), active pull up to internal 5 V-dc	Unused pins may be left unconnected	Note 3
Disable Input Input Current Logic "0" Logic "1"	 -0.4 mA maximum 40 μA maximum	 Synchro outputs enabled Synchro outputs disabled	Note 3
Register Controls		Active-high transparent latches	
HBE	Logic "1" Logic "0"	Data bits 1-8 enter high-byte input register High-byte input register holds data	Note 1
LBE	Logic "1" Logic "0"	Data bits 9-16 enter low-byte input register Low-byte input register holds data	Note 1
LDC	Logic "1" Logic "0"	Data from input register enters holding register Holding register holds data	Note 1
Pulse Width HBE, LBE, and LDC	600 ns minimum	For guaranteed data transfer	Note 3
Data Set-up Time	200 ns minimum	Data stable before HBE,LBE low-to-high transition	Note 3
Data Hold Time	200 ns minimum	Data stable after HBE,LBE high-to-low transition	Note 3
BIT Output		Referenced to Digital Ground	
Output Current Sink Source	 3 mA minimum @ 0.8 V-dc 300μA minimum @ 2.4 V-dc	 "LS" TTL output	Note 3
Logic "0" Logic "1"	-0.3 to +0.8 V-dc 2.4 to +5 V-dc	For no fault detected Fault detected	Note 1

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Synchro Analog Outputs			
Voltages (Line-to-Line)	90 V-rms nominal (option 9) 11.8 V-rms nominal (option 1)	For nominal reference voltages. The outputs vary in direct proportion to the reference for 6206 and signal input for 6200	
Scale Factor Accuracy (No Load) (With Remote Sense)	±1% maximum	Signal to Output (6200) Reference to Output (6206)	Note 1
Radius Accuracy (DSC6206)	0.05% maximum	Scale factor variation with digital angle	Note 2
Drive Capability	25 VA minimum	All options	Note 1
Output Current Drive	455 mA peak minimum (option 9) 3.5 A peak minimum (option 1)	Between S1, S2, and S3 outputs	Note 3
Output Impedance (dc to 440 Hz)	Less than 0.05 (2.5) ohms	Using output remote sense For 11.8 (90) V-rms output	Note 3
Load Regulation	1% maximum	From no load to full load (with Remote Sense)	Note 2
Synchro load impedance	$\|Z_{so}\| > 4.2\Omega$ (option 1) $\|Z_{so}\| > 243\Omega$ (option 9)	25 VA limits For $\|Z_{ss}\|$ refer to pages 6 and 7	
Output Settling Time	500 μs (2 ms) maximum	179° step for 400 Hz (60 Hz)	Note 2
Phase Shift	Less than 2 (5) degrees	Ref/Signal to output for 400 Hz (60 Hz)	Note 3
Quadrature Output	0.25% maximum		Note 2
Output dc Offset (Line-to-Line)	±10 mV typical, ±50 mV max. ±1.5 mV typical, ± 8 mV max.	For 90 V-rms L-L output models For 11.8 V-rms L-L output models	Note 2
Thermal Cut-off	85°C base-plate temperature min.		Note 2
Output Short Circuit Duration	Indefinite	All outputs together simultaneously	Note 3
Power Dissipation		**Internal**	
No Load 25 VA Load	10 watts maximum 35 watts maximum (90V Output) 50 watts maximum (11.8V Output)	For resistive loads. Does not include power dissipated in the load	Note 3
Thermal Resistance		**Based on internal module dissipation**	
Baseplate to Ambient Junction to baseplate	2°C per watt typical 1.5°C per watt maximum	Actual value depends upon cooling configuration For the worst case device junction	Note 3 Note 3
Physical Characteristics			
Size	7.4 X 5.1 X 1.8 inches (188 X 130 X 46 mm) 7.4 X 5.1 X 2.6 inches (188 X 130 X 66 mm)	For 400 Hz version For 60 Hz version	Note 3
Weight	4 pounds (1.8 Kg) maximum 7 pounds (3.2 Kg) maximum	For 400 Hz version For 60 Hz version	Note 3

NOTE 1: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3 Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

Pin Designations

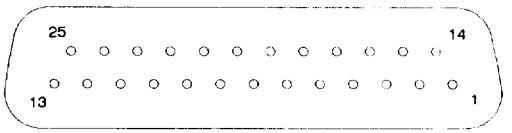


Figure 2 Model SPA6200 Pin Assignments
Connector is 25 pin, D-type, male pins, or equivalent
(Viewed from terminals)

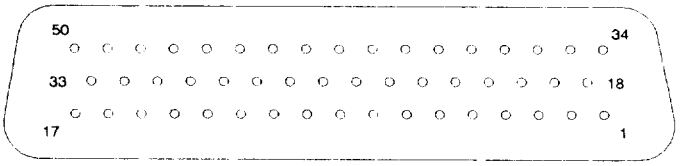


Figure 3 Model DSC6206 Pin Assignments
Connector is 50 pin, D-type, male pins, or equivalent
(Viewed from terminals)

Pin	Function/Description
1	No Connection
2	BIT - Built-in-Test Logic Output - "LS" TTL output signal referenced to "GND" (pin 16) Logic "0" = no fault condition present Logic "1" = fault condition
3	No Connection.
4	S1 Output - Isolated analog synchro output.
5	S1 Remote Sense Input - Connect to S1 output for remote sense
6	"KICK" Logic Input - Jumper to pin 18 (CO) to enable "KICK" circuit. Otherwise leave open.
7	Internal Test Point - Do not use or connect to this pin
8	S3 Remote Sense Input - Connect to S3 output for remote sense.
9	S1 Input - Synchro Analog Input (SPA6200 Only)
10	S3 Input - Synchro Analog Input (SPA6200 Only)
11	S4 Input - Resolver Analog Input (SPA6200 Only)
12	S2 Input - Synchro Analog Input (SPA6200 Only) For 90 and 11.8 V-rms synchro input versions, (option 9, 1) S1, S2, S3 are inputs, S4 is N.C. For 6.8 V-rms resolver input version (option 6), S2 is cosine input, S3 is sine input, S4 is cosine return, S1 is sine return.
13	Internal Test Point.
14	"DISABLE" Logic Input - "LS" TTL input signal referenced to "GND" (pin 16) Logic "0" = enable output Logic "1" = disable output Open circuit = disable output
15	No Connection.
16	Digital Ground - Ground to the systems logic ground.
17	S3 Output - Isolated analog synchro output.
18	"CO" Logic Output - Connect to "KICK" input (pin 6) to enable internal kick circuit. Otherwise, leave open.
19	No Connection.
20	S2 Remote Sense Input - Connect to S2 output for remote sense.
21	S2 Output - Isolated analog synchro output.
22	No Connection.
23	RH - Reference High Input - 115 V-rms for options 5 and 9. 26 V-rms for option 1.
24	RL - Reference Low Input.
25	No Connection.
26	No Connection.
27	No Connection.
28	No Connection.
29	No Connection.
30	HBE - High-Byte Enable - Data bits 1-8 enter the input buffer register when HBE is set to a logic "1." When HBE is at logic "0," input data bits are ignored.
31	LBE - Low-Byte Enable - Data bits 9-16 enter the input buffer register when LBE is set to a logic "1." When LBE is at Logic "0," input data bits 9-16 are ignored.
32	LDC - Load Converter - When LDC is set to logic "1," the converter transfers the contents of the two 8-bit input registers to the internal D-to-R converter. When LDC is at logic "0," data held in the 8-bit input registers is ignored.
33	GND - Digital Ground - Ground reference for data bits 1-16, HBE, LBE, and LDC. Internally connected to pin 16.
34	No Connection.
35	BIT 1 - Parallel Input Data Bits (MSB = 180°).
36	BIT 2 -
37	BIT 3 -
38	BIT 4 -
39	BIT 5 -
40	BIT 6 -
41	BIT 7 -
42	BIT 8 -
43	BIT 9 -
44	BIT 10 -
45	BIT 11 -
46	BIT 12 -
47	BIT 13 -
48	BIT 14 -
49	BIT 15 -
50	BIT 16 - Parallel Input Data Bits (LSB = 0.0055°)

Shaded area pins apply to Model 6206 only.

Output Protection

The **Model 6206** incorporates several protection methods that together make the **6206** virtually indestructible. These methods are:

1. Active current limiting
2. Thermal cut-off
3. Overvoltage transient protection

The active current limiting circuitry in the **6206** continuously monitors the instantaneous current in each of the three output drivers. When an overcurrent or output short circuit condition exists, the peak current that can be supplied to the load is instantly limited to a value that is safe for the components used within the **6206**.

The thermal cut-off circuit of the **6206** uses a solid-state temperature-sensing element attached to the top plate. The voltage from this temperature sensor provides an indication when the power amplifiers temperature reaches 125°C. If this occurs, a disable signal is applied to each of the output power amplifiers, which removes all output current drive capability. The result is that the outputs go into a high-impedance state and are no longer capable of driving load current. When the internal temperature drops to a safe level, the output stages are automatically restored to their normal state.

The **6206** incorporates overvoltage transient protection on both the reference input and the synchro outputs. These transient protection networks utilize rugged transient suppression diodes that automatically conduct to suppress transient energy whenever the applied voltages reach dangerous levels. The reference-protection diode is connected internally across RH-RL and may begin to conduct if the reference input (RH-RL) reaches 190 volts peak (42 volts peak for option 1). The output-protection diodes are connected in a "delta" configuration, with one diode between each of the S1-S2, S2-S3, and S1-S3 output pairs. Transient protection is necessary at the output of the **6206** due to the fact that synchros are, by nature, inductive loads and can produce voltage transients many times their nominal voltage due to inductive "kick."

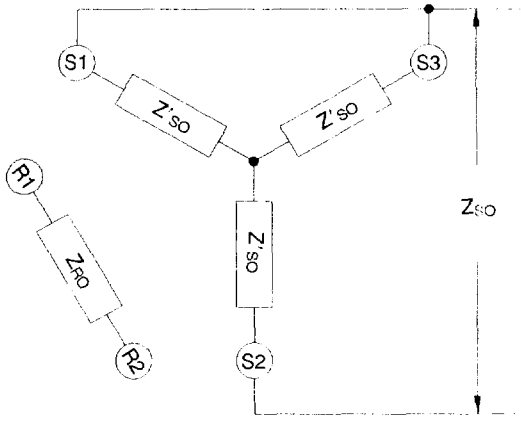


FIGURE 4 Synchro Load Schematic

Synchro Loads

There are several types of synchro loads, including Control Transformers (CT's), Torque Receivers (TR's), and Control Differential Transmitters (CDX's). The 25 VA output drive of the **6206** makes it possible to drive all but the heaviest TR loads easily. In many cases, the **6206** can drive multiple loads. The two most common loads driven by the **6206** are CT's and TR's.

CT's are electromechanical synchro devices which provide a null voltage output from the rotor winding whenever the actual shaft angle of the CT matches the angle sent to the CT from the S1, S2, and S3 outputs of the **6206**. The actual transfer function of a CT is as follows:

$$V_{rotor}\ (rms) = K \times V_{L\text{-}L} \times \sin(\theta - \phi)$$

where:

K	=	gain of the CT
$V_{L\text{-}L}$	=	line-to-line voltage from **6206**
θ	=	the angle represented by the **6206** output
ϕ	=	the CT shaft angle

In systems that use CT's, they are utilized as position sensing elements rather than as torque or motor elements. The force that is used to position the shaft generally is provided by a motor coupled to the common shaft. CT impedances, therefore are relatively high.

A schematic diagram of a typical synchro load is shown in Figure 4. Z_{so} is the impedance measured between one leg (S2, for example) and the other two legs (S1, S3) shorted together, with the rotor open circuit. The relationship between Z_{so} and the individual winding impedances (Z'_{so}) is given by:

$$Z_{so} = (3/2) \times Z'_{so}$$

The relationship between the synchro output voltages, output VA, and Z_{so} is as follows:

$$VA = 3/4 \times V^2/Z_{so}$$

where:

VA is the VA required from the **6206** to drive the load and V is the rms value of the maximum line-to-line **6206** output voltage*

*The maximum value of an rms voltage refers to the rms voltage level when the voltage is at its maximum value, since the line-to-line output voltages vary with input digital angle. For example, the rms voltage between S3 and S1 is maximum when the input angle is 90°.

Example:

From **6206** Data Sheet, page 4, the 90 V-rms output option can drive $|Z_{so}| = 243$ ohms. To calculate the VA drive:

$$VA = 3/4 \times V^2/Z_{so} = 3/4 \times (90)^2/243$$

$$VA = 25.0$$

Absolute Maximum Ratings

Reference Input (options 5, 9)	.138 V-rms
Reference Input (option 1)	.35 V-rms
Digital Inputs	−0.3 to +6.5 V-dc
Storage Temperature	−65°C to +135°C

Although the digital inputs have integral transient protection, this protection is not a substitute for proper electrostatic handling procedures. This part is ELECTROSTATIC SENSITIVE and must be treated as such.

Driving Torque Receivers

The **Model 6206** can be used to drive single or multiple Torque Receiver (TR) loads. TRs are constructed in the same manner as CTs, except that they generally have much lower impedances than CTs and are meant to provide torque to the rotating shaft.

TRs provide torque as a result of the interaction of two magnetic fields within the TR; one field produced by the S1, S2, and S3 stator windings, and one field from a reference source applied to the rotor windings. The TR can be considered an "active" load in that it "acts" against the opposing **6206** output, depending upon shaft angle, to produce a torque at the TR shaft. Torque is produced whenever the TR shaft angle and the **6206** input angle are different, thereby producing a voltage gradient between the **6206** output and the TR stator output. Circulating currents are developed as a result of this voltage gradient to provide the "magnetomotive force" that produces the "opposing" magnetic field against the rotor field. The opposing magnetic fields within the TR apply a torque gradient in attempting to rotate the TR shaft until the shaft angle is equal to the **6206** input angle. When the two angles are equal, the result is a "null" condition where the torque gradient is zero.

Theoretically, the TR represents an infinite load impedance to the **6206** output when the TR shaft angle is exactly equal to the **6206** input angle. In actual practice, however, the effective load impedance at "null" (shaft angle = **6206** input angle) will be reduced by the effects of two variables:

1. Line-to-line voltage differential between the TR stator and **6206** output.

2. Line-to-line phase-shift differential between the TR stator and **6206** output.

Any such line-to-line voltage and/or phase-shift differentials will give rise to an additional VA (voltage-ampere) requirement from the **6206**, resulting in a loss of available VA for producing torque. This additional VA requirement is as follows:

$$VA_{D/S} = [3(V_{L\text{-}L})^2/2Z_{SS}] \times \sqrt{(\Delta E/2V_{L\text{-}L})^2 + [\sin(\Delta\sigma/2)]^2}$$

where:

$V_{L\text{-}L}$ = **6206** maximum L-L voltage
ΔE = (**6206** - TR) L-L voltage differential
Z_{SS} = Stator impedance with rotor shorted
$\Delta\sigma$ = (**6206** - TR) phase shift differential (°)

For example, to find the additional VA required by the **6206** (excluding the VA required to produce torque), consider the following example of driving a type 18TRX4a torque receiver:

$V_{L\text{-}L}$ = 90 V-rms
ΔE = 2.7 V-rms (3% of 90 V-rms)
$|Z_{SS}|$ = 17 ohms
$\Delta\sigma$ = 20.0°
VA_{6206} = 24.3 VA

As this example demonstrates, VA is easily "stolen" from the **6206** due to line-voltage and phase-shift differentials. This is an important point to consider when designing TR systems.

The torque gradient required from the TR shaft will depend upon the particular application. Some applications, such as driving indicators or other visual readouts will not require much torque. Other applications, where the TR may be driving heavier loads, will require more VA. The torque that can be provided to the shaft will depend upon the type of TR; the "available" VA after the effects outlined above are accounted for and the difference between the shaft angle and the input angle to the **6206**. The VA required by the TR to produce a torque gradient is described by the following equation:

$$VA_{6206} = [3(V_{L\text{-}L})^2/2Z_{SS}] \times \sin[(\theta-\phi)/2]$$

where:

$V_{L\text{-}L}$ = **6206** maximum L-L voltage
Z_{SS} = TR stator impedance with rotor shorted
θ = **6206** input angle
ϕ = TR shaft angle
VA_{6206} = Volt-amperes needed from **6206**

Consider an example where a type 26V11TR4c torque receiver is required to produce a torque gradient of 6 g-cms at a differential angle ($\theta-\phi$) of 5°. The operating parameters are the same as the previous example. The required VA from the **6206** can be calculated as follows:

$$VA = [3 \times (11.8)^2/(2 \times 3.7)] \times \sin(5/2)$$
$$= 2.5 \text{ VA}$$

This calculation should be combined with the previous calculation for the "additional" VA in order to predict the total VA required from the **6206**. In order to combine the calculations, the equation below should be used in order to take into account the phase relationship between the various current components supplied by the **6206**.

$$VA_{6206} =$$

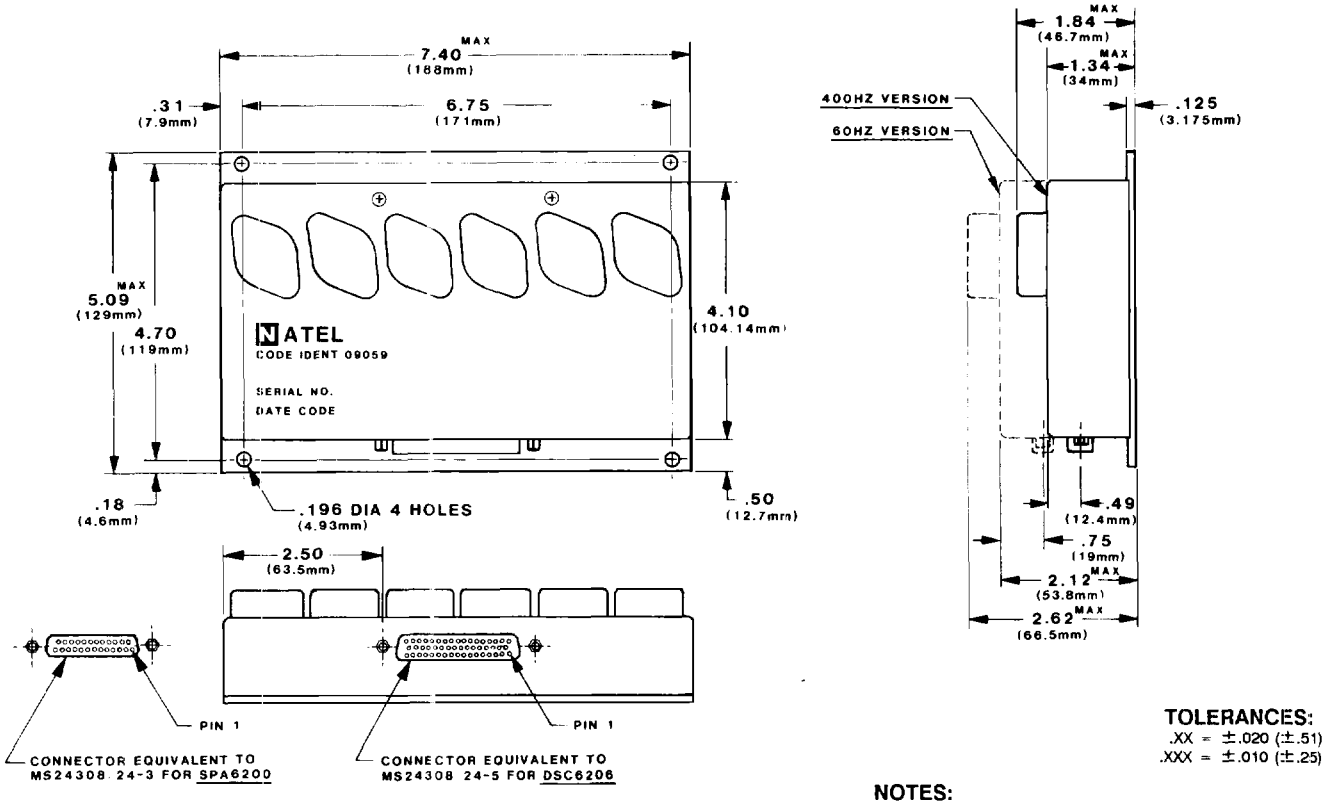
$$[3(V_{L\text{-}L})^2/2Z_{SS}] \times \sqrt{[(\Delta E/2V_{L\text{-}L}) + \sin\{(\theta-\phi)/2\}]^2 + [\sin(\Delta\sigma/2)]^2}$$

The terms for this equation are defined in the previous examples.

TABLE 1 VA Load on 6206 with TR at "Null"

TR Type	Frequency	Voltage ($V_{L\text{-}L}$)	$\lvert Z_{SS} \rvert$ (Nom)	Phase Shift (Maximum)	VA "Null"
26V11TR4c	400	11.8	3.7	6.0°	3.1
11TR4c	400	90.0	215.0	6.0°	3.1
15TRX4a	400	90.0	66.0	5.0°	8.5
18TRX4a	400	90.0	19.0	4.0°	24.3
15TRX6a	60	90.0	920.0	20.0°	2.3
18TRX6b	60	90.0	390.0	16.0°	4.4
23TRX6b	60	90.0	128.0	11.0°	9.2

Voltage imbalance ($\Delta E/V_{LL}$) used in calculations: ±3%.



TOLERANCES:
.XX = ±.020 (±.51)
.XXX = ±.010 (±.25)

NOTES:
Dimensions shown in inches and (mm)

MECHANICAL OUTLINE

Ordering Information

DSC6206 - T F R A M

Temperature Range

1 = 0°C to +70°C
2 = −40°C to +85°C

Frequency

4 = 400 (360 to 440) Hz
6 = 60 (54 to 440) Hz

Reference/Output Voltage

1 = 26 V-rms ref/11.8 V-rms output (400Hz Only)
5 = 115 V-rms ref/11.8 V-rms output (400Hz Only)
9 = 115 V-rms ref/ 90 V-rms output

Accuracy

P = ± 8 Arc minutes
S = ± 4 Arc minutes

Mil Specification

B = MIL-STD-883B
S = Standard

SPA6200 - T F R I M

Temperature Range

1 = 0°C to +70°C
2 = −40°C to +85°C

Frequency

4 = 400 (360 to 440) Hz
6 = 60 (54 to 440) Hz

Reference/Output Voltage

1 = 26 V-rms ref/11.8 V-rms output (400Hz Only)
5 = 115 V-rms ref/11.8 V-rms output (400Hz Only)
9 = 115 V-rms ref/ 90 V-rms output

Input Voltage

1 = 11.8 V-rms Synchro
6 = 6.8 V-rms Resolver
9 = 90 V-rms Synchro

Mil Specification

B = MIL-STD-883B
S = Standard

A wide range of applications assistance is available from Natel. Application notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

TEL: (805) 581-3950

NATEL ENGINEERING CO., INC.

4550 RUNWAY STREET • SIMI VALLEY, CA 93063-3493
TWX: (910) 494-1959 FAX: (805) 584-4357