

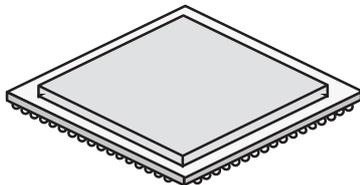
Features

- PowerPC single issue integer core.
- Precise exception model.
- Extensive system development support
 - on-chip watchpoints and breakpoints,
 - program flow tracking,
 - On-chip emulation (OnCE) development interface.
- High performance (Dhrystone 2.1: 52 MIPS @ 50 MHz, 3.3V, 1.3 Watts total power).
- Low power (< 241 mW @25 MHz, 2.4 V internal, 3.3 V I/O-core, caches, MMUs, I/O).
- MPC8XX PowerPC system interface, including a periodic interrupt timer, a bus monitor, and real-time clocks.
- Single Issue, 32-Bit Version of the Embedded PowerPC Core (fully Compatible with Book 1 of the PowerPC Architecture Definition) with 32 X 32 – Bit Fixed Point Registers
 - Embedded PowerPC Performs Branch Folding, Branch Prediction with Conditional Prefetch, without Conditional Execution
 - 4 Kbyte Data Cache and 4 Kbyte Instruction Cache, Each with an MMU
 - Instruction and Data Caches are two way, Set Associative, Physical Address, 4 Word Line Burst, Least Recently Used (LRU) Replacement, Lockable On-Line Granularity
 - MMUs with 32 Entry TLB, Fully associative Instruction and Data TLBs
 - MMUs Support Multiple Page Sizes of 4kB, 16 kB, 256 KB, 512 KB and 8 MB ; 16 Virtual Address Spaces and 8 Protection Groups
 - Advanced On-Chip-Emulation Debug Mode
- Up to 32-bit Data Bus (Dynamic Bus Sizing for 8 and 16 bits).
- 32 Address Lines
- Fully Static Design.
- $V_{CC} = +3.3 V \pm 5\%$
- $f_{max} = 66\text{ MHz}$ (80 MHz tbc)
- Military temperature range : $-55^{\circ}\text{C} < T_C < +125^{\circ}\text{C}$.
- $P_D = 0.75\text{ W}$ typical @ 66 MHz
- ATM SAR support available on TSPC860SR version

Description

The TSPC860 PowerPC™ QUad Integrated Communication Controller (**Power QUICC™**) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications and networking systems. The Power QUICC (pronounced "quick") can be described as a PowerPC-based derivative of TS68EN360 (QUICC™).

The CPU on the TSPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) of the TS68EN360 QUICC has been enhanced with the addition of the interprocessor-integrated controller (I²C) channel. Moderate to high digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the TSPC860 to support any type of memory, including high performance memories and newer dynamic random access memories (DRAMs). Overall system functionality is completed with the addition of a PCMCIA socket controller supporting up to two sockets and a real-time clock.



PBGA 357
ZP suffix

Screening / Quality

- This product will be manufactured in full compliance with :
- Or according to ATMEL-Grenoble standard.



TSPC860

32 BIT QUAD INTEGRATED POWER QUICC™ COMMUNICATION CONTROLLER

PRELIMINARY SPECIFICATION beta SITE



August 2000



SUMMARY

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A. GENERAL DESCRIPTION

The TSPC860 is functionally composed of three major blocks :

- A 32-bit PowerPC core with MMUs and caches
- A system interface unit
- A communications processor module

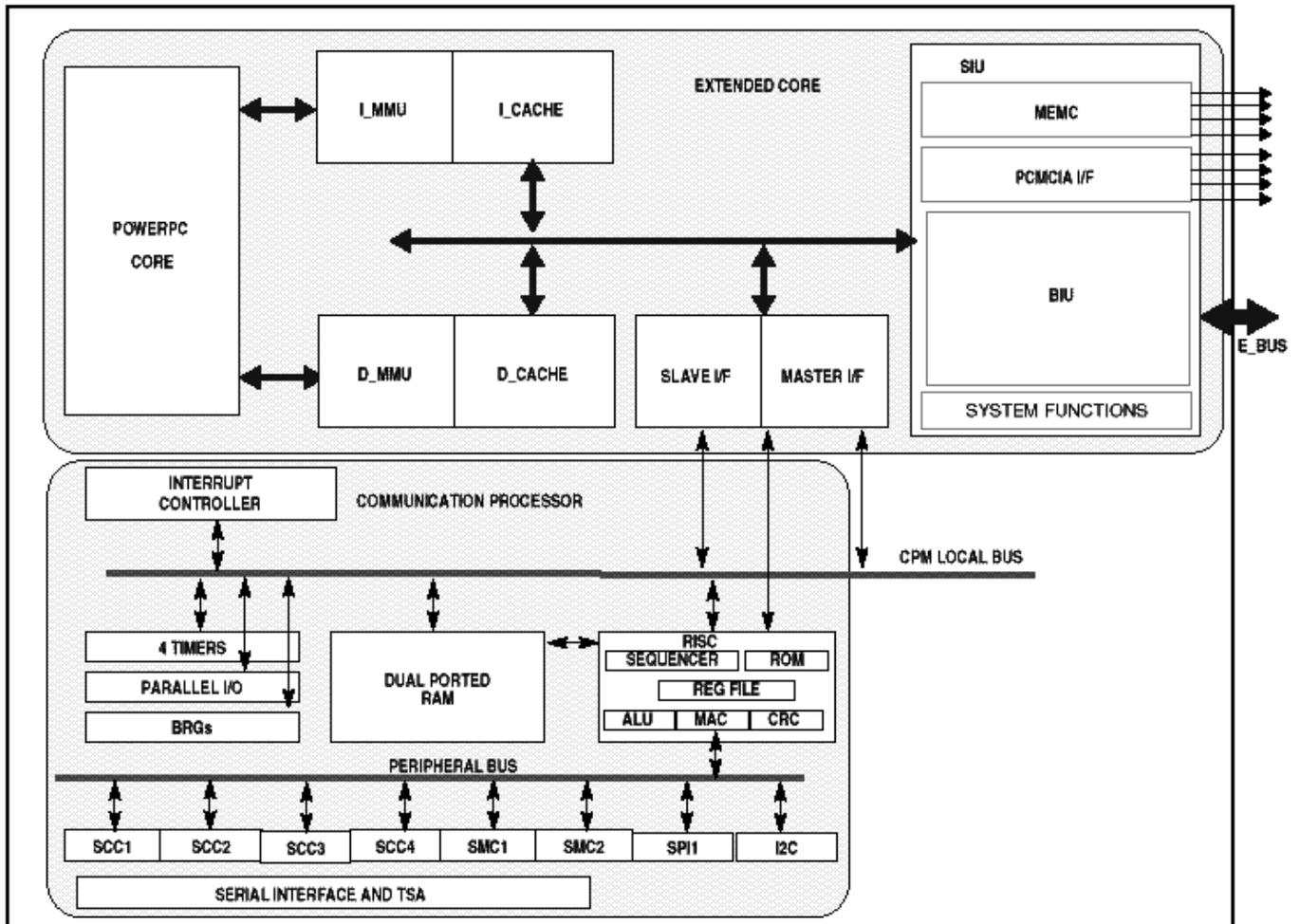


Figure 1 : Block diagram view of the TSPC860

1. MAIN FEATURES

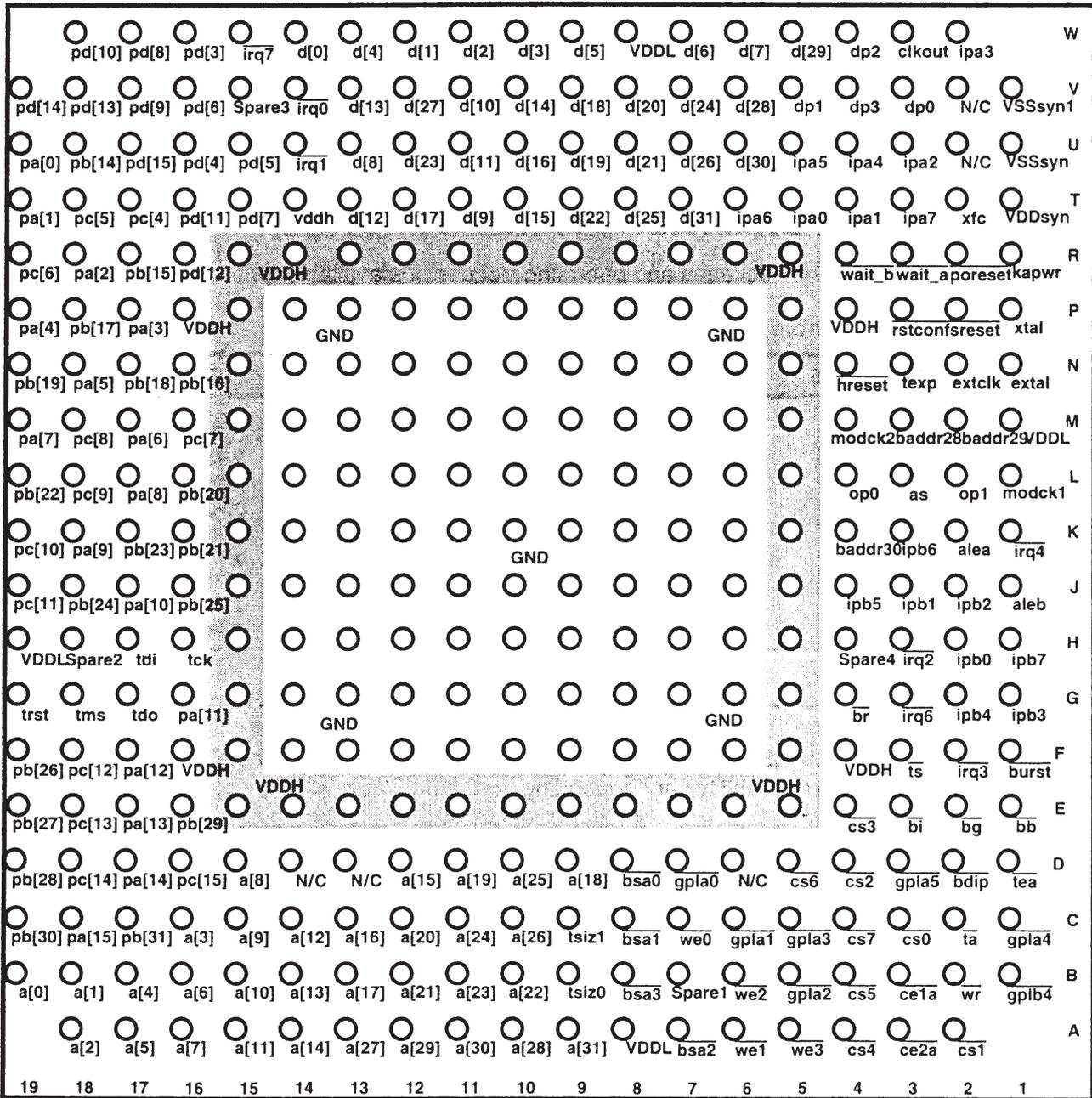
The following is a list of the TSPC860's important features:

- Fully static design
- Four major power saving modes
- 357 OMPAC ball grid array packaging (plastic)
- 32-bit address and data busses
- Flexible memory management
- 4-kbyte physical address, two-way, set-associative data cache
- 4-kbyte physical address, two-way, set-associative instruction cache
- Eight-bank memory controller
 - Glueless interface to SRAM, DRAM, EPROM, FLASH and other peripherals
 - Byte write enables and selectable parity generation
 - 32-bit address decodes with bit masks

- System interface unit-
 - Clock synthesizer-
 - Power management-
 - Reset controller-
 - PowerPC decrementer and time base-
 - Real-time clock register-
 - Periodic interrupt timer-
 - Hardware bus monitor and software watchdog timer-
 - IEEE 1149.1 JTAG test access port
- Communications processor module
 - Embedded 32-bit RISC controller architecture for flexible I/O
 - Interfaces to PowerPC core through on-chip dual-port RAM and virtual DMA channel controller
 - Continuous mode transmission and reception on all serial channels
 - Serial DMA channels for reception and transmission on all serial channels
 - I/O registers with open-drain and interrupt capability
 - Memory-memory and memory-I/O transfers with virtual DMA functionality
 - **Protocols** supported by ROM or downloadable microcode and include, but limited to, the digital portion of :
 - Ethernet / IEEE 802.3 CS/CDMA
 - HDLC2 / SDLC and HDLC bus
 - Apple talk
 - Signaling system #7 (RAM microcode only)
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BiSync) communications
 - Totally transparent
 - Totally transparent with CRC
 - Profibus (RAM microcode option)
 - Asynchronous HDLC
 - DDCMP
 - V.14 (RAM microcode option)
 - X.21 (RAM microcode option)
 - V.32bis datapump filters
 - IrDA serial infrared
 - Basis rate ISDN (BRI) in conjunction with SMC channels
 - Primary rate ISDN (MH version only)
 - Four hardware serial communications controller channels supporting the protocols
 - Two hardware serial management channels
 - Management for BRI devices as general circuit interface controller multiplexed channels
 - low-speed UART operation
 - Hardware serial peripheral interfaces
 - I²C (microwire compatible) interface
 - Time-slot assigner
 - Port supports Centronics interfaces and chip-to-chip
 - Four independent baud rate generators and four input clock pins for supplying clocks to SMC and SCC serial channels
 - Four independent 16-bit timers which can be interconnected as two 32-bit timers

2. PIN ASSIGNMENT

2.1. Plastic Ball Grid Array



TOP VIEW

Figure 2 : Pin Assignment

3. SIGNALS DESCRIPTION

This section describes the signals on the TSPC860.



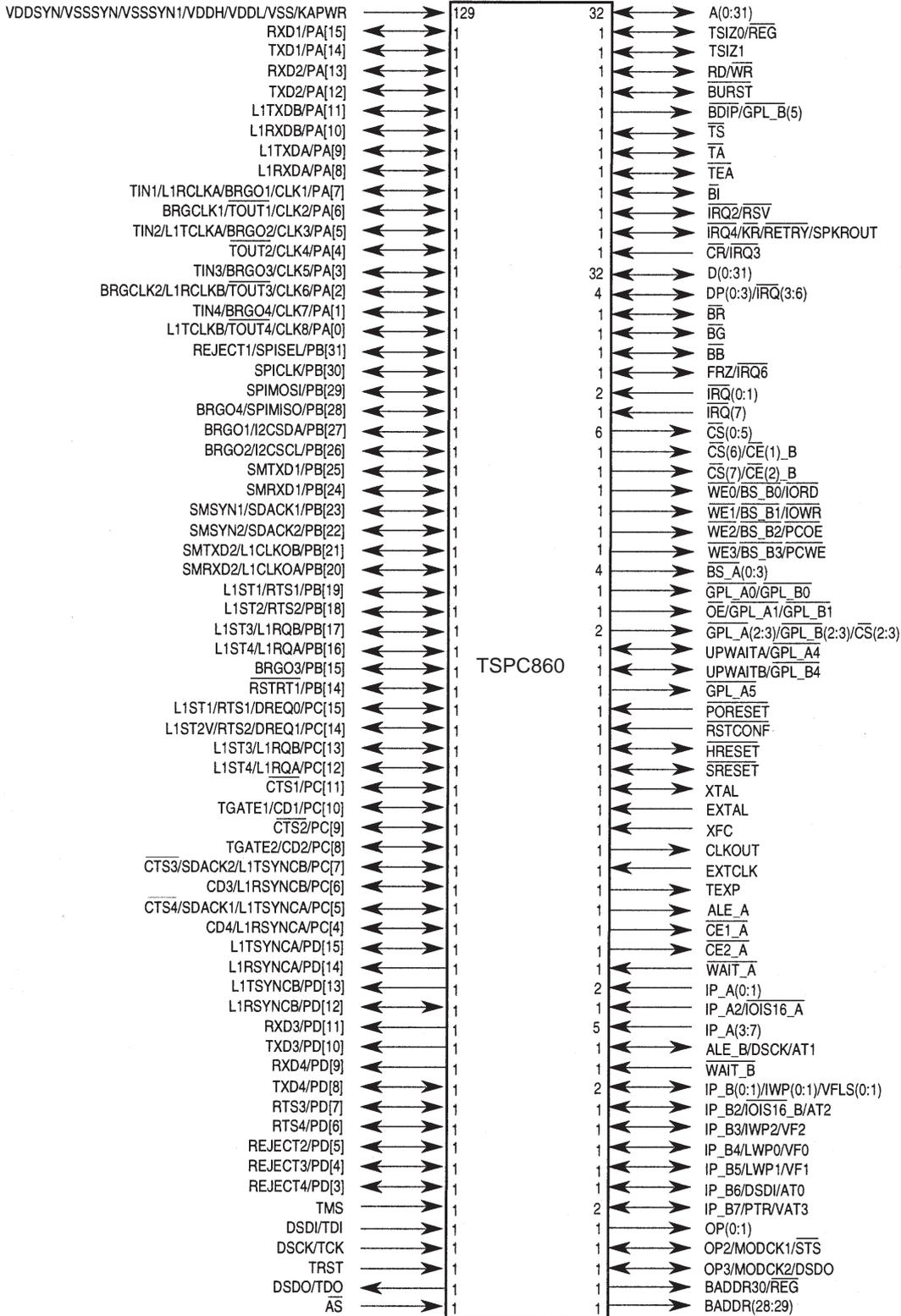


Figure 3 : TSPC860 External Signals

VDDSYN/VSSSYN/VSSSYN1/VDDH/VDDL/VSS/KAPWR	→	129	←	VDDSYN—T1
RXD1/PA[15]	↔	1—C18		VSSSYN—U1
TXD1/PA[14]	↔	1—D17		VSSSYN1—V1
RXD2/PA[13]	↔	1—E17		VDDH—F4
TXD2/PA[12]	↔	1—F17		F16
L1TXDB/PA[11]	↔	1—G16		P4
L1RXDB/PA[10]	↔	1—J17		P16
L1TXDA/PA[9]	↔	1—K18		T14
L1RXDA/PA[8]	↔	1—L17		VDDL—A8
TIN1/L1RCLKA/BRGO1/CLK1/PA[7]	↔	1—M19		H19
BRGCLK1/TOU1/CLK2/PA[6]	↔	1—M17		M1
TIN2/L1TCLKA/BRGO2/CLK3/PA[5]	↔	1—N18		W8
TOU2/CLK4/PA[4]	↔	1—P19		KAPWR—R1
TIN3/BRGO3/CLK5/PA[3]	↔	1—P17		
BRGCLK2/L1RCLKB/TOU3/CLK6/PA[2]	↔	1—R18		
TIN4/BRGO4/CLK7/PA[1]	↔	1—T19		
L1TCLKB/TOU4/CLK8/PA[0]	↔	1—U19		
REJECT1/SPISEL/PB[31]	↔	1—C17		
SPICLK/PB[30]	↔	1—C19		
SPIMOSI/PB[29]	↔	1—E16		
BRGO4/SPIMISO/PB[28]	↔	1—D19		
BRGO1/I2CSDA/PB[27]	↔	1—E19		
BRGO2/I2CSCS/PB[26]	↔	1—F19		
SMTXD1/PB[25]	↔	1—J16		
SMRXD1/PB[24]	↔	1—J18		
SMSYN1/SDACK1/PB[23]	↔	1—K17		
SMSYN2/SDACK2/PB[22]	↔	1—L19		
SMTXD2/L1CLKOB/PB[21]	↔	1—K16		
SMRXD2/L1CLKOA/PB[20]	↔	1—L16		
L1ST1/RTS1/PB[19]	↔	1—N19		
L1ST2V/RTS2/PB[18]	↔	1—N17		
L1ST3/L1RQB/PB[17]	↔	1—P18		
L1ST4/L1RQA/PB[16]	↔	1—N16		
BRGO3/PB[15]	↔	1—R17		
RSTRT1/PB[14]	↔	1—U18		
L1ST1/RTS1/DREQ0/PC[15]	↔	1—D16		
L1ST2/RTS2/DREQ1/PC[14]	↔	1—D18		
L1ST3/L1RQB/PC[13]	↔	1—E18		
L1ST4/L1RQA/PC[12]	↔	1—F18		
CTS1/PC[11]	↔	1—J19		
TGATE1/CD1/PC[10]	↔	1—K19		
CTS2/PC[9]	↔	1—L18		
TGATE2/CD2/PC[8]	↔	1—M18		
CTS3/SDACK2/L1TSYNCB/PC[7]	↔	1—M16		
CD3/L1RSYNCB/PC[6]	↔	1—R19		
CTS4/SDACK1/L1TSYNCA/PC[5]	↔	1—T18		
CD4/L1RSYNCA/PC[4]	↔	1—T17		
L1TSYNCA/PD[15]	↔	1—U17		
L1RSYNCA/PD[14]	↔	1—V19		
L1TSYNCB/PD[13]	↔	1—V18		
L1RSYNCB/PD[12]	↔	1—R16		
RXD3/PD[11]	↔	1—T16		
TXD3/PD[10]	↔	1—W18		
RXD4/PD[9]	↔	1—V17		
TXD4/PD[8]	↔	1—W17		
RTS3/PD[7]	↔	1—T15		
RTS4/PD[6]	↔	1—V16		
REJECT2/PD[5]	↔	1—U15		
REJECT3/PD[4]	↔	1—U16		
REJECT4/PD[3]	↔	1—W16		
TMS	→	1—G18		
DSDI/TDI	→	1—H17		
DSCK/TCK	→	1—H16		
TRST	→	1—G19		
DSDO/TDO	←	1—G17		
AS	→	1—		

TSPC860

Figure 4 : TSPC860 Signals and Pin Numbers (Part 1)

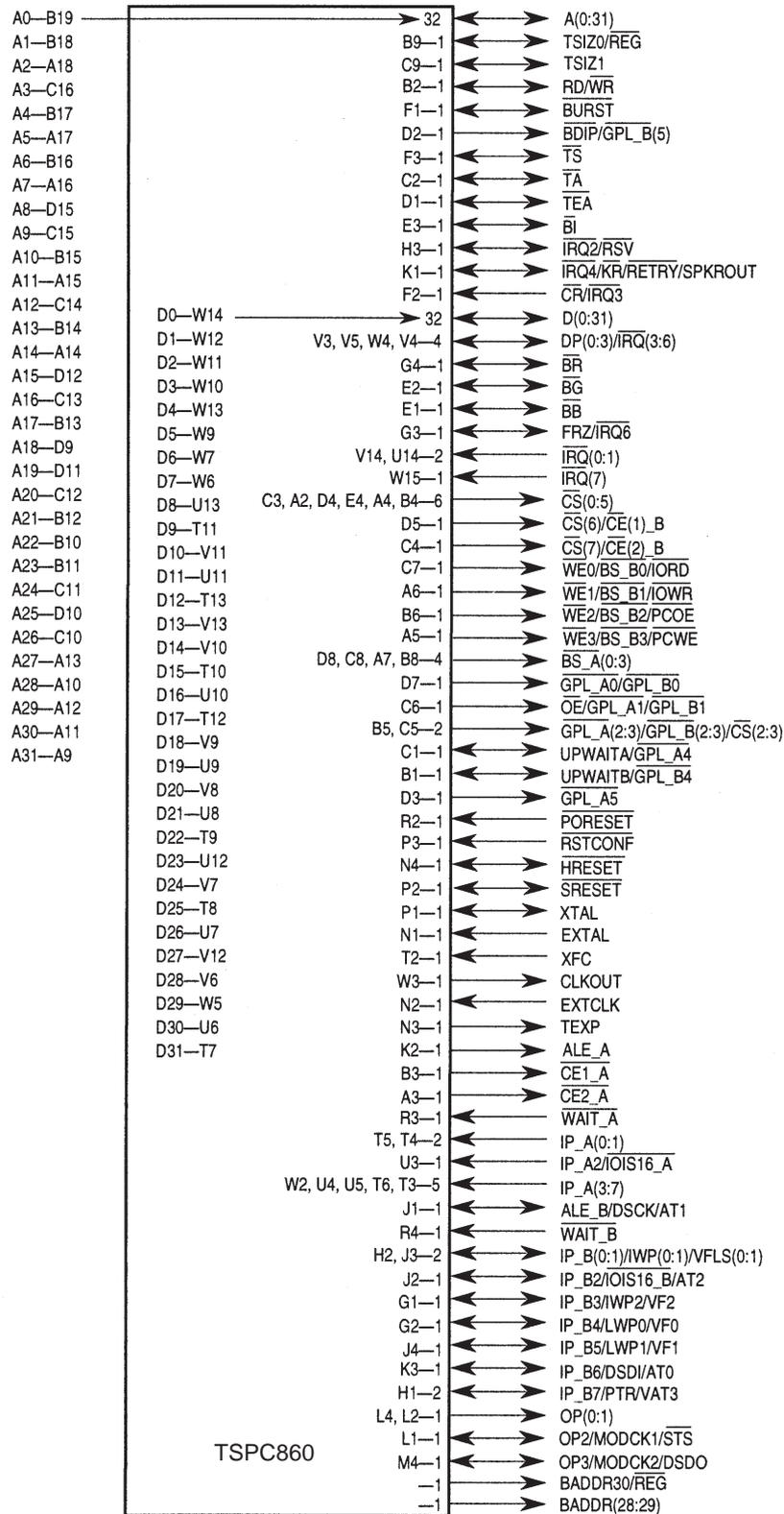


Figure 5 : TSPC860 Signals and Pin Numbers (Part 2)

3.1. System Bus Signals

The TSPC860 system bus consists of all signals that interface with the external bus. Many of these signals perform different functions, depending on how the user assigns them. The following input and output signals are identified by their abbreviation. Each signal's pin number can be found in Figure 4 and Figure 5.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
A(0–31)	Hi-Z	See Figure 5	Bidirectional Three-state	Address Bus—Provides the address for the current bus cycle. A0 is the most-significant signal. The bus is output when an internal master starts a transaction on the external bus. The bus is input when an external master starts a transaction on the bus.
TSIZ0 REG	Hi-Z	B9	Bidirectional Three-state	Transfer Size 0—When accessing a slave in the external bus, used (together with TSIZ1) by the bus master to indicate the number of operand bytes waiting to be transferred in the current bus cycle. TSIZ0 is an input when an external master starts a bus transaction. Register—When an internal master initiates an access to a slave controlled by the PCMCIA interface, REG is output to indicate which space in the PCMCIA card is accessed.
TSIZ1	Hi-Z	C9	Bidirectional Three-state	Transfer Size 1—Used (with TSIZ0) by the bus master to indicate the number of operand bytes waiting to be transferred in the current bus cycle. The TSPC860 drives TSIZ1 when it is bus master. TSIZ1 is input when an external master starts a bus transaction.
RD/WR	Hi-Z	B2	Bidirectional Three-state	Read/Write—Driven by the bus master to indicate the direction of the bus's data transfer. A logic one indicates a read from a slave device and a logic zero indicates a write to a slave device. The TSPC860 drives this signal when it is bus master. Input when an external master initiates a transaction on the bus.
BURST	Hi-Z	F1	Bidirectional Three-state	Burst Transaction—Driven by the bus master to indicate that the current initiated transfer is a burst. The TSPC860 drives this signal when it is bus master. This signal is input when an external master initiates a transaction on the bus.
BDIP GPL_B5	See Section 1.5	D2	Bidirectional Three-state	Burst Data in Progress—When accessing a slave device in the external bus, the master on the bus asserts this signal to indicate that the data beat in front of the current one is the one requested by the master. BDIP is negated before the expected last data beat of the burst transfer. General-Purpose Line B5—Used by the memory controller when UPMB takes control of the slave access.
TS	Hi-Z	F3	Bidirectional Active Pull-up	Transfer Start—Asserted by the bus master to indicate the start of a bus cycle that transfers data to or from a slave device. Driven by the master only when it has gained the ownership of the bus. Every master should negate this signal before the bus relinquish. TS requires the use of an external pull-up resistor. The TSPC860 samples TS when it is not the external bus master to allow the memory controller/PCMCIA interface to control the accessed slave device. It indicates that an external synchronous master initiated a transaction.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
$\overline{\text{TA}}$	Hi-Z	C2	Bidirectional Active Pull-up	Transfer Acknowledge—Indicates that the slave device addressed in the current transaction accepted data sent by the master (write) or has driven the data bus with valid data (read). This is an output when the PCMCIA interface or memory controller controls the transaction. The only exception occurs when the memory controller controls the slave access by means of the GPCM and the corresponding option register is instructed to wait for an external assertion of $\overline{\text{TA}}$. Every slave device should negate $\overline{\text{TA}}$ after a transaction ends and immediately three-state it to avoid bus contention if a new transfer is initiated addressing other slave devices. $\overline{\text{TA}}$ requires the use of an external pull-up resistor.
$\overline{\text{TEA}}$	Hi-Z	D1	Open-drain	Transfer Error Acknowledge—Indicates that a bus error occurred in the current transaction. The TSPC860 asserts $\overline{\text{TEA}}$ when the bus monitor does not detect a bus cycle termination within a reasonable amount of time. Asserting $\overline{\text{TEA}}$ terminates the bus cycle, thus ignoring the state of $\overline{\text{TA}}$. $\overline{\text{TEA}}$ requires the use of an external pull-up resistor.
$\overline{\text{BI}}$	Hi-Z	E3	Bidirectional Active Pull-up	Burst Inhibit—Indicates that the slave device addressed in the current burst transaction cannot support burst transfers. It acts as an output when the PCMCIA interface or the memory controller takes control of the transaction. $\overline{\text{BI}}$ requires the use of an external pull-up resistor.
$\overline{\text{RSV}}$ $\overline{\text{IRQ2}}$	See Section 1.5	H3	Bidirectional Three-state	Reservation—The TSPC860 outputs this three-state signal in conjunction with the address bus to indicate that the core initiated a transfer as a result of a stwcx. or lwarx. Interrupt Request 2—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{\text{KR/RETRY}}$ $\overline{\text{IRQ4}}$ SPKROUT	See Section 1.5	K1	Bidirectional Three-state	Kill Reservation—This input is used as a part of the memory reservation protocol, when the TSPC860 initiated a transaction as the result of a stwcx. instruction. Retry—This input is used by a slave device to indicate it cannot accept the transaction. The TSPC860 must relinquish mastership and reinitiate the transaction after winning in the bus arbitration. Interrupt Request 4. One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal that is sent to the interrupt controller is the logical AND of this line (if defined as $\overline{\text{IRQ4}}$) and DP1/ $\overline{\text{IRQ4}}$ (if defined as $\overline{\text{IRQ4}}$). SPKROUT—Digital audio wave form output to be driven to the system speaker.
$\overline{\text{CR}}$ $\overline{\text{IRQ3}}$	Hi-Z	F2	Input	Cancel Reservation—This input is used as a part of the storage reservation protocol. Interrupt Request 3—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal sent to the interrupt controller is the logical AND of $\overline{\text{CR/IRQ3}}$ (if defined as $\overline{\text{IRQ3}}$) and DP0/ $\overline{\text{IRQ3}}$ if defined as $\overline{\text{IRQ3}}$.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
D(0–31)	Hi-Z(Pulled Low if RSTCONF pulled down)	See Figure 5	Bidirectional Three-state	Data Bus—This bidirectional three-state bus provides the general-purpose data path between the TSPC860 and all other devices. The 32-bit data path can be dynamically sized to support 8-, 16-, or 32-bit transfers. D0 is the MSB of the data bus.
DP0 $\overline{\text{IRQ3}}$	Hi-Z	V3	Bidirectional Three-state	Data Parity 0—Provides parity generation and checking for D(0–7) for transfers to a slave device initiated by the TSPC860. The parity function can be defined independently for each one of the addressed memory banks (if controlled by the memory controller) and for the rest of the slaves sitting on the external bus. Parity generation and checking is not supported for external masters. Interrupt Request 3—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal sent to the interrupt controller is the logical AND of DP0/ $\overline{\text{IRQ3}}$ (if defined as $\overline{\text{IRQ3}}$) and $\overline{\text{CR}}/\overline{\text{IRQ3}}$ (if defined as $\overline{\text{IRQ3}}$).
DP1 $\overline{\text{IRQ4}}$	Hi-Z	V5	Bidirectional Three-state	Data Parity 1—Provides parity generation and checking for D(8–15) for transfers to a slave device initiated by the TSPC860. The parity function can be defined independently for each one of the addressed memory banks (if controlled by the memory controller) and for the rest of the slaves on the external bus. Parity generation and checking is not supported for external masters. Interrupt Request 4—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal sent to the interrupt controller is the logical AND of this line (if defined as $\overline{\text{IRQ4}}$) and $\overline{\text{KR}}/\overline{\text{IRQ4}}/\text{SPKROUT}$ (if defined as $\overline{\text{IRQ4}}$).
DP2 $\overline{\text{IRQ5}}$	Hi-Z	W4	Bidirectional Three-state	Data Parity 2—Provides parity generation and checking for D(16–23) for transfers to a slave device initiated by the TSPC860. The parity function can be defined independently for each one of the addressed memory banks (if controlled by the memory controller) and for the rest of the slaves on the external bus. Parity generation and checking is not supported for external masters. Interrupt Request 5—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core.
DP3 $\overline{\text{IRQ6}}$	Hi-Z	V4	Bidirectional Three-state	Data Parity 3—Provides parity generation and checking for D(24–31) for transfers to a slave device initiated by the TSPC860. The parity function can be defined independently for each one of the addressed memory banks (if controlled by the memory controller) and for the rest of the slaves on the external bus. Parity generation and checking is not supported for external masters. Interrupt Request 6—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal sent to the interrupt controller is the logical AND of this line (if defined as $\overline{\text{IRQ6}}$) and the $\text{FRZ}/\overline{\text{IRQ6}}$ (if defined as $\overline{\text{IRQ6}}$).

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
\overline{BR}	Hi-Z	G4	Bidirectional	Bus Request—Asserted low when a possible master is requesting ownership of the bus. When the TSPC860 is configured to work with the internal arbiter, this signal is configured as an input. When the TSPC860 is configured to work with an external arbiter, this signal is configured as an output and asserted every time a new transaction is intended to be initiated (no parking on the bus).
\overline{BG}	Hi-Z	E2	Bidirectional	Bus Grant—Asserted low when the arbiter of the external bus grants the bus to a specific device. When the TSPC860 is configured to work with the internal arbiter, \overline{BG} is configured as an output and asserted every time the external master asserts \overline{BR} and its priority request is higher than any internal sources requiring a bus transfer. However, when the TSPC860 is configured to work with an external arbiter, BG is an input.
\overline{BB}	Hi-Z	E1	Bidirectional Active Pull-up	Bus Busy—Asserted low by a master to show that it owns the bus. The TSPC860 asserts \overline{BB} after the arbiter grants it bus ownership and \overline{BB} is negated.
FRZ $\overline{IRQ6}$	See Section 1.5	G3	Bidirectional	Freeze—Output asserted to indicate that the core is in debug mode. Interrupt Request 6—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal sent to the interrupt controller is the logical AND of FRZ/ $\overline{IRQ6}$ (if defined as $\overline{IRQ6}$) and DP3/ $\overline{IRQ6}$ (if defined as $\overline{IRQ6}$).
$\overline{IRQ0}$	Hi-Z	V14	Input	Interrupt Request 0—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{IRQ1}$	Hi-Z	U14	Input	Interrupt Request 1—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{IRQ7}$	Hi-Z	W15	Input	Interrupt Request 7—One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{CS}(0-5)$	High	C3, A2, D4, E4, A4, B4	Output	Chip Select—These outputs enable peripheral or memory devices at programmed addresses if they are appropriately defined. $\overline{CS0}$ can be configured to be the global chip-select for the boot device.
$\overline{CS6}$ CE1_B	High	D5	Output	Chip Select 6—This output enables a peripheral or memory device at a programmed address if defined appropriately in the BR6 and OR6 in the memory controller. Card Enable 1 Slot B—This output enables even byte transfers when accesses to the PCMCIA Slot B are handled under the control of the PCMCIA interface.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
<u>CS7</u> <u>CE2_B</u>	High	C4	Output	Chip Select 7—This output enables a peripheral or memory device at a programmed address if defined appropriately in the BR7 and OR7 in the memory controller. Card Enable 2 Slot B—This output enables odd byte transfers when accesses to the PCMCIA Slot B are handled under the control of the PCMCIA interface.
<u>WE0</u> <u>BS_B0</u> <u>IORD</u>	High	C7	Output	Write Enable 0—Output asserted when a write access to an external slave controlled by the GPCM is initiated by the TSPC860. <u>WE0</u> is asserted if D(0–7) contains valid data to be stored by the slave device. Byte Select 0 on UPMB—Output asserted under control of the UPMB, as programmed by the user. In a read or write transfer, the line is only asserted if D(0–7) contains valid data. IO Device Read—Output asserted when the TSPC860 starts a read access to a region controlled by the PCMCIA interface. Asserted only for accesses to a PC card I/O space.
<u>WE1</u> <u>BS_B1</u> <u>IOWR</u>	High	A6	Output	Write Enable 1—Output asserted when the TSPC860 initiates a write access to an external slave controlled by the GPCM. <u>WE1</u> is asserted if D(8–15) contains valid data to be stored by the slave device. Byte Select 1 on UPMB—Output asserted under control of the UPMB, as programmed by the user. In a read or write transfer, the line is only asserted if D(8–15) contains valid data. I/O Device Write—This output is asserted when the TSPC860 initiates a write access to a region controlled by the PCMCIA interface. <u>IOWR</u> is asserted only if the access is to a PC card I/O space.
<u>WE2</u> <u>BS_B2</u> <u>PCOE</u>	High	B6	Output	Write Enable 2—Output asserted when the TSPC860 starts a write access to an external slave controlled by the GPCM. <u>WE2</u> is asserted if D(16–23) contains valid data to be stored by the slave device. Byte Select 2 on UPMB—Output asserted under control of the UPMB, as programmed by the user. In a read or write transfer, <u>BS_B2</u> is asserted only if D(16–23) contains valid data. PCMCIA Output Enable—Output asserted when the TSPC860 initiates a read access to a memory region under the control of the PCMCIA interface.
<u>WE3</u> <u>BS_B3</u> <u>PCWE</u>	High	A5	Output	Write Enable 3—Output asserted when the TSPC860 initiates a write access to an external slave controlled by the GPCM. <u>WE3</u> is asserted if D(24–31) contains valid data to be stored by the slave device. Byte Select 3 on UPMB—Output asserted under control of the UPMB, as programmed by the user. In a read or write transfer, <u>BS_B3</u> is asserted only if D(24–31) contains valid data. PCMCIA Write Enable—Output asserted when the TSPC860 initiates a write access to a memory region under control of the PCMCIA interface.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
$\overline{BS_A(0-3)}$	High	D8, C8, A7, B8	Output	Byte Select 0 to 3 on UPMA—Outputs asserted under requirement of the UPMB, as programmed by the user. For read or writes, asserted only if their corresponding data lanes contain valid data: $\overline{BS_A0}$ for D(0–7), $\overline{BS_A1}$ for D(8–15), $\overline{BS_A2}$ for D(16–23), $\overline{BS_A3}$ for D(24–31)
$\overline{GPL_A0}$ $\overline{GPL_B0}$	High	D7	Output	General–Purpose Line 0 on UPMA—This output reflects the value specified in the UPMA when an external transfer to a slave is controlled by the UPMA. General–Purpose Line 0 on UPMB—This output reflects the value specified in the UPMB when an external transfer to a slave is controlled by the UPMB.
\overline{OE} $\overline{GPL_A1}$ $\overline{GPL_B1}$	High	C6	Output	Output Enable—Output asserted when the TSPC860 initiates a read access to an external slave controlled by the GPCM. General–Purpose Line 1 on UPMA—This output reflects the value specified in the UPMA when an external transfer to a slave is controlled by UPMA. General–Purpose Line 1 on UPMB—This output reflects the value specified in the UPMB when an external transfer to a slave is controlled by UPMB.
$\overline{GPL_A(2-3)}$ $\overline{GPL_B(2-3)}$ $\overline{CS(2-3)}$	High	B5, C5	Output	General–Purpose Line 2 and 3 on UPMA—These outputs reflect the value specified in the UPMA when an external transfer to a slave is controlled by UPMA. General–Purpose Line 2 and 3 on UPMB—These outputs reflect the value specified in the UPMB when an external transfer to a slave is controlled by UPMB. Chip Select 2 and 3—These outputs enable peripheral or memory devices at programmed addresses if they are appropriately defined. The double drive capability for $\overline{CS2}$ and $\overline{CS3}$ is independently defined for each signal in the SIUMCR.
$\overline{UPWAITA}$ $\overline{GPL_A4}$	Hi–Z	C1	Bidirectional	User Programmable Machine Wait A—This input is sampled as defined by the user when an access to an external slave is controlled by the UPMA. General–Purpose Line 4 on UPMA—This output reflects the value specified in the UPMA when an external transfer to a slave is controlled by UPMA.
$\overline{UPWAITB}$ $\overline{GPL_B4}$	Hi–Z	B1	Bidirectional	User Programmable Machine Wait B—This input is sampled as defined by the user when an access to an external slave is controlled by the UPMB. General–Purpose Line 4 on UPMB—This output reflects the value specified in the UPMB when an external transfer to a slave is controlled by UPMB.
$\overline{GPL_A5}$	High	D3	Output	General–Purpose Line 5 on UPMA—This output reflects the value specified in the UPMA when an external transfer to a slave is controlled by UPMA. This signal can also be controlled by the UPMB.
$\overline{PORESET}$	Hi–Z	R2	Input	Power on Reset—When asserted, this input causes the TSPC860 to enter the power–on reset state.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
$\overline{\text{RSTCONF}}$	Hi-Z	P3	Input	Reset Configuration—The TSPC860 samples this input while $\overline{\text{HRESET}}$ is asserted. If $\overline{\text{RSTCONF}}$ is asserted, the configuration mode is sampled in the form of the hard reset configuration word driven on the data bus. When $\overline{\text{RSTCONF}}$ is negated, the TSPC860 uses the default configuration mode. Note that the initial base address of internal registers is determined in this sequence.
$\overline{\text{HRESET}}$	Low	N4	Open-drain	Hard Reset—Asserting this open drain signal puts the TSPC860 in hard reset state.
$\overline{\text{SRESET}}$	Low	P2	Open-drain	Soft Reset—Asserting this open drain line puts the TSPC860 in soft reset state.
XTAL	Analog Driving	P1	Analog Output	This output is one of the connections to an external crystal for the internal oscillator circuitry.
EXTAL	Hi-Z	N1	Analog Input (3.3V only)	This line is one of the connections to an external crystal for the internal oscillator circuitry.
XFC	Analog Driving	T2	Analog Input	External Filter Capacitance—This input is the connection pin for an external capacitor filter for the PLL circuitry.
CLKOUT	See note. (High until SPLL locked, then oscillating)	W3	Output	Clock Out—This output is the clock system frequency.
EXTCLK	Hi-Z	N2	Input (3.3V only)	External Clock—This input is the external input clock from an external source.
TEXP	High	N3	Output	Timer Expired—This output reflects the status of $\text{PLPRCR}[\text{TEXPS}]$.
ALE_A	Low	K2	Output	Address Latch Enable A—This output is asserted when TSPC860 initiates an access to a region under the control of the PCMCIA interface to socket A.
$\overline{\text{CE1}}_A$	High	B3	Output	Card Enable 1 Slot A—This output enables even byte transfers when accesses to PCMCIA Slot A are handled under the control of the PCMCIA interface.
$\overline{\text{CE2}}_A$	High	A3	Output	Card Enable 2 Slot A—This output enables odd byte transfers when accesses to PCMCIA Slot A are handled under the control of the PCMCIA interface.
$\overline{\text{WAIT}}_A$	Hi-Z	R3	Input	Wait Slot A—This input, if asserted low, causes a delay in the completion of a transaction on the PCMCIA controlled Slot A.
$\overline{\text{WAIT}}_B$	Hi-Z	R4	Input	Wait Slot B—This input, if asserted low, causes a delay in the completion of a transaction on the PCMCIA controlled Slot B.
IP_A(0-1)	Hi-Z	T5, T4	Input	Input Port A 0-1—The TSPC860 monitors these inputs that are reflected in the PIPR and PSCR of the PCMCIA interface.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
IP_A2 IOIS16_A	Hi-Z	U3	Input	Input Port A 2—The TSPC860 monitors these inputs; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. I/O Device A is 16 Bits Ports Size—The TSPC860 monitors this input when a transaction under the control of the PCMCIA interface is initiated to an I/O region in socket A of the PCMCIA space.
IP_A(3-7)	Hi-Z	W2, U4, U5, T6, T3	Input	Input Port A 3-7—The TSPC860 monitors these inputs; their values and changes are reported in the PIPR and PSCR of the PCMCIA interface.
ALE_B DSCK/AT1	See Section 1.5	J1	Bidirectional Three-state	Address Latch Enable B—This output is asserted when the TSPC860 initiates an access to a region under the control of the PCMCIA socket B interface. Development Serial Clock—This input is the clock for the debug port interface. Address Type 1—The TSPC860 drives this bidirectional three-state line when it initiates a transaction on the external bus. When the transaction is initiated by the core, it indicates if the transfer is for user or supervisor state. This signal is not used for transactions initiated by external masters.
IP_B(0-1) IWP(0-1) VFLS(0-1)	See Section 1.5	H2, J3	Bidirectional	Input Port B 0-1—The TSPC860 senses these inputs; their values and changes are reported in the PIPR and PSCR of the PCMCIA interface. Instruction Watchpoint 0-1—These outputs report the detection of an instruction watchpoint in the program flow executed by the core. Visible History Buffer Flushes Status—The TSPC860 outputs VFLS(0-1) when program instruction flow tracking is required. They report the number of instructions flushed from the history buffer in the core.
IP_B2 IOIS16_B AT2	Hi-Z	J2	Bidirectional Three-state	Input Port B 2—The TSPC860 senses this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. I/O Device B is 16 Bits Port Size—The TSPC860 monitors this input when a PCMCIA interface transaction is initiated to an I/O region in socket B in the PCMCIA space. Address Type 2—The TSPC860 drives this bidirectional three-state signal when it initiates a transaction on the external bus. If the core initiates the transaction, it indicates if the transfer is instruction or data. This signal is not used for transactions initiated by external masters.
IP_B3 IWP2 VF2	See Section 1.5	G1	Bidirectional	Input Port B 3—The TSPC860 monitors this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Instruction Watchpoint 2—This output reports the detection of an instruction watchpoint in the program flow executed by the core. Visible Instruction Queue Flush Status—The TSPC860 outputs VF2 with VF0/VF1 when instruction flow tracking is required. VF _n reports the number of instructions flushed from the instruction queue in the core.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
IP_B4 LWP0 VF0	Hi-Z	G2	Bidirectional	Input Port B 4—The TSPC860 monitors this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Load/Store Watchpoint 0—This output reports the detection of a data watchpoint in the program flow executed by the core. Visible Instruction Queue Flushes Status—The TSPC860 outputs VF0 with VF1/VF2 when instruction flow tracking is required. VF n reports the number of instructions flushed from the instruction queue in the core.
IP_B5 LWP1 VF1	Hi-Z	J4	Bidirectional	Input Port B 5—The TSPC860 monitors this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Load/Store Watchpoint 1—This output reports the detection of a data watchpoint in the program flow executed by the core. Visible Instruction Queue Flushes Status—The TSPC860 outputs VF1 with VF0 and VF2 when instruction flow tracking is required. VF n reports the number of instructions flushed from the instruction queue in the core.
IP_B6 DSDI AT0	Hi-Z	K3	Bidirectional Three-state	Input Port B 6—The TSPC860 senses this input and its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Development Serial Data Input—Data input for the debug port interface. Address Type 0—The TSPC860 drives this bidirectional three-state line when it initiates a transaction on the external bus. If high (1), the transaction is the CPM. If low (0), the transaction initiator is the CPU. This signal is not used for transactions initiated by external masters.
IP_B7 PTR AT3	Hi-Z	H1	Bidirectional Three-state	Input Port B 7—The TSPC860 monitors this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Program Trace—To allow program flow tracking, the TSPC860 asserts this output to indicate an instruction fetch is taking place. Address Type 3—The TSPC860 drives the bidirectional three-state signal when it starts a transaction on the external bus. When the core initiates a transfer, AT3 indicates whether it is a reservation for a data transfer or a program trace indication for an instruction fetch. This signal is not used for transactions initiated by external masters.
OP(0-1)	Low	L4, L2	Output	Output Port 0-1—The TSPC860 generates these outputs as a result of a write to the PGCRA register in the PCMCIA interface.
OP2 MODCK1 STS	Hi-Z	L1	Bidirectional	Output Port 2—This output is generated by the TSPC860 as a result of a write to the PGCRB register in the PCMCIA interface. Mode Clock 1—Input sampled when $\overline{\text{PORESET}}$ is negated to configure PLL/clock mode. Special Transfer Start—The TSPC860 drives this output to indicate the start of an external bus transfer or of an internal transaction in show-cycle mode.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
OP3 MODCK2 DSDO	Hi-Z	M4	Bidirectional	Output Port 3—This output is generated by the TSPC860 as a result of a write to the PGCRB register in the PCMCIA interface. Mode Clock 2—This input is sampled at the $\overline{\text{PORESET}}$ negation to configure the PLL/clock mode of operation. Development Serial Data Output—Output data from the debug port interface.
BADDR30 REG	Hi-Z	K4	Output	Burst Address 30—This output duplicates the value of A30 when the following is true: <ul style="list-style-type: none"> • An internal master in the TSPC860 initiates a transaction on the external bus. • An asynchronous external master initiates a transaction. • A synchronous external master initiates a single beat transaction. The memory controller uses BADDR30 to increment the address lines that connect to memory devices when a synchronous external master or an internal master initiates a burst transfer. Register—When an internal master initiates an access to a slave under control of the PCMCIA interface, this signal duplicates the value of TSIZ0/REG. When an external master initiates an access, REG is output by the PCMCIA interface (if it must handle the transfer) to indicate the space in the PCMCIA card being accessed.
BADDR(28–29)	Hi-Z	M3 M2	Output	Burst Address—Outputs that duplicate A(28–29) values when one of the following occurs: <ul style="list-style-type: none"> • An internal master in the TSPC860 initiates a transaction on the external bus. • An asynchronous external master initiates a transaction. • A synchronous external master initiates a single beat transaction. The memory controller uses these signals to increment the address lines that connect to memory devices when a synchronous external or internal master starts a burst transfer.
$\overline{\text{AS}}$	Hi-Z	L3	Input	Address Strobe—Input driven by an external asynchronous master to indicate a valid address on A(0–31). The TSPC860 memory controller synchronizes $\overline{\text{AS}}$ and controls the memory device addressed under its control.
PA[15] RXD1	Hi-Z	C18	Bidirectional	General-Purpose I/O Port A Bit 15—Bit 15 of the general-purpose I/O port A. RXD1—Receive data input for SCC1.
PA[14] TXD1		D17	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port A Bit 14—Bit 14 of the general-purpose I/O port A. TXD1—Transmit data output for SCC1. TXD1 has an open-drain capability.
PA[13] RXD2		E17	Bidirectional	General-Purpose I/O Port A Bit 13—Bit 13 of the general-purpose I/O port A. RXD2—Receive data input for SCC2.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
PA[12] TXD2		F17	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port A Bit 12–Bit 12 of the general-purpose I/O port A. TXD2–Transmit data output for SCC2. TXD2 has an open-drain capability.
PA[11] L1TXDB		G16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port A Bit 11–Bit 11 of the general-purpose I/O port A. L1TXDB–Transmit data output for the serial interface TDM port B. L1TXDB has an open-drain capability.
PA[10] L1RXDB		J17	Bidirectional	General-Purpose I/O Port A Bit 10–Bit 10 of the general-purpose I/O port A. L1RXDB–Receive data input for the serial interface TDM port B.
PA[9] L1TXDA		K18	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port A Bit 11–Bit 9 of the general-purpose I/O port A. L1TXDA–Transmit data output for the serial interface TDM port A. L1TXDA has an open-drain capability.
PA[8] L1RXDA		L17	Bidirectional	General-Purpose I/O Port A Bit 8–Bit 8 of the general-purpose I/O port A. L1RXDA–Receive data input for the serial interface TDM port A.
PA[7] CLK1 TIN1 L1RCLKA BRGO1		M19	Bidirectional	General-Purpose I/O Port A Bit 7–Bit 7 of the general-purpose I/O port A. CLK1–One of eight clock inputs that can be used to clock SCCs and SMCs. TIN1–Timer 1 external clock. L1RCLKA–Receive clock for the serial interface TDM port A. BRGO1–Output clock of BRG1.
PA[6] CLK2 <u>TOUT1</u> BRGCLK1		M17	Bidirectional	General-Purpose I/O Port A Bit 6–Bit 6 of the general-purpose I/O port A. CLK2–One of eight clock inputs that can be used to clock SCCs and SMCs. <u>TOUT1</u> –Timer 1 output. BRGCLK1–One of two external clock inputs of the BRGs.
PA[5] CLK3 TIN2 L1TCLKA BRGO2		N18	Bidirectional	General-Purpose I/O Port A Bit 5–Bit 5 of the general-purpose I/O port A. CLK3–One of eight clock inputs that can be used to clock SCCs and SMCs. TIN2–Timer 2 external clock input. L1TCLKA–Transmit clock for the serial interface TDM port A. BRGO2–Output clock of BRG2.
PA[4] CLK4 <u>TOUT2</u>	Hi-Z	P19	Bidirectional	General-Purpose I/O Port A Bit 4–Bit 4 of the general-purpose I/O port A. CLK4–One of eight clock inputs that can be used to clock SCCs and SMCs. <u>TOUT2</u> –Timer 2 output.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
PA[3] CLK5 TIN3 BRGO3		P17	Bidirectional	General-Purpose I/O Port A Bit 3–Bit 3 of the general-purpose I/O port A. CLK5—One of eight clock inputs that can be used to clock SCCs and SMCs. TIN3—Timer 3 external clock input. BRGO3—Output clock of BRG3.
PA[2] CLK6 TOUT3 L1RCLKB BRGCLK2		R18	Bidirectional	General-Purpose I/O Port A Bit 2–Bit 2 of the general-purpose I/O port A. CLK6—One of eight clock inputs that can be used to clock the SCCs and SMCs. TOUT3—Timer 3 output. L1RCLKB—Receive clock for the serial interface TDM port B. BRGCLK2—One of the two external clock inputs of the BRGs.
PA[1] CLK7 TIN4 BRGO4		T19	Bidirectional	General-Purpose I/O Port A Bit 1–Bit 1 of the general-purpose I/O port A. CLK7—One of eight clock inputs that can be used to clock SCCs and SMCs. TIN4—Timer 4 external clock input. BRGO4—BRG4 output clock.
PA[0] CLK8 TOUT4 L1TCLKB		U19	Bidirectional	General-Purpose I/O Port A Bit 0–Bit 0 of the general-purpose I/O port A. CLK8—One of eight clock inputs that can be used to clock SCCs and SMCs. TOUT4—Timer 4 output. L1TCLKB—Transmit clock for the serial interface TDM port B.
PB[31] SPISEL REJECT1		C17	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 31—Bit 31 of the general-purpose I/O port B. SPISEL—SPI slave select input. REJECT1—SCC1 CAM interface reject pin.
PB[30] SPICLK RSTRT2		C19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 30—Bit 30 of the general-purpose I/O port B. SPICLK—SPI output clock when it is configured as a master or SPI input clock when it is configured as a slave. RSTRT2—SCC2 serial CAM interface output signal that marks the start of a frame.
PB[29] SPIMOSI		E16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 29—Bit 29 of the general-purpose I/O port B. SPIMOSI—SPI output data when it is configured as a master or SPI input data when it is configured as a slave.
PB[28] SPIMISO BRGO4		D19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 28–Bit 29 of the general-purpose I/O port B. SPIMISO—SPI input data when the TSPC860 is a master; SPI output data when it is a slave. BRGO4—BRG4 output clock.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
PB[27] I2CSDA BRGO1	Hi-Z	E19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 27–Bit 27 of the general-purpose I/O port B. I2CSDA–I ² C serial data pin. Bidirectional; should be configured as an open-drain output. BRGO1–BRG1 output clock.
PB[26] I2CSCL BRGO2		F19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 26–Bit 26 of the general-purpose I/O port B. I2CSCL–I ² C serial clock pin. Bidirectional; should be configured as an open-drain output. BRGO2–BRG2 output clock.
PB[25] SMTXD1		J16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 25–Bit 25 of the general-purpose I/O port B. SMTXD1–SMC1 transmit data output.
PB[24] SMRXD1		J18	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 24–Bit 24 of the general-purpose I/O port B. SMRXD1–SMC1 receive data input.
PB[23] SMSYN1 SDACK1		K17	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 23–Bit 23 of the general-purpose I/O port B. SMSYN1–SMC1 external sync input. SDACK1–SDMA acknowledge 1 output that is used as a peripheral interface signal for IDMA emulation, or as a CAM interface signal for Ethernet.
PB[22] SMSYN2 SDACK2		L19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 22–Bit 22 of the general-purpose I/O port B. SMSYN2–SMC2 external sync input. SDACK2–SDMA acknowledge 2 output that is used as a peripheral interface signal for IDMA emulation, or as a CAM interface signal for Ethernet.
PB[21] SMTXD2 L1CLKOB		K16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 21–Bit 21 of the general-purpose I/O port B. SMTXD2–SMC2 transmit data output. L1CLKOB–Clock output from the serial interface TDM port B.
PB[20] SMRXD2 L1CLKOA		L16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 20–Bit 20 of the general-purpose I/O port B. SMRXD2–SMC2 receive data input. L1CLKOA–Clock output from the serial interface TDM port A.
PB[19] RTS1 L1ST1		N19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 19–Bit 19 of the general-purpose I/O port B. RTS1–Request to send modem line for SCC1. L1ST1–One of four output strobes that can be generated by the serial interface.
PB[18] RTS2 L1ST2		N17	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 18–Bit 18 of the general-purpose I/O port B. RTS2–Request to send modem line for SCC2. L1ST2–One of four output strobes that can be generated by the serial interface.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
PB[17] <u>L1RQB</u> L1ST3	Hi-Z	P18	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 17–Bit 17 of the general-purpose I/O port B. <u>L1RQB</u> –D-channel request signal for the serial interface TDM port B. L1ST3–One of four output strobes that can be generated by the serial interface.
PB[16] <u>L1RQA</u> L1ST4		N16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 16–Bit 16 of the general-purpose I/O port B. <u>L1RQA</u> –D-channel request signal for the serial interface TDM port A. L1ST4–One of four output strobes that can be generated by the serial interface.
PB[15] BRGO3		R17	Bidirectional	General-Purpose I/O Port B Bit 15–Bit 15 of the general-purpose I/O port B. BRGO3–BRG3 output clock.
PB[14] <u>RSTRT1</u>		U18	Bidirectional	General-Purpose I/O Port B Bit 14–Bit 14 of the general-purpose I/O port B. <u>RSTRT1</u> –SCC1 serial CAM interface outputs that marks the start of a frame.
PC[15] <u>DREQ0</u> <u>RTS1</u> L1ST1		D16	Bidirectional	General-Purpose I/O Port C Bit 15–Bit 15 of the general-purpose I/O port C. <u>DREQ0</u> –IDMA channel 0 request input. <u>RTS1</u> –Request to send modem line for SCC1. L1ST1–One of four output strobes that can be generated by the serial interface.
PC[14] <u>DREQ1</u> <u>RTS2</u> L1ST2		D18	Bidirectional	General-Purpose I/O Port C Bit 14–Bit 14 of the general-purpose I/O port C. <u>DREQ1</u> –IDMA channel 1 request input. <u>RTS2</u> –Request to send modem line for SCC2. L1ST2–One of four output strobes that can be generated by the serial interface.
PC[13] <u>L1RQB</u> L1ST3		E18	Bidirectional	General-Purpose I/O Port C Bit 13–Bit 13 of the general-purpose I/O port C. <u>L1RQB</u> –D-channel request signal for the serial interface TDM port B. L1ST3–One of four output strobes that can be generated by the serial interface.
PC[12] <u>L1RQA</u> L1ST4		F18	Bidirectional	General-Purpose I/O Port C Bit 12–Bit 12 of the general-purpose I/O port C. <u>L1RQA</u> –D-channel request signal for the serial interface TDM port A. L1ST4–One of four output strobes that can be generated by the serial interface.
PC[11] CTS1		J19	Bidirectional	General-Purpose I/O Port C Bit 11–Bit 11 of the general-purpose I/O port C. CTS1–Clear to send modem line for SCC1.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
PC[10] CD1 TGATE1	Hi-Z	K19	Bidirectional	General-Purpose I/O Port C Bit 10–Bit 10 of the general-purpose I/O port C. CD1–Carrier detect modem line for SCC1. TGATE1–Timer 1/timer 2 gate signal.
PC[9] CTS2		L18	Bidirectional	General-Purpose I/O Port C Bit 9–Bit 9 of the general-purpose I/O port C. CTS2–Clear to send modem line for SCC2.
PC[8] CD2 TGATE2		M18	Bidirectional	General-Purpose I/O Port C Bit 8–Bit 8 of the general-purpose I/O port C. CD2–Carrier detect modem line for SCC2. TGATE2–Timer 3/timer 4 gate signal.
PC[7] CTS3 L1TSYNCB SDACK2		M16	Bidirectional	General-Purpose I/O Port C Bit 7–Bit 7 of the general-purpose I/O port C. CTS3–Clear to send modem line for SCC3. L1TSYNCB–Transmit sync input for the serial interface TDM port B. SDACK2–SDMA acknowledge 2 output that is used as a peripheral interface signal for IDMA emulation or as a CAM interface signal for Ethernet.
PC[6] CD3 L1RSYNCB		R19	Bidirectional	General-Purpose I/O Port C Bit 6–Bit 6 of the general-purpose I/O port C. CD3–Carrier detect modem line for SCC3. L1RSYNCB–Receive sync input for the serial interface TDM port B.
PC[5] CTS4 L1TSYNCA SDACK1		T18	Bidirectional	General-Purpose I/O Port C Bit 5–Bit 5 of the general-purpose I/O port C. CTS4–Clear to send modem line for SCC4. L1TSYNCA–Transmit sync input for the serial interface TDM port A. SDACK1–SDMA acknowledge 1 output that is used as a peripheral interface signal for IDMA emulation or as a CAM interface signal for Ethernet.
PC[4] CD4 L1RSYNCA		T17	Bidirectional	General-Purpose I/O Port C Bit 4–Bit 4 of the general-purpose I/O port C. CD4–Carrier detect modem line for SCC4. L1RSYNCA–Receive sync input for the serial interface TDM port A.
PD[15] L1TSYNCA		U17	Bidirectional	General-Purpose I/O Port D Bit 15–Bit 15 of the general-purpose I/O port D. L1TSYNCA–Input transmit data sync signal to the TDM channel A.
PD[14] L1RSYNCA		V19	Bidirectional	General-Purpose I/O Port D Bit 14–Bit 14 of the general-purpose I/O port D. L1RSYNCA–Input receive data sync signal to the TDM channel A.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
PD[13] L1TSYNCB		V18	Bidirectional	General-Purpose I/O Port D Bit 13–Bit 13 of the general-purpose I/O port D. L1TSYNCB–Input transmit data sync signal to the TDM channel B.
PD[12] L1RSYNCB	Hi-Z	R16	Bidirectional	General-Purpose I/O Port D Bit 12–Bit 12 of the general-purpose I/O port D. L1RSYNCB–Input receive data sync signal to the TDM channel B.
PD[11] RXD3		T16	Bidirectional	General-Purpose I/O Port D Bit 11–Bit 11 of the general-purpose I/O port D. RXD3–Receive data for serial channel 3.
PD[10] TXD3		W18	Bidirectional	General-Purpose I/O Port D Bit 10–Bit 10 of the general-purpose I/O port D. TXD3–Transmit data for serial channel 3.
PD[9] RXD4		V17	Bidirectional	General-Purpose I/O Port D Bit 9–Bit 9 of the general-purpose I/O port D. RXD4–Receive data for serial channel 4.
PD[8] TXD4		W17	Bidirectional	General-Purpose I/O Port D Bit 8–Bit 8 of the general-purpose I/O port D. TXD4–Transmit data for serial channel 4.
PD[7] <u>RTS3</u>		T15	Bidirectional	General-Purpose I/O Port D Bit 7–Bit 7 of the general-purpose I/O port D. <u>RTS3</u> –Active low request to send output indicates that SCC3 is ready to transmit data.
PD[6] <u>RTS4</u>		V16	Bidirectional	General-Purpose I/O Port D Bit 6–Bit 6 of the general-purpose I/O port D. <u>RTS4</u> –Active low request to send output indicates that SCC4 is ready to transmit data.
PD[5] <u>REJECT2</u>		U15	Bidirectional	General-Purpose I/O Port D Bit 5–Bit 5 of the general-purpose I/O port D. <u>REJECT2</u> –This input to SCC2 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match.
PD[4] <u>REJECT3</u>		U16	Bidirectional	General-Purpose I/O Port D Bit 4–Bit 4 of the general-purpose I/O port D. <u>REJECT3</u> –This input to SCC3 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match.
PD[3] <u>REJECT4</u>		W16	Bidirectional	General-purpose I/O Port D Bit 3–Bit 3 of the general-purpose I/O port D. <u>REJECT4</u> –This input to SCC4 allows a CAM to reject the current Ethernet frame after it determines the frame address did not match.

Table 10. Signal Descriptions

Name	Reset	Number	Type	Description
TCK DSCK	Hi-Z(Pulled up on rev 0 to rev A.3)	H16	Input	Provides clock to scan chain logic or for the development port logic. Should be tied to Vcc if JTAG or development port are not used.
TMS	Pulled up	G18	Input	Controls the scan chain test mode operations. Should be tied to power (1) through a pull-up resistor if unused.
TDI DSDI	Pulled up (Hi-Z on rev 0 to rev A.3)	H17	Input	Input serial data for either the scan chain logic or the development port and determines the operating mode of the development port at reset.
TDO DSDO	Low	G17	Output	Output serial data for either the scan chain logic or for the development port.
$\overline{\text{TRST}}$	Pulled up	G19	Input	Reset for the scan chain logic. If JTAG is not used, connect $\overline{\text{TRST}}$ to ground. If JTAG is used, connect $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$. In case $\overline{\text{PORESET}}$ logic is powered by the keep-alive power supply (KAPWR), connect $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ through a diode (anode connected to $\overline{\text{TRST}}$ and cathode to $\overline{\text{PORESET}}$).
SPARE[1–4]	Hi-Z	B7, H18, V15, H4	No-connect	Spare signals–Not used on current chip revisions. Leave unconnected.
Power Supply		See Figure 4	Power	VDDL–Power supply of the internal logic. VDDH–Power supply of the I/O buffers and certain parts of the clock control. VDDSYN–Power supply of the PLL circuitry. KAPWR–Power supply of the internal OSCM, RTC, PIT, DEC, and TB. VSS–Ground for circuits, except for the PLL circuitry. VSSSYN, VSSSYN1–Ground for the PLL circuitry.

3.2. Active Pull-up Buffers

Active pull-up buffers are a special variety of bidirectional three-state buffer with the following properties:

- When enabled as an output and driving low, they behave as a normal output driver (that is, the pin is constantly driven low).
- When enabled as an output and driving high, drive high until an internal detection circuit determines that the output has reached the logic high threshold and then stop driving (that is, the pin switches to high-impedance).
- When disabled as an output or functioning as an input, it should not be driven.

Due to the behavior of the buffer when being driven high, a pull-up resistor is required externally to function as a ‘bus keep’ for these shared signals in periods when no drivers are active and to keep the buffer from oscillating when the buffer is driving high, because if the voltage ever dips below the logic high threshold while the buffer is enabled as an output, the buffer will reactivate. Further, external logic must not attempt to drive these signals low while active pull-up buffers are enabled as outputs, because the buffers will reactivate and drive high, resulting in a buffer fight and possible damage to the TSPC860, to the system, or to both.

Figure 6 compares three-state buffers and active pull-up buffers graphically in general terms. It makes no implication as to which edges trigger which events for any particular signal.

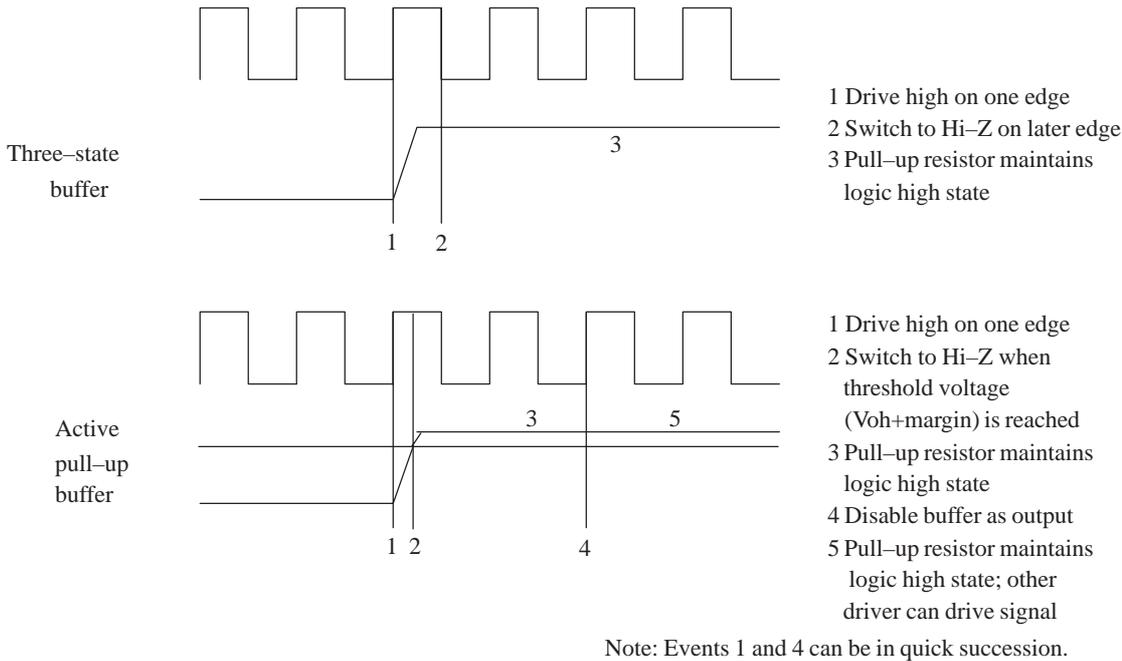


Figure 6 : Three-State Buffers and Active Pull-Up Buffers

Table 11 summarizes when active pull-up drivers are enabled as outputs.

Table 11. Active Pull-Up Resistors Enabled as Outputs	
Signal	Description
\overline{TS} , \overline{BB}	When the TSPC860 is the external bus master throughout the entire bus cycle.
BI	When the TSPC860's memory controller responds to the access on the external bus, throughout the entire bus cycle.
TA	When the TSPC860's memory controller responds to the access on the external bus, then: <ul style="list-style-type: none"> • For chip-selects controlled by the GPCM set for external \overline{TA}, the TSPC860's \overline{TA} buffer is not enabled as an output. • For chip-selects controlled by the GPCM set to terminate in n wait-states, \overline{TA} is enabled as an output on cycle (n-1) and driven high, then is driven low on cycle n, terminating the bus transaction. External logic can drive \overline{TA} at any point before this, thus terminating the cycle early. [For example, assume the GPCM is programmed to drive \overline{TA} after 15 cycles. If external logic drives \overline{TA} before 14 clocks have elapsed then the \overline{TA} will be accepted by the TSPC860 as a cycle termination.] • For chip-selects controlled by the UPM, the \overline{TA} buffer is enabled as an output throughout the entire bus cycle.

The purpose of active pull-up buffers is to allow access to zero wait-state logic that drives a shared signal on the clock cycle immediately following a cycle in which the signal is driven by the TSPC860. In other words, it eliminates the need for a bus turn-around cycle.

3.3. Internal Pull-Up and Pull-Down Resistors

The TMS and \overline{TRST} pins have internal pull-up resistors. TSPC860 devices from Rev 0 to Rev A.3 (masks xE64C and xF84C) have an internal pull-up resistor on TCK/DSCK but no internal pull-up resistor on TDI/DSDI. This was corrected on Rev B and later; on these chips, the internal pull-up resistor was removed from TCK/DSCK and an internal pull-up resistor was added to TDI/DSDI.

If $\overline{RSTCONF}$ is pulled down, during hardware reset (initiated by \overline{HRESET} or $\overline{PORESET}$), the data bus D[0-31] is pulled down with internal pull-down resistors. These internal pull-down resistors are to provide a logic-zero default for these pins when programming the hard reset configuration word. These internal pull-down resistors are disconnected after \overline{HRESET} is negated.

No other pins have internal pull-ups or pull-downs.

Resistance values for internal pull-up and pull-down resistors are not specified because their values may vary due to process variations and shrinks in die size, and they are not tested. Typical values are on the order of 5 kΩ but can vary by approximately a factor of 2.

3.4. Recommended Basic Pin Connections

3.4.1. Reset Configuration

Some external pin configuration is determined at reset by the hard reset configuration word. Thus, some decisions as to system configuration (for example, location of BDM pins) should be made before required application of pull-up and pull-down resistors can be determined.

$\overline{\text{RSTCONF}}$ should be grounded if the hard reset configuration word is used to configure the TSPC860 or should be connected to VCC if the default configuration is used.

Pull-up resistors may not be used on D[0–31] to set the hard reset configuration word, as the values of the internal pull-down resistors are not specified or guaranteed. To change a data bus signal from its default logic low state during reset, actively drive that signal high. MODCK[1–2] must be used to determine the default clocking mode for the TSPC860. After hardware reset, the MODCK[1–2] pins change function and become outputs. Thus, if these alternate functions are also desired, then the MODCK[1–2] configuration should be set with three-state drivers that turn off after $\overline{\text{HRESET}}$ is negated; however, if MODCK[1–2] pins' alternate output functions are not used in the system, they can be configured with pull-up and pull-down resistors.

3.3.1.1. Reset Configuration

Signals with open-drain buffers and active pull-up buffers ($\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{TEA}}$, $\overline{\text{TS}}$, $\overline{\text{TA}}$, $\overline{\text{BI}}$, and $\overline{\text{BB}}$) must have external pull-up resistors. These signals include the following:

Some other input signals do not absolutely require a pull-up resistor, as they may be actively driven by external logic. However, if they are not used externally, or if the external logic connected to them is not always actively driving, they may need external pull-up resistors to hold them negated. These signals include the following:

- $\overline{\text{PORESET}}$
- AS
- CR/ $\overline{\text{IRQ3}}$
- KR/ $\overline{\text{RETRY}}$ / $\overline{\text{IRQ4}}$ /SPKROUT (if configured as $\overline{\text{KR}}$ / $\overline{\text{RETRY}}$ or $\overline{\text{IRQ4}}$)
- Any $\overline{\text{IRQx}}$ (if configured as $\overline{\text{IRQx}}$)
- BR (if the TSPC860's internal bus arbiter is used)
- BG (if an external bus arbiter is used)

3.4.2. JTAG and Debug Ports

TCK/DSCK or ALE_B/DSCK/AT1 (depending on the configuration of the DSCK function) should be connected to ground through a pull-down resistor to disable Debug Mode as a default. When required, a debug mode controller tool externally drives this signal high actively to put the TSPC860 into debug mode.

Two pins need special attention, depending on the version of TSPC860 used.

- For TSPC860 rev B and later, TDI/DSDI should be pulled up to VCC to keep it from oscillating when unused.
- For TSPC860 rev A.3 and earlier, TCK/DSCK should be connected to ground if it is configured for its DSCK function, as stated above. However, for these versions of the TSPC860, the pull-down resistor must be strong (for example, 1 kΩ to overcome the internal pull-up resistor).

To allow application of any version of processor, perform both of the above actions.

3.4.3. Unused Inputs

In general, pull-up resistors should be used on any unused inputs to keep them from oscillating. For example, if PCMCIA is not used, the PCMCIA input pins (WAIT_A, WAIT_B, IP_A[0–8], IP_B[0–8]) should have external pull-up resistors. However, unused pins of port A, B, C, or D can be configured as outputs, and, if they are configured as outputs they do not require external terminations.

3.4.4. Unused Outputs

Unused outputs can be left unterminated.

3.5. Signal States during Hardware Reset

During hardware reset ($\overline{\text{HRESET}}$ or $\overline{\text{PORESET}}$), the signals of the TSPC860 behave as follows:

- The bus signals are high-impedance.
- The port I/O signals are configured as inputs, and are therefore high-impedance.
- The memory controller signals are driven to their inactive state.

However, some signal functions are determined by the reset configuration. When $\overline{\text{HRESET}}$ is asserted, these signals immediately begin functioning as determined by the reset configuration and are either high-impedance or are driven to their inactive state accordingly. The behavior of these signals is shown in Table 12.

Table 12. Signal States during Hardware Reset

Signal	Behavior
$\overline{\text{BDIP}}/\text{GPL_B5}$	$\overline{\text{BDIP}}$: high impedance GPL_B5: high
RSV/ $\overline{\text{IRQ2}}$	RSV: high $\overline{\text{IRQ2}}$: high impedance
$\overline{\text{KR}}/\text{RETRY}/\overline{\text{IRQ4}}/\text{SPKROUT}$	$\overline{\text{KR}}/\text{RETRY}/\overline{\text{IRQ4}}$: high impedance SPKROUT: low
FRZ/ $\overline{\text{IRQ6}}$	FRZ: low $\overline{\text{IRQ6}}$: high impedance
ALE_B/DSCK/AT1	ALE_B: low DSCK/AT1: high impedance
IP_B[0–1]/IWP[0–1]/VFLS[0–1]	IP_B[0–1]: high impedance. IWP[0–1]: high VFLS[0–1]: low
IP_B3/IWP2/VF2	IP_B3: high impedance IWP2: high VF2: low
IP_B4/LWP0/VF0	IP_B4: high impedance LWP0: high VF0: low
IP_B5/LWP1/VF1	IP_B5: high impedance LWP1: high; VF1: low

B. DETAILED SPECIFICATIONS

1. SCOPE

This drawing describes the specific requirements for the microcontroller TSPC860, in compliance ATMEL-Grenoble standard screening.

2. APPLICABLE DOCUMENTS

Quality levels for supplied components SQ32S0100.0.

3. REQUIREMENTS

3.1. General

The microcircuits are in accordance with the applicable documents and as specified herein.

3.2. Design and construction

3.2.1. Terminal connections

The terminal connections shall be as shown in chap A. GENERAL DESCRIPTION.

3.2.2. Lead material and finish

Lead material and finish shall be as specified at § 11.

3.2.3. Package

The macrocircuits are packaged in 357 ceramic ball grid array packages.

The precise case outlines are described at the end of the specification (§ 11.1).

3.3. Absolute maximum ratings

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

Table 1 : Absolute maximum rating for the TSPC860

Parameter	Symbol	Min	Max	Unit
I/O Supply voltage	V_{DDH}	-0.3	4.0	V
Internal Supply voltage	V_{DDL}	-0.3	4.0	V
Backup Supply voltage	KAPWR	-0.3	4.0	V
PLL Supply voltage	V_{DDSYN}	-0.3	4.0	V
Input voltage	V_{IN}	-0.3	5.8	V
Storage temperature range	T_{STG}	-55	+150	°C

3.4. Thermal Characteristics

Table 2 : *Thermal Characteristics*

Characteristic	Symbol	Value	Unit
Thermal resistance for BGA ⁽¹⁾ (junction-to-ambient)	θ_{JA}	47 ⁽²⁾	°C/W
	θ_{JA}	30 ⁽³⁾	°C/W
	θ_{JA}	15 ⁽⁴⁾	°C/W
Thermal Resistance for BGA (junction-to-case) (Top)	θ_{JC}	4.9	°C/W

Note : (1) For more information on the design of thermal vias on multilayer boards and BGA layout considerations in general, refer to Motorola's documentation AN-1231/D, Plastic Ball Grid Array Application Note.

(2) Assumes natural convection and a single layer board (no thermal vias).

(3) Assumes natural convection, a multilayer board with thermal vias, 1W PC860 dissipation, and a board temperature rise of 20°C above ambient.

(4) Assumes natural convection, a multilayer board with thermal vias, 1W PC860 dissipation, and a board temperature rise of 10°C above ambient.

Table 3 : *Power Dissipation (P_D)*

Die Revision	Frequency	Typical ¹	Maximum ²	Unit
B and later	33 MHz	375	460	mW
	50 MHz	575	700	mW
	66 MHz	750	900	mW

Note : 1 Typical power dissipation is measured at 3.3 V.

2 Maximum power dissipation is measured at 3.65 V.

3.5. Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo,
- Manufacturer's part number,
- Date-code of inspection lot,
- ESD identifier if available,
- Country of manufacturing.

4. ELECTRICAL CHARACTERISTICS

4.1. General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below.

4.2. DC Electrical Specifications

Table 4 : DC Electrical Specification

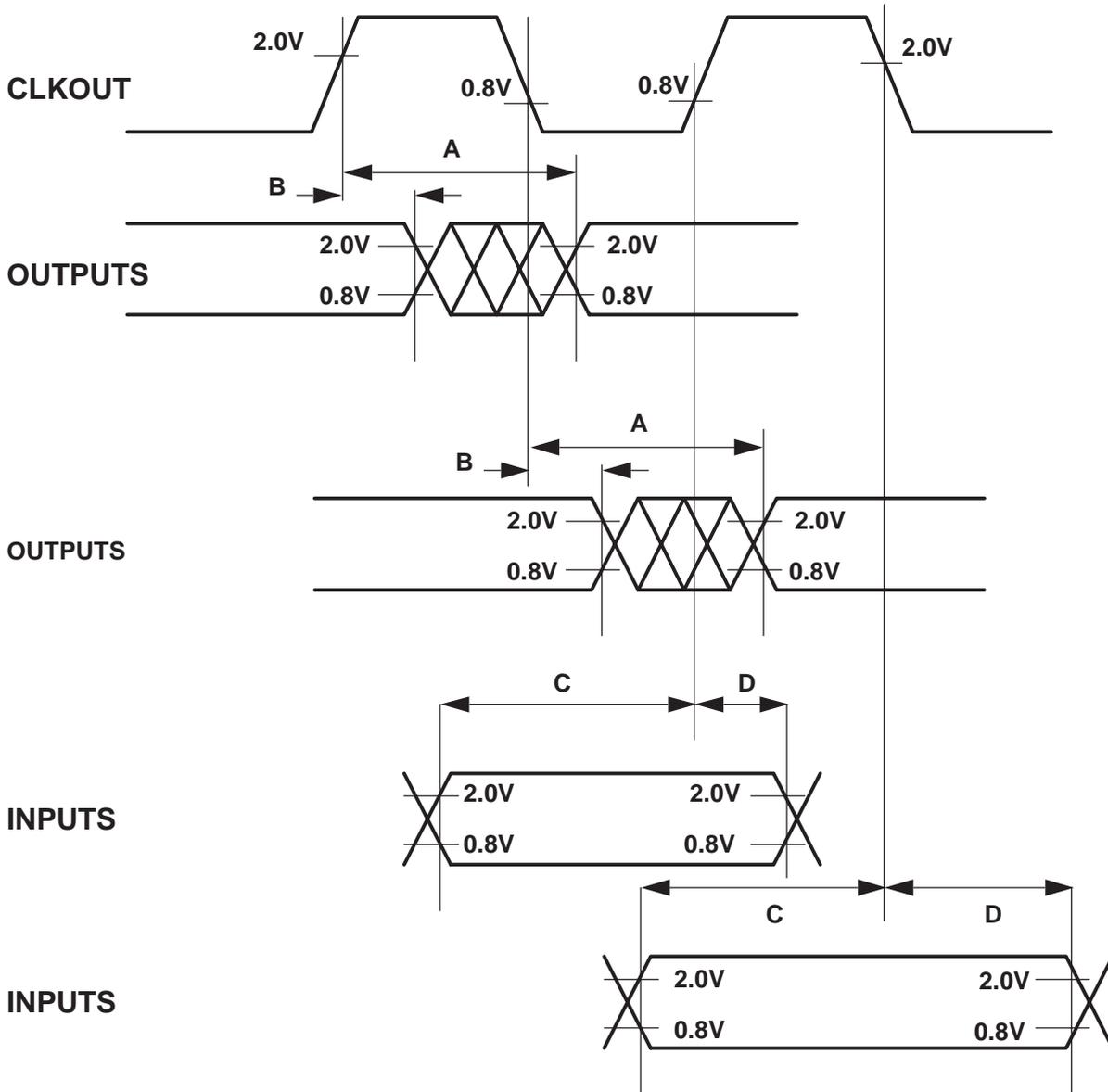
V_{CC} = 3.3 ± 5 % V dc, GND = 0 V dc, -55°C ≤ T_c ≤ 125°C

Characteristic	Symbol	Min	Max	Unit
Operating voltage	VDDH, VDDL, KAPWR, VDDSYN	3.135	3.465	V
	KAPWR (power-down mode)	2.0	3.6	V
	KAPWR (all other operating modes)	VDDH - 0.4	VDDH	V
Input High Voltage (all inputs except EXTAL and EXTCLK)	VIH	2.0	5.5	V
Input Low Voltage	VIL	GND	0.8	V
EXTAL, EXTCLK Input High Voltage	VIHC	0.7*(VCC)	VCC+0.3	V
Input Leakage Current, Vin = 5.5V (Except TMS, TRST, DSCK and DSDI pins)	I _{in}	-	100	μA
Input Leakage Current, Vin = 3.6V (Except TMS, TRST, DSCK and DSDI pins)	I _{in}	-	10	μA
Input Leakage Current, Vin = 0V (Except TMS, TRST, DSCK and DSDI pins)	I _{in}	-	10	μA
Output High Voltage, IOH = -2.0 mA, VDDH = 3.0V Except XTAL, XFC, and Open drain pins	VOH	2.4	-	V

<p>Output Low Voltage</p> <p>IOL = 2.0 mA CLKOUT</p> <p>IOL = 3.2 mA A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, RRJCT1/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/sdack1/PB23, SMSYN2/sdack2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, CTS3/SDACK2/L1TSYNCB/PC7, CD3/L1RSYNCB/PC6, CTS4/SDACK1/L1TSYNCA/PC5, CD4/L1RSYNCA/PC4, PD15/L1TSYNCA, PD14/L1RSYNCA, PD13/L1TSYNCB, PD12/L1RSYNCB, PD11/RXD3, PD10/TXD3, PD9/RXD4, PD8/TXD4, PD5/RRJCT2, PD6/RTS4, PD7/RTS3, PD4/RRJCT3, PD3</p> <p>IOL = 5.3 mA \overline{BDIP}/GPL_B(5), \overline{BR}, \overline{BG}, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30)</p> <p>IOL = 7.0 mA TXD1/PA14, TXD2/PA12</p> <p>IOL = 8.9 mA \overline{TS}, \overline{TA}, \overline{TEA}, \overline{BI}, \overline{BB}, HRESET, SRESET</p>	VOL	-	0.5	V
Input Capacitance	Cin	-	20	pF

4.3. AC Electrical Specifications Control Timing

Figure 7 : AC Electrical Specifications Control Timing Diagram



- A. Maximum Output Delay Specification**
- B. Minimum Output Hold Time**
- C. Minimum input Setup Time Specification**
- D. Minimum input Hold Time Specification**

The timing for the TSPC860 bus shown assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. For loads other than 50 pF, maximum delays can be derated by 1 ns per 10 pF

When operating at frequencies other than the frequency marked on the part, new bus timing must be calculated for all frequency-dependent AC parameters. Frequency-dependent AC parameters are those with an entry in the 'FFACT' column. AC parameters without an FFactor entry are not frequency-dependent and therefore do not need to be recalculated.





To calculate the AC parameters for a frequency F, the following equation should be applied to each one of the above parameters :
for minima :

$$D = D_{50} + \frac{\text{FFACTOR} (1000 - 20 \times F)}{F}$$

where

D is the parameter value in nanoseconds for the frequency required

F is the operation frequency in MHz

D50 is the parameter defined for 50 MHz

FFACTOR is the one defined for each one of the parameters in the table.

$$V_{cc} = 3.3 \pm 5\% \text{ V dc, GND} = 0 \text{ V dc, } -55^{\circ}\text{C} \leq T_c \leq 125^{\circ}\text{C}$$

Table 5 : Bus Operation Timings

	Characteristic	50MHz		33MHz ¹		Unit	FFACTOR
		Min	Max	Min	Max		
B1	CLKOUT Period	20		30.30		ns	
B1a	EXTCLK to CLKOUT Phase Skew (EXTCLK>15MHZ and MF <=2)	-0.90	0.90	-0.90	0.90	ns	
B1b	EXTCLK to CLKOUT Phase Skew (EXTCLK>10MHZ and MF <10)	-2.30	2.30	-2.30	2.30	ns	
B1c	CLKOUT Phase Jitter (EXTCLK>15MHZ and MF <=2)	-0.60	0.60	-0.60	0.60	ns	
B1d	CLKOUT Phase Jitter ²	-2.00	2.00	-2.00	2.00	ns	
B1e	CLKOUT Frequency Jitter (MF<10) ²		0.50		0.50	%	
B1f	CLKOUT Frequency Jitter (10<MF<500) ²		2.00		2.00	%	
B1g	CLKOUT Frequency Jitter (MF>500) ²		3.00		3.00	%	
B1h	Frequency Jitter on EXTCLK ³		0.50		0.50	%	
B2	CLKOUT pulse width low	8.00		12.12		ns	
B3	CLKOUT width high	8.00		12.12		ns	
B4	CLKOUT rise time		4.00		4.00	ns	
B5	CLKOUT fall time		4.00		4.00	ns	
B6							
B7	CLKOUT to A(0:31), BADDR(28:30), RD/ $\overline{\text{WR}}$, BURST, D(0:31), DP(0:3) Invalid	5.00		7.58		ns	0.250
B7a	CLKOUT to TSIZ(0:1), $\overline{\text{REG}}$, $\overline{\text{RSV}}$, AT(0:3), $\overline{\text{BDIP}}$, PTR Invalid	5.00		7.58		ns	0.250
B7b	CLKOUT to $\overline{\text{BR}}$, $\overline{\text{BG}}$, FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), STS Invalid ⁴	5.00		7.58		ns	0.250

	Characteristic	50MHz		33MHz ¹		Unit	FFACTOR
		Min	Max	Min	Max		
B8	CLKOUT to A(0:31), BADDR(28:30), RD \overline{WR} , \overline{BURST} , D(0:31), DP(0:3) valid	5.00	11.75	7.58	14.33	ns	0.250
B8a	CLKOUT to TSIZ(0:1), \overline{REG} , \overline{RSV} , AT(0:3), \overline{BDIP} , PTR valid	5.00	11.75	7.58	14.33	ns	0.250
B8b	CLKOUT to \overline{BR} , \overline{BG} , VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), \overline{STS} valid ⁴	5.00	11.75	7.58	14.33	ns	0.250
B9	CLKOUT to A(0:31), BADDR(28:30), RD \overline{WR} , \overline{BURST} , D(0:31), DP(0:3), TSIZ(0:1), \overline{REG} , \overline{RSV} , AT(0:3), PTR High Z	5.00	11.75	7.58	14.33	ns	0.250
B10						ns	
B11	CLKOUT to \overline{TS} , \overline{BB} assertion	5.00	11.00	7.58	13.58	ns	0.250
B11a	CLKOUT to \overline{TA} , \overline{BI} assertion (when driven by the Memory Controller or PCMCIA I/F)	2.50	9.25	2.5	9.25	ns	-
B12	CLKOUT to \overline{TS} , \overline{BB} negation	5.00	11.75	7.58	14.33	ns	0.250
B12a	CLKOUT to \overline{TA} , \overline{BI} negation (when driven by the Memory Controller or PCMCIA interface)	2.50	11.00	2.50	11.00	ns	-
B13	CLKOUT to \overline{TS} , \overline{BB} High Z	5.00	19.00	7.58	21.58	ns	0.25
B13a	CLKOUT to \overline{TA} , \overline{BI} High Z (when driven by the Memory Controller or PCMCIA interface)	2.50	15.00	2.50	15.00	ns	-
B14	CLKOUT to \overline{TEA} assertion	2.50	10.00	2.50	10.00	ns	-
B15	CLKOUT to \overline{TEA} High Z	2.50	15.00	2.50	15.00	ns	-
B16	\overline{TA} , \overline{BI} valid to CLKOUT (Setup Time)	9.75		9.75		ns	
B16a	\overline{TEA} , \overline{KR} , \overline{RETRY} , \overline{CR} valid to CLKOUT (Setup Time)	10.00		10.00		ns	
B16b	BB, BG, BR, valid to CLKOUT (setup time) ⁵	8.50		8.50		ns	
B17	CLKOUT to \overline{TA} , \overline{TEA} , \overline{BI} , \overline{BB} , \overline{BG} , \overline{BR} valid (Hold Time)	1.00		1.00		ns	
B17a	CLKOUT to \overline{KR} , \overline{RETRY} , \overline{CR} valid (Hold Time)	2.00		2.00		ns	
B18	D(0:31), DP(0:3) valid to CLKOUT Rising Edge (Setup Time) ⁶	6.00		6.00		ns	
B19	CLKOUT Rising Edge to D(0:31), DP(0:3) ⁻ valid (Hold Time) ⁶	1.00		1.00		ns	
B20	D(0:31), DP(0:3) valid to CLKOUT Falling Edge (Setup Time) ⁷	4.00		4.00		ns	

	Characteristic	50MHz		33MHz ¹		Unit	FFACTOR
		Min	Max	Min	Max		
B21	CLKOUT Falling Edge to D(0:31), DP(0:3) valid (Hold Time) ⁷	2.00		2.00		ns	
B22	CLKOUT Rising Edge to \overline{CS} asserted -GPCM-ACS = 00	5.00	11.75	7.58	14.33	ns	0.250
B22a	CLKOUT Falling Edge to \overline{CS} asserted -GPCM-ACS = 11, TRLX = 0, EBDF = 0		8.00		8.00	ns	
B22b	CLKOUT Falling Edge to \overline{CS} asserted -GPCM-ACS = 11, TRLX = 0, EBDF = 0	5	11.75	7.58	14.33	ns	0.250
B22c	CLKOUT Falling Edge to \overline{CS} asserted -GPCM-ACS = 11, TRLX = 0, EBDF = 1	7.00	14.13	10.86	17.99	ns	0.375
B23	CLKOUT Rising Edge to \overline{CS} negated -GPCM- Read Access, -GPCM- write access, ACS = '00', TRLX = '0' & CSNT = '0'	2.00	8.00	2.00	8.00	ns	-
B24	A(0:31) and BADDR(28:30) to \overline{CS} asserted -GPCM- ACS = 10, TRLX = 0	3.00		5.58		ns	0.250
B24a	A(0:31) and BADDR(28:30) to \overline{CS} asserted -GPCM- ACS = 11, TRLX = 0	8.00		13.15		ns	0.500
B25	CLKOUT Rising Edge to \overline{OE} , \overline{WE} (0:3) asserted		9.00		9.00	ns	-
B26	CLKOUT Rising Edge to \overline{OE} negated	2.00	9.00	2.00	9.00	ns	-
B27	A(0:31) and BADDR(28:30) to \overline{CS} asserted -GPCM- ACS = 10, TRLX = 1	23.00		35.88		ns	1.250
B27a	A(0:31) and BADDR(28:30) to \overline{CS} asserted -GPCM- ACS = 11, TRLX = 1	28.00		43.45		ns	1.500
B28	CLKOUT rising edge to \overline{WE} (0:3) negated GPCM write access CSNT = 0		9.00		9.00	ns	
B28a	CLKOUT falling Edge to \overline{WE} (0:3) negated -GPCM-write access TRLX = 0, CSNT = 1, EBDF = 0	5.00	11.75	7.58	14.33	ns	0.250
B28b	CLKOUT Falling Edge to \overline{WE} (0:3) negated -GPCM-write access TRLX = '0', CSNT = '1', EBDF=0		11.75		14.33	ns	0.250
B28c	CLKOUT Falling Edge to \overline{WE} (0:3) negated -GPCM-write access TRLX = '0', CSNT = '1' write access TRLX = 0, CSNT = 1, EBDF = 1	7.00	14.13	10.86	17.99	ns	0.375
B28d	CLKOUT Falling Edge to \overline{CS} negated negated -GPCM-write access TRLX = '0', CSNT = '1', ACS = 10, or ACS = 11', EBDF=1		14.13		17.99	ns	0.375

	Characteristic	50MHz		33MHz ¹		Unit	FFACTOR
		Min	Max	Min	Max		
B29	WE (0:3) negated to DP (0:3) High-Z-GPCM-write access, CSNT = 0, EBDF = 0	3.00		5.58		ns	0.250
B29a	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '0', CSNT = '1', EBDF = 0	8.00		13.15		ns	0.500
B29b	\overline{CS} negated to D(0:31), DP(0:3) High Z -GPCM- write access, ACS = '00', TRLX = '0' & CSNT = '0'	3.00		5.58		ns	0.250
B29c	\overline{CS} negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '0', CSNT = '1', , ACS = '11', EBDF = 0	8.00		13.15		ns	0.500
B29d	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '1', CSNT = '1', EBDF = 0	28.00		43.45		ns	1.500
B29e	\overline{CS} negated to D (0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11 EBDF = 0	28.00		43.45		ns	1.500
B29f	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '0', CSNT = '1', EBDF = 1	5.00		8.86		ns	0.375
B29g	\overline{CS} negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '0', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	5.00		8.86		ns	0.375
B29h	\overline{WE} (0:3) negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '1', CSNT = '1', EBDF = 1	24.50		38.67		ns	1.375
B29i	\overline{CS} negated to D(0:31), DP(0:3) High Z -GPCM- write access, TRLX = '1', CSNT = '1', ACS = '10' or ACS='11', EBDF = 1	24.50		38.67		ns	1.375
B30	\overline{CS} , \overline{WE} (0:3) negated to A(0:31), BADDR(28:30) invalid -GPCM- write access ⁸	3.00		5.58			0.250
B30a	\overline{WE} (0:3) negated to A(0:31), BADDR(28:30) invalid -GPCM- write access, TRLX='0', CSNT = '1'. \overline{CS} negated to A(0:31) invalid -GPCM- write access, TRLX='0', CSNT = '1', ACS = 10 , ACS = '11', EBDF = 0	8.00		13.15		ns	0.500

	Characteristic	50MHz		33MHz ¹		Unit	FFACTOR
		Min	Max	Min	Max		
B30b	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid –GPCM– write access, $TRLX='1'$, $CSNT = '1'$. CS negated to A(0:31) invalid –GPCM– write access, $TRLX='1'$, $CSNT = '1'$, $ACS = 10$, $ACS = '1 1'$, $EBDF = 0$	28.00		43.45		ns	1.500
B30c	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid –GPCM– write access, $TRLX='0'$, $CSNT = '1'$. \overline{CS} negated to A(0:31) invalid –GPCM– write access, $TRLX='0'$, $CSNT = '1'$, $ACS = 10$, $ACS = '11'$, $EBDF = 1$	4.50		8.36		ns	0.375
B30d	$\overline{WE}(0:3)$ negated to A(0:31), BADDR(28:30) invalid –GPCM– write access, $TRLX='1'$, $CSNT = '1'$. CS negated to A(0:31) invalid –GPCM– write access, $TRLX='1'$, $CSNT = '1'$, $ACS = 10$, $ACS = '11'$, $EBDF = 1$	24.50		38.67		ns	1.375
B31	CLKOUT Falling Edge to \overline{CS} valid –as requested by control bit CST4 in the corresponding word in the UPM	1.5	6.00	1.50	6.00	ns	–
B31a	CLKOUT Falling Edge to \overline{CS} valid – as requested by control bit CST1 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B31b	CLKOUT Rising Edge to \overline{CS} valid – as requested by control bit CST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	ns	–
B31c	CLKOUT Rising Edge to \overline{CS} valid – as requested by control bit CST3 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B31d	CLKOUT Falling Edge to \overline{CS} valid – as requested by control bit CST1 in the corresponding word in the UPM, $EBDF = 1$	9.40	14.13	13.26	17.99	ns	0.375
B32	CLKOUT Falling Edge to \overline{BS} valid –as requested by control bit BST4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	ns	–
B32a	CLKOUT Falling Edge to \overline{BS} valid – as requested by control bit BST1 in the corresponding word in the UPM, $EBDF = 0$	5	11.75	7.58	14.33	ns	0.250
B32b	CLKOUT Rising Edge to \overline{BS} valid – as requested by control bit BST2 in the corresponding word in the UPM	1.50	8.00	1.50	8.00	ns	–
B32c	CLKOUT Rising Edge to \overline{BS} valid – as requested by control bit BST3 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.25

	Characteristic	50MHz		33MHz (1)		Unit	FFACTOR
		Min	Max	Min	Max		
B32d	CLKOUT Falling Edge to \overline{BS} valid – as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1	9.40	14.13	13.26	17.99	ns	0.375
B33	CLKOUT Falling Edge to \overline{GPL} valid –as requested by control bit GxT4 in the corresponding word in the UPM	1.50	6.00	1.50	6.00	ns	–
B33a	CLKOUT Rising Edge to \overline{GPL} valid – as requested by control bit GxT3 in the corresponding word in the UPM	5.00	11.75	7.58	14.33	ns	0.250
B34	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid as requested by control bit CST4 in the corresponding word in the UPM	3		5.58		ns	0.250
B34a	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid as requested by control bit CST1 in the corresponding word in the UPM	8.00		13.15		ns	0.500
B34b	A(0:31), BADDR(28:30), and D(0:31) to \overline{CS} valid as requested by control bit CST2 in the corresponding word in the UPM	13		20.73		ns	0.750
B35	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid as requested by control bit BST4 in the corresponding word in the UPM	3.00		5.58		ns	0.250
B35a	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid as requested by control bit BST1 in the corresponding word in the UPM	8.00		13.15		ns	0.500
B35b	A(0:31), BADDR(28:30), and D(0:31) to \overline{BS} valid as requested by control bit BST2 in the corresponding word in the UPM	13.00		20.73		ns	0.750
B36	A(0:31), BADDR(28:30), and D(0:31) to \overline{GPL} valid as requested by control bit GxT4 in the corresponding word in the UPM	3.00		5.58		ns	0.250
B37	UPWAIT valid to CLKOUT Faling Edge ⁹	6.00		6.00		ns	
B38	CLKOUT Falling Edge to UPWAIT valid ⁹	1.00		1.00		ns	
B39	\overline{AS} valid to CLKOUT Rising Edge ¹⁰	7.00		7.00		ns	
B40	A(0:31), TSIZ(0:1), RD/ \overline{WR} , \overline{BURST} , valid to CLKOUT Rising Edge.	7.00		7.00		ns	
B41	\overline{TS} valid to CLKOUT Rising Edge (SetUp Time).	7.00		7.00		ns	
B42	CLKOUT Rising Edge to TS Valid (Hold Time).	2.00		2.00		ns	
B43	\overline{AS} negation to Memory Controller Signals Negation		TBD			ns	

1. The values in the 33 MHz column are derived from the 50 MHz values.
2. Phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed value.
3. If the rate of change of the frequency of EXTAL is slow (i.e. it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e. it does not stay at an extreme value for a long time) then the maximum allowed jitter on EXTAL can be up to 2 %.
4. The timing for BR output is relevant when the PC860 is selected to work with external bus arbiter. The timing for BG output is relevant when the PC860 is selected to work with internal bus arbiter.
5. The timing required for $\overline{\text{BR}}$ input is relevant when the MPC860 is selected to work with internal bus arbiter. The timing for $\overline{\text{BG}}$ input is relevant when the PC860 is selected to work with external bus arbiter.
6. The D (0:31) and DP (0:3) input timings B20 and B21 refer to the rising edge of the CLKOUT in which the $\overline{\text{TA}}$ input signal is asserted.
7. The D (0:31) and DP (0:3) input timings B20 and B21 refer to the falling edge of the CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the Memory Controller, for data beats where DLT3 = 1 in the UPM RAM words. (This is only the cases where data is latched on the falling edge of CLKOUT).
8. The timing B30 refers to $\overline{\text{CS}}$ when ACS = 00 and to $\overline{\text{WE}}$ (0:3) when CSNT = 0
9. The signal UPWAIT is considered asynchronous to the CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 22.
10. The AS signal is considered asynchronous to the CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 25.

Figure 8 : External Clock Timing

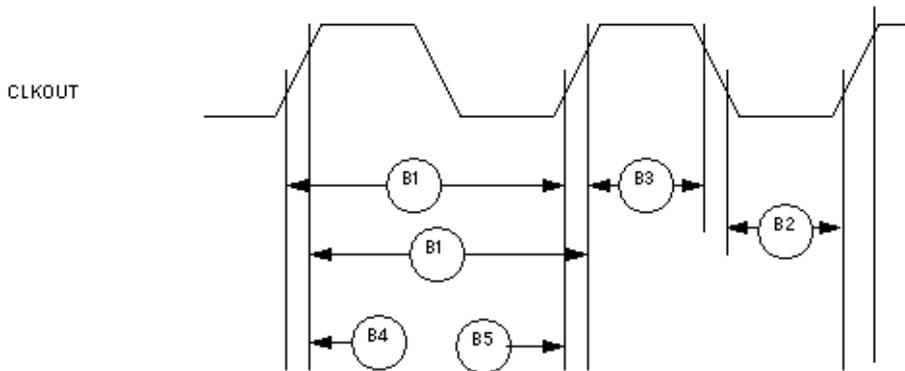


Figure 9 : Synchronous Output Signals Timing

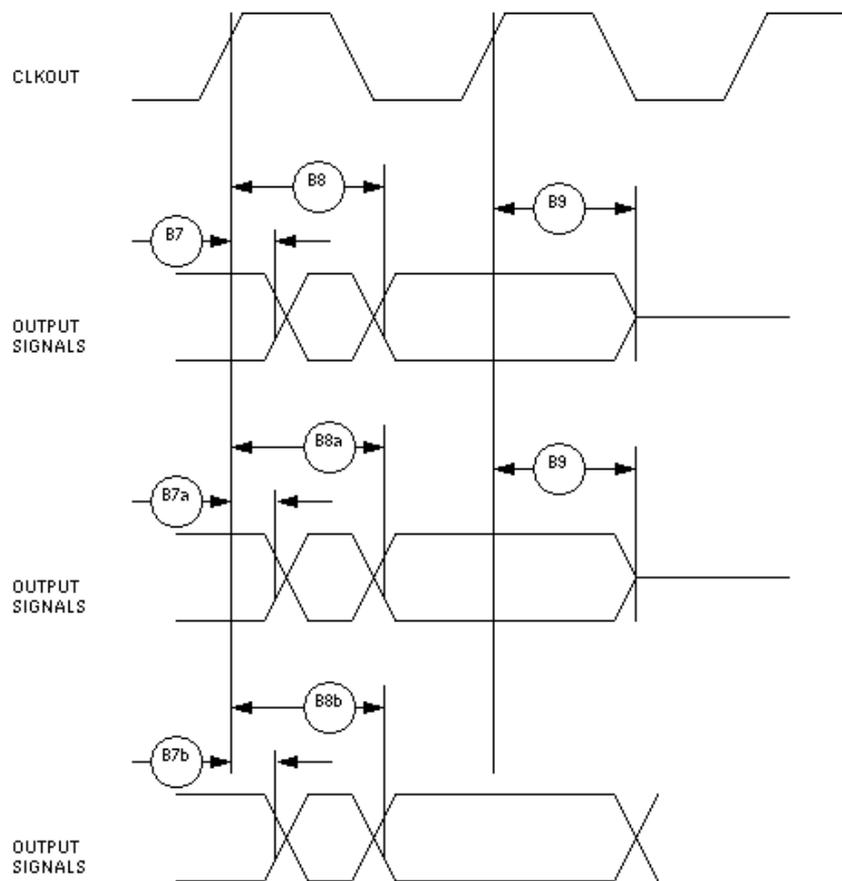


Figure 10 : Synchronous Active Pullup And Open Drain Outputs Signals Timing

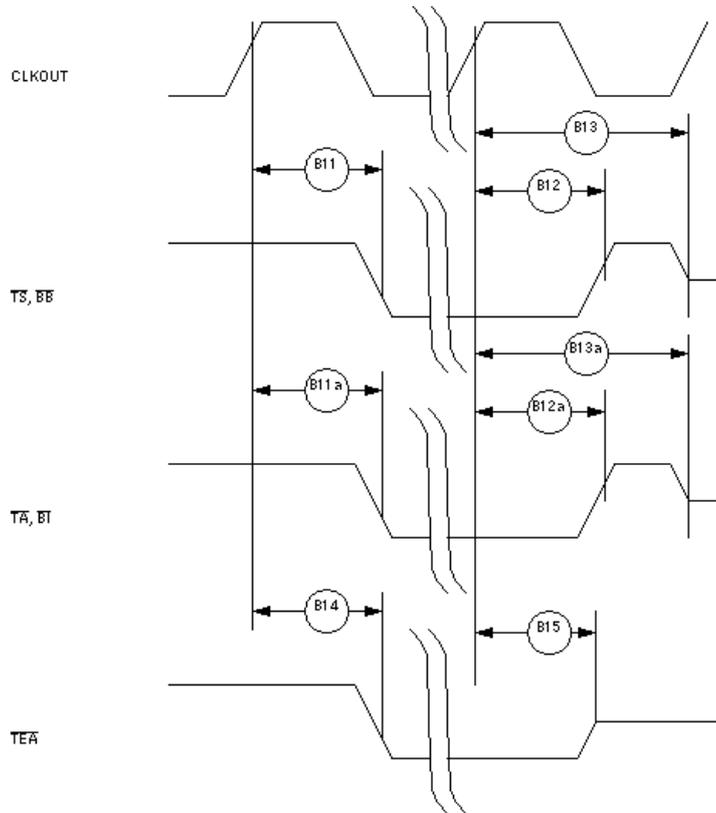


Figure 11 : Synchronous Input Signals Timing

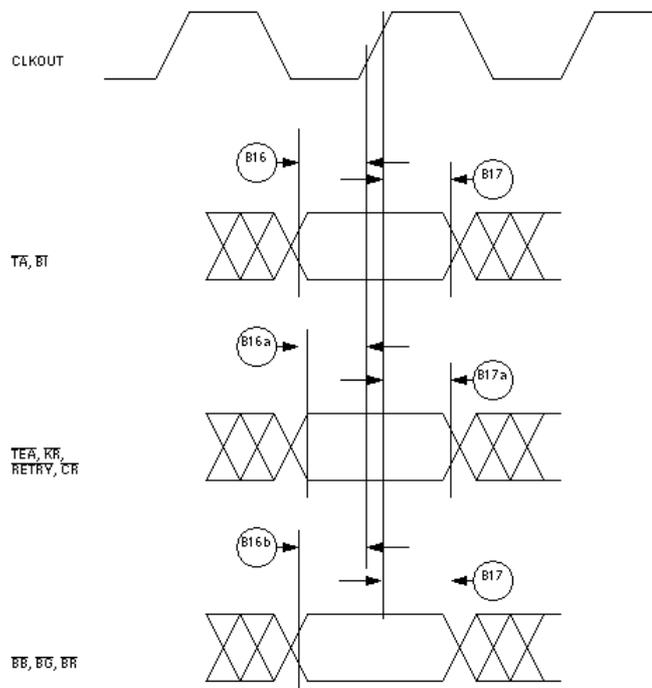


Figure 12 : Input Data Timing in Normal case

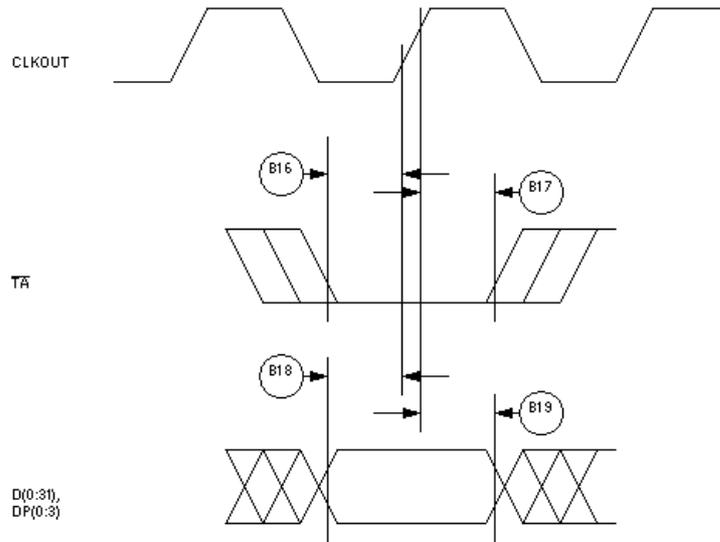


Figure 13 : Input Data Timing when controlled by UPM in the Memory Controller

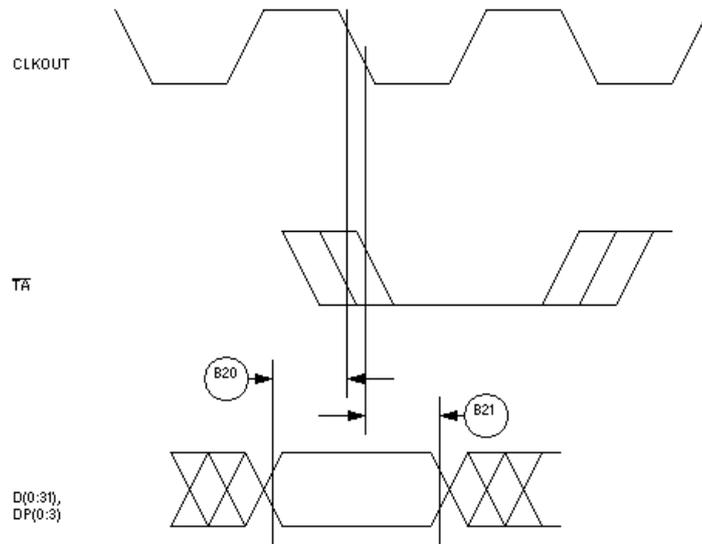


Figure 14 : External Bus Read Timing (GPCM Controlled - ACS = '00')

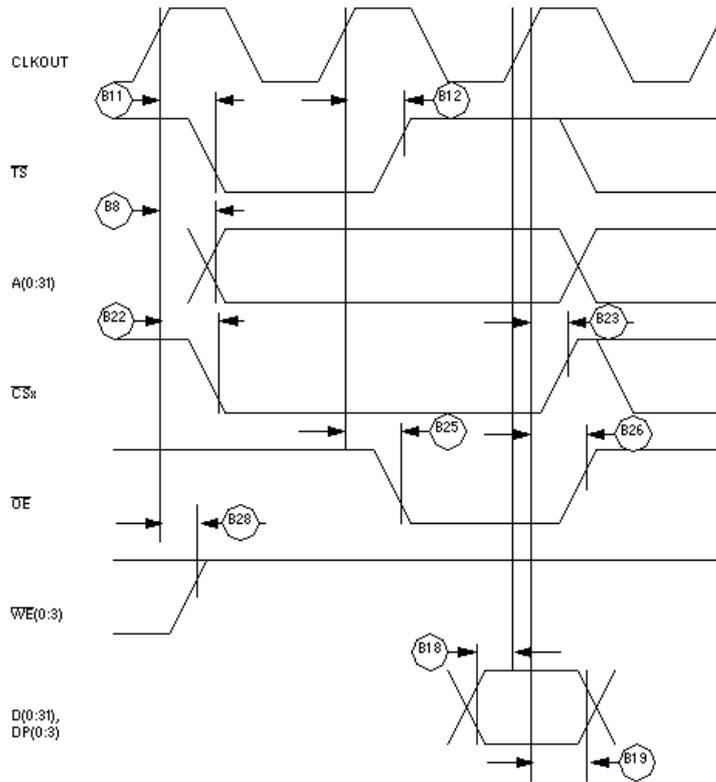


Figure 15 : External Bus Read Timing (GPCM Controlled - TRLX = '0' ACS = '10')

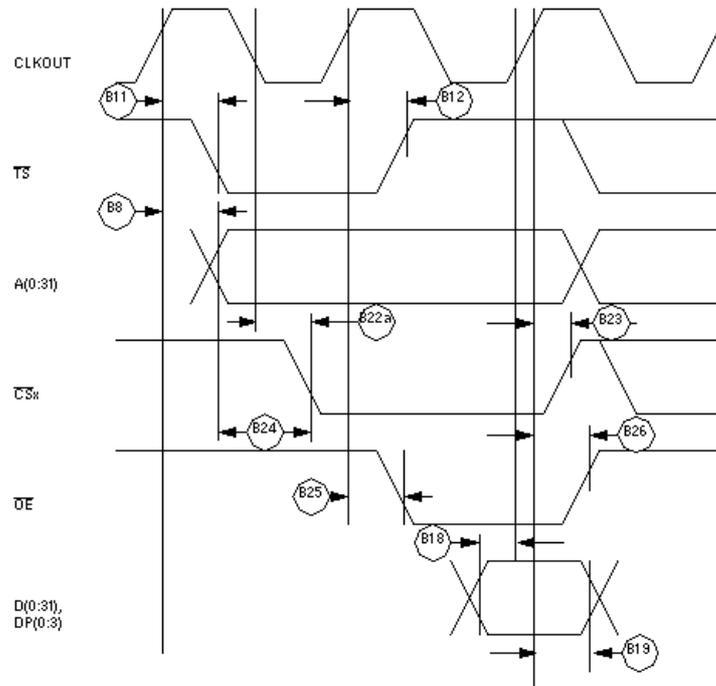


Figure 16 : External Bus Read Timing (GPCM Controlled - TRLX = '0' ACS = '11')

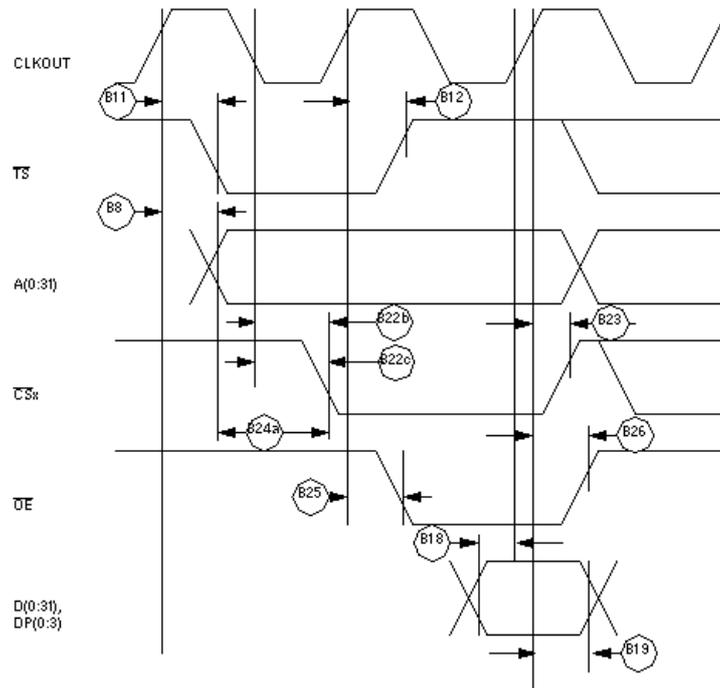


Figure 17 : External Bus Read Timing (GPCM Controlled - TRLX = '1', ACS = '10', ACS = '11')

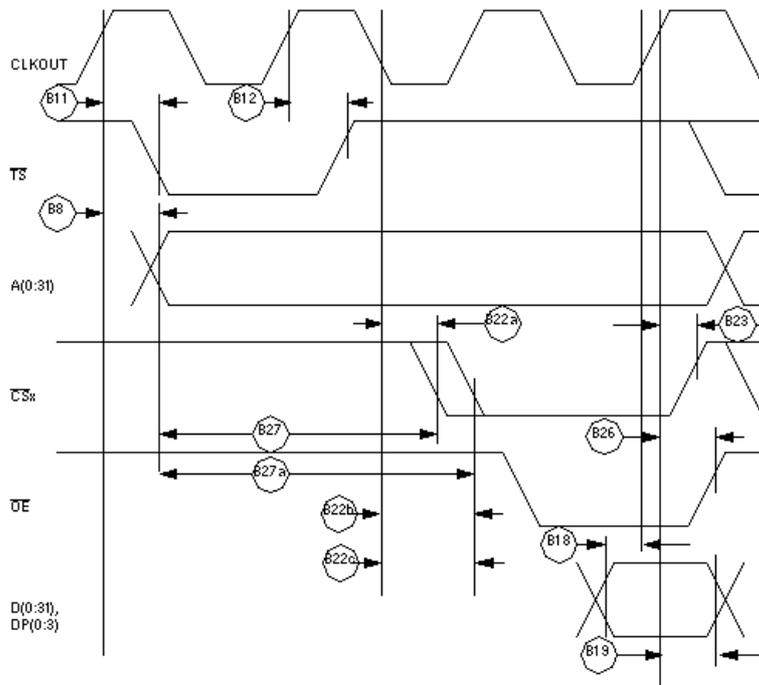


Figure 18 : External Bus Write Timing (GPCM controlled - TRLX = '0', CSNT = '0')

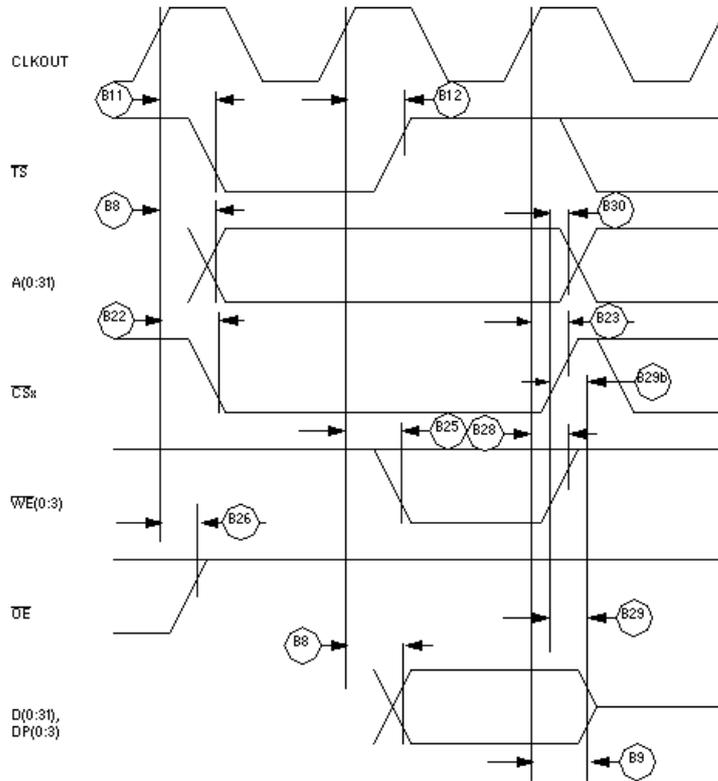


Figure 19 : External Bus Write Timing (GPCM controlled - TRLX = '0', CSNT = '1')

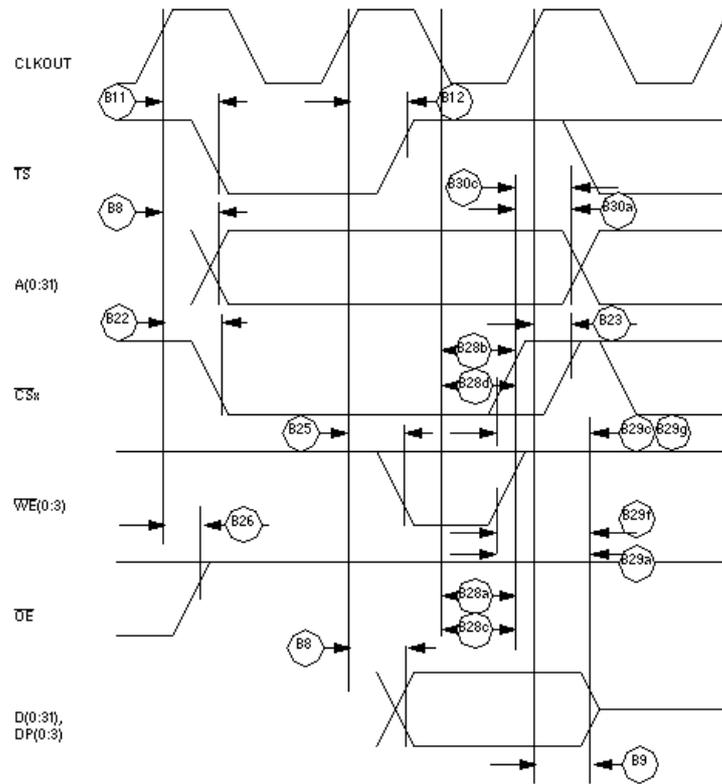


Figure 20 : External Bus Write Timing (GPCM controlled - TRLX = '1', CSNT = '1')

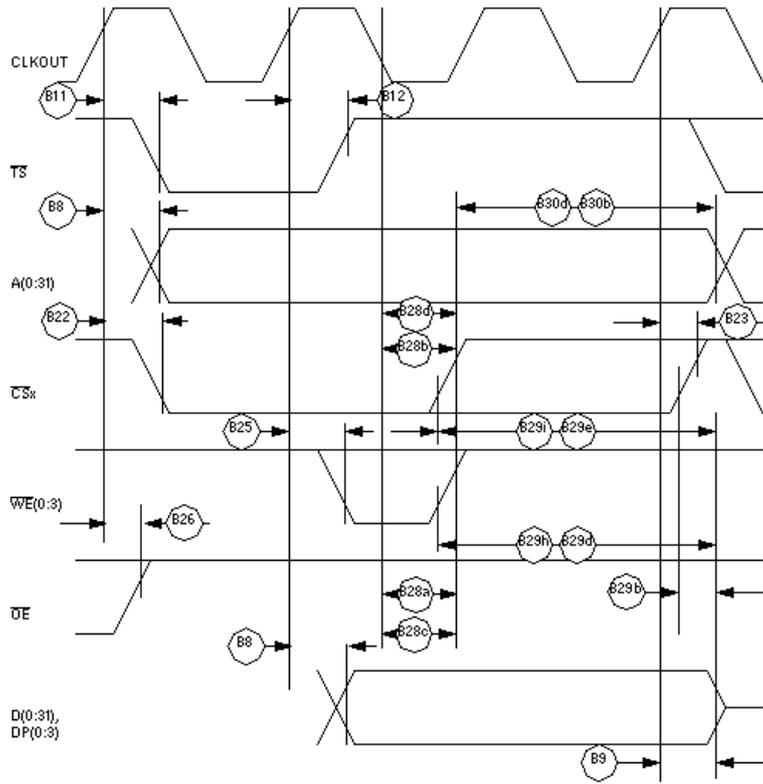


Figure 21 : External Bus Timing (UPM Controlled Signals)

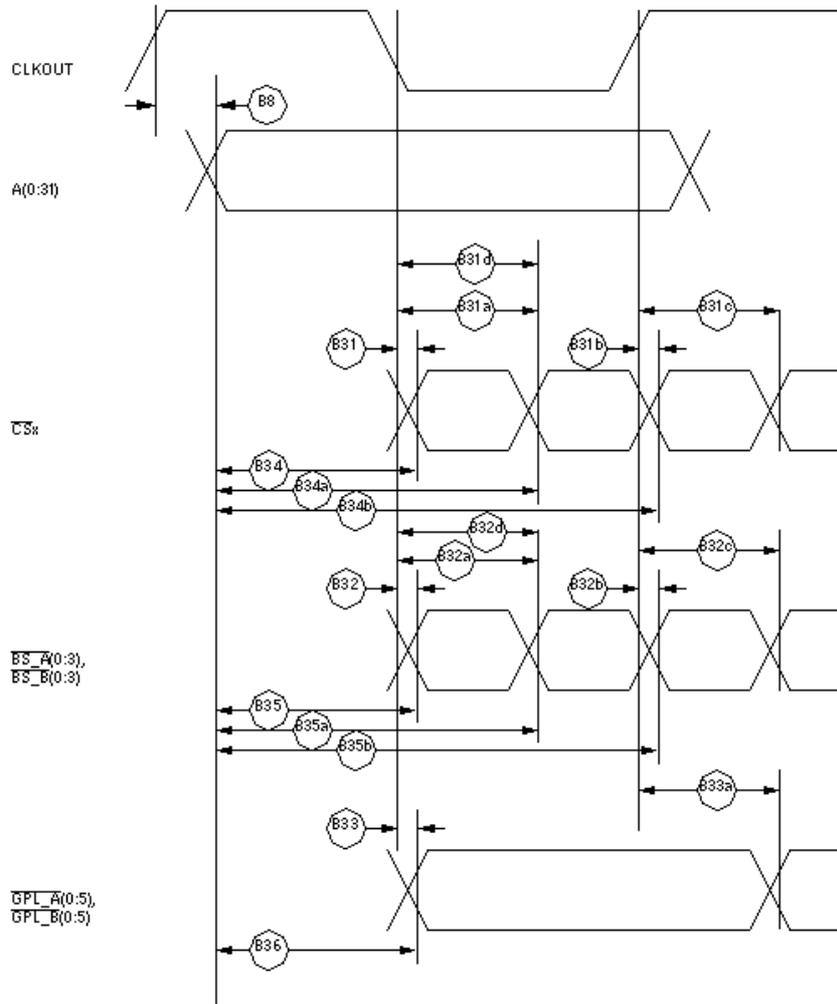


Figure 22 : Asynchronous UPWAIT asserted detection in UPM handled cycles Timing

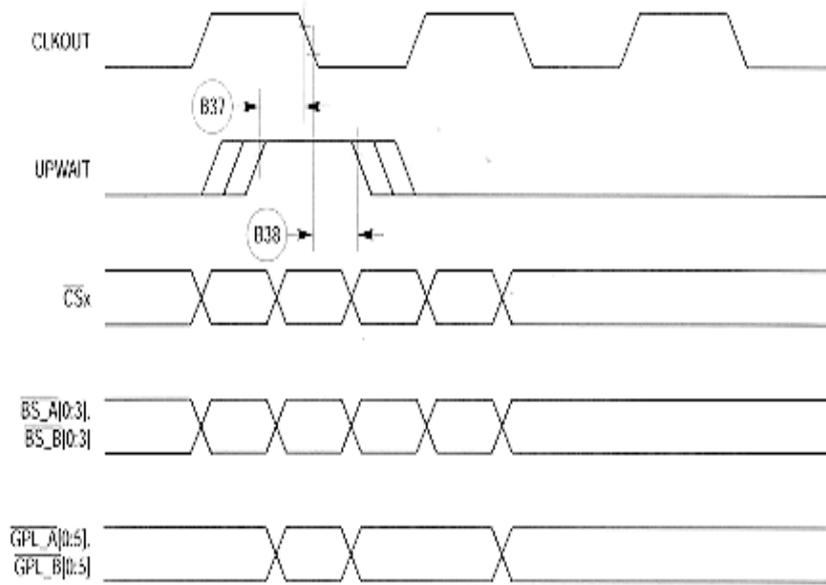


Figure 23 : Asynchronous UPWAIT negated detection in UPM handled cycles Timing

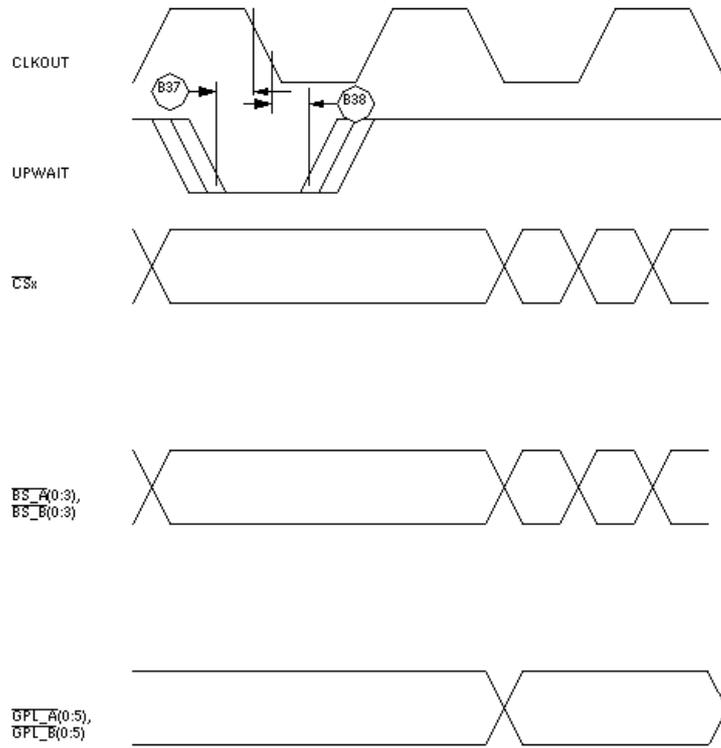
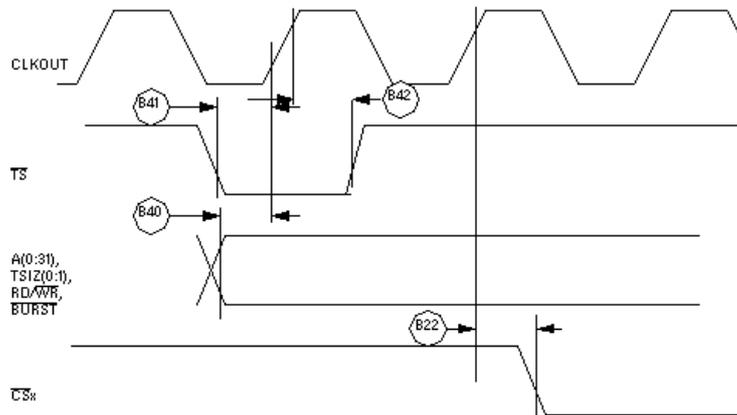


Figure 24 : Synchronous External Master Access Timing - GPCM handled ACS = '00'



**Figure 25 : Asynchronous External Master Memory Access Timing
(GPCM Controlled-ACS = '00')**

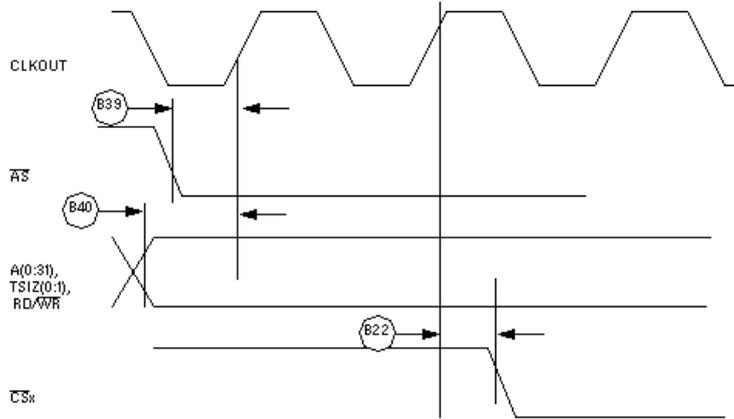


Figure 26 : Asynchronous External Master - Control Signals Negation Time

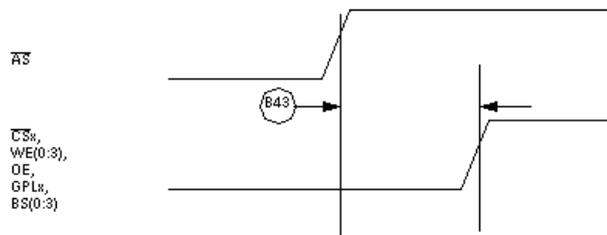


Table 6 : Interrupt Timing

Num	Characteristic	33MHz		50MHz		Unit
		Min	Max	Min	Max	
I39	\overline{IRQx} valid to CLKOUT rising edge (set up time)	6.00		6.00		ns
I40	\overline{IRQx} hold time after CLKOUT	2.00		2.00		ns
I41	\overline{IRQx} Pulse width Low	3.00		3.00		ns
I42	\overline{IRQx} Pulse width High	3.00		3.00		ns
I43	\overline{IRQx} Edge to Edge time	4XT- CLOCKOUT		4XT CLOCKOUT		-

NOTES:

The timings I39 and I40 describe the testing conditions under which the \overline{IRQ} lines are tested when being defined as level sensitive. The \overline{IRQ} lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.

The timings I41, I42 and I43 are specified to allow the correct function of the \overline{IRQ} lines detection circuitry, and has no direct relation with the total system interrupt latency that the TSPC860 is able to support.

Figure 27 : Interrupt Detection Timing for External Level Sensitive Lines

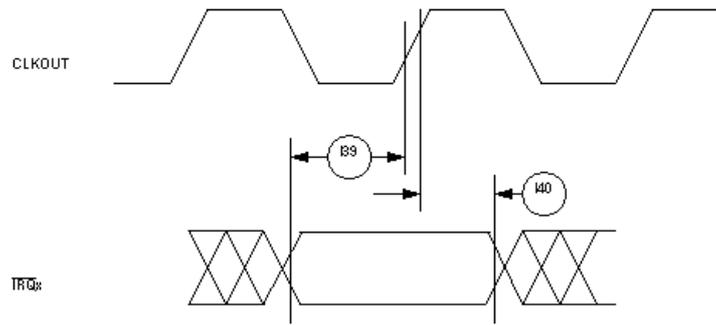


Figure 28 : Interrupt Detection Timing for External Edge Sensitive Lines

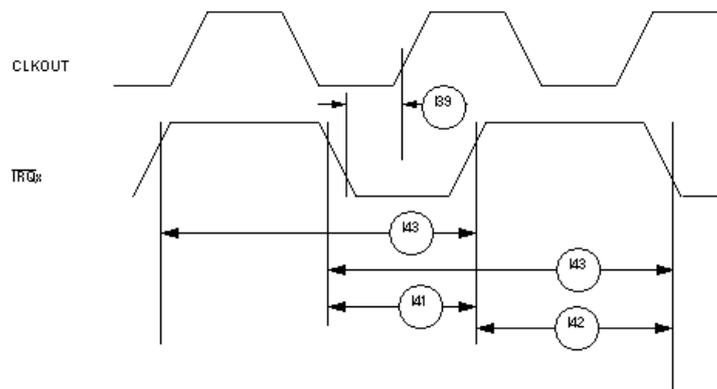


Table 7 : PCMCIA Timing

	Characteristic	33MHz		50MHz		FFACTOR	Unit
		Min	Max	Min	Max		
P44	A(0:31), \overline{REG} valid to PCMCIA Strobe asserted. ¹	20.73		13.00		0.750	ns
P45	A(0:31), \overline{REG} valid to ALE negation. ¹	28.30		18.00		1.000	ns
P46	CLKOUT to \overline{REG} valid	7.58	15.58	5.00	13.00	0.250	ns
P47	CLKOUT to \overline{REG} Invalid.	8.58		6.00		0.250	ns
P48	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted.	7.58	15.58	5.00	13.00	0.250	
P49	CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated.	7.58	15.58	5.00	13.00	0.250	ns
P50	CLKOUT to \overline{PCOE} , \overline{IORD} , \overline{PCWE} , \overline{IOWR} assert time.		11.00		11.00	-	ns
P51	CLKOUT to \overline{PCOE} , \overline{IORD} , \overline{PCWE} , \overline{IOWR} negate time.	2.00	11.00	2.00	11.00	-	ns
P52	CLKOUT to ALE assert time	7.58	15.58	5.00	13.00	0.250	ns
P53	CLKOUT to ALE negate time		15.58		13.00	0.250	ns

P54	\overline{PCWE} , \overline{IOWR} negated to D(0:31) invalid ¹	5.58		3.00		0.250	ns
P55	\overline{WAITA} and \overline{WAITB} valid to CLKOUT rising edge ¹	8.00		8.00			ns
P56	CLKOUT rising edge to \overline{WAITA} and \overline{WAITB} invalid. ¹	2.00		2.00			ns

NOTES:

PSST = 1. Otherwise add PSST times cycle time.

PSHT = 1. Otherwise add PSHT times cycle time.

These synchronous timings define when the WAITx signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The WAITx assertion will be effective only if it is detected 2 cycles before the PSL timer expiration.

Figure 29 : PCMCIA access cycles Timing External Bus Read

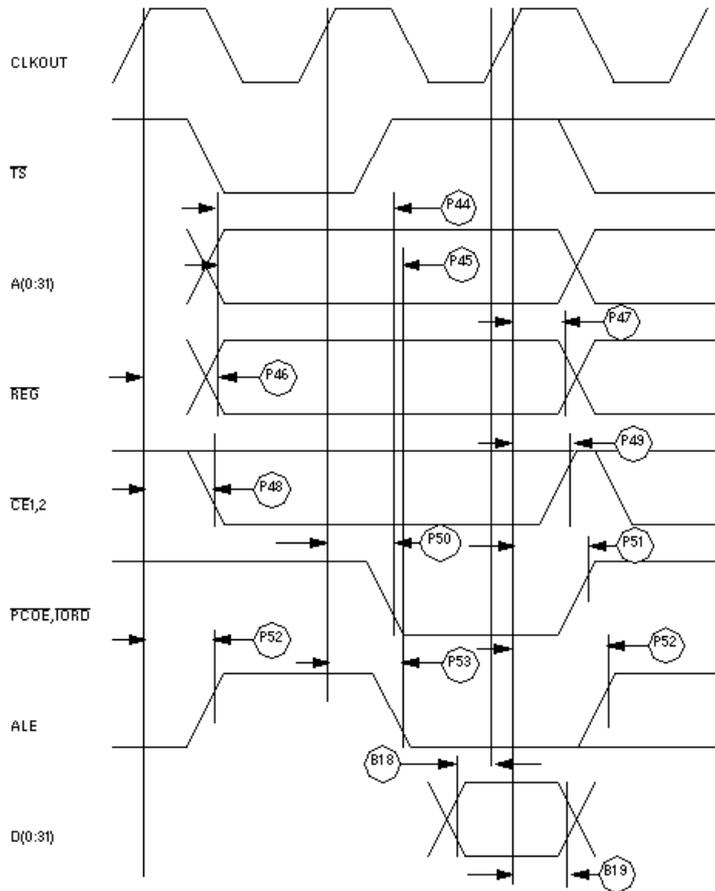


Figure 30 : PCMCIA access cycles Timing External Bus Write

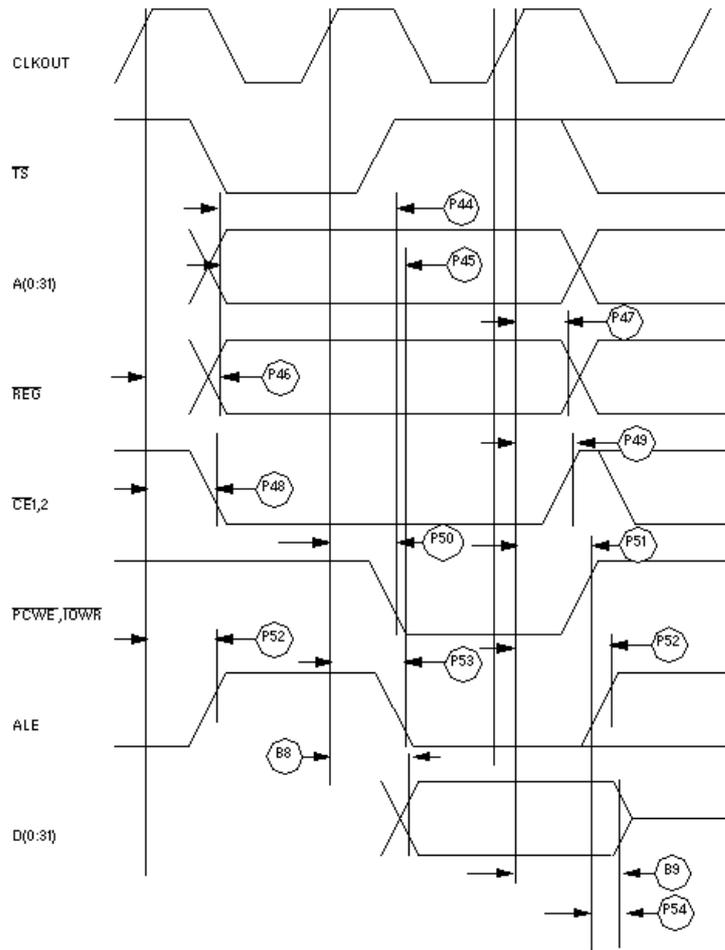


Figure 31 : PCMCIA Wait signals detection Timing

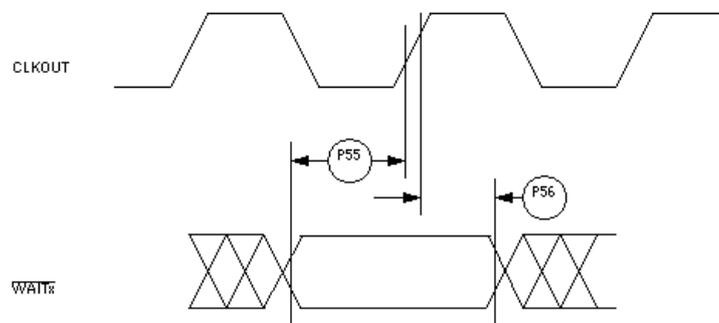


Table 8 : PCMCIA Port Timing

	Characteristic	33MHz		50MHz		FFactor	Unit
		Min	Max	Min	Max		
P57	CLKOUT to OPx Valid		19.00		19.00		ns
P58	$\overline{\text{HRESET}}$ negated to OPx drive ¹	25.73		18.00		0.75	ns
P59	IP_Xx valid to CLKOUT Rising Edge	5.00		5.00			ns
P60	CLKOUT Rising Edge to IP_Xx invalid	1.00		1.00			ns

NOTE:
OP2 and OP3 only.

Figure 32 : PCMCIA Output port timing

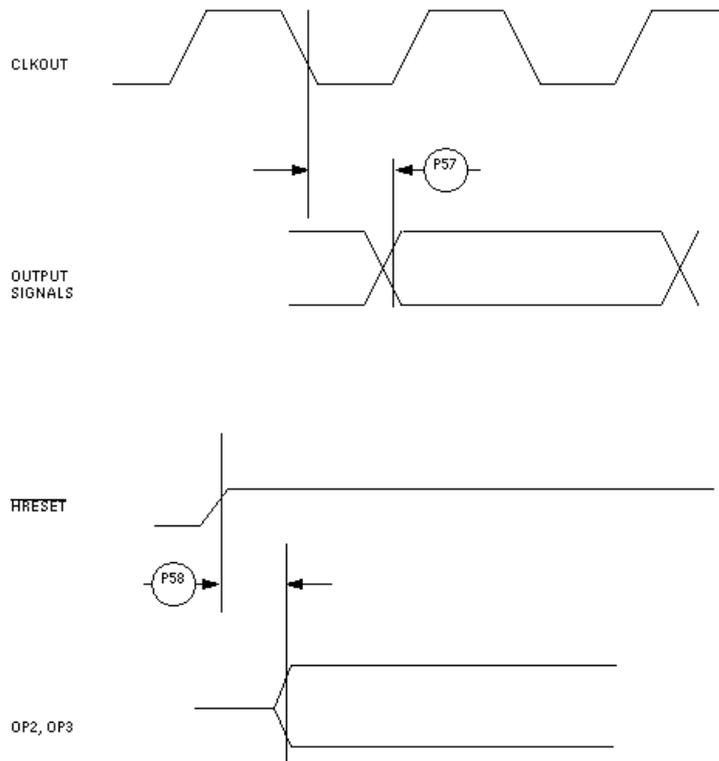


Figure 33 : PCMCIA Input Port Timing

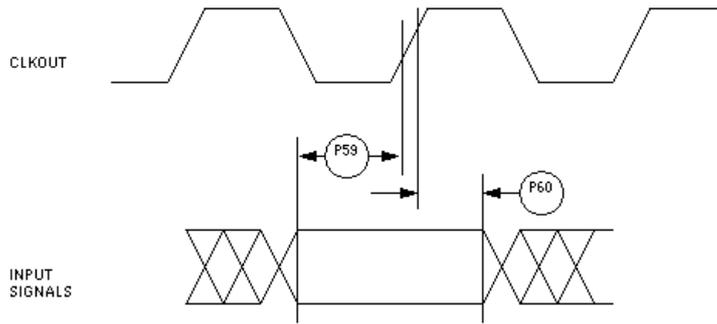


Table 9 : Debug Port Timing

	Characteristic	33MHz		50MHz		Unit
		Min	Max	Min	Max	
D61	DSCK Cycle Time	$3 \times T_{\text{CLOCKOUT}}$	—	$3 \times T_{\text{CLOCKOUT}}$	—	ns
D62	DSCK Clock Pulse Width	$1.25 \times T_{\text{CLOCKOUT}}$	—	$1.25 \times T_{\text{CLOCKOUT}}$	—	ns
D63	DSCK Rise and Fall Times	0.00	3.00	0.00	3.00	ns
D64	DSDI Input Data Setup Time	8.00	—	8.00	—	ns
D65	DSDI Data Hold Time	5.00	—	5.00	—	ns
D66	DSCK Low to DSDO Data Valid	0.00	15.00	0.00	15.00	ns
D67	DSCK Low to DSDO Invalid	0.00	2.00	0.00	2.00	ns

Figure 34 : Debug Port Clock Input Timing

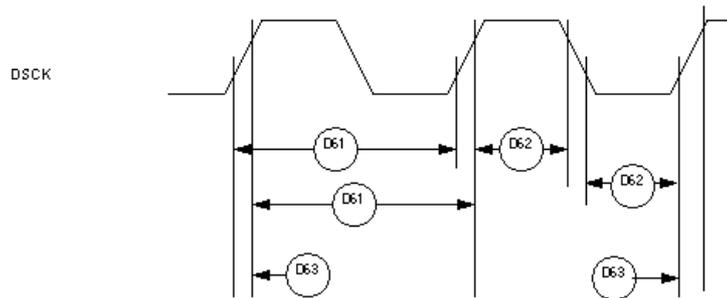


Figure 35 : Debug Port Timings

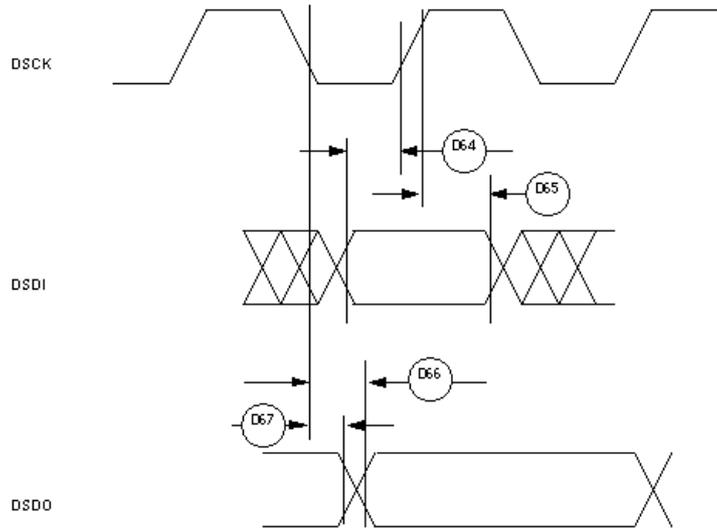


Table 10 : RESET Timing

	Characteristic	33MHz		50MHz		FFACTOR	Unit
		Min	Max	Min	Max		
R69	CLKOUT to $\overline{\text{HRESET}}$ high impedance		20.00		20.00		ns
R70	CLKOUT to $\overline{\text{SRESET}}$ high impedance		20.00		20.00		ns
R71	$\overline{\text{RSTCONF}}$ pulse width	515.15		340.00		17.000	ns
R72							
R73	Configuration Data to $\overline{\text{HRESET}}$ rising edge set up time	504.55		350.00		15.000	ns
R74	Configuration Data to $\overline{\text{RSTCONF}}$ rising edge set up time	350.00		350.00			ns
R75	Configuration Data hold time after $\overline{\text{RSTCONF}}$ negation	0.00		0.00			ns
R76	Configuration Data hold time after $\overline{\text{HRESET}}$ negation	0.00		0.00			ns
R77	$\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to Data out drive		25.00		25.00		ns
R78	$\overline{\text{RSTCONF}}$ negated to Data out high impedance.		25.00		25.00		ns
R79	CLKOUT of last rising edge before chip tristates $\overline{\text{HRESET}}$ to Data out high impedance.		25.00		25.00		ns
R80	DSDI, DSCK set up	90.91		60.00		3.000	ns
R81	DSDI, DSCK hold time	0.00		0.00			ns
R82	$\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample	242.42		160.00		8.000	ns

Figure 36 : Reset Timing - Configuration from Data Bus

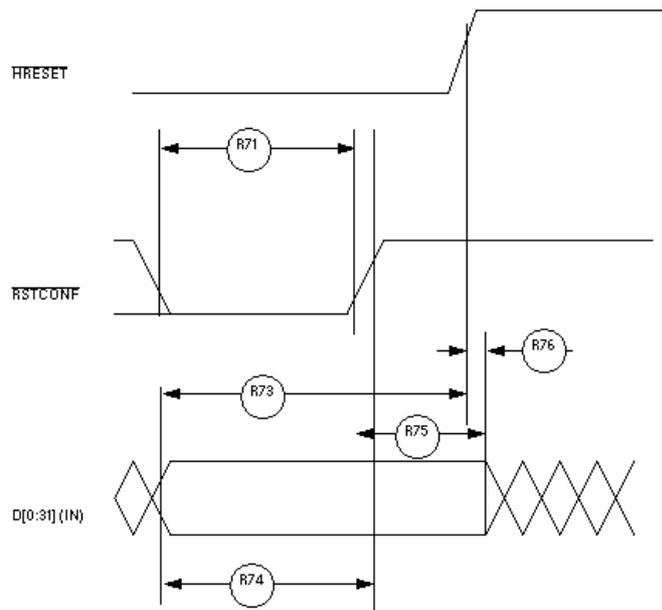


Figure 37 : Reset Timing - TSPC860 Data bus weak drive during Configuration

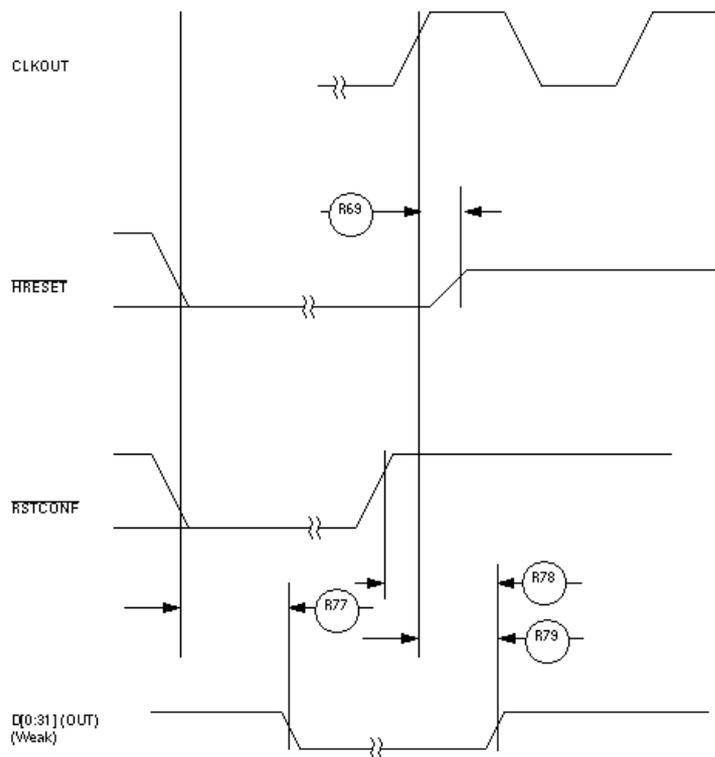
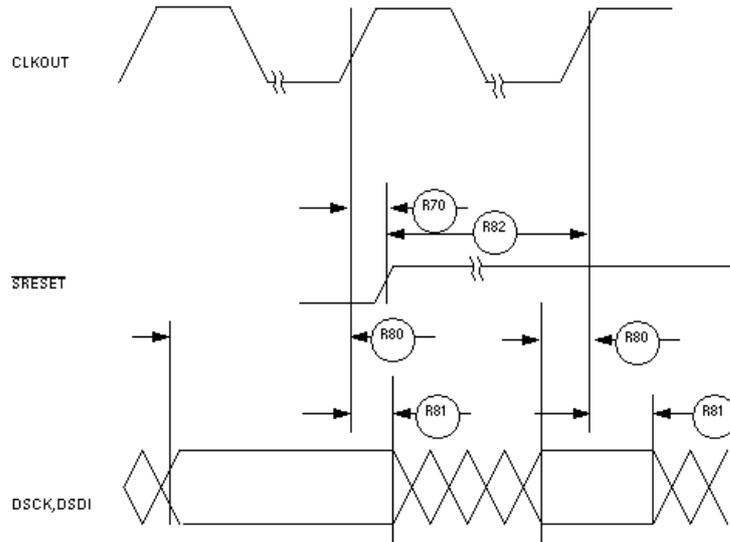


Figure 38 : Reset Timing - Debug Port Configuration



4.4. IEEE 1149.1 ELECTRICAL SPECIFICATIONS

Table 11 : JTAG Timing

	Characteristic	33MHz		50MHz		Unit
		Min	Max	Min	Max	
J82	TCK Cycle Time	100		100		ns
J83	TCK Clock Pulse Width Measured at 1.5 V	40		40		ns
J84	TCK Rise and Fall Times	0	10	0	10	ns
J85	TMS, TDI Data Setup Time	5		5		ns
J86	TMS, TDI Data Hold Time	25		25		ns
J87	TCK Low to TDO Data Valid		27		27	ns
J88	TCK Low to TDO Data Invalid	0		0		ns
J90	TRST Assert Time	100		100		ns
J91	TRST Setup Time to TCK Low	40		40		ns
J92	TCK Falling Edge to Output Valid		50		50	ns
J93	TCK Falling Edge to Output Valid out of High Impedance		50		50	ns
J94	TCK Falling Edge to Output High Impedance		50		50	ns
J95	Boundary Scan Input Valid to TCK Rising Edge	50		50		ns
J96	TCK Rising Edge to Boundary Scan Input Invalid	50		50		ns

Figure 39 : JTAG Test Clock Input Timing

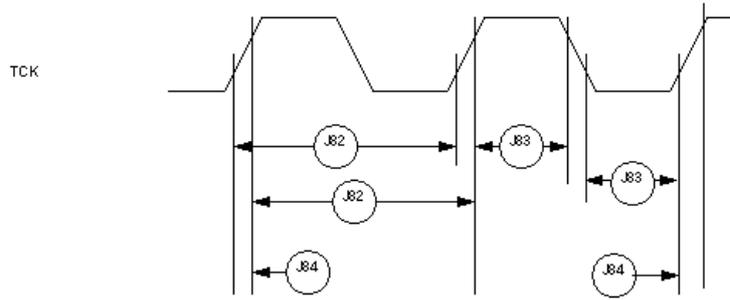


Figure 40 : JTAG-Test Access Port Timing Diagram

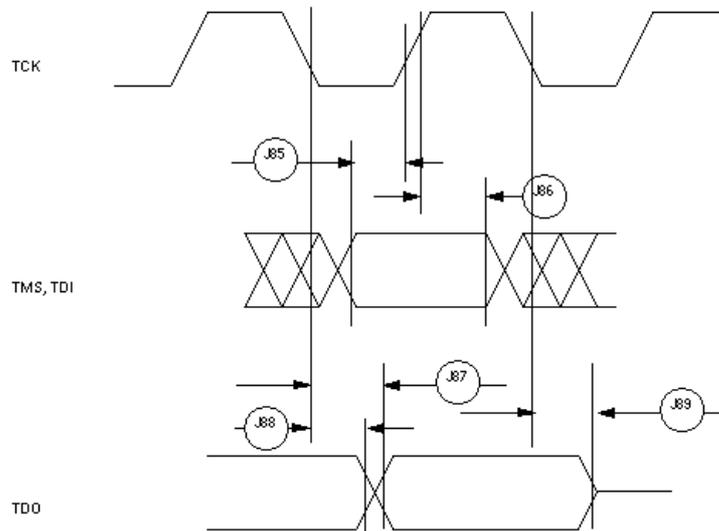


Figure 41 : JTAG-TRST Timing Diagram

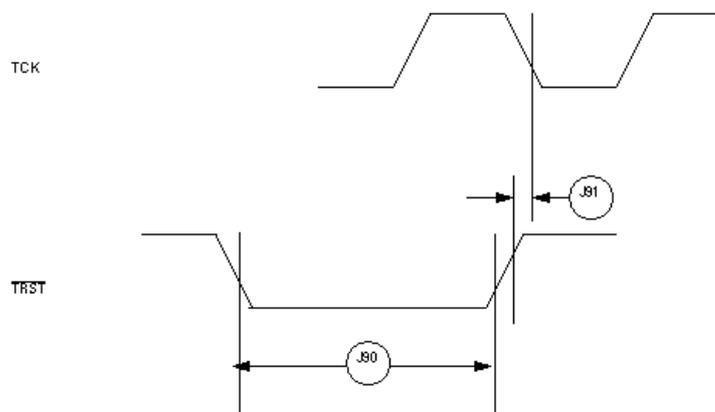
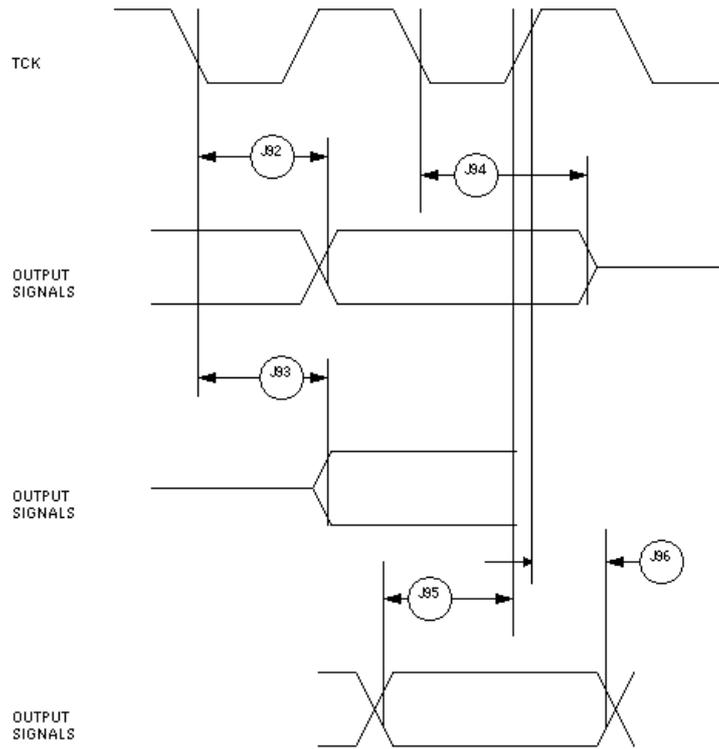


Figure 42 : Boundary Scan (JTAG) Timing Diagram



5. CPM ELECTRICAL CHARACTERISTICS

5.1. PIP/PIO AC Electrical Specifications

Table 12 : PIP/PIO Timing

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
21	Data-In Setup Time to STBI Low	0	—	ns
22	Data-In Hold Time to STBI High	2.5 – t3	—	clk
23	STBI Pulse Width	1.5	—	clk
24	STBO Pulse Width	1 clk 5ns	—	ns
25	Data-Out Setup Time to STBO Low	2	—	clk
26	Data-Out Hold Time from STBO High	5	—	clk
27	STBI Low to STBO Low (Rx Interlock)	—	2	clk
28	STBI Low to STBO High (Tx Interlock)	2	—	clk
29	Data-In Setup Time to Clock Low	15	—	ns
30	Data-In Hold Time from Clock Low	7.5	—	ns
31	Clock High to Data-Out Valid (CPU Writes Data, Control, or Direction)	—	25	ns
t3 = Specification 23				

Figure 43 : PIP RX (Interlock Mode) Timing Diagram

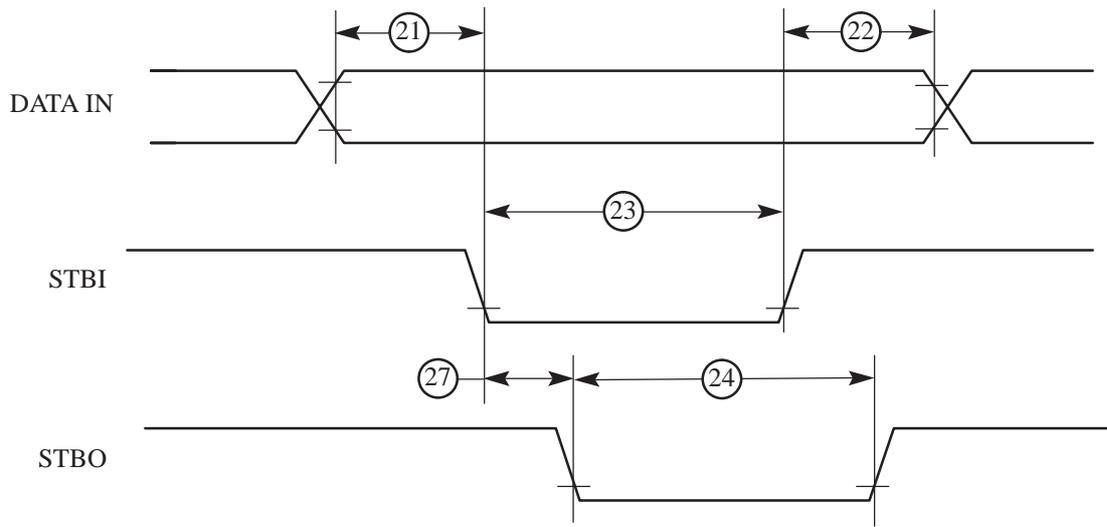


Figure 44 : PIP TX (Interlock Mode) Timing Diagram

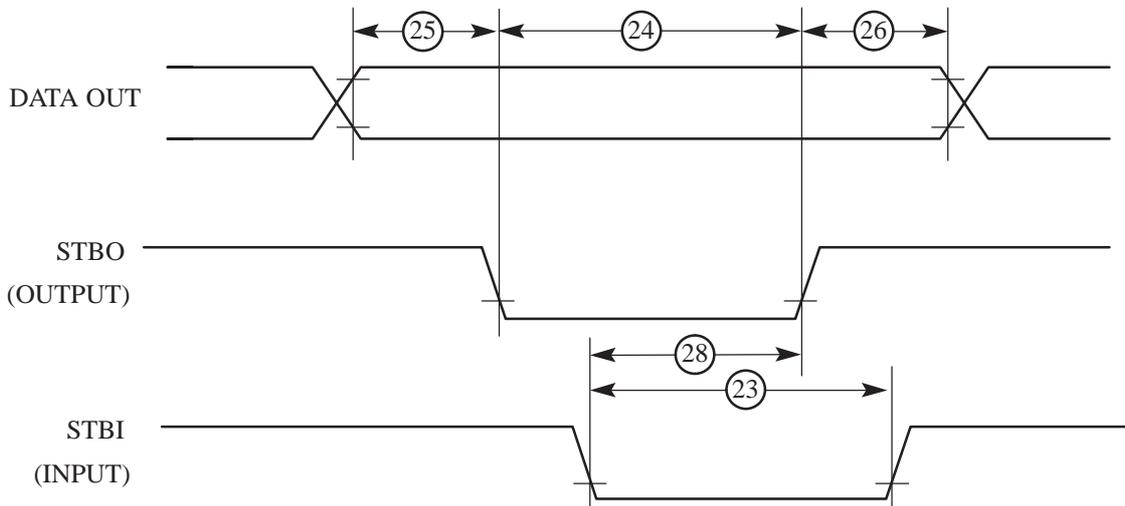


Figure 45 : PIP RX (Pulse Mode) Timing Diagram

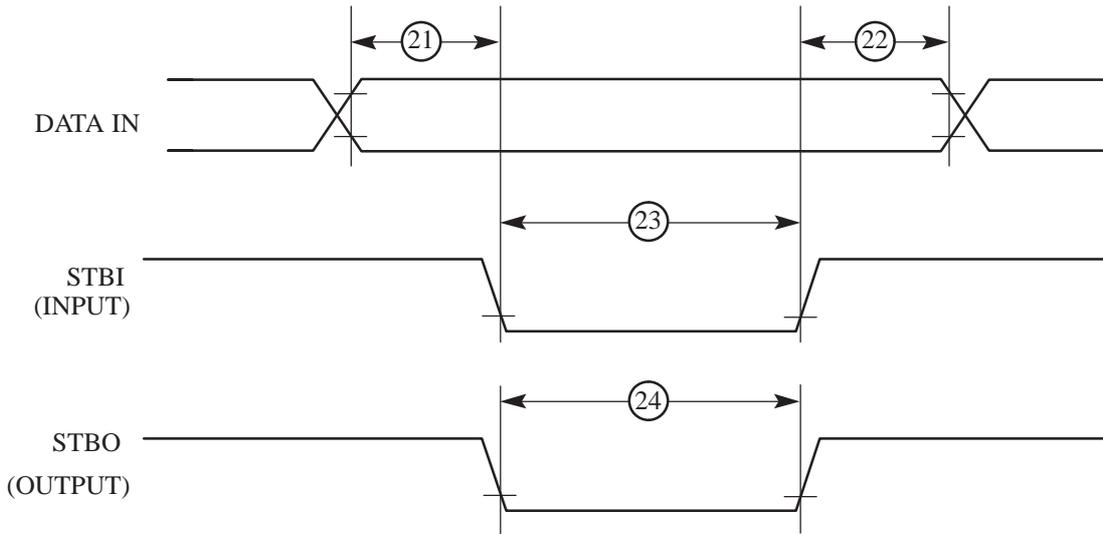


Figure 46 : PIP TX (Pulse Mode) Timing Diagram

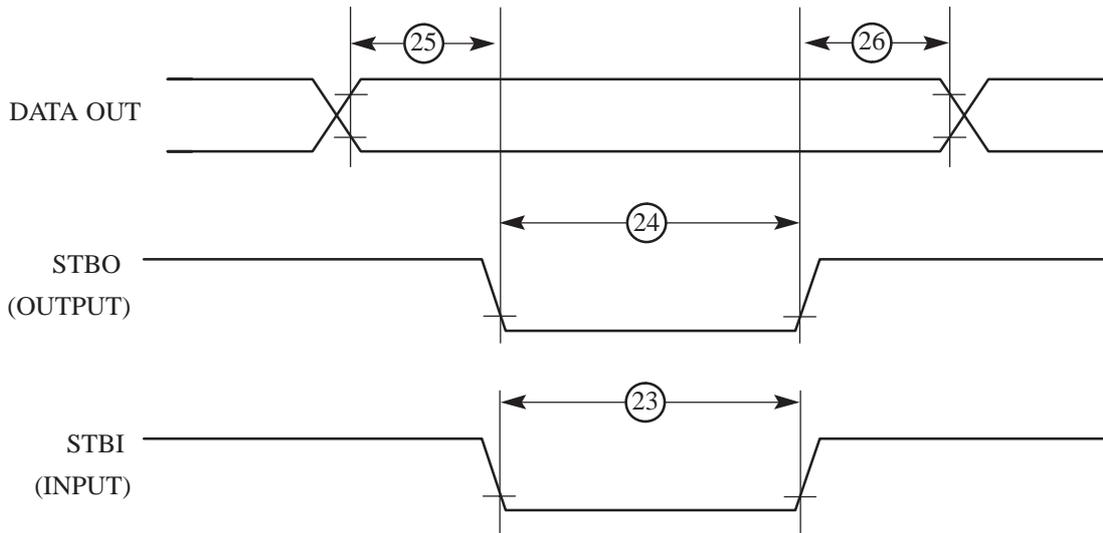
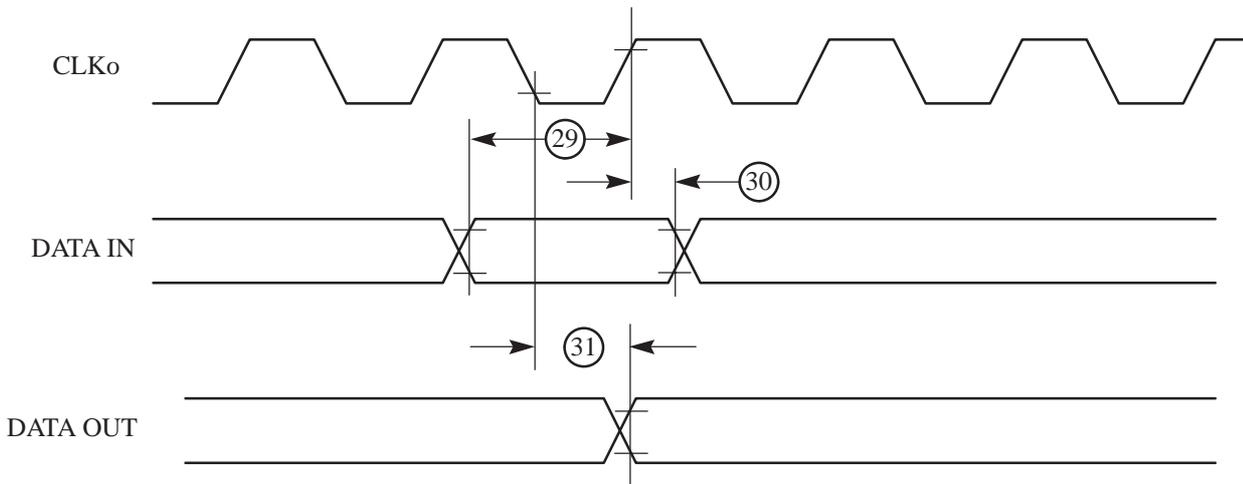


Figure 47 : Parallel I/O Data-In/Data-Out Timing Diagram



5.2. IDMA Controller AC Electrical Specifications

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
40	DREQ Setup Time to Clock High	7	—	ns
41	DREQ Hold Time from Clock High	3	—	ns
42	SDACK Assertion Delay from Clock High	—	12	ns
43	SDACK Negation Delay from Clock Low	—	12	ns
44	SDACK Negation Delay from TA Low	—	20	ns
45	SDACK Negation Delay from Clock High	—	15	ns
46	TA Assertion to Falling Edge of the Clock Setup Time *	7	—	ns
* Applies to external TA.				

Figure 48 : IDMA External Requests Timing Diagram

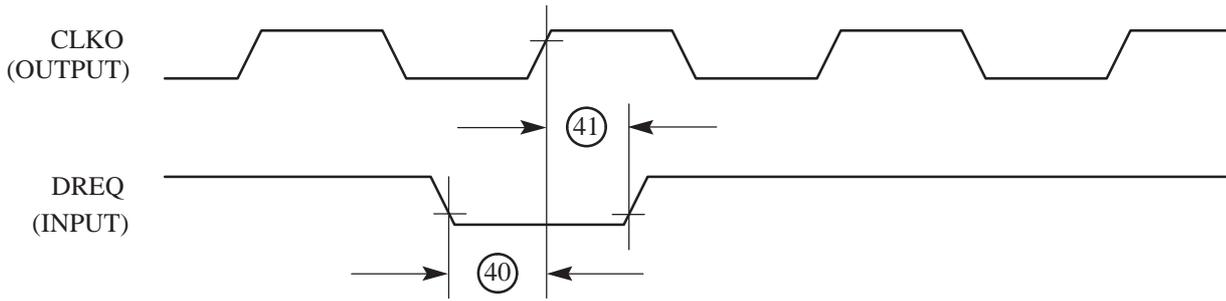


Figure 49 : SDACK Timing Diagram—Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

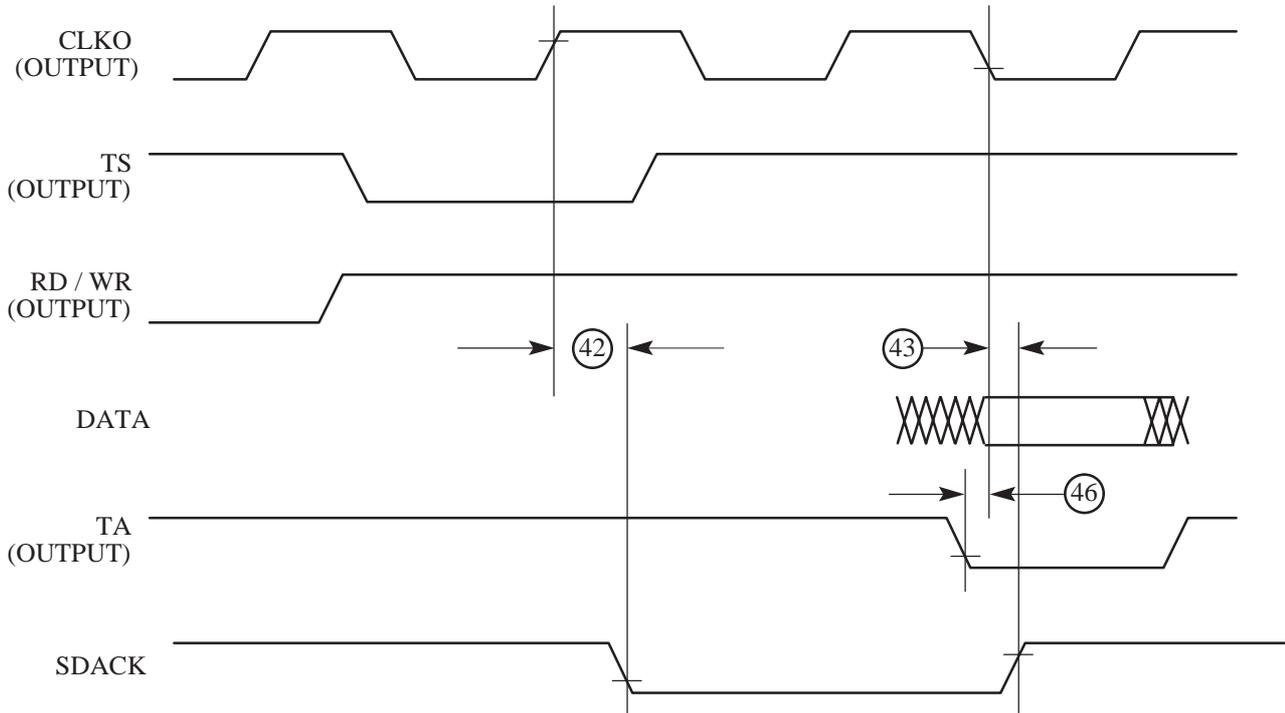


Figure 50 : SDACK Timing Diagram—Peripheral Write, TA Sampled High at the Falling Edge of the Clock

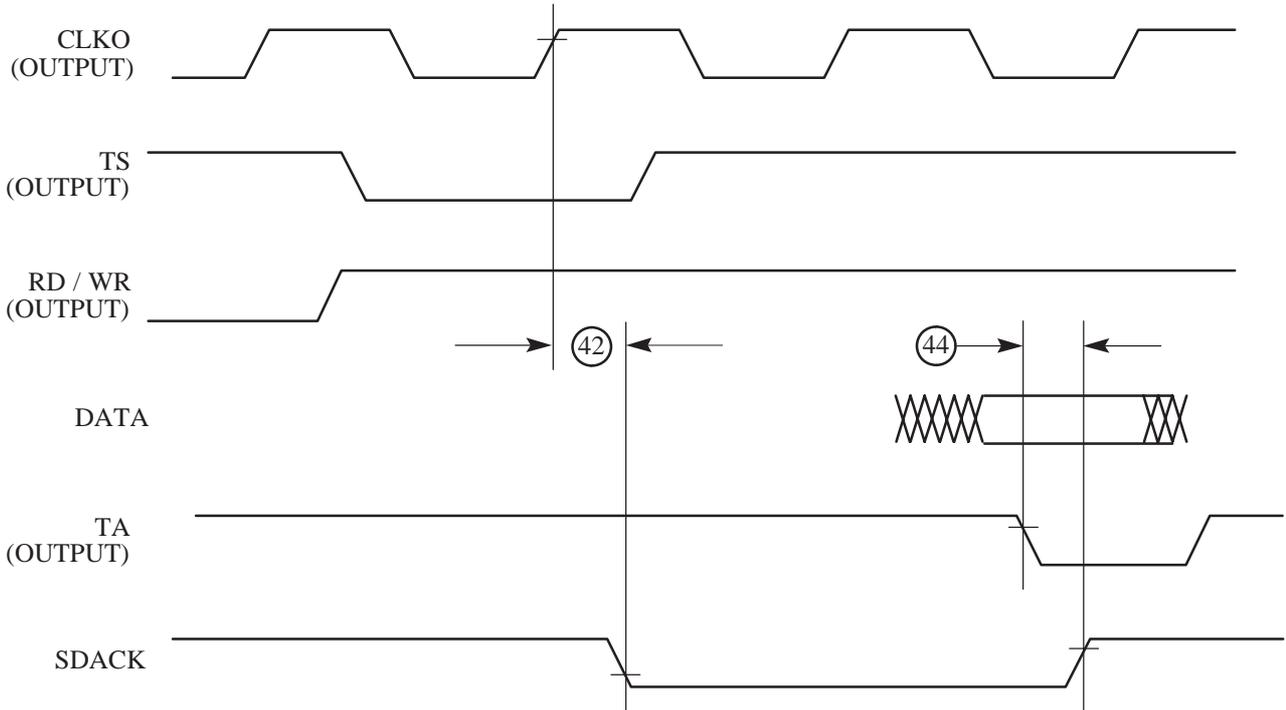
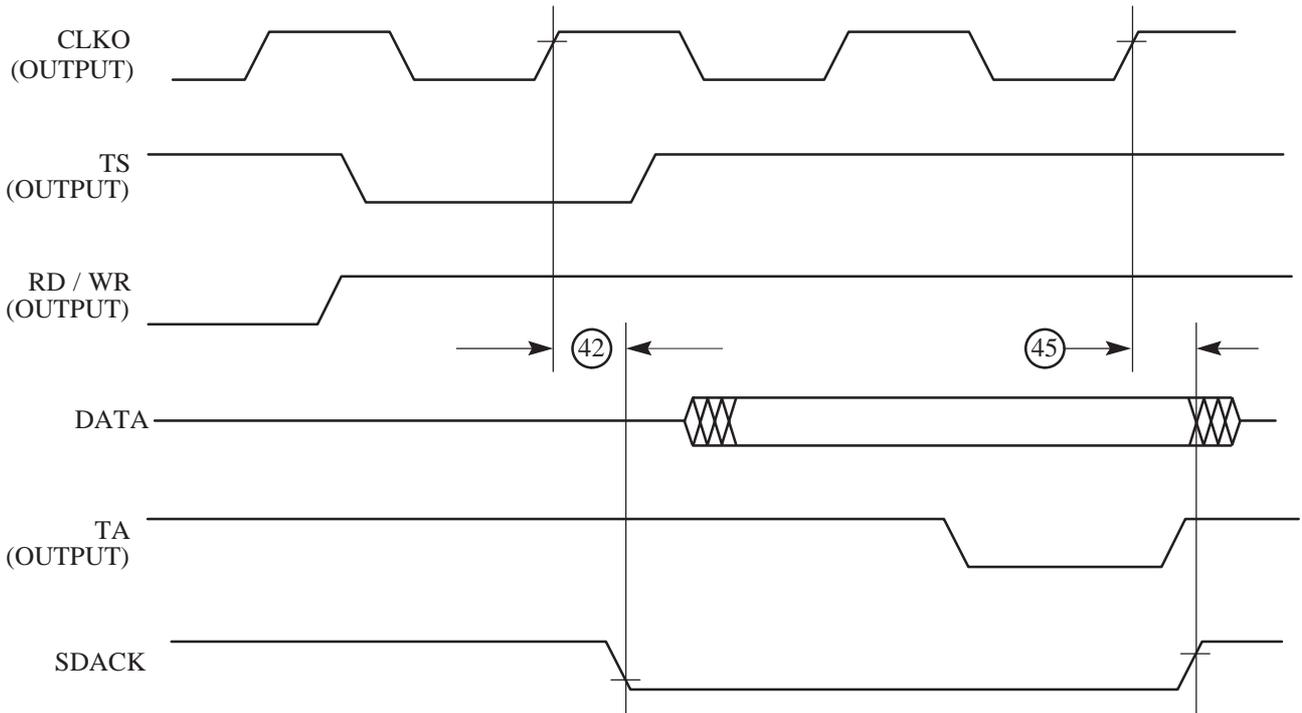


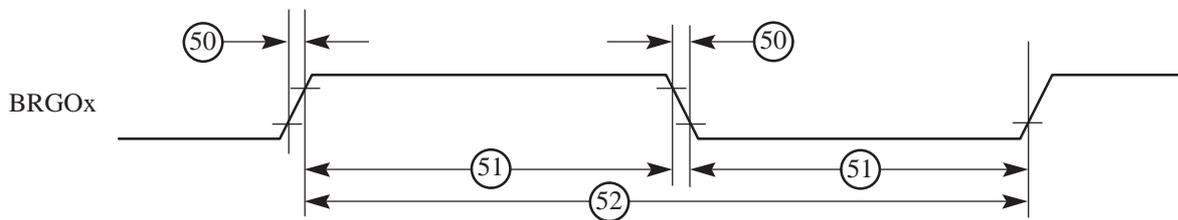
Figure 51 : SDACK Timing Diagram–Peripheral Read



5.3. Baud Rate Generator AC Electrical Specifications

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
50	BRGO Rise and Fall Time	—	10	ns
51	BRGO Duty Cycle	40	60	%
52	BRGO Cycle	40	—	ns

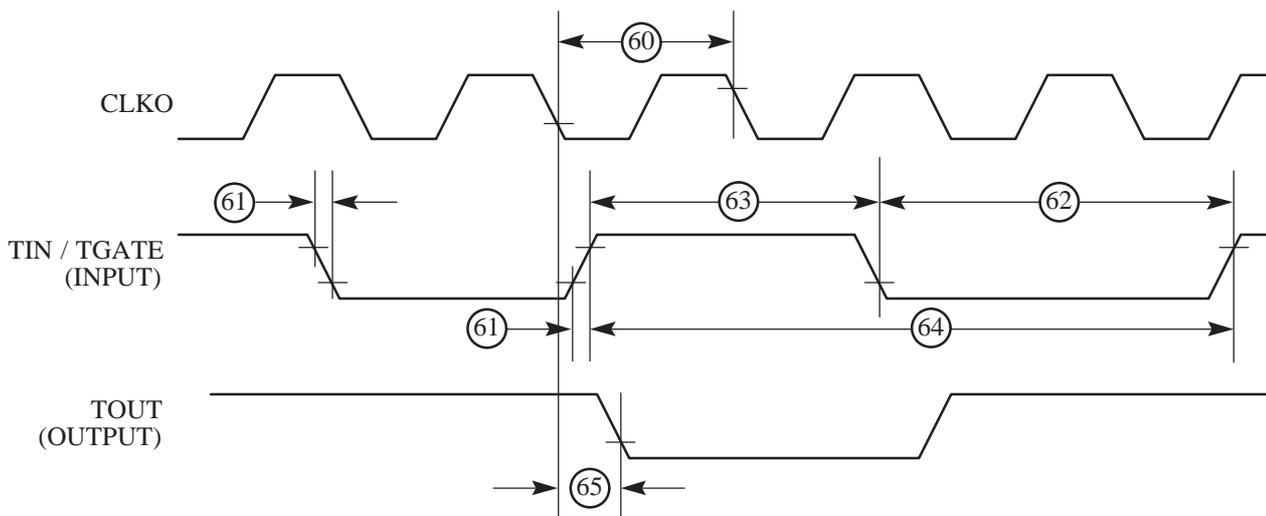
Figure 52 : Baud Rate Generator Timing Diagram



5.4. Timer AC Electrical Specifications

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
61	TIN/TGATE Rise and Fall Time	10	—	ns
62	TIN/TGATE Low Time	1	—	clk
63	TIN/TGATE High Time	2	—	clk
64	TIN/TGATE Cycle Time	3	—	clk
65	CLKO High to TOUT Valid	3	25	ns

Figure 53 : CPM General-Purpose Timers Timing Diagram



5.5. Serial Interface AC Electrical Specifications

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
70	L1RCLK, L1TCLK Frequency (DSC=0) ^{1 3}	—	SYNCCLK/2.5	MHz
71	L1RCLK, L1TCLK Width Low (DSC=0) ³	P+10		ns
71A	L1RCLK, L1TCLK Width High (DSC=0) ²	P+10	—	ns
72	L1TXD, L1ST(1–4), L1RQ, L1CLKO Rise/Fall Time	—	15	ns
73	L1RSYNC, L1TSYNC Valid to L1CLK Edge (SYNC Setup Time)	20	—	ns
74	L1CLK Edge to L1RSYNC, L1TSYNC Invalid (SYNC Hold Time)	35	—	ns
75	L1RSYNC, L1TSYNC Rise/Fall Time	—	15	ns
76	L1RXD Valid to L1CLK Edge (L1RXD Setup Time)	17	—	ns
77	L1CLK Edge to L1RXD Invalid (L1RXD Hold Time)	13	—	ns
78	L1CLK Edge to L1ST(1–4) Valid	10	45	ns
78A	L1SYNC Valid to L1ST(1–4) Valid ⁴	10	45	ns
79	L1CLK Edge to L1ST(1–4) Invalid	10	45	ns
80	L1CLK Edge to L1TXD Valid	10	55	ns
80A	L1TSYNC Valid to L1TXD Valid ⁴	10	55	ns
81	L1CLK Edge to L1TXD High Impedance	0	42	ns
82	L1RCLK, L1TCLK Frequency (DSC=1)	—	16 or SYNCCLK/2	MHz
83	L1RCLK, L1TCLK Width Low (DSC=1)	P+10	—	ns
83A	L1RCLK, L1TCLK Width High (DSC=1) ²	P+10	—	ns

		MIN	MAX	
84	L1CLK Edge to L1CLKO Valid (DSC=1)	—	30	ns
85	L1RQ Valid Before Falling Edge of L1TSYNC 4	1	—	L1TCLK
86	L1GR Setup Time (See Note 3)	42	—	ns
87	L1GR Hold Time	42	—	ns
88	L1CLK Edge to L1SYNC Valid (FSD = 00, CNT = 0000, BYT = 0, DSC=0)	—	0	ns

1. The ratio SyncCLK/L1RCLK must be greater than 2.5/1.
2. Where $P=1/CLKO1$. Thus for a 25 MHz CLKO1 rate, $P= 40$ ns.
3. These specs are valid for IDL mode only.
4. The strobes and Txd on the first bit of the frame becomes valid after L1CLK edge or L1SYNC, whichever is later.

Figure 54 : SI Receive Timing Diagram With Normal Clocking (DSC =0)

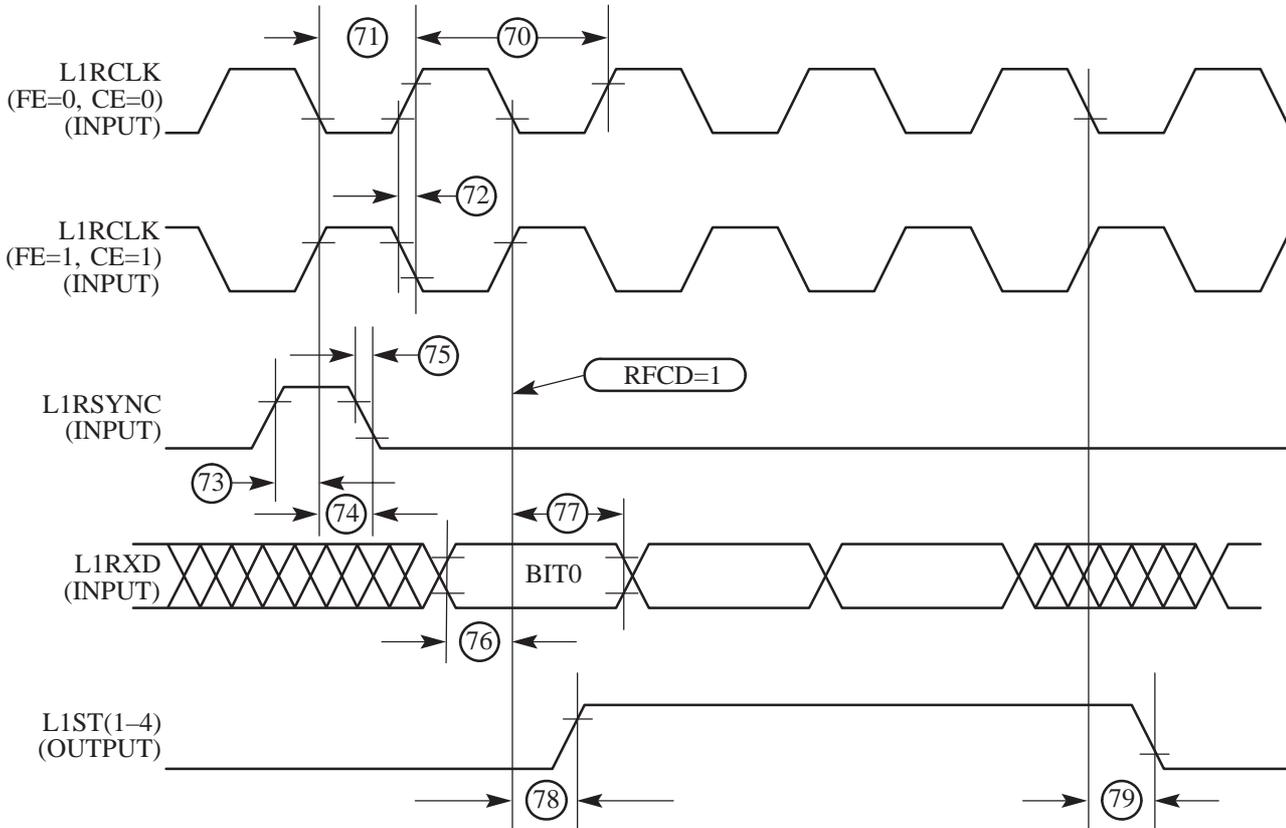


Figure 55 : SI Transmit Timing Diagram

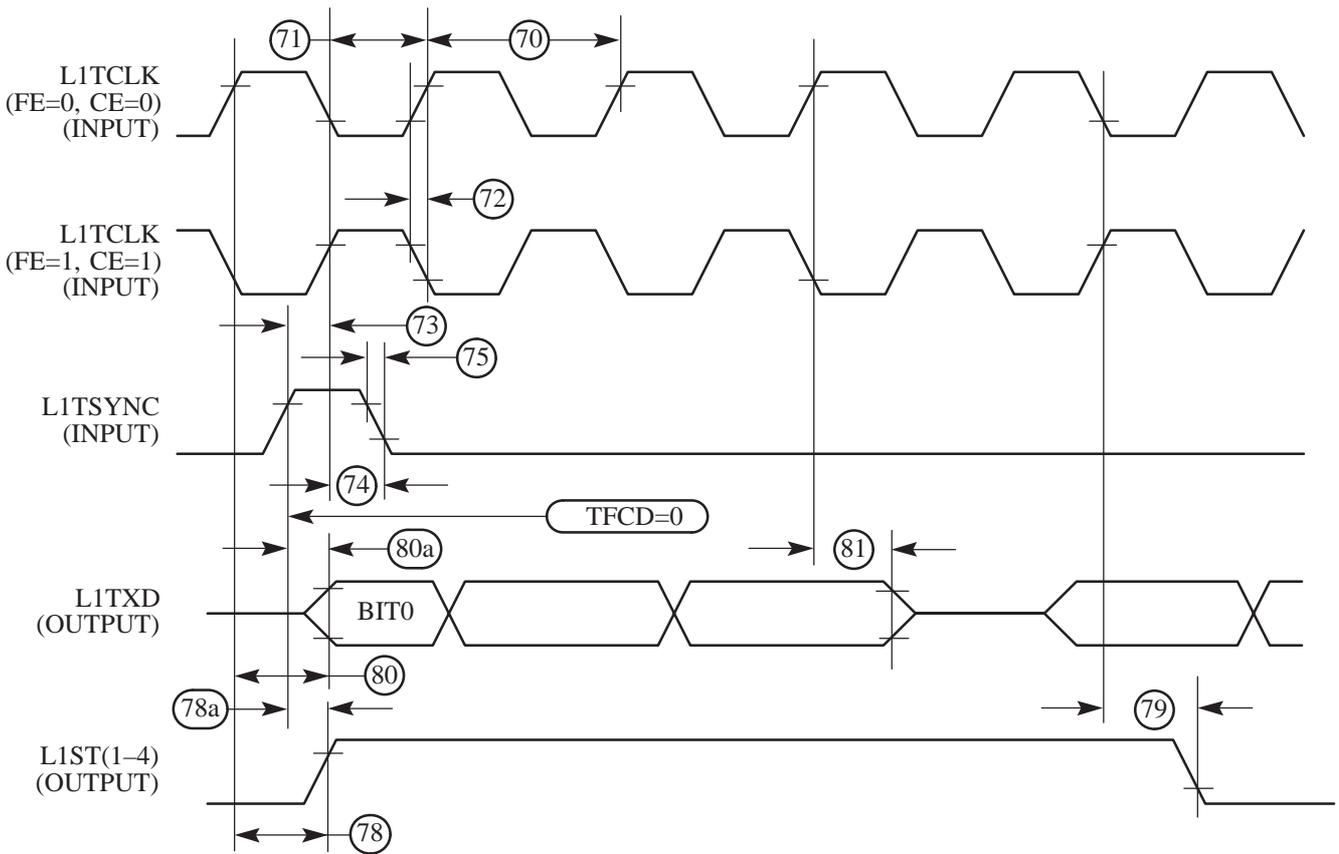
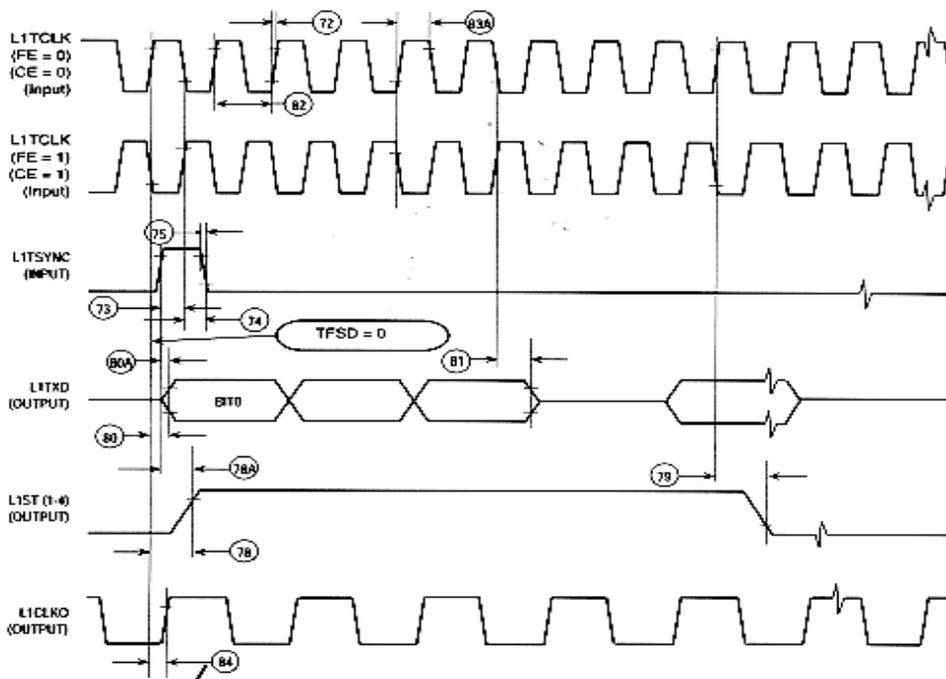


Figure 56 : SI Transmit Timing with Double Speed Clocking (DSC = 1)



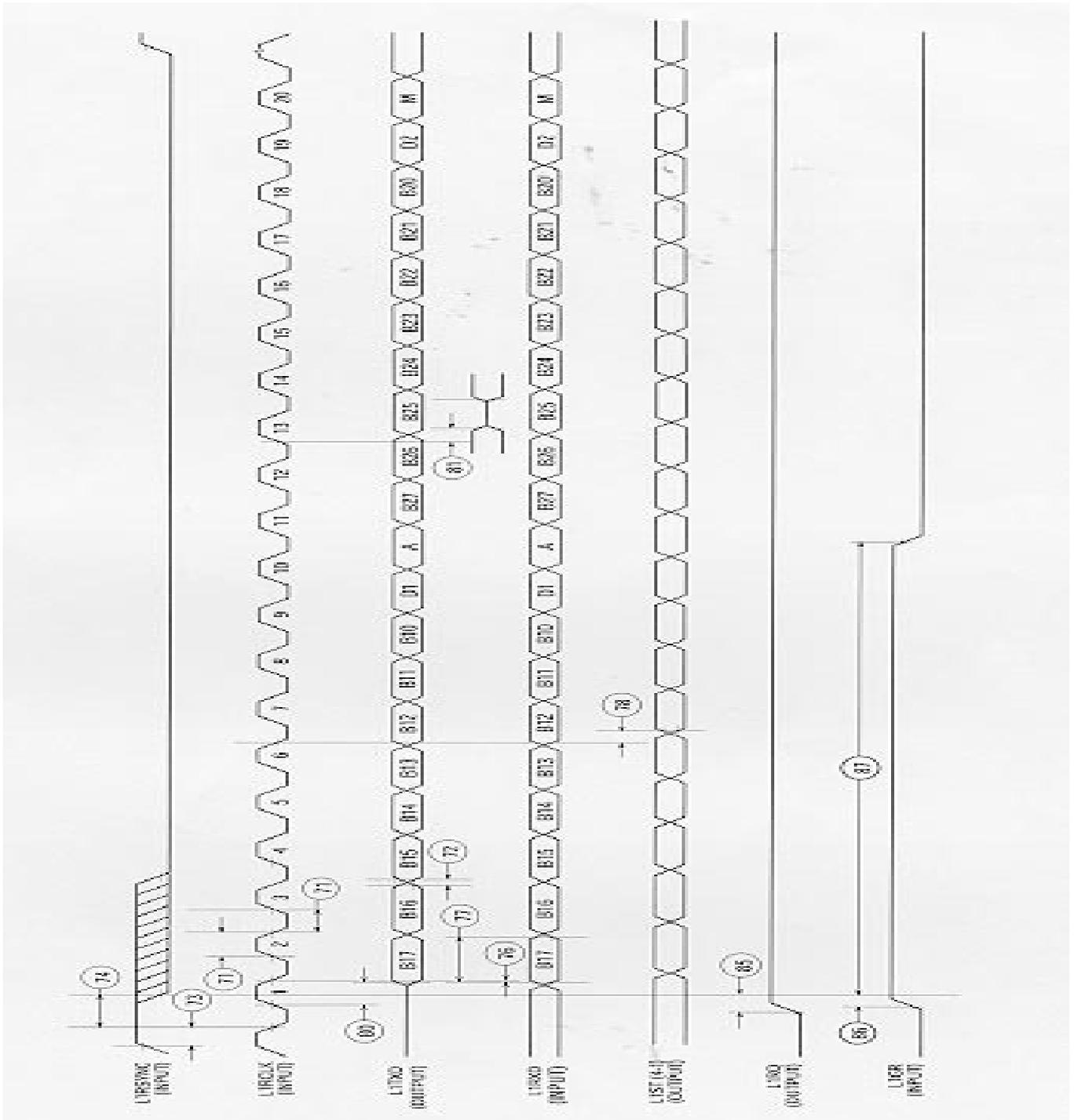


Figure 57 : IDL Timing

5.6. SCC In NMSI Mode—External Clock Electrical Specifications

The electrical specifications in this document are preliminary.

NUM	CHARACTERISTIC	40 MHZ / 50 MHZ		UNIT
		MIN	MAX	
100	RCLK1 and TCLK1 Width High16	1/SYNCCLK	—	ns
101	RCLK1 and TCLK1 Width Low	1/SYNCCLK+5	—	ns
102	RCLK1 and TCLK1 Rise/Fall Time	—	15	ns
103	TXD1 Active Delay (From TCLK1 Falling Edge)	0	50	ns
104	RTS1 Active/Inactive Delay (From TCLK1 Falling Edge)	0	50	ns
105	CTS1 Setup Time to TCLK1 Rising Edge	5	—	ns
106	RXD1 Setup Time to RCLK1 Rising Edge	5	—	ns
107	RXD1 Hold Time from RCLK1 Rising Edge 2	5	—	ns
108	CD1 Setup Time to RCLK1 Rising Edge	5	—	ns
<ol style="list-style-type: none"> 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1. 2. Also applies to CD and CTS hold time when they are used as an external sync signals. 				

5.7. SCC In NMSI Mode—Internal Clock Electrical Specifications

The electrical specifications in this document are preliminary.

Table 13 : *NMSI External Clock Timing*

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
100	RCLK1 and TCLK1	0	SYNOCLK/3	MHz
102	RCLK1 and TCLK1 Rise/Fall Time	—	—	ns
103	TXD1 Active Delay (From TCLK1 Falling Edge)	0	30	ns
104	$\overline{\text{RTS1}}$ Active/Inactive Delay (From TCLK1 Falling Edge)	0	30	ns
105	$\overline{\text{CTS1}}$ Setup Time to TCLK1 Rising Edge	40	—	ns
106	RXD1 Setup Time to RCLK1 Rising Edge	40	—	ns
107	RXD1 Hold Time from RCLK1 Rising Edge 2	0	—	ns
108	$\overline{\text{CD1}}$ Setup Time to RCLK1 Rising Edge	40	—	ns
<ol style="list-style-type: none"> 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1 2. Also applies to CD and CTS hold time when they are used as an external sync signals. 				

Table 14 : NMSI Internal Clock Timing

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
100	RCLK1 and TCLK1width high ¹	1 /SYNCCLK		ns
101	RCLK1 and TCLK1width low	1/ SYNCCLK +5	15	ns
102	RCLK1 and TCLK1 Rise/Fall Time	—	—	ns
103	TXD1 Active Delay (From TCLK1 Falling Edge)	0	50	ns
104	$\overline{RTS1}$ Active/Inactive Delay (From TCLK1 Falling Edge)	0	50	ns
105	$\overline{CTS1}$ Setup Time to TCLK1 Rising Edge	5	—	ns
106	RXD1 Setup Time to RCLK1 Rising Edge	5	—	ns
107	RXD1 Hold Time from RCLK1 Rising Edge ²	5	—	ns
108	$\overline{CD1}$ Setup Time to RCLK1 Rising Edge	5	—	ns
<p>1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1</p> <p>2. Also applies to CD and CTS hold time when they are used as an external sync signals.</p>				

Figure 58 : SCC NMSI Receive Timing Diagram

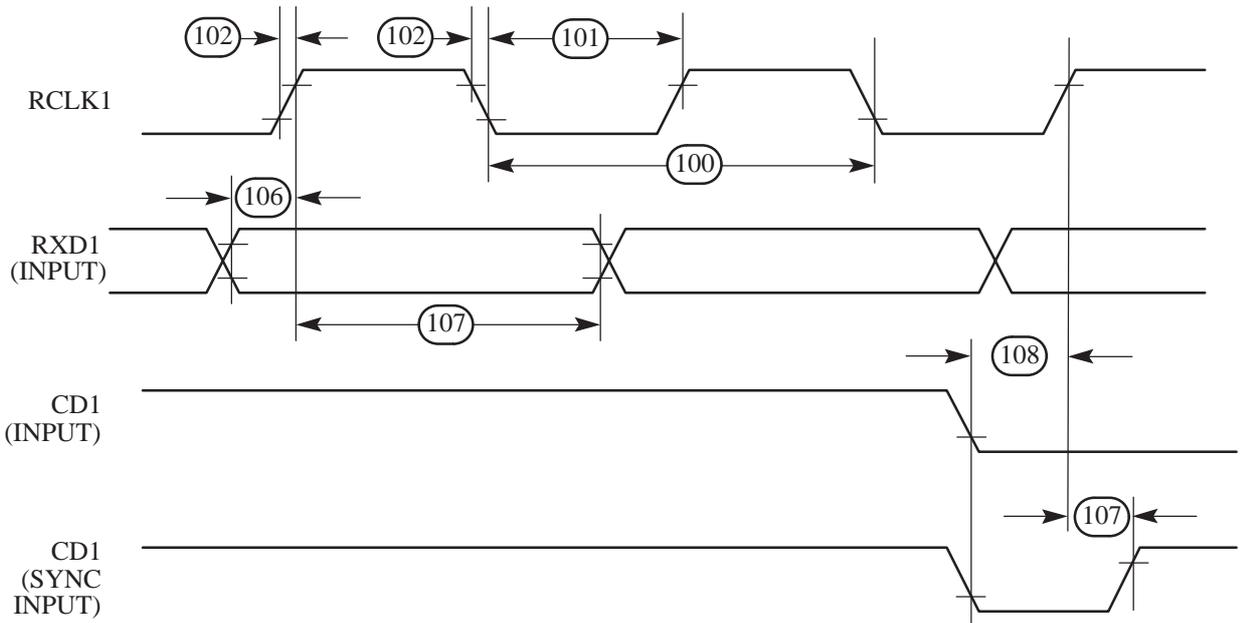


Figure 59 : SCC NMSI Transmit Timing Diagram

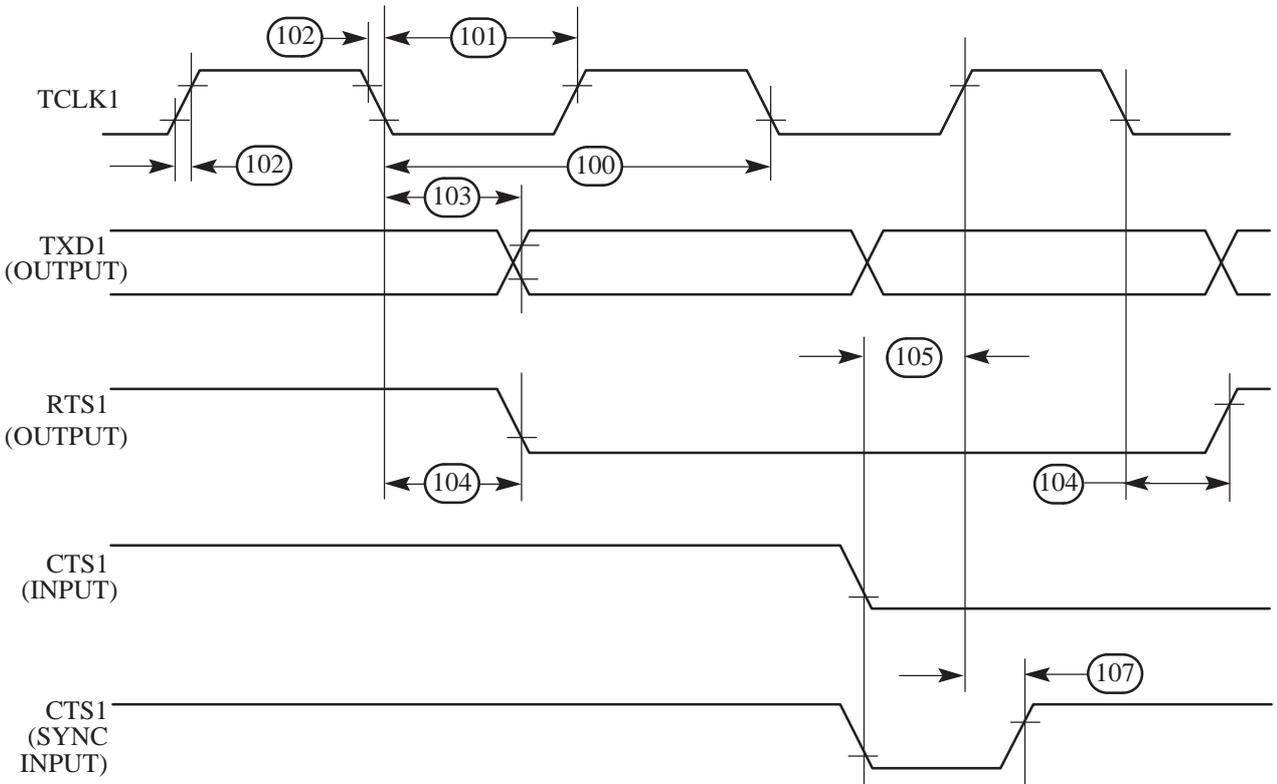
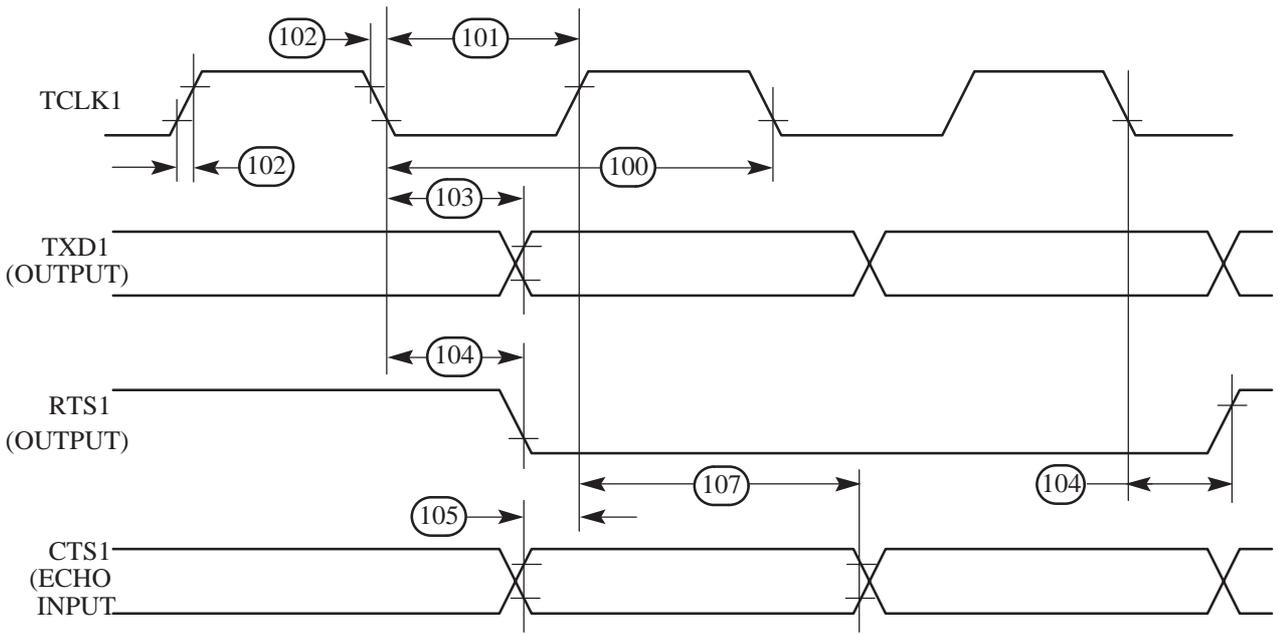


Figure 60 : HDLC Bus Timing Diagram



5.8. Ethernet Electrical Specifications

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
120	CLSN Width High	40	—	ns
121	RCLK1 Rise/Fall Time	—	15	ns
122	RCLK1 Width Low	40	—	ns
123	RCLK1 Clock Period (See note 1)	80	120	ns
124	RXD1 Setup Time	20	—	ns
125	RXD1 Hold Time	5	—	ns
126	RENA Active Delay (From RCLK1 Rising Edge of the Last Data Bit)	10	—	ns
127	RENA Width Low	100	—	ns
128	TCLK1 Rise/Fall Time	—	15	ns
129	TCLK1 Width Low	40	—	ns
130	TCLK1 Clock Period (See note 1)	99	101	ns
131	TXD1 Active Delay (From TCLK1 Rising Edge)	10	50	ns
132	TXD1 Inactive Delay (From TCLK1 Rising Edge)	10	50	ns
133	TENA Active Delay (From TCLK1 Rising Edge)	10	50	ns
134	TENA Inactive Delay (From TCLK1 Rising Edge)	10	50	ns
135	RSTRT Active Delay (From TCLK1 Falling Edge)	10	50	ns
136	RSTRT Inactive Delay (From TCLK1 Falling Edge)	10	50	ns
137	REJECT Width Low	1	—	CLK
138	CLKO1 Low to SDACK Asserted (See note 2)	—	20	ns
139	CLKO1 Low to SDACK Negated (See note 2)	—	20	ns

Notes : 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1

2. SDACK is asserted whenever the SDMA writes the incoming frame DA into memory.1.

Figure 61 : Ethernet Collision Timing Diagram

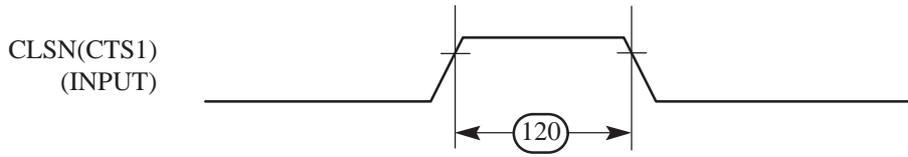


Figure 62 : Ethernet Receive Timing Diagram

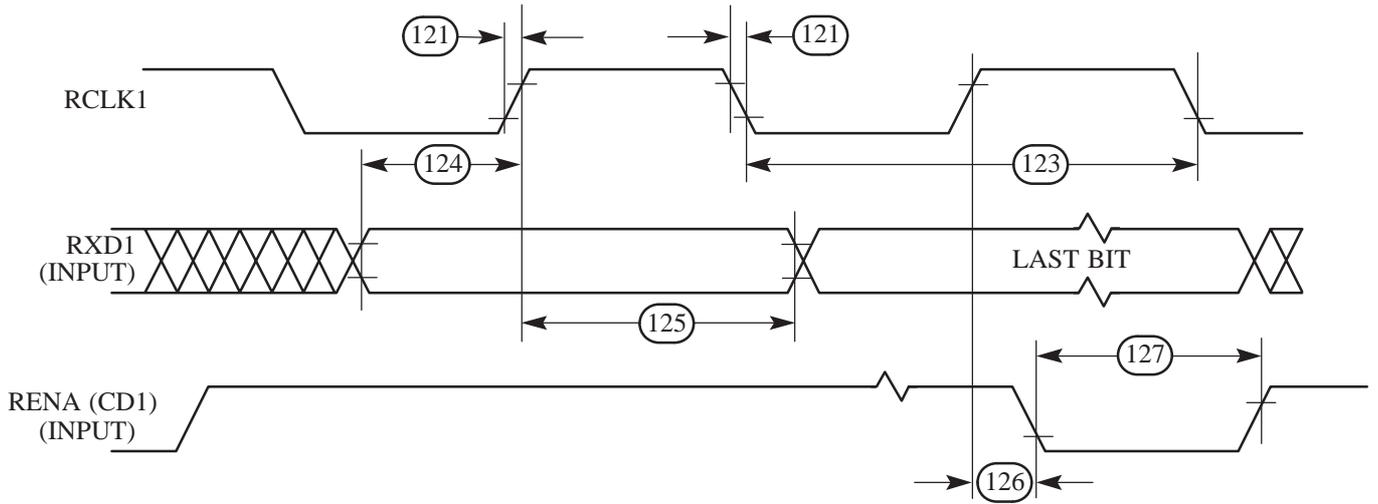
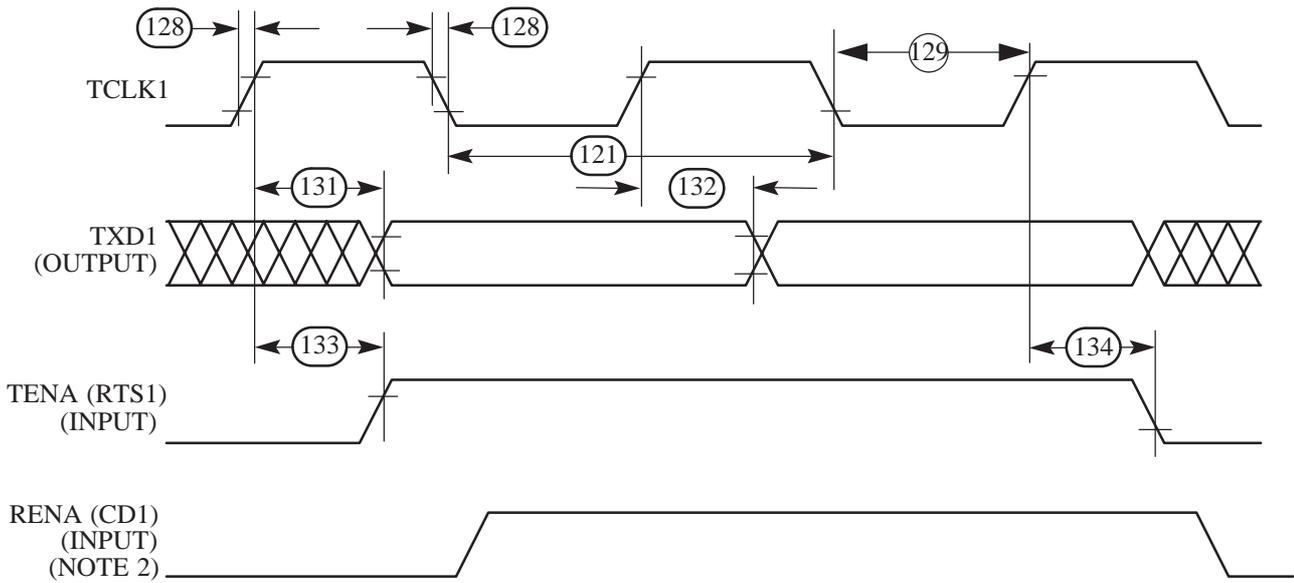


Figure 63 : Ethernet Transmit Timing Diagram



- Notes :
1. Transmit clock invert (TCI) bit in GSMR is set.
 2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

Figure 64 : CAM Interface Receive Start Timing Diagram

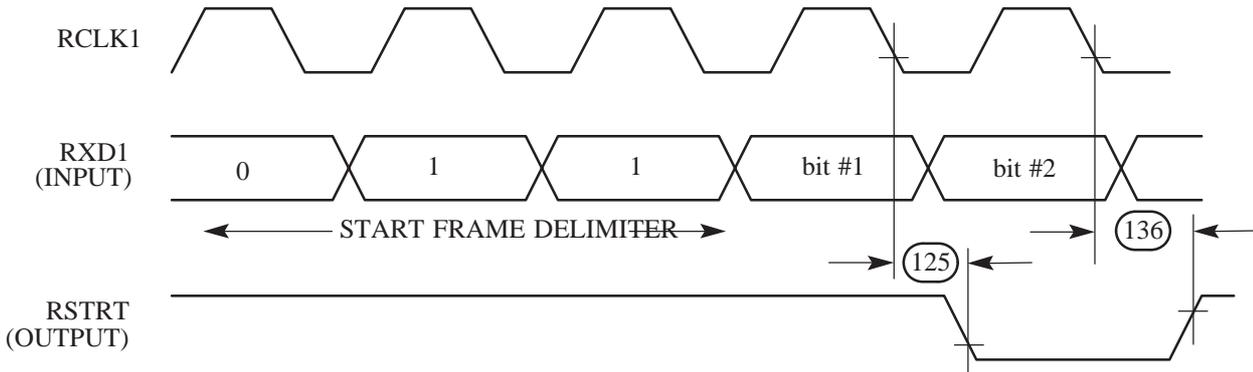
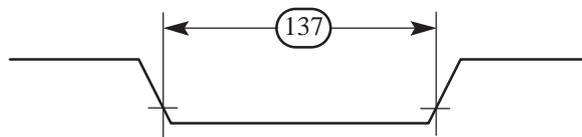


Figure 65 : CAM Interface Reject Timing Diagram

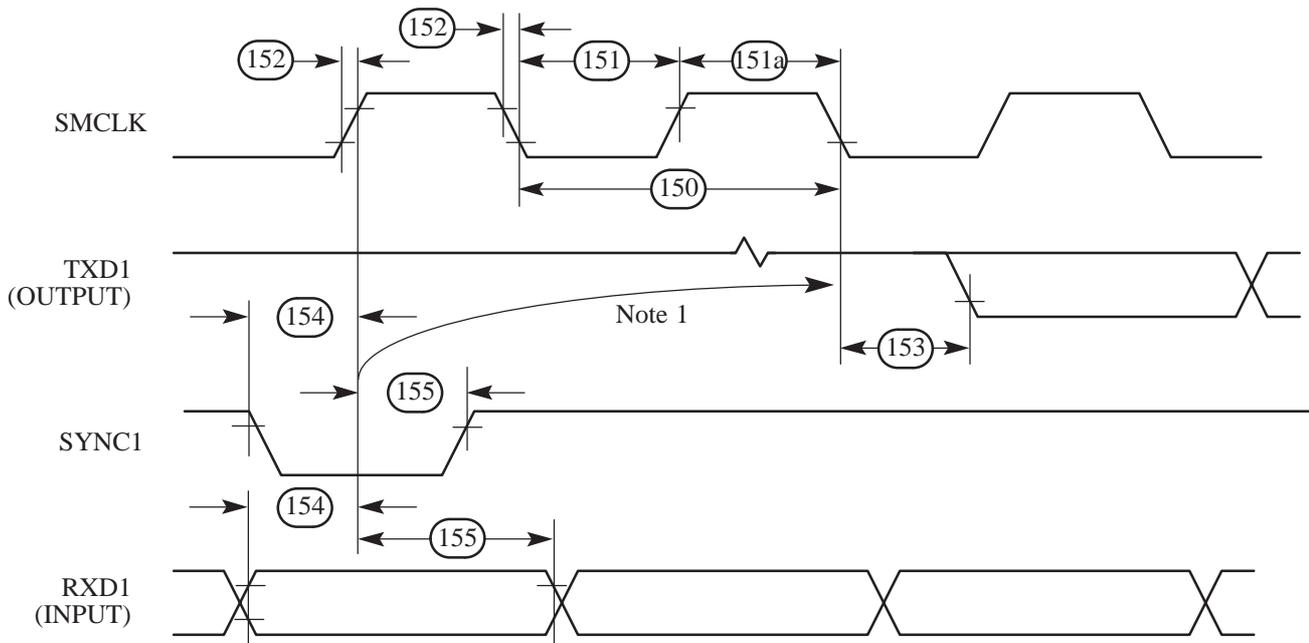


5.9. I2C AC Electrical Specifications—SCL < 100 KHz

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
150	CLK1 Clock Period *	100	—	ns
151	CLK1 Width Low	50	—	ns
151A	CLK1 Width High	50	—	ns
152	CLK1 Rise/Fall Time	—	15	ns
153	TXD1 Active Delay (From CLK1 Falling Edge)	10	50	ns
154	RXD1/SYNC1 Setup Time	20	—	ns
155	RXD1/SYNC1 Hold Time	5	—	ns

NOTE : * The ratio SyncCLK/SMCLK must be greater or equal to 2/1.

Figure 66 : SMC Transparent Timing Diagram



Note:1.This delay is equal to an integer number of "character length" clocks



5.10. SPI Master AC Electrical Specifications

NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
160	Master Cycle Time	4	1024	tcyc
161	Master Clock (SCK) High or Low Time	2	512	tcyc
162	Master Data Setup Time (Inputs)	50	—	ns
163	Master Data Hold Time (Inputs)	0	—	ns
164	Master Data Valid (After SCK Edge)	—	20	ns
165	Master Data Hold Time (Outputs)	0	—	ns
166	Rise Time Output	—	15	ns
167	Fall Time Output	—	15	ns

Figure 67 : SPI Master (CP=0) Timing Diagram

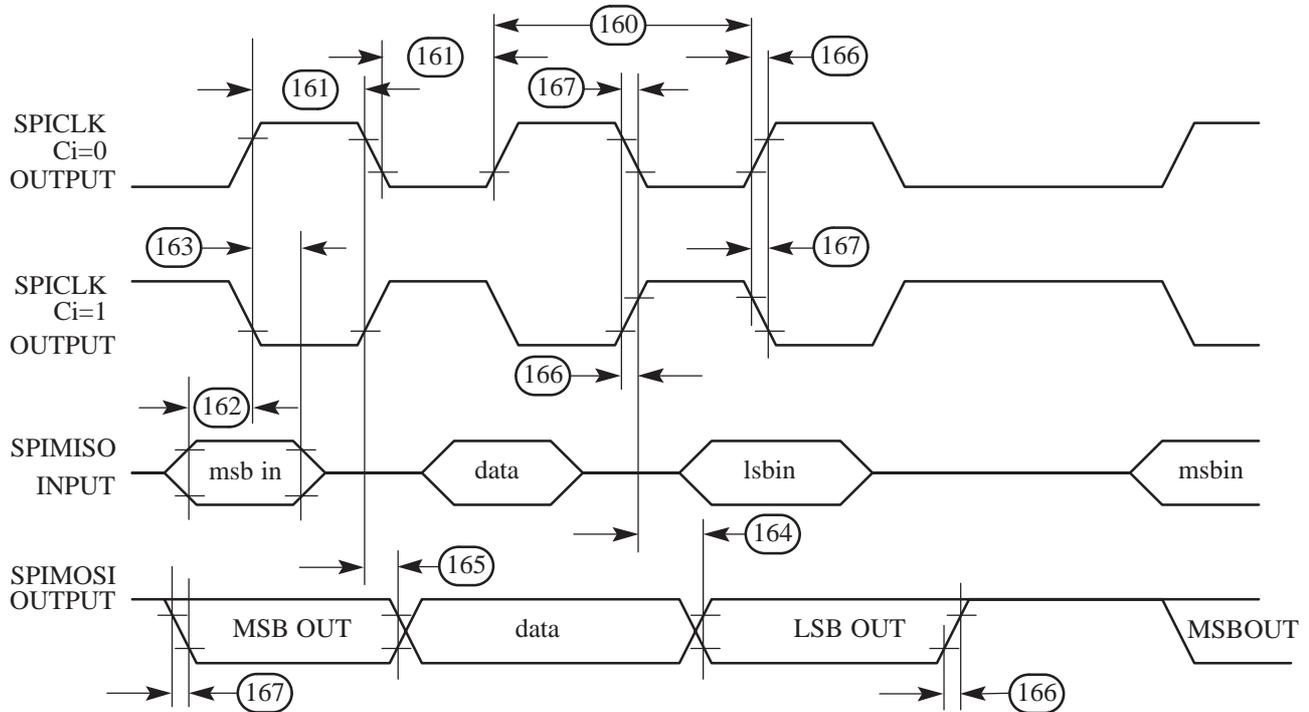
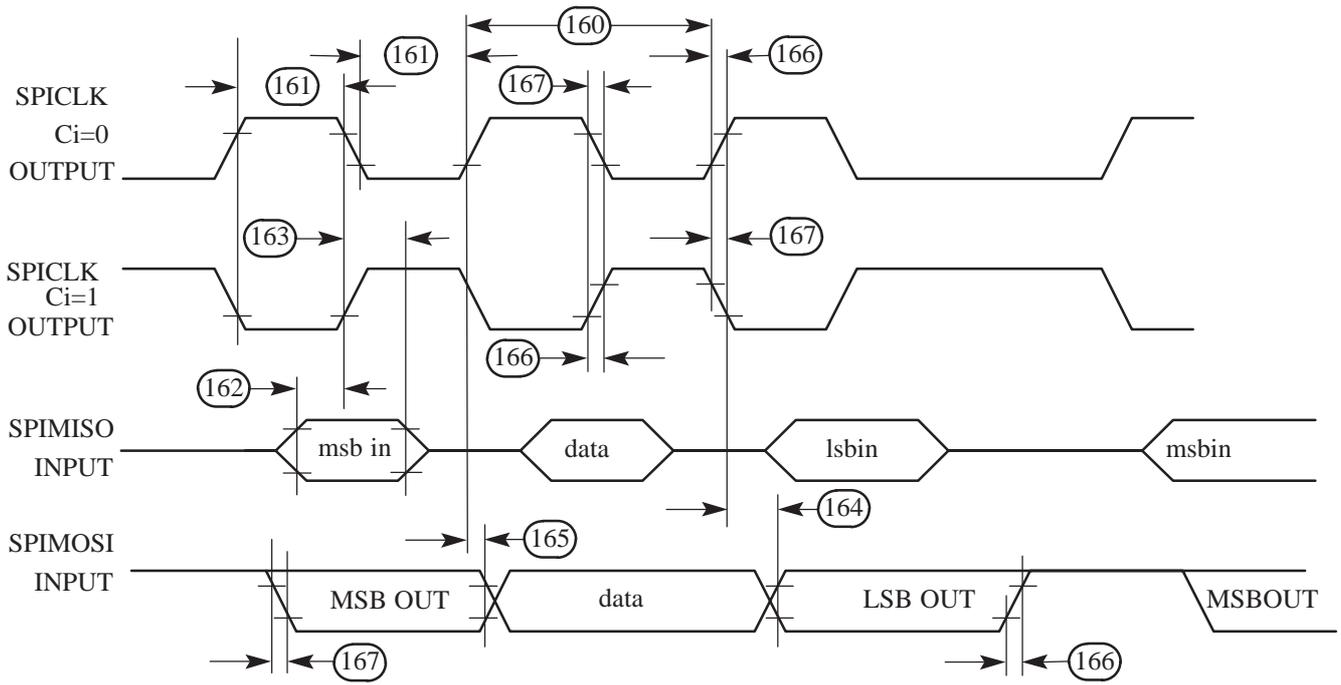


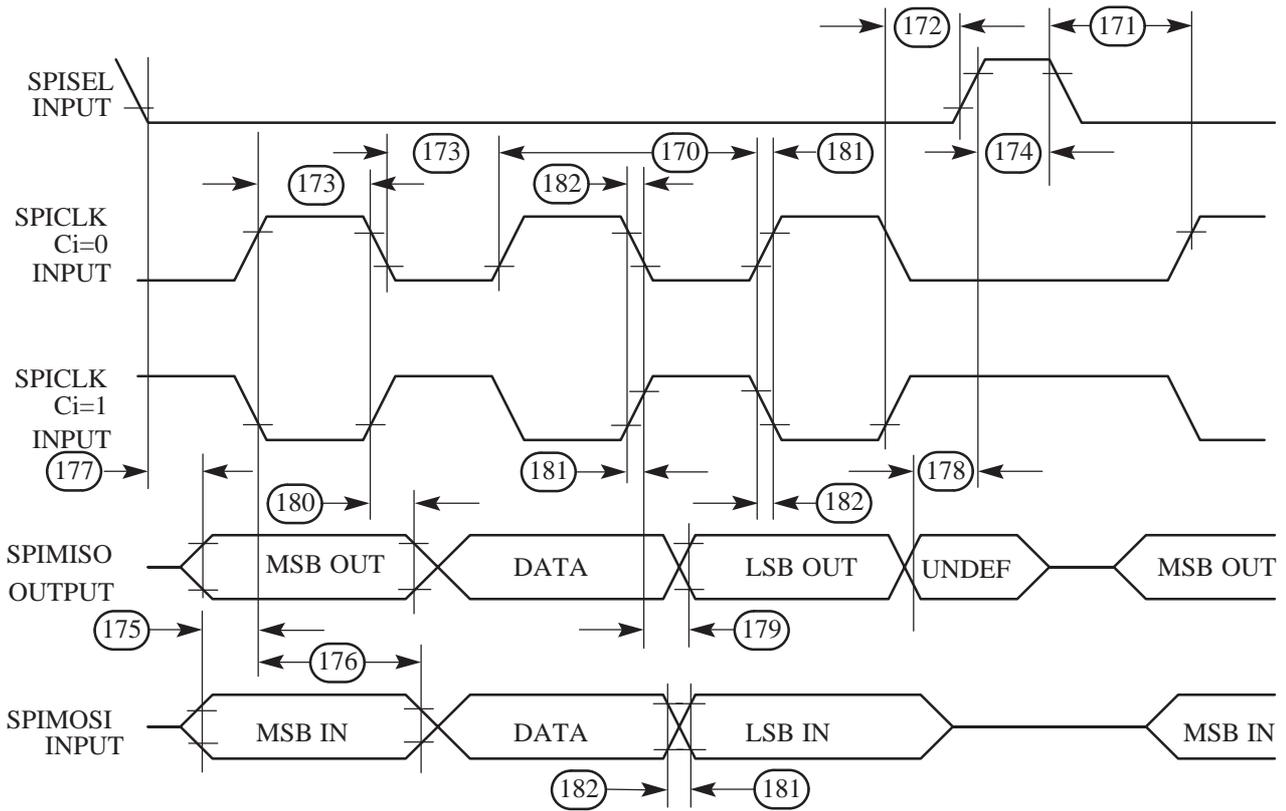
Figure 68 : SPI Master (CP=1) Timing Diagram



5.11. SPI Slave AC Electrical Specifications

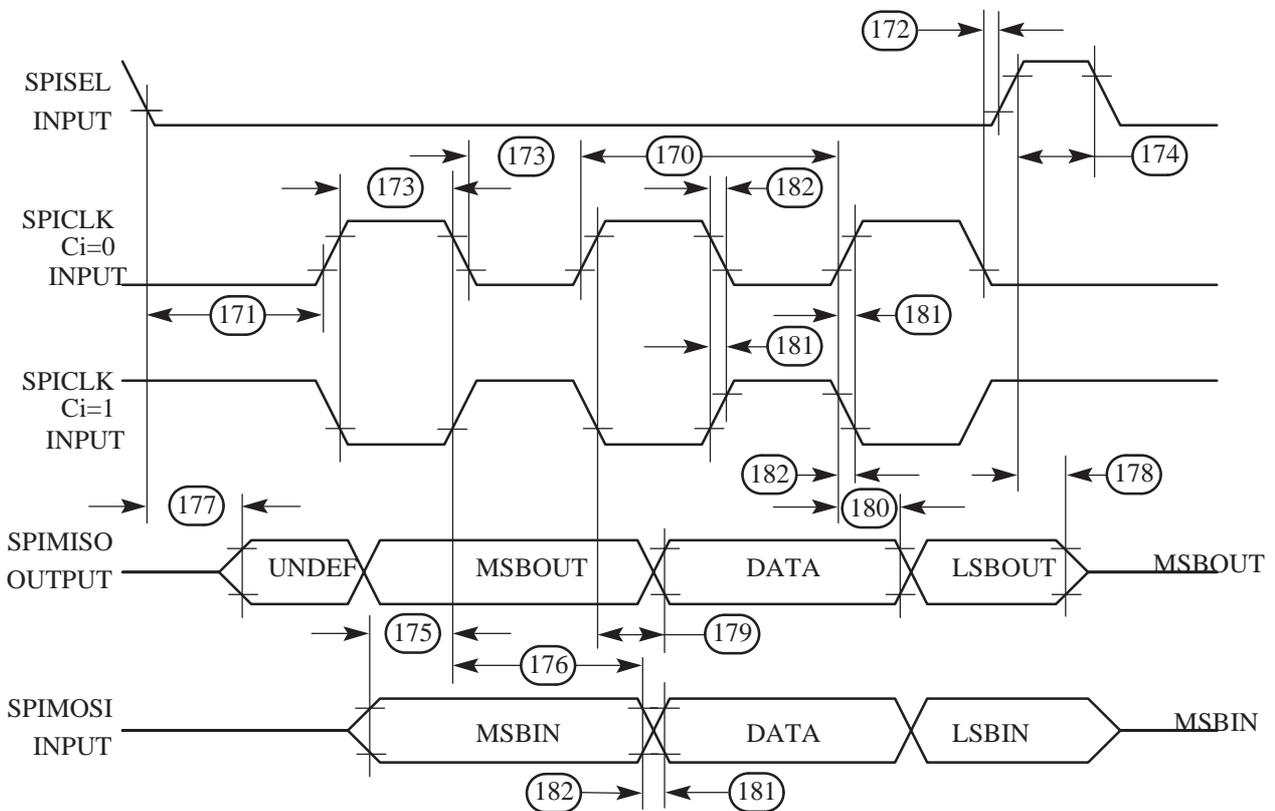
NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
170	Slave Cycle Time	2	—	tcyc
171	Slave Enable Lead Time	15	—	ns
172	Slave Enable Lag Time	15	—	ns
173	Slave Clock (SPICLK) High or Low Time	1	—	tcyc
174	Slave Sequential Transfer Delay (Does Not Require Deselect)	1	—	tcyc
175	Slave Data Setup Time (Inputs)	20	—	ns
176	Slave Data Hold Time (Inputs)	20	—	ns
177	Slave Access Time	—	50	ns

Figure 69 : SPI Slave (CP=0) Timing Diagram



33

Figure 70 : SPI Slave (CP=1) Timing Diagram





5.12. I²C AC Electrical Specifications–SCL < 100 KHz

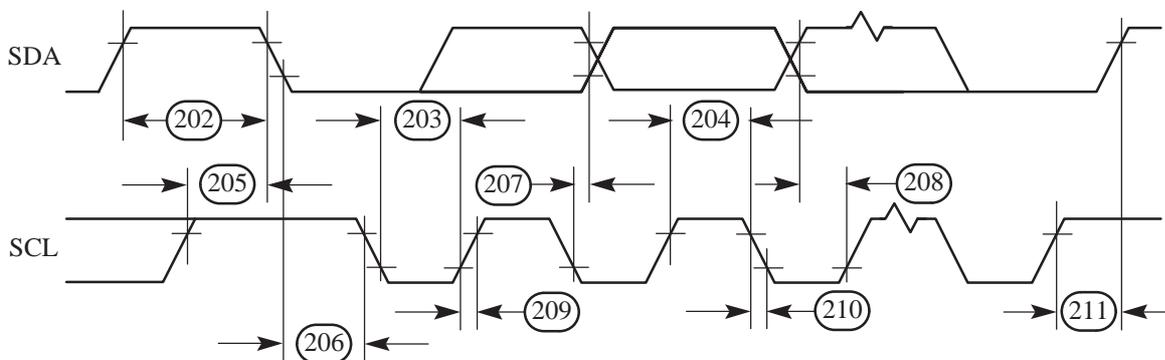
NUM	CHARACTERISTIC	ALL FREQUENCIES		UNIT
		MIN	MAX	
200	SCL Clock Frequency (SLAVE)	0	100	KHz
200	SCL Clock Frequency (MASTER) *	1.5	100	KHz
202	Bus Free Time Between Transmissions	4.7	—	μs
203	LOW Period of SCL	4.7	—	μs
204	HIGH Period of SCL	4.0	—	μs
205	START Condition Setup Time	4.7	—	μs
206	START Condition Hold Time	4.0	—	μs
207	DATA Hold Time	0	—	μs
208	DATA Setup Time	250	—	ns
209	SDL/SCL Rise Time	—	1	μs
210	SDL/SCL Fall Time	—	300	ns
211	STOP Condition Setup Time	4.7	—	μs
NOTE : * SCL frequency is given by $SCL = BRGCLK_frequency / ((BRG_register + 3) * pre_scaler * 2)$. The ratio $SyncClk / (BRGCLK / pre_scaler)$ must be greater or equal to 4/1.				

5.13. I²C AC Electrical Specifications–SCL > 100 KHz

NUM	CHARACTERISTIC	EXPRESSION	MIN	MAX	UNIT
200	SCL Clock Frequency (SLAVE)	fSCL	0	BRGCLK/48	Hz
200	SCL Clock Frequency (MASTER) *	fSCL	BRGCLK/16512	BRGCLK/48	Hz
202	Bus Free Time Between Transmissions		1/(2.2 * fSCL)	—	s
203	LOW Period of SCL		1/(2.2 * fSCL)	—	s
204	HIGH Period of SCL		1/(2.2 * fSCL)	—	s
205	START Condition Setup Time		1/(2.2 * fSCL)	—	s
206	START Condition Hold Time		1/(2.2 * fSCL)	—	s
207	DATA Hold Time		0	—	s
208	DATA Setup Time		1/(40 * fSCL)	—	s
209	SDL/SCL Rise Time		—	1/(10 * fSCL)	s
210	SDL/SCL Fall Time		—	1/(33 * fSCL)	s
211	STOP Condition Setup Time		1/(2.2 * fSCL)	—	s

NOTE : * SCL frequency is given by $SCL = BrgClk_frequency / ((BRG\ register + 3) * pre_scaler * 2)$. The ratio $SyncClk/(Brg_Clk/pre_scaler)$ must be greater or equal to 4/1.

Figure 71 : I²C Bus Timing Diagram



6. PREPARATION FOR DELIVERY

6.1. Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

6.2. Certificate of compliance

ATMEL-Grenoble offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

7. POWER CONSIDERATION

The average chip-junction temperature, T_j , in °C can be obtained from the equation :

$$T_j = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

where

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$$P_D = P_{INT} + P_{I/O}$$

$P_{INT} = I_{DD} \times V_{DD}$, watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications $P_{I/O} < 0.3 \bullet P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_j is :

$$P_D = K \div (T_j + 273^\circ\text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives :

$$K = P_D \bullet T (T_A + 273^\circ\text{C}) + \theta_{JA} \bullet P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_j can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

8. LAYOUT PRACTICES

Each V_{CC} pin on the TSPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the TSPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient current in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

9. FUNCTIONAL UNITS DESCRIPTION

The TSPC860 PowerQUICC integrates the Embedded PowerPC Core with high performance, low power peripherals to extend the Motorola Data Communications family of embedded processors even farther into high end communications and networking products.

The TSPC860 PowerQUICC is comprised of three modules which all use the 32-bit internal bus : the Embedded PowerPC Core, the System Integration Unit (SIU), and the Communication Processor Module (CPM). The TSPC860 PowerQUICC block diagram is shown in Figure 1.

9.1. Embedded PowerPC Core

The Embedded PowerPC Core is compliant with the Book 1 specification for the PowerPC architecture. The Embedded PowerPC Core is a fully static design that consists of two functional blocks ; the integer block and the load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits. The core uses a two instruction load/store queue, a four instruction prefetch queue, and a six instruction history buffer. The core does branch folding and branch prediction with conditional pre-fetch but without conditional execution. The Embedded PowerPC Core can operate on 32-bit external operands with one bus cycle.

The PowerPC integer block supports 32 x 32-bit fixed point general purpose registers. It can execute one integer instruction each clock cycle. Each element in the integer block is clocked only when valid data is present in the data queue ready for operation. This assures that the power consumption of the device is held to the absolute minimum required to perform an operation.

The Embedded PowerPC Core is integrated with MMU's as well as 4 kbyte instruction and data caches. Each MMU provides a 32 entry, fully associative instruction and data TLB, with multiple page sizes of : 4 kB, 16 kB, 512kB, 256 kB and 8 MB. It will support 16 virtual address spaces with 8 protection groups. Three special registers are available as scratch registers to support software table walk and update. The instruction cache is 4 kilobytes, two-way, set associative with physical addressing. It allows single cycle access on hit with no added latency for miss. It has four words per line, supporting burst line fill using Least Recently Used (LRU) replacement. The cache can be locked on a per line basis for application critical routines.

The data cache is 4 kilobytes, two-way, set associative with physical addressing. It allows single cycle access on hit with one added clock latency for miss. It has four words per line, supporting burst line fill using LRU replacement. The cache can be locked on a per line basis for application critical routines. The data cache can be programmed to support copy-back or write-through via the MMU. The inhibit mode can be programmed per MMU page.

The Embedded PowerPC Core with its Instruction and data caches delivers approximately 52 MIPS at 40 MHz, using Dhrystone 2.1, based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94 %.

The Embedded PowerPC Core contains a much improved debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. This interface supports six watchpoint pins that are used to detect software events. Internally it has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators the effective address on the data bus, and two comparators operating on the data on the data bus. The Embedded PowerPC Core can compare using =, \neq , <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

9.2. System Interface Unit (SIU)

The SIU on the TSPC860 PowerQUICC integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the TS68EN360 QUICC device.

Although the Embedded PowerPC Core is always a 32-bit device internally, it may be configured to operate with an 8-, 16- or 32-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, Reset control, PowerPC decremter, PowerPC time base and PowerPC real time clock.

The memory controller will support up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock access to external SRAM and bursting support. It provides variable block sizes from 32 kilobytes to 256 megabytes. The memory controller will provide 0 to 15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It provides four byte enable signals for varying width devices, one output enable signal and one boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined in depths of 256k, 512k, 1M, 2M, 4M, 8M, 16M, 32M, or 64M for all port sizes. In addition the memory depth can be defined as 64k and 128k for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The TSPC860 will support a glueless interface to one bank of DRAM while external buffers are required for additional memory banks. The refresh unit provides CAS before RAS, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking up to 7 refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

9.2.1.PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface will support up to two independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides 8 memory or I/O windows where each window can be allocated to a particular socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

9.2.2. Power Management

The TSPC860 PowerQUICC supports a wide range of power management features including Full On, Doze, Sleep, Deep Sleep, and Low Power Stop. In Full On mode the TSPC860 processor is fully powered with all internal units operating at the full speed of the processor. A Gear mode is provided which is determined by a clock divider, allowing the OS to reduce the operational frequency of the processor. Doze mode disables core functional units other than the time base decremter, PLL, memory controller, RTC, and then places the CPM in low power standby mode. Sleep mode disables everything except the RTC and PIT, leaving the PLL for lower power but slower wake-up. Low Power Stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption but requiring the longest wake-up time.

9.2.3. Communications Processor Module (CPM)

The TSPC860 PowerQUICC is the next generation TS68EN360 QUICC and like its predecessor implements a dual processor architecture. This dual processor architecture provides both a high performance general purpose processor for application programming use as well as a special purpose communication processor (CPM) uniquely designed for communications needs.

The CPM contains features that allow the TSPC860 PowerQUICC to excel in communications and networking products as did the TS68EN360 QUICC which predated it. These features may be divided into three sub-groups :

- . Communications Processor (CP)
- . Sixteen Independent DMA (SDMA) Controllers
- . Four General-Purpose Timers

The CP provides the communication features of the TSPC860 PowerQUICC. Included are a RISC processor, four Serial Communication Controllers (SCC) four Serial Management Controllers (SMC), one Serial Peripheral Interface (SPI), one I² Interface , 5 kilobytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and sixteen serial DMA channels to support the SCCs, SMCs, SPI, and I² C.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on the MC68360 and still support the internal cascading of two timers to form a 32-bit timer.

The TSPC860 PowerQUICC maintains the best features of the TS68EN360 QUICC, while making changes required to provide for the increased flexibility, integration, and performance requested by customers demanding the performance of the powerPC architecture. The addition of a Multiply-And-Accumulate (MAC) function on the CPM further enhances the TSPC860 PowerQUICC, enabling various modem and DSP applications. Because the CPM architectural approach remains intact between the TSPC860 PowerQUICC and the TS68EN360 QUICC, a user of the TS68EN360 QUICC can easily become familiar with the TSPC860 PowerQUICC.

9.3. Software Compatibility Issues

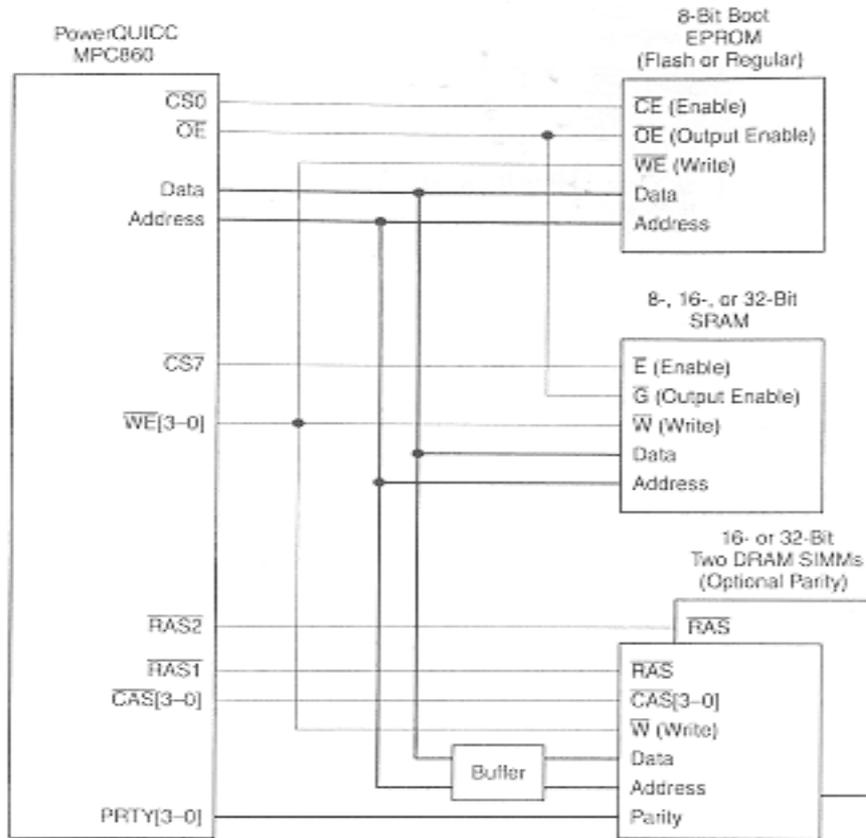
The following list summarizes the major software differences between the TS68EN360 QUICC and the TSPC860 PowerQUICC :

- Since the TSPC860 PowerQUICC uses an Embedded PowerPC Core, code written for the TS68EN360 must be recompiled for the PowerPC instruction set. Code which accesses the TS68EN360 peripherals requires only minor modifications for use with the TSPC860. Although the functions performed by the PowerQUICC SIU are similar to those performed by the QUICC SIM, the initialization sequence for the SIU is different and therefore code that accesses the SIU must be rewritten. Many developers of 68K compilers now provide compilers which also support the PowerPC architecture.
- The addition of the MAC function to the TSPC860 CPM block to support the needs of higher performance communication software is the only major difference between the CPM on the TS68EN360 and that on the TSPC860. Therefore the registers used to initialize the QUICC CPM are similar to the TSPC860 CPM, but there are some minor changes necessary for supporting the MAC function.
- When porting code from the TS68EN360 CPM to the TSPC860 CPM, the software writer will find new options for hardware breakpoint on CPU commands, address, and serial request which are useful for software debugging. Support for single step operation with all the registers of the CPM visible makes software development for the CPM on the TSPC860 processor even simpler.

9.4. TSPC860 PowerQUICC Glueless System Design

A fundamental design goal of the TSPC860 PowerQUICC was ease of interface to other system components. Figure 72 shows a system configuration that offers one EPROM, one flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

Figure 72 : TSPC860 System Configuration



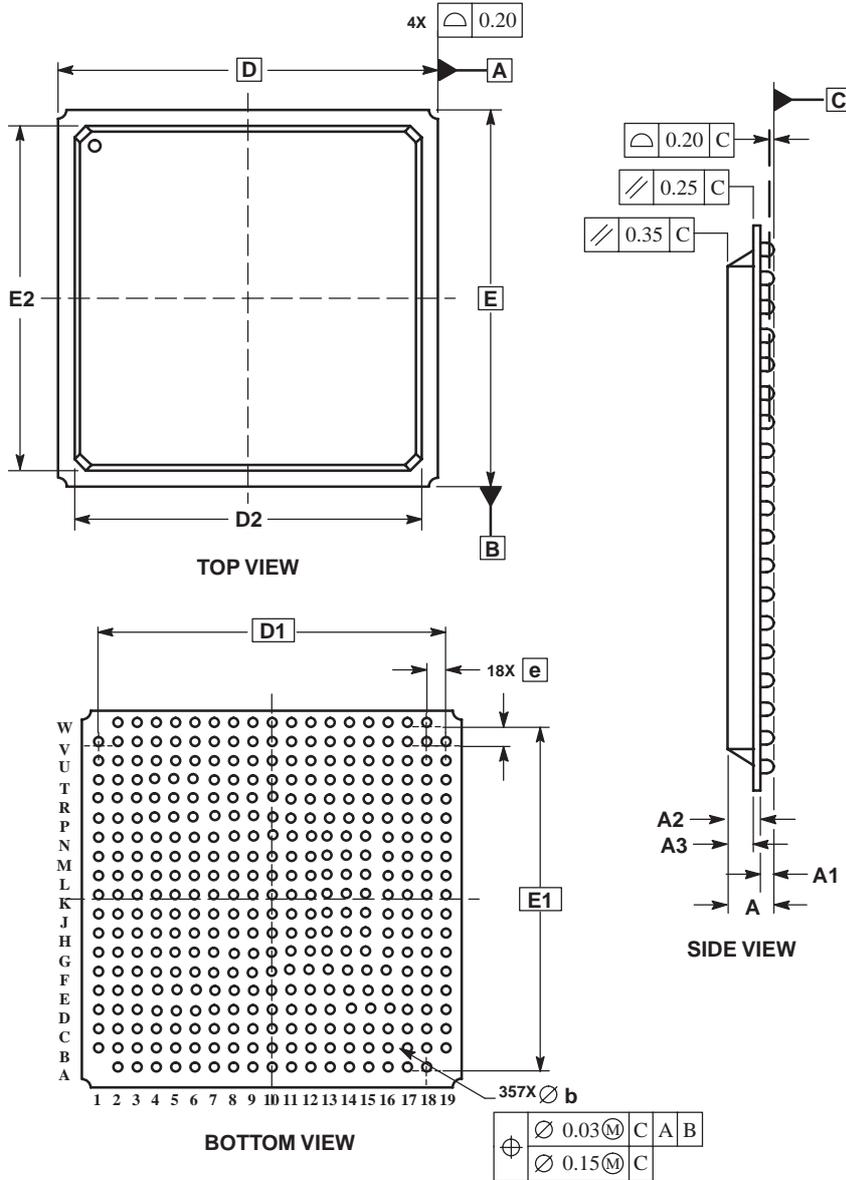
10. HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

- a) Devices should be handled on benches with conductive and grounded surfaces.
- b) Ground test equipment, tools and operator.
- c) Do not handle devices by the leads.
- d) Store devices in conductive foam or carriers.
- e) Avoid use of plastic, rubber, or silk in MOS areas.
- f) Maintain relative humidity above 50 percent if practical.

11. PACKAGE DIMENSIONS

11.1. Plastic Ball Grid Array



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS IN MILLIMETERS.
 3. DIMENSION b IS THE SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

MILLIMETERS		
DIM	MIN	MAX
A	—	2.05
A1	0.50	0.70
A2	0.95	1.35
A3	0.70	0.90
b	0.60	0.90
D	25.00 BSC	
D1	22.86 BSC	
D2	22.40	22.60
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	22.40	22.60

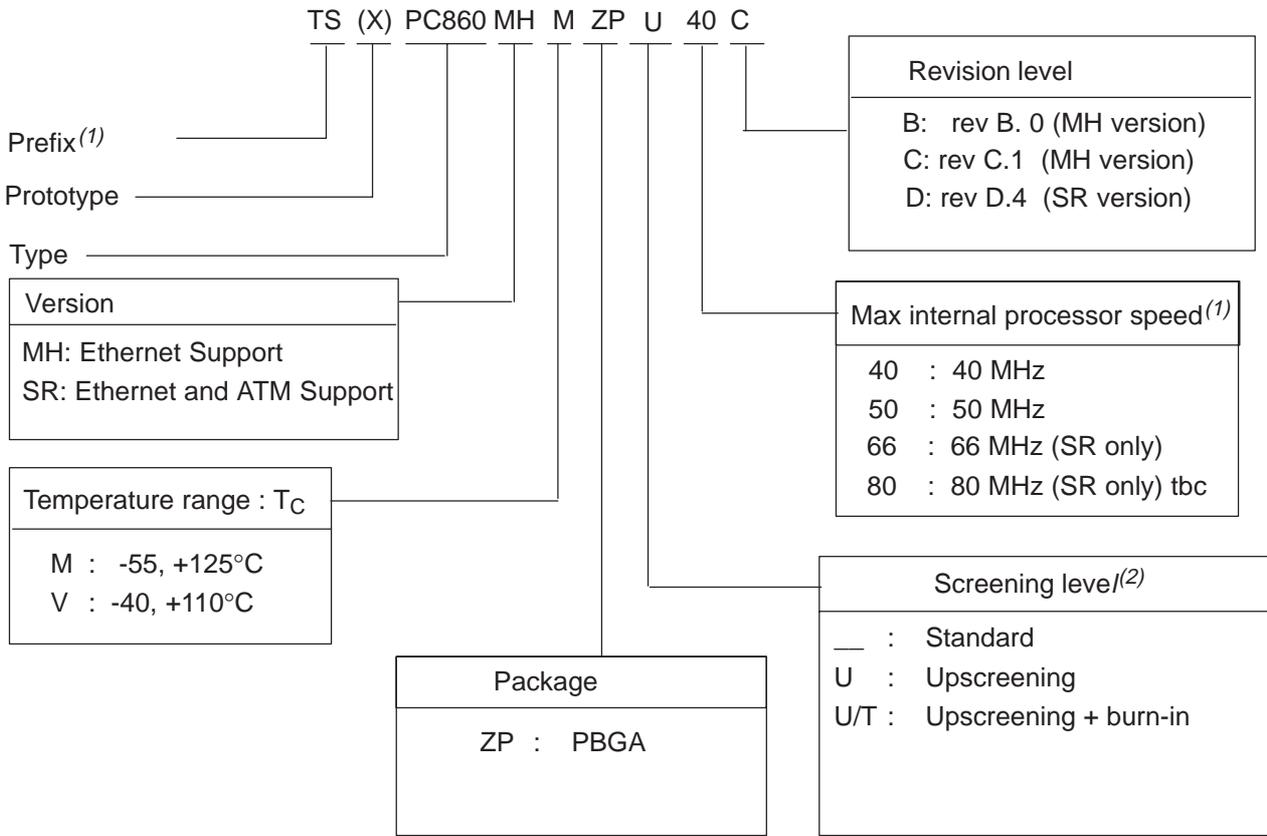
12. DEFINITIONS

Datasheet status		Validity
Objective specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Before design phase.
Target specification	This datasheet contains target or goal specification for product development.	Valid during the design phase.
Preliminary specification ∞ site	This datasheet contains preliminary data. Additional data may be published later ; could include simulation result.	Valid before characterization phase.
Preliminary specification β site	This datasheet contains also characterization results.	Valid before the industrialization phase.
Product specification	This datasheet contains final product specification.	Valid for production purpose.
Limiting values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. ATMEL-Grenoble customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify ATMEL-Grenoble for any damages resulting from such improper use or sale.

13. ORDERING INFORMATION



(1) For availability of the different versions, contact your ATMEL-Grenoble sale office

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