8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD789415, μPD789416, and μPD789417 are μPD789417 sub-series products (LCD drivers) of the 78K/0S series.

These microcontrollers feature an 8-bit CPU, LCD controller/driver, I/O ports, timers, a serial interface, A/D converters, a comparator, and interrupt control circuits.

The instruction set of the μPD789415, μPD789416, and μPD789417 is a subset of the 78K/0 series standard instruction set.

In addition, a flash memory product (μPD78F9418) that can operate within the same voltage range as the mask ROM models, and a range of related development tools are being developed.

The functions of these microcontrollers are described in the following user's manual. Refer to this manual when designing a system based on any of these microcontrollers.

μPD789407 and μPD789417 Sub-Series User's Manual: Under development

FEATURES

- ROM and RAM sizes

Item / Product name	Program memory (ROM)	Data memory		Package
		Internal high-speed RAM	LCD data RAM	
μPD789415	12 Kbytes	512×8 bits	28×8 bits	80-pin plastic QFP (14×14 mm) 80-pin plastic TQFP (fine pitch) (12×12 mm)
μPD789416	16 Kbytes			
μPD789417	24 Kbytes			

- Variable instruction execution time: From high-speed (0.4 μs with the main system clock running at 5.0 MHz) to ultra-low speed (122 μs with the subsystem clock running at 32.768 kHz)
- 43 I/O ports
- Serial interface channel: Switchable between three-wire serial I/O and UART modes
- LCD controller/driver:
  - Up to 28 segment signal outputs
  - Up to 4 common signal outputs
  - Bias switchable between 1/2 and 1/3
- Seven A/D converters with an 10-bit resolution
- Six timers:
  - 16-bit timer/counter
  - Two 8-bit timer/event counters
  - 8-bit timer/counter
  - Clock timer
  - Watchdog timer
- Power supply voltage V_{DD}: 1.8 to 5.5 V

APPLICATIONS

APS compact cameras, manometers, and rice cookers

ORDERING INFORMATION

Part number	Package
μPD789415GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD789415GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD789416GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD789416GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD789417GC-×××-8BT	80-pin plastic QFP (14 × 14 mm)
μPD789417GK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)

Remark ××× indicates the ROM code number.

78K/0S SERIES DEVELOPMENT

The 78K/0S series products are shown below. The sub-series names are indicated in frames.

```
/-------------/  Under development
/-------------/
```

The Y sub-series products are compatible with the I²C bus.

For small-scale, general-purpose applications

42/44-pin μPD789026   Device developed by adding a 16-bit timer to the μPD789014

28-PIN μPD789014   With built-in UART bus and capable of low-voltage (1.8 V) operation

78K/0S series

For LCD driving

80-pin μPD789417   Device developed by enhancing the A/D function of the μPD789407

80-pin μPD789407   Device developed by adding an A/D function and enhancing the timers of the μPD789026

For ASSP

42/44-pin μPD789800   Device for a PC keyboard, with a built-in USB function

42-pin μPD789806Y   Device for a PC monitor, with a built-in USB function and synchronizing separator

The following table lists the major differences in functions between the sub-series.

Function / Sub-series		ROM size	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	Minimum V_{DD} value
			8-bit	16-bit	Clock	WDT						
Small-scale general purpose	μPD789026	4 K-16 K	1 ch	1 ch	–	1 ch	–	–	–	1 ch (UART: 1 ch)	34 pins	1.8 V
	μPD789014	2 K-4 K	2 ch	–							22 pins	
LCD driving	μPD789417	12 K-24 K	3 ch	1 ch	1 ch	1 ch	–	7 ch	–	1 ch (UART: 1 ch)	43 pins	1.8 V
	μPD789407	12 K-24 K					7 ch	–				
ASSP	μPD789800	8 K	2 ch	–	–	1 ch	–	–	–	2 ch (USB: 1 ch)	31 pins	4.0 V
	μPD789806Y	16 K	2 ch	–	–	1 ch	–	–	–	2 ch (USB: 1 ch, I²C: 1 ch)	20 pins	4.5 V

3

78K/0 SERIES DEVELOPMENT

The 78K/0 series products are shown below. The sub-series names are indicated in frames.

In production

Under development

The Y sub-series products are compatible with the I²C bus.

78K/0 series

Used for control

Pin	Device	Device (Y)	Description
100-pin	μPD78075B	μPD78075BY	Low EMI noise version of the μPD78078
100-pin	μPD78078	μPD78078Y	Device with enhanced external interface, developed by adding a timer to the μPD78054
100-pin	μPD78070A	μPD78070AY	ROM-less version of the μPD78078
100-pin	μPD780018**Note**	μPD780018Y	Device developed by enhancing the serial I/O bus of the μPD78078 and limiting its functions
80-pin	μPD780058	μPD780058Y**Note**	Low EMI noise version of the μPD78054, developed by enhancing its serial I/O bus
80-pin	μPD78058F	μPD78058FY	Low EMI noise version of the μPD78054
80-pin	μPD78054	μPD78054Y	Device developed by adding UART and D/A functions to the μPD78014 and enhancing the I/O bus
64-pin	μPD780034	μPD780034Y	Device developed by enhancing the A/D function of the μPD780024
64-pin	μPD780024	μPD780024Y	Low EMI noise version of the μPD78018F, developed by enhancing its serial I/O bus
64-pin	μPD78014H		Low EMI noise version of the μPD78018F
64-pin	μPD78018F	μPD78018FY	Low-voltage (1.8 V) version of the μPD78014, with enhanced ROM and RAM variations
64-pin	μPD78014	μPD78014Y	Device developed by adding A/D and 16-bit timer functions to the μPD78002
64-pin	μPD780001		Device developed by adding A/D functions to the μPD78002
64-pin	μPD78002	μPD78002Y	Basic series for control use
42/44-pin	μPD78083		With built-in UART bus and capable of low-voltage (1.8 V) operation

For inverter control

Pin	Device	Description
64-pin	μPD780964	Device developed by enhancing the A/D function of the μPD780924
64-pin	μPD780924	Built-in inverter control circuit and UART bus. Low EMI noise version.

For driving FIP™

Pin	Device	Description
100-pin	μPD780208	Device developed by enhancing the I/O and FIP C/D functions of the μPD78044F, with a total of 53 display outputs
100-pin	μPD780228	Device developed by enhancing the I/O and FIP C/D functions of the μPD78044H, with a total of 48 display outputs
80-pin	μPD78044H	Device developed by adding N-channel, open-drain input/output ports, with a total of 34 display outputs
80-pin	μPD78044F	Basic sub-series for FIP driving, with a total of 34 display outputs

For LCD driving

Pin	Device	Device (Y)	Description
100-pin	μPD780308	μPD780308Y	Device developed by enhancing the SIO bus of the μPD78064, with expanded ROM and RAM
100-pin	μPD78064B		Low EMI noise version of the μPD78064
100-pin	μPD78064	μPD78064Y	Basic sub-series for LCD driving, with built-in UART

Device supporting IEBus™

Pin	Device	Description
80-pin	μPD78098B	Device developed by adding the IEBus controller to the μPD78054
80-pin	μPD78098	Low EMI noise version of the μPD78098

For meter control

Pin	Device	Description
80-pin	μPD780973	Device developed by modifying the automobile meter controller/driver of the μPD780805 to a general-purpose version
100-pin	μPD780805	Device with built-in automobile meter controller/driver

For LV

Pin	Device	Description
64-pin	μPD78P0914	Device with PWM output, LV digital code decoder, and Hsync counter

Note Device in the planning stage

The following table lists the major functional differences between the sub-series.

Function / Sub-series		ROM size	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	Minimum V_DD value	External expansion
			8-bit	16-bit	Clock	WDT							
For control use	μPD78075B	32 K-40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88 pins	1.8 V	○
	μPD78078	48 K-60 K											
	μPD78070A	–									61 pins	2.7 V	
	μPD780018	48 K-60 K						–	2 ch (3-wire time-division: 1 ch)		88 pins		
	μPD780058	24 K-60 K	2 ch						2 ch	3 ch (UART time-division: 1 ch)	68 pins	1.8 V	
	μPD78058F	48 K-60 K								3 ch (UART: 1 ch)	69 pins	2.7 V	
	μPD78054	16 K-60 K										2.0 V	
	μPD780034	8 K-32 K					–	8 ch	–	3 ch (UART : 1 ch, 3-wire time division: 1 ch)	51 pins	1.8 V	
	μPD780024						8 ch	–					
	μPD78014H									2 ch	53 pins		
	μPD78018F	8 K-60 K											
	μPD78014	8 K-32 K										2.7 V	
	μPD780001	8 K		–	–					1 ch	39 pins		–
	μPD78002	8 K-16 K			1 ch		–				53 pins		○
	μPD78083				–		8 ch			1 ch (UART: 1 ch)	33 pins	1.8 V	–
For inverter control	μPD780964	8 K-32 K	3 ch	Note	–	1 ch	–	8 ch	–	2 ch (UART: 2 ch)	47 pins	2.7 V	○
	μPD780924						8 ch	–					
For FIP driving	μPD780208	32 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74 pins	2.7 V	–
	μPD780228	48 K-60 K	3 ch	–	–					1 ch	72 pins	4.5 V	
	μPD78044H	32 K-48 K	2 ch	1 ch	1 ch						68 pins	2.7 V	
	μPD78044F	16 K-40 K								2 ch			
For LCD driving	μPD780308	48 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART time division: 1 ch)	57 pins	2.0 V	–
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K-32 K											
For supporting the IEBus	μPD78098B	40 K-60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	69 pins	2.7 V	○
	μPD78098	32 K-60 K											
For meter control	μPD780973	24 K-32 K	3 ch	1 ch	1 ch	1ch	5 ch	–	–	2 ch (UART: 1 ch)	56 pins	4.5 V	–
	μPD780805	40 K-60 K	2 ch				8 ch				39 pins	2.7 V	
For LV	μPD78P0914	32 K	6 ch	–	–	1 ch	8 ch	–	–	2 ch	54 pins	4.5 V	○

Note One 10-bit timer

FUNCTIONS

Item		μPD789415	μPD789416	μPD789417
Built-in memory	ROM	12 Kbytes	16 Kbytes	24 Kbytes
	High-speed RAM	512 bytes		
	LCD data RAM	28 bytes		
Instruction cycle		Built-in function for changing the instruction execution time 0.4/1.6 μs (operation with main system clock running at 5.0 MHz) 122 μs (operation with subsystem clock running at 32.768 kHz).		
General-purpose registers		8 bits × 8 registers		
Instruction set		• 16-bit operations • Bit manipulations (such as set, reset, and test)		
I/O ports		Total of 43 port pins • 7 CMOS input pins • 32 CMOS input/output pins • 4 N-channel open-drain pins (dielectric strength of 12 V)		
A/D converters		Seven channels with 10-bit resolution		
Comparator		With timer output control function		
Serial interface		• Switchable between three-wire serial I/O and UART modes		
LCD controller/driver		• Up to 28 segment signal outputs • Up to 4 common signal outputs • Bias switchable between 1/2 and 1/3		
Timers		• 16-bit timer/counter • 8-bit timer/counter • Two 8-bit timer/event counters • Clock timer • Watchdog timer		
Timer output		Two outputs		
Vector interrupt sources	Maskable	12 internal and 4 external interrupts		
	Non-maskable	Internal interrupt		
Power supply voltage		V_{DD} = 1.8 to 5.5 V		
Operating ambient temperature		T_A = −40 to +85 °C		
Package		• 80-pin plastic QFP (14 × 14 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)		

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14 mm)
  μPD789415GC-×××-8BT
  μPD789416GC-×××-8BT
  μPD789417GC-×××-8BT

- 80-pin plastic TQFP (fine pitch)(12 × 12 mm)
  μPD789415GK-×××-BE9
  μPD789416GK-×××-BE9
  μPD789417GK-×××-BE9

Top pins (80–61): P40/KR0, P41/KR1, P42/KR2, P43/KR3, P44/KR4, P45/KR5, IC, XT1, XT2, V_{DD0}, V_{SS0}, X1, X2, RESET, P46, P47, P00, P01, P02, P03

Left pins (1–20):
- 1 V_{DD1}
- 2 BIAS
- 3 V_{LC0}
- 4 V_{LC1}
- 5 V_{LC2}
- 6 V_{SS1}
- 7 COM0
- 8 COM1
- 9 COM2
- 10 COM3
- 11 S0
- 12 S1
- 13 S2
- 14 S3
- 15 S4
- 16 S5
- 17 S6
- 18 S7
- 19 S8
- 20 S9

Right pins (60–41):
- 60 P50
- 59 P51
- 58 P52
- 57 P53
- 56 P20/$\overline{SCK}$/ASCK
- 55 P21/SO/TxD
- 54 P22/SI/RxD
- 53 P23/CMPTOUT0/TO2
- 52 P24/INTP0/TI0
- 51 P25/INTP1/TI1
- 50 P26/INTP2/TO5
- 49 P27/INTP3/CPT5
- 48 AVss
- 47 P60/ANI0/CMPIN0
- 46 P61/ANI1/CMPREF0
- 45 P62/ANI2
- 44 P63/ANI3
- 43 P64/ANI4
- 42 P65/ANI5
- 41 P66/ANI6

Bottom pins (21–40): S10, S11, S12, S13, S14, S15, P93/S16, P92/S17, P91/S18, P90/S19, P87/S20, P86/S21, P85/S22, P84/S23, P83/S24, P82/S25, P81/S26, P80/S27, AV$_{DD}$, AV$_{REF}$

Cautions 1. Connect the IC pin (internally connected) directly to V_{SS0} or V_{SS1}.

   2. Connect the AV$_{DD}$ pin to V_{DD0}.

   3. Connect the AV$_{SS}$ pin to V_{SS0}.

ANI0-ANI6	: Analog Input	P60-P66	: Port 6
ASCK	: Asynchronous Serial Input	P80-P87	: Port 8
AV_{DD}	: Analog Power Supply	P90-P93	: Port 9
AV_{REF}	: Analog Reference Voltage	$\overline{RESET}$	: Reset
AV_{SS}	: Analog Ground	RxD	: Receive Data
BIAS	: LCD Power Supply Bias Control	S0-S27	: Segment Output
CMPIN0	: Comparator Input	$\overline{SCK}$	: Serial Clock
CMPREF0	: Comparator Reference	SI	: Serial Input
CMPTOUT0	: Comparator Output	SO	: Serial Output
COM0-COM3	: Common Output	TI0, TI1	: Timer Input
CPT5	: Capture Trigger Input	TO2, TO5	: Timer Output
IC	: Internally Connected	TxD	: Transmit Data
INTP0-INTP3	: Interrupt from Peripherals	V_{DD0}, V_{DD1}	: Power Supply
KR0-KR5	: Key Return	V_{LC0}-V_{LC2}	: LCD Power Supply
P00-P03	: Port 0	V_{SS0}, V_{SS1}	: Ground
P20-P27	: Port 2	X1, X2	: Crystal (Main System Clock)
P40-P47	: Port 4	XT1, XT2	: Crystal (Subsystem Clock)
P50-P53	: Port 5		

2. BLOCK DIAGRAM
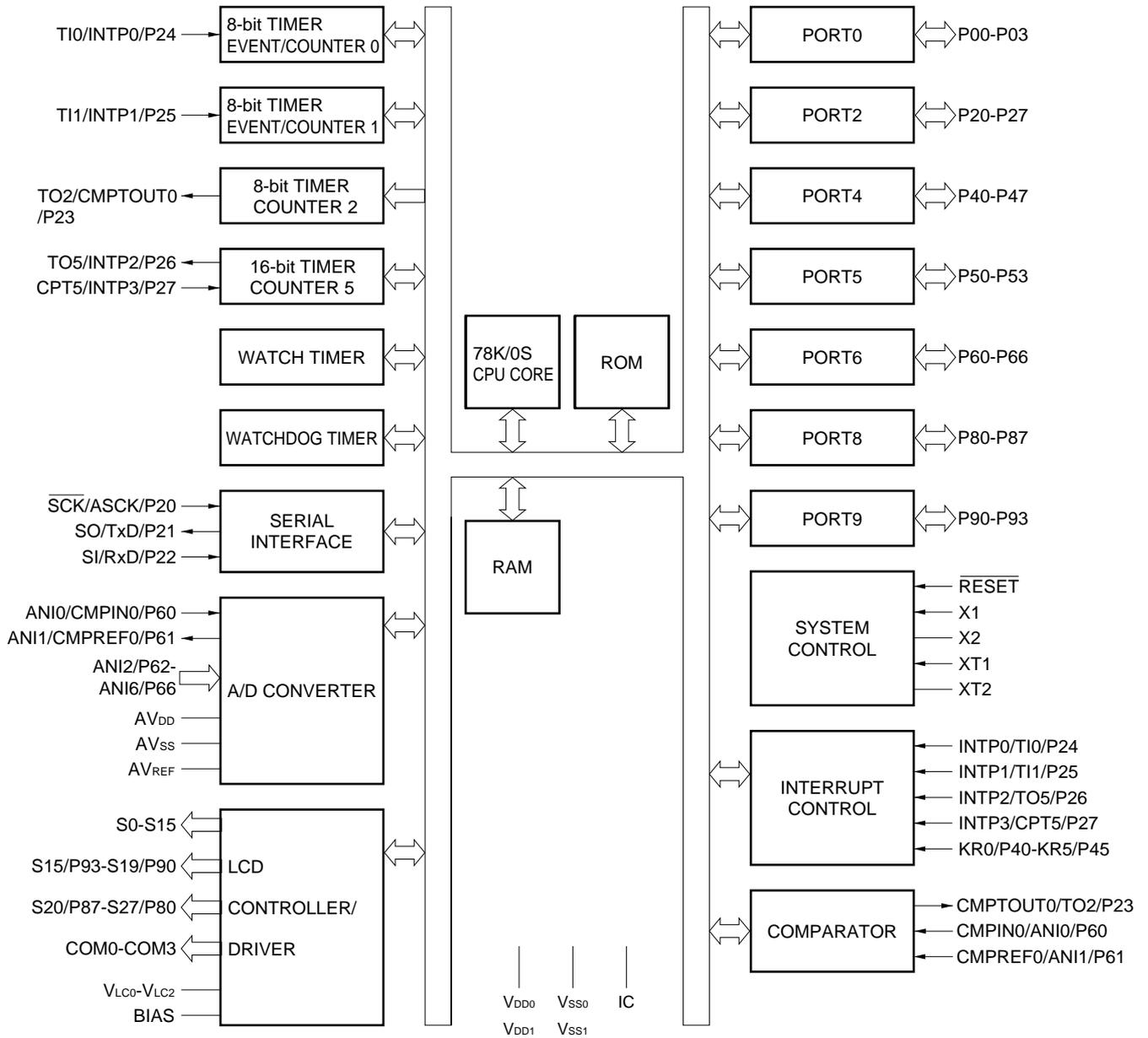
Remark   The size of the built-in ROM varies depending on the model.

3. PIN FUNCTIONS

3.1 Port Pins

Pin name	I/O	Function	When reset	Also used as
P00-P03	I/O	Port 0 4-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software.	Input	–
P20	I/O	Port 2 8-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software.	Input	$\overline{\text{SCK}}$/ASCK
P21				SO/TxD
P22				SI/RxD
P23				CMPTOUT0/TO2
P24				INTP0/TI0
P25				INTP1/TI1
P26				INTP2/TO5
P27				INTP3/CPT5
P40-P45	I/O	Port 4 8-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software.	Input	KR0-KR5
P46, P47				–
P50-P53	I/O	Port 5 4-bit N-channel open-drain input/output port Can be set to either input or output in 1-bit units Whether a pull-up resistor is to be incorporated can be specified by a mask option.	Input	–
P60	Input	Port 6 7-bit input-only port	Input	ANI0/CMPIN0
P61				ANI1/CMPREF0
P62-P66				ANI2-ANI6
P80-P87	I/O	Port 8 8-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software.	Input	S27-S20
P90-P93	I/O	Port 9 4-bit input/output port Can be set to either input or output in 1-bit units When used as an input port, whether the built-in pull-up resistor is to be used can be specified by software.	Input	S19-S16

3.2 Non-Port Pins

Pin name	I/O	Function	When reset	Also used as
INTP0	Input	External interrupt input for which effective edges (rising and/or falling edges) can be specified	Input	P24/TI0
INTP1				P25/TI1
INTP2				P26/TO5
INTP3				P27/CPT5
KR0-KR5	Input	Key return signal detection	Input	P40-P45
SI	Input	Serial data input to serial interface	Input	P22/RxD
SO	Output	Serial data output from serial interface	Input	P21/TxD
$\overline{\text{SCK}}$	I/O	Serial clock input/output for serial interface	Input	P20/ASCK
ASCK	Input	Serial clock input to asynchronous serial interface	Input	P20/$\overline{\text{SCK}}$
RxD	Input	Serial data input to asynchronous serial interface	Input	P22/SI
TxD	Output	Serial data output from asynchronous serial interface	Input	P21/SO
TI0	Input	External count clock input to 8-bit timer (TM0)	Input	P24/INTP0
TI1	Input	External count clock input to 8-bit timer (TM1)	Input	P25/INTP1
TO2	Output	8-bit timer (TM2) output	Input	P23/CMPTOUT0
TO5	Output	16-bit timer (TM5) output	Input	P26/INTP2
CPT5	Input	Capture edge input	Input	P27/INTP3
CMPTOUT0	Output	Comparator output	Input	P23/TO2
CMPIN0	Input	Comparator input	Input	P60/ANI0
CMPREF0	Input	Comparator reference voltage input	Input	P61/ANI1
ANI0	Input	A/D converter analog input	Input	P60/CMPIN0
ANI1				P61/CMPREF0
ANI2-ANI6				P62-P66
AV$_{REF}$	–	A/D converter reference voltage	–	–
AV$_{SS}$	–	A/D converter ground potential	–	–
AV$_{DD}$	–	A/D converter analog power supply	–	–
S0-S15	Output	LCD controller/driver segment signal output	Output	–
S16-S19			Input	P93-P90
S20-S27				P87-P80
COM0-COM3	Output	LCD controller/driver common signal output	Output	–
V$_{LC0}$-V$_{LC2}$	–	LCD driving voltage	–	–
BIAS	–	Supply voltage for LCD driving	–	–
X1	Input	Connected to crystal for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connected to crystal for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V$_{DD0}$	–	Positive supply voltage for ports	–	–
V$_{DD1}$	–	Positive supply voltage for circuits other than ports	–	–
V$_{SS0}$	–	Port section ground potential	–	–
V$_{SS1}$	–	Ground potential of circuits other than ports	–	–
IC	–	Internally connected directly to V$_{SS0}$ or V$_{SS1}$	–	–

3.3 Pin Input/Output Circuits and Handling of Unused Pins

Table 3-1 lists the types of input/output circuits for each pin and explains how unused pins are handled.
Figure 3-1 shows the configuration of each type of input/output circuit.

Table 3-1. Type of Input/Output Circuit for Each Pin and Handling of Unused Pins

Pin name	I/O circuit type	I/O	Recommended connection of unused pins
P00-P03	5-H	I/O	Separately connected to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via respective resistors
P20/$\overline{SCK}$/ASCK	8-C		
P21/SO/TxD			
P22/SI/RxD			
P23/CMPTOUT0/TO2	10-B		
P24/INTP0/TI0	8-C		
P25/INTP1/TI1			
P26/INTP2/TO5			
P27/INTP3/CPT5			
P40/KR0-P45/KR5			
P46, P47	5-H		
P50-P53	13-Q		
P60/ANI0/CMPIN0	9-D	Input	
P61/ANI1/CMPREF0			
P62/ANI2-P66/ANI6	9-C		
P80/S27-P87/S20	17-F	I/O	
P90/S19-P93/S16			
S0-S15	17-B	Output	Open
COM0-COM3	18-A		
V_{LC0}-V_{LC2}	–	–	
BIAS			Open (alternatively, connected to V_{SS0} or V_{SS1} via a resistor independently of the other pins, when none of V_{LC0} to V_{LC2} are used, however)
XT1		Input	Connected to V_{SS0} or V_{SS1}, via a resistor, independently of the other pins
XT2		–	Open
$\overline{RESET}$	2	Input	–
IC	–	–	Connected directly to V_{SS0} or V_{SS1}

Figure 3-1. Pin Input/Output Circuits (1/2)
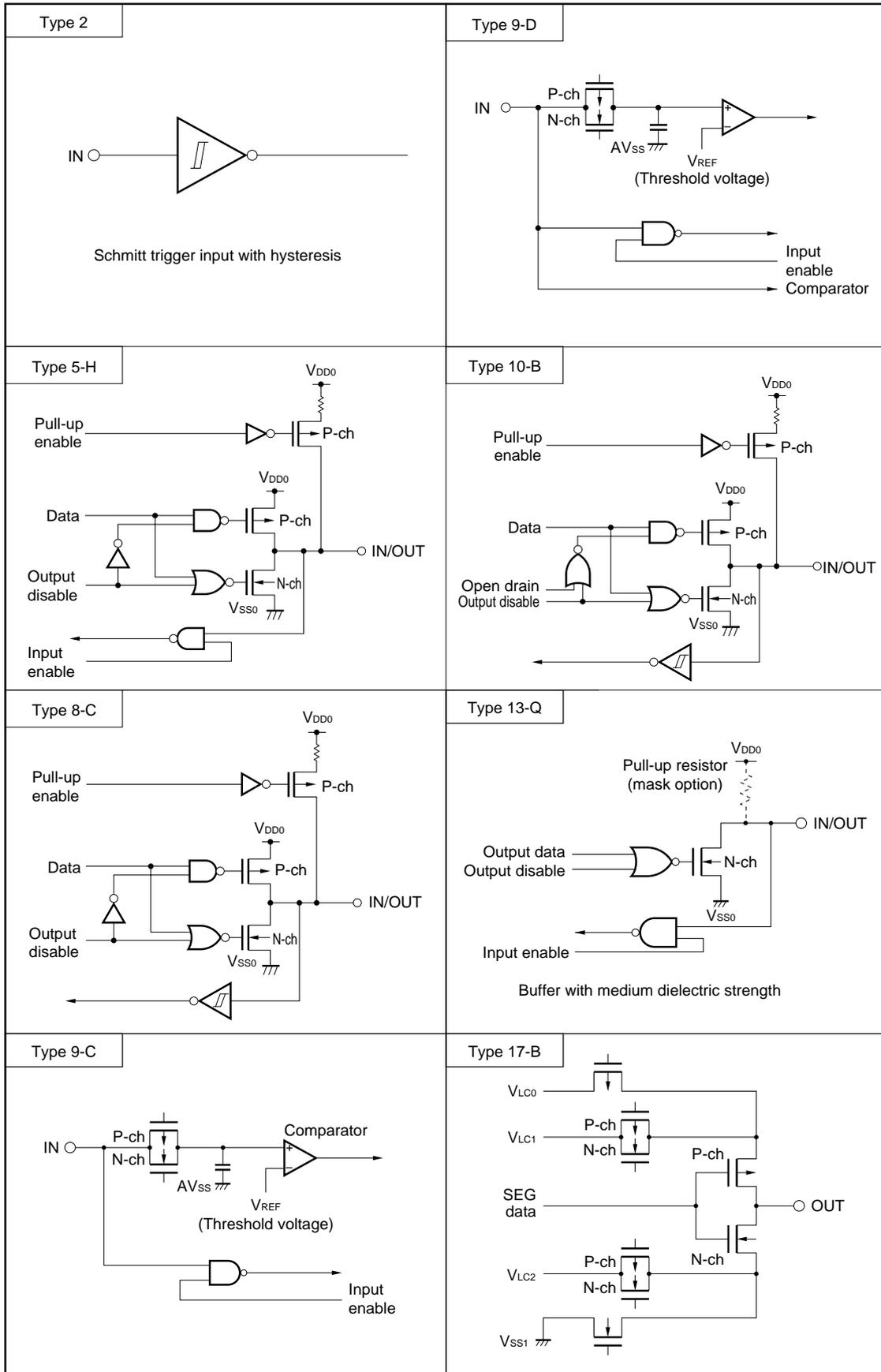
Figure 3-1. Pin Input/Output Circuits (2/2)
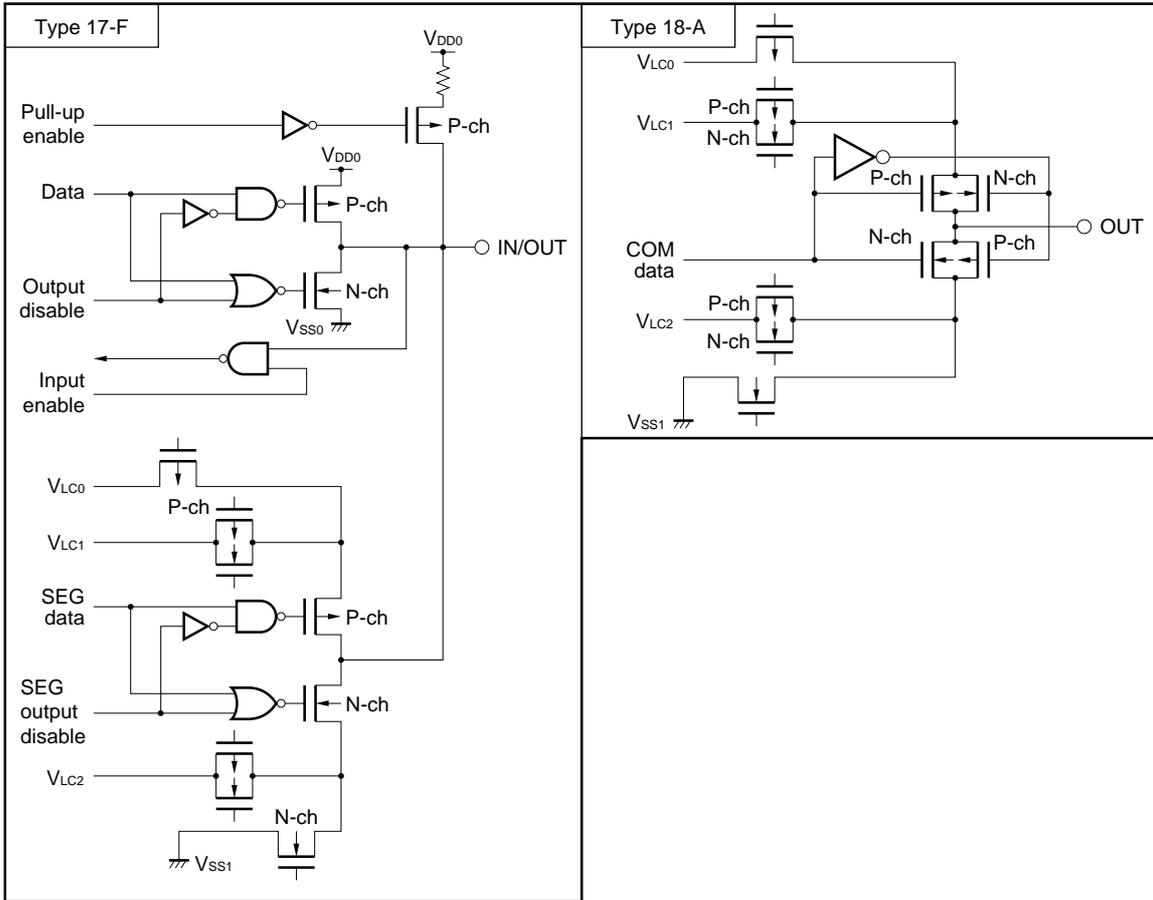
4. CPU ARCHITECTURE

4.1 Memory Space

The μPD789415, μPD789416, and μPD789417 can each access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map
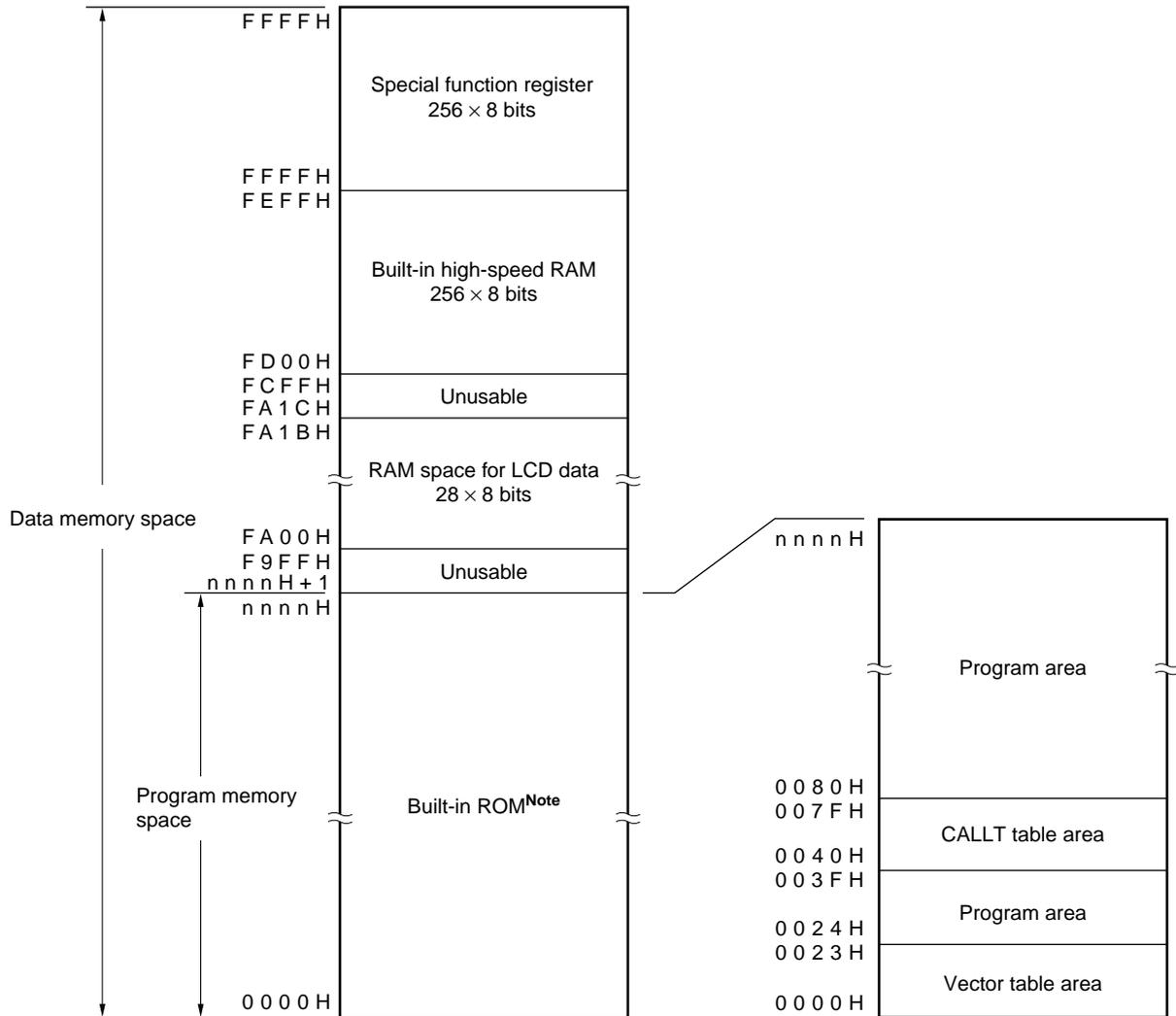
Note The size of the built-in ROM varies depending on the model. (See the following table.)

Product name	Last address of built-in ROM nnnnH
μPD789415	2FFFH
μPD789416	3FFFH
μPD789417	5FFFH

4.2 Data Memory Addressing

Each of the μPD789415, μPD789416, and μPD789417 is provided with a wide range of addressing modes to make memory manipulation as efficient as possible. A data memory area (FD00H to FFFFH) can be accessed using a unique addressing mode according to its use, such as a special function register (SFR). Figure 4-2 illustrates the data memory addressing modes.

Figure 4-2. Data Memory Addressing Modes
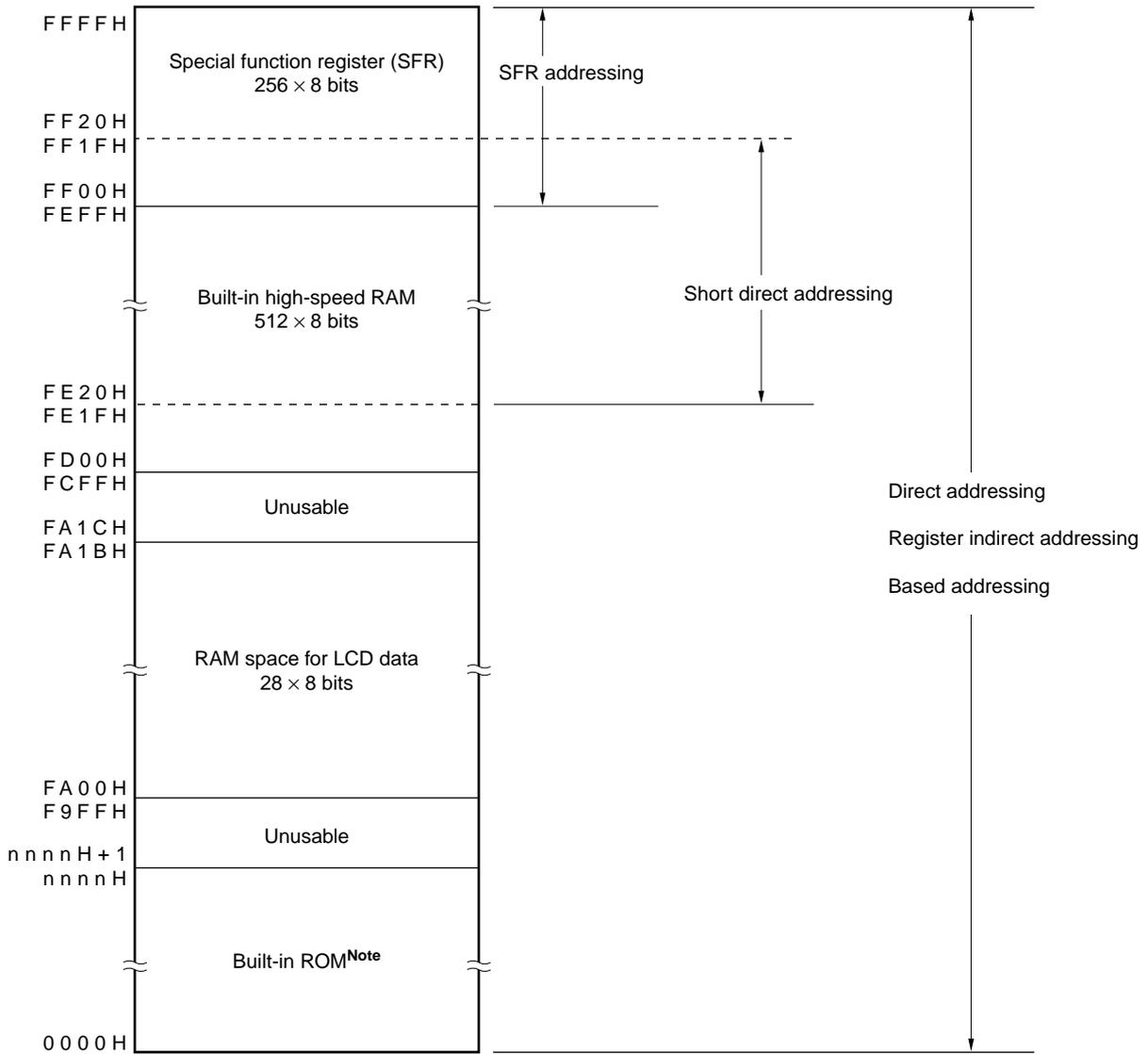
Note The size of built-in ROM varies depending on the model. (See the following table.)

Product name	Last address of built-in ROM nnnnH
μPD789415	2FFFH
μPD789416	3FFFH
μPD789417	5FFFH

4.3 Processor Registers

4.3.1 Controller registers

(1) Program counter (PC)

The PC is a 16-bit register for holding address information that indicates the next program to be executed.

Figure 4-3. Program Counter Configuration
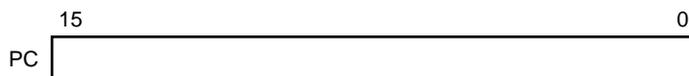
(2) Program status word (PSW)

The PSW is an 8-bit register for holding the status of the CPU according to the results of instruction execution.

Figure 4-4. Program Status Word Configuration
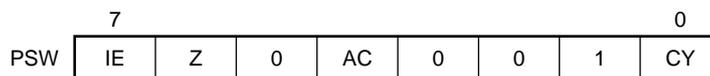
(a) Interrupt enable flag (IE)

IE is used to control whether interrupt requests are to be accepted by the CPU.

(b) Zero flag (Z)

Z is set (1) if the result of operation is zero. Otherwise, it is reset (0).

(c) Auxiliary carry flag (AC)

AC is set (1) if the result of the operation has a carry from bit 3 or a borrow to bit 3. Otherwise, it is reset (0).

(d) Carry flag (CY)

CY is used to indicate whether an overflow or underflow has occurred during the execution of a subtract or add instruction.

(3) Stack pointer (SP)

SP is a 16-bit register for holding the start address of a stack area. The stack area can be specified only in an area (FD00H to FEFFH) of built-in high-speed RAM.

Figure 4-5. Stack Pointer Configuration
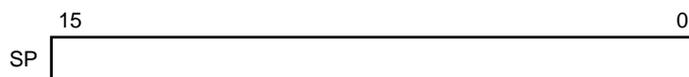
Caution A $\overline{\text{RESET}}$ input makes the SP content undefined. Before executing an instruction, always initialize the SP.

4.3.2 General-purpose registers

Each device has eight 8-bit general-purpose registers (X, A, C, B, E, D, L, and H).

These registers can be used as 16-bit registers (two 8-bit registers used in pairs like AX, BC, DE, and HL) as well as ordinary 8-bit registers.

These registers are identified using functional register names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute register names (R0 to R7 and RP0 to RP3).

Figure 4-6. General Register Configuration

(a) Absolute register names

16-bit processing	8-bit processing
RP3	R7
	R6
RP2	R5
	R4
RP1	R3
	R2
RP0	R1
	R0

15   0   7   0

(b) Functional register names

16-bit processing	8-bit processing
HL	H
	L
DE	D
	E
BC	B
	C
AX	A
	X

15   0   7   0
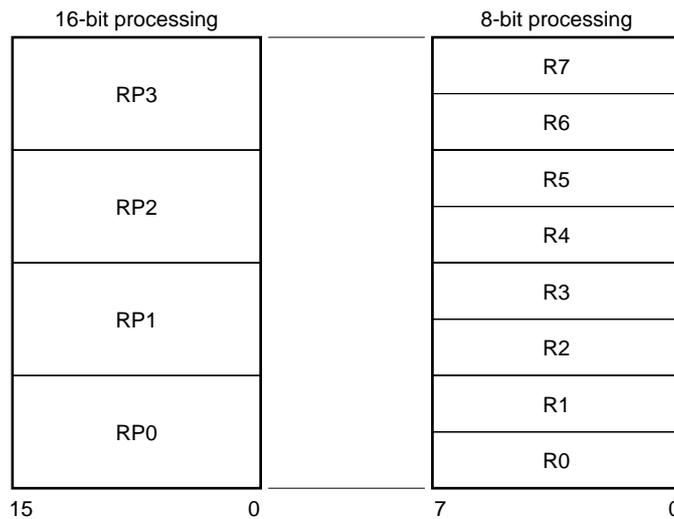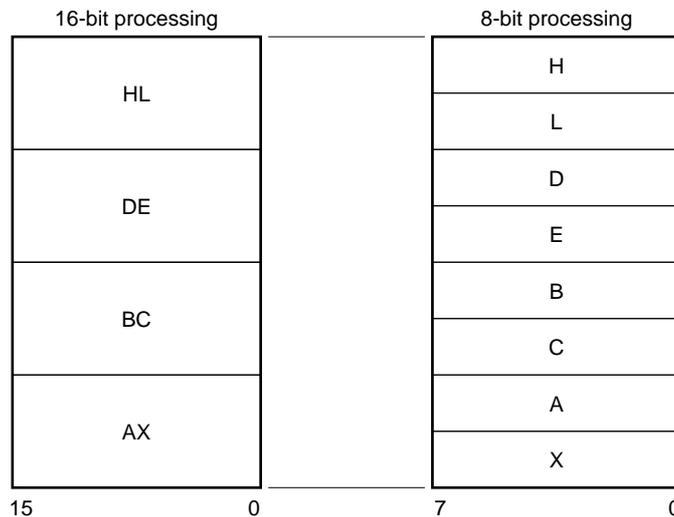
4.3.3 Special function registers (SFRs)

The SFRs are used as peripheral hardware mode registers and control registers. They are mapped in a 256-byte space, from FF00H to FFFFH.

Table 4-1. Special Function Registers (1/2)

Address	Special function register (SFR) name	Symbol		R/W	Number of bits manipulated simultaneously			When reset
					1 bit	8 bits	16 bits	
FF00H	Port 0	P0		R/W	○	○	–	00H
FF02H	Port 2	P2			○	○	–	
FF04H	Port 4	P4			○	○	–	
FF05H	Port 5	P5			○	○	–	
FF06H	Port 6	P6		R	○	○	–	
FF08H	Port 8	P8		R/W	○	○	–	
FF09H	Port 9	P9			○	○	–	
FF10H	Transmission shift register	TXS	SIO0	W	–	○	–	FFH
	Reception buffer register	RXB		R	–	○	–	Undefined
FF14H	10-bit A/D conversion result register	ADCR		R/W	–	–Note 1	○Note 3	
FF15H								
FF16H	16-bit compare register 5	CR50L	CR50	W	–	–Note 2	○Note 3	FFFFH
FF17H		CR50H						
FF18H	16-bit timer register 5	TM5		R	–	–Note 2	○Note 3	0000H
FF19H								
FF1AH	16-bit capture register 5	TCP5			–	–Note 2	○Note 3	Undefined
FF1BH								
FF20H	Port mode register 0	PM0		R/W	○	○	–	FFH
FF22H	Port mode register 2	PM2			○	○	–	
FF24H	Port mode register 4	PM4			○	○	–	
FF25H	Port mode register 5	PM5			○	○	–	
FF28H	Port mode register 8	PM8			○	○	–	
FF29H	Port mode register 9	PM9			○	○	–	
FF42H	Timer clock selection register 2	TCL2			–	○	–	00H
FF48H	16-bit timer mode control register 5	TMC5			○	○	–	
FF4AH	Clock timer mode control register	WTM			○	○	–	
FF4EH	Comparator mode register 0	CMPRM0			○	○	–	
FF50H	8-bit compare register 0	CR00		W	–	○	–	Undefined
FF51H	8-bit timer register 0	TM0		R	–	○	–	00H
FF53H	8-bit timer mode control register 0	TMC0		R/W	○	○	–	
FF54H	8-bit compare register 1	CR10		W	–	○	–	Undefined
FF55H	8-bit timer register 1	TM1		R	–	○	–	00H

Notes 1. When read with an 8-bit memory manipulation instruction, the eight high-order bits of the 10-bit conversion result are read.

2. CR50, TM5, and TCP5 are designed for 16-bit access. They can also be accessed in 8-bit mode, however. In 8-bit access mode, use direct addressing.

3. 16-bit access is allowed only with short direct addressing.

Table 4-1. Special Function Registers (2/2)

Address	Special function register (SFR) name	Symbol	R/W	Number of bits manipulated simultaneously			When reset
				1 bit	8 bits	16 bits	
FF57H	8-bit timer mode control register 1	TMC1	R/W	○	○	–	00H
FF58H	8-bit compare register 2	CR20	W	–	○	–	Undefined
FF59H	8-bit timer register 2	TM2	R	–	○	–	00H
FF5BH	8-bit timer mode control register 2	TMC2	R/W	○	○	–	
FF70H	Asynchronous serial interface mode register	ASIM		○	○	–	
FF71H	Asynchronous serial interface status register	ASIS	R	–	○	–	
FF72H	Serial operation mode register 0	CSIM0	R/W	○	○	–	
FF73H	Baud rate generator control register	BRGC		–	○	–	
FF80H	A/D converter mode register	ADM		○	○	–	
FF84H	A/D input selection register	ADS		○	○	–	
FFB0H	LCD display mode register	LCDM		○	○	–	
FFB1H	LCD port selector	LPS		○	○	–	
FFB2H	LCD clock control register	LCDC		○	○	–	
FFE0H	Interrupt request flag register 0	IF0		○	○	–	
FFE1H	Interrupt request flag register 1	IF1		○	○	–	
FFE4H	Interrupt mask flag register 0	MK0		○	○	–	FFH
FFE5H	Interrupt mask flag register 1	MK1		○	○	–	
FFECH	External interrupt mode register 0	INTM0		–	○	–	00H
FFEDH	External interrupt mode register 1	INTM1		–	○	–	
FFF0H	Subsystem clock oscillation mode register	SCKM		○	○	–	
FFF2H	Subclock control register	CSS		○	○	–	
FFF3H	Pull-up resistor option register 1	PU1		○	○	–	
FFF4H	Pull-up resistor option register 2	PU2		○	○	–	
FFF5H	Key return mode register	KRM		○	○	–	
FFF7H	Pull-up resistor option register 0	PU0		○	○	–	
FFF9H	Watchdog timer mode register	WDTM		○	○	–	
FFFAH	Oscillation settling time selection register	OSTS		–	○	–	04H
FFFBH	Processor clock control register	PCC		○	○	–	02H

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

5.1.1 Port functions

The μPD789415, μPD789416, and μPD789417 are provided with the ports shown in Figure 5-1. These ports are used to enable several types of control. Table 5-1 lists the functions of each port.

These ports, while originally designed as digital input/output ports, can also be used for other functions, as summarized in **Chapter 3**.

Figure 5-1. Port Types
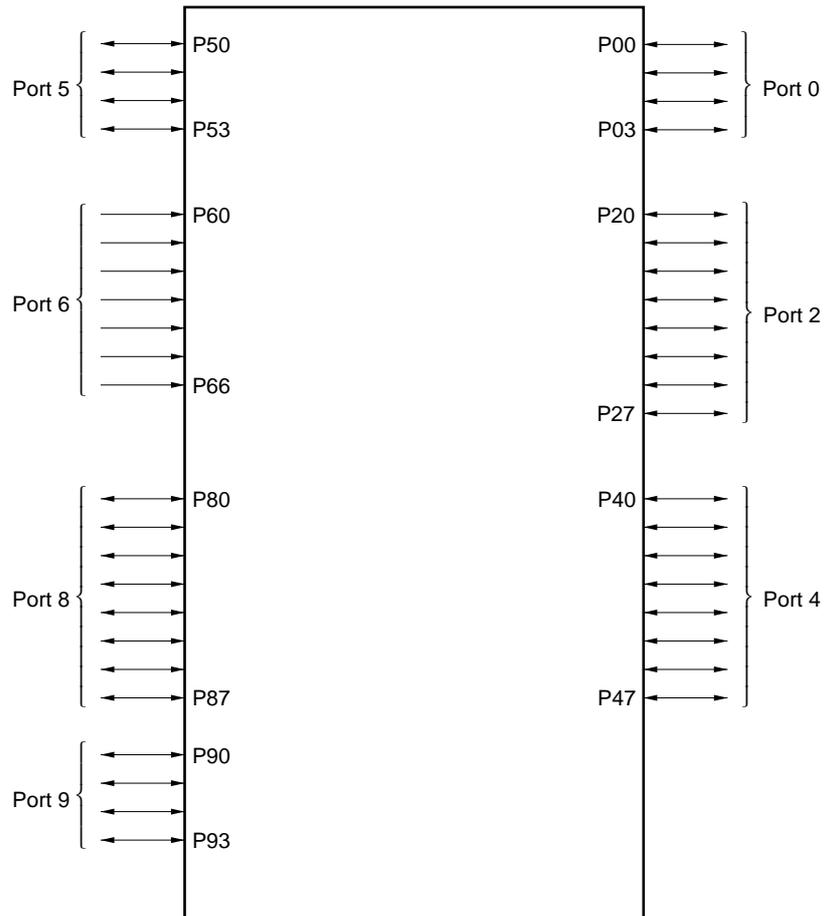
Table 5-1. Port Functions

Port name	Pin name	Description
Port 0	P00-P03	Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.
Port 2	P20-P27	Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.
Port 4	P40-P47	Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.
Port 5	P50-P53	N-channel open-drain input/output port. Each bit of the port can be separately specified as being for input or output. Whether the port itself is to contain a pull-up resistor is specified with a mask option.
Port 6	P60-P66	Input-only port
Port 8	P80-P87	Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.
Port 9	P90-P93	Input/output port. Each bit of the port can be separately specified as being for input or output. A port used for input can be connected to an internal pull-up resistor by means of software specification.

5.1.2 Port configuration

The hardware configuration of the ports is as follows.

Table 5-2. Port Configuration

Item	Configuration
Control register	Port mode register (PMm, where m = 0, 2, 4, 5, 8, or 9) Pull-up resistor option register (PU0 to PU2)
Port pins	Total: 43 (36 input/output and 7 input-only pins)
Pull-up resistors	Total: 36 (internal pull-up resistors can be used as specified by software, and whether a port itself is to contain pull-up resistors can be specified with a mask option)

Figure 5-2. Basic Port Configuration
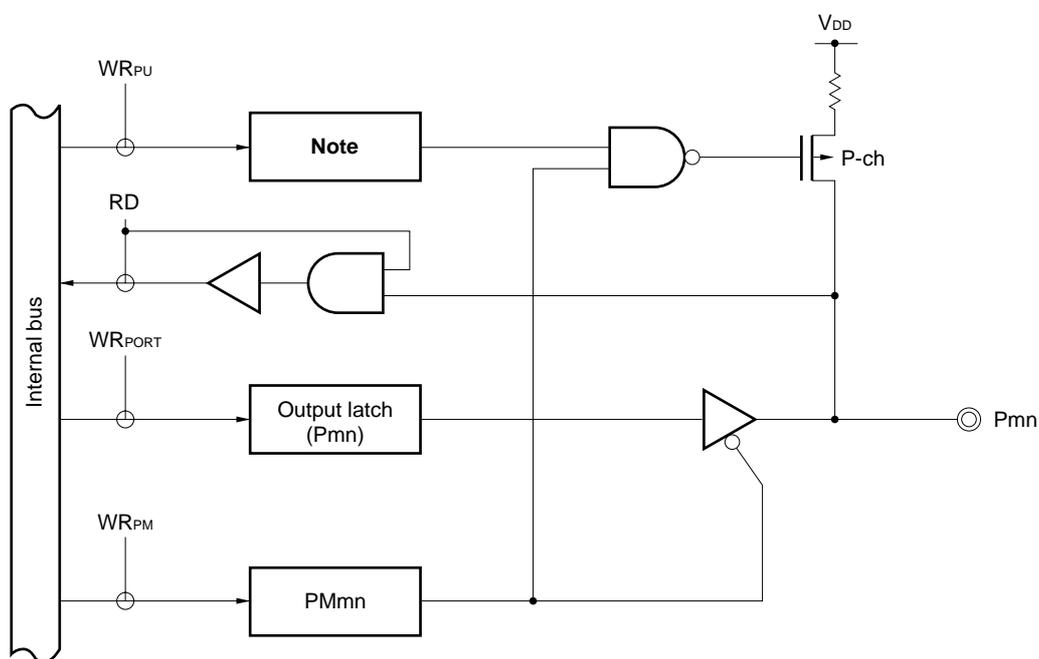
Note Each bit of the pull-up resistor option registers (PU0 to PU2)
   PU00 and PU04 for PU0
   PU120 to PU127 for PU1
   PU280, PU282, PU284, PU286, PU290, and PU292 for PU2
   For details, see **(2)** in **Section 5.1.3**.

Caution   **Figure 5-2 shows the basic configuration of the input/output ports. The configuration differs depending on the functions assigned to the dual-function pins.**

Remark PMmn : Bit n of port mode register m, where m = 0, 2, 4, 5, 8, or 9, and n = 0 to 7
   Pmn : Bit n of port m
   RD   : Port read signal
   WR   : Port write signal

5.1.3 Port function control registers

The following two types of registers are used to control the ports.

- Port mode registers (PM0, PM2, PM4, PM5, PM8, and PM9)
- Pull-up resistor option registers (PU0 to PU2)

(1) Port mode registers (PM0, PM2, PM4, PM5, PM8, and PM9)

The port mode registers separately specify each port bit as being for input or output.

Each port mode register is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input writes FFH into the port mode registers.

When port pins are used for secondary functions, the corresponding port mode register and output latch must be set or reset as described in Table 5-3.

Caution When port 2 is acting as an output port, and its output level is changed, an interrupt request flag is set, because this port is also used as the input for an external interrupt. To use port 2 in output mode, therefore, the interrupt mask flag must be set to 1 in advance.

Table 5-3. Port Mode Register and Output Latch Settings for Using Secondary Functions

Pin name	Secondary function		PMxx	Pxx
	Name	Input/output		
P23	CMPTOUT0	Output	0	0
	TO2	Output	0	0
P24	INTP0	Input	1	×
	TI0	Input	1	×
P25	INTP1	Input	1	×
	TI1	Input	1	×
P26	INTP2	Input	1	×
	TO5	Output	0	0
P27	INTP3	Input	1	×
	CPT5	Input	1	×
P40-P45[Note]	KR0-KR5	Input	1	×
P60	ANI0	Input	1	×
	CMPIN0	Input	1	×
P61	ANI1	Input	1	×
	CMPREF0	Input	1	×
P62-P66	ANI2-ANI6	Input	1	×
P80-P87	S27-S20	Output	0	0
P90-P93	S19-S16	Output	0	0

Note To use the secondary functions, set the key return mode register (KRM) to 1.
(See **(6)** in **Section 6.3**.)

Caution When port 2 is being used as a serial interface, it is necessary to specify whether the port is an input or output port, and to set the output latch accordingly. See Table 5-13 for an explanation of how to make this specification.

Remark × : Don't care
PMxx : Port mode register
Pxx : Port output latch

Figure 5-3. Port Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
PM0	1	1	1	1	PM03	PM02	PM01	PM00	FF20H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FF24H	FFH	R/W
PM5	1	1	1	1	PM53	PM52	PM51	PM50	FF25H	FFH	R/W
PM8	PM87	PM86	PM85	PM84	PM83	PM82	PM81	PM80	FF28H	FFH	R/W
PM9	1	1	1	1	PM93	PM92	PM91	PM90	FF29H	FFH	R/W

PMmn	Pmn pin input/output mode selection (m = 0, 2, 4, 5, 8, or 9; n = 0 to 7)
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

(2) Pull-up resistor option registers (PU0 to PU2)

These registers are used to specify whether an internal pull-up resistor is to be used at each port. An internal pull-up resistor can be used only for a port that is in input mode and for which the use of the internal pull-up resistor is selected using the corresponding pull-up resistor option register. If a port is in output mode, an internal pull-up resistor is not used with it, even if the use of an internal pull-up resistor has been specified using the corresponding option register. The same applies when the port pin is used for a secondary function.

PU0 to PU2 are manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears PU0 to PU2 to 00H.

Figure 5-4. Format of Pull-Up Resistor Option Register 0

	7	6	5	④	3	2	1	⓪	Address	When reset	R/W
PU0	0	0	0	PU04	0	0	0	PU00	FFF7H	00H	R/W

PU0m	Pm internal pull-up resistor selection[Note]
	(m = 0 or 4)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Note PU0 selects whether internal pull-up resistors are to be used in 8-bit units, except for port 0, for which internal pull-up resistors can be used with only four bits (P00 to P03).

Caution   Bits 1, 2, 3, 5, 6, and 7 must be fixed to 0.

Figure 5-5. Format of Pull-Up Resistor Option Register 1

	⑦	⑥	⑤	④	③	②	①	⓪	Address	When reset	R/W
PU1	PU127	PU126	PU125	PU124	PU123	PU122	PU121	PU120	FFF3H	00H	R/W

PU12m	P2 internal pull-up resistor selection[Note]
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Note PU1 selects whether internal pull-up resistors are to be used in 1-bit units.

Figure 5-6. Format of Pull-Up Resistor Option Register 2

	7	6	⑤	④	③	②	①	⓪	Address	When reset	R/W
PU2	0	0	PU292	PU290	PU286	PU284	PU282	PU280	FFF4H	00H	R/W

PU2mn	Pm internal pull-up resistor selection[Note]
	(m = 8 or 9; n = 0, 2, 4, or 6)
0	Internal pull-up resistor not used
1	Internal pull-up resistor used

Note PU2 selects whether internal pull-up resistors are to be used in 2-bit units (bit n and bit n+1).

Caution   Bits 6 and 7 must be fixed to 0.

5.2 Clock Generator

5.2.1 Clock generator functions

The clock generator generates the clock pulse to be supplied to the CPU and peripheral hardware. There are two types of system clock oscillators:

- Main system clock oscillator
  This circuit generates a frequency of 1 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction or by using the processor clock control register.
- Subsystem clock oscillator
  This circuit generates 32.768 kHz. Oscillation can be stopped by using the suboscillation mode register.

5.2.2 Clock generator configuration

The clock generator consists of the following hardware.

Table 5-4. Clock Generator Configuration

Item	Configuration
Control register	Processor clock control register (PCC) Suboscillation mode register (SCKM) Subclock control register (CSS)
Oscillators	Main system clock oscillator Subsystem clock oscillator

Figure 5-7. Clock Generator Block Diagram
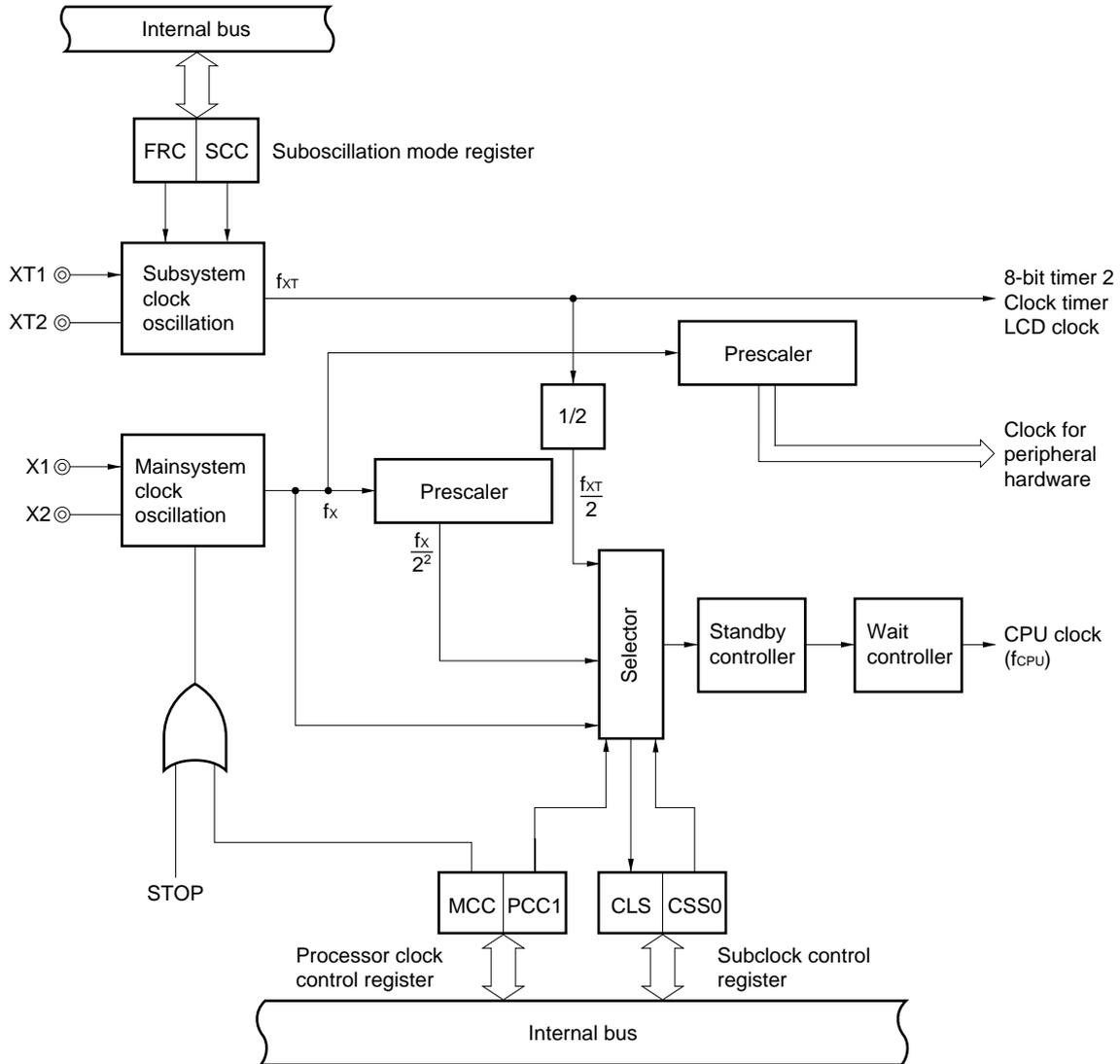
5.2.3 Clock generator control registers

The clock generator is controlled using the following registers.

- Processor clock control register (PCC)
- Suboscillation mode register (SCKM)
- Subclock control register (CSS)

(1) Processor clock control register (PCC)

The PCC selects a CPU clock and specifies a corresponding frequency division ratio.

It is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input loads 02H into the PCC.

Figure 5-8. Processor Clock Control Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
PCC	MCC	0	0	0	0	0	PCC1	0	FFFBH	02H	R/W

MCC	Control of main system clock oscillator operation
0	Operation enabled
1	Operation disabled

CSS0	PCC1	CPU clock (f_{CPU}) selection[Note]
0	0	f_X (0.2 μs)
0	1	$f_X/2^2$ (0.8 μs)
1	0	$f_{XT}/2$ (61 μs)
1	1	

Note A CPU clock is selected by a combination of the PCC1 flag in the processor clock control register (PCC) and the CSS0 flag in the subclock control register (CSS). (See **(3)** in **Section 5.2.3**.)

Caution   Bit 0 and bits 2 to 6 must be fixed to 0.

Remarks 1. f_X : Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The parenthesized values apply to operation with f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

4. Minimum instruction execution time: 2 f_{CPU}

- f_{CPU} = 0.2 μs : 0.4 μs
- f_{CPU} = 0.8 μs : 1.6 μs
- f_{CPU} = 61 μs : 122 μs

(2) Suboscillation mode register (SCKM)

The SCKM selects a feedback resistor for the subsystem clock, and controls the oscillation of the clock.

The subsystem clock is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the SCKM to 00H.

Figure 5-9. Suboscillation Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
SCKM	0	0	0	0	0	0	FRC	SCC	FFF0H	00H	R/W

FRC	Feedback resistor selection
0	Internal feedback resistor used
1	Internal feedback resistor not used

SCC	Control of subsystem clock oscillator operation
0	Operation enabled
1	Operation disabled

Caution   Bits 2 to 7 must be fixed to 0.

(3) Subclock control register (CSS)

The CSS specifies whether the main system or subsystem clock oscillator is to be selected. It also specifies how the CPU clock operates.

It is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the CSS to 00H.

Figure 5-10. Subclock Control Register Format

	7	6	5	4	3	2	1	0	Address	When reset	R/W
CSS	0	0	CLS	CSS0	0	0	0	0	FFF2H	00H	R/W

CLS	CPU clock operation status
0	Operation based on the output of the divided main system clock
1	Operation based on the subsystem clock

CSS0	Selection of the main system or subsystem clock oscillator
0	Divided output from the main system clock oscillator
1	Output form the subsystem clock oscillator

Caution   Bits 0, 1, 2, 3, 6, and 7 must be fixed to 0.

5.3 16-Bit Timer/Counter

5.3.1 16-Bit timer/counter functions
The 16-bit timer/counter (TM5) has the following functions.

(1) Timer interrupt
An interrupt is generated if the TM5 count matches a comparison value.

(2) Timer output
The timer output can be controlled if the count matches a comparison value.

(3) Count capture
The count in TM5 is captured into the capture register in synchronization with a capture trigger.

5.3.2 16-bit timer/counter configuration
The 16-bit timer/counter (TM5) consists of the following hardware.

Table 5-5. 16-Bit Timer/Counter Configuration

Item	Configuration
Timer register	16 bits × 1 (TM5)
Register	Compare register : 16 bits × 1 (CR50) Capture register : 16 bits × 1 (TCP5)
Timer output	1 (TO5)
Control register	16-bit timer mode control register 5 (TMC5) Port mode register 2 (PM2)

Figure 5-11. 16-Bit Timer/Counter Block Diagram
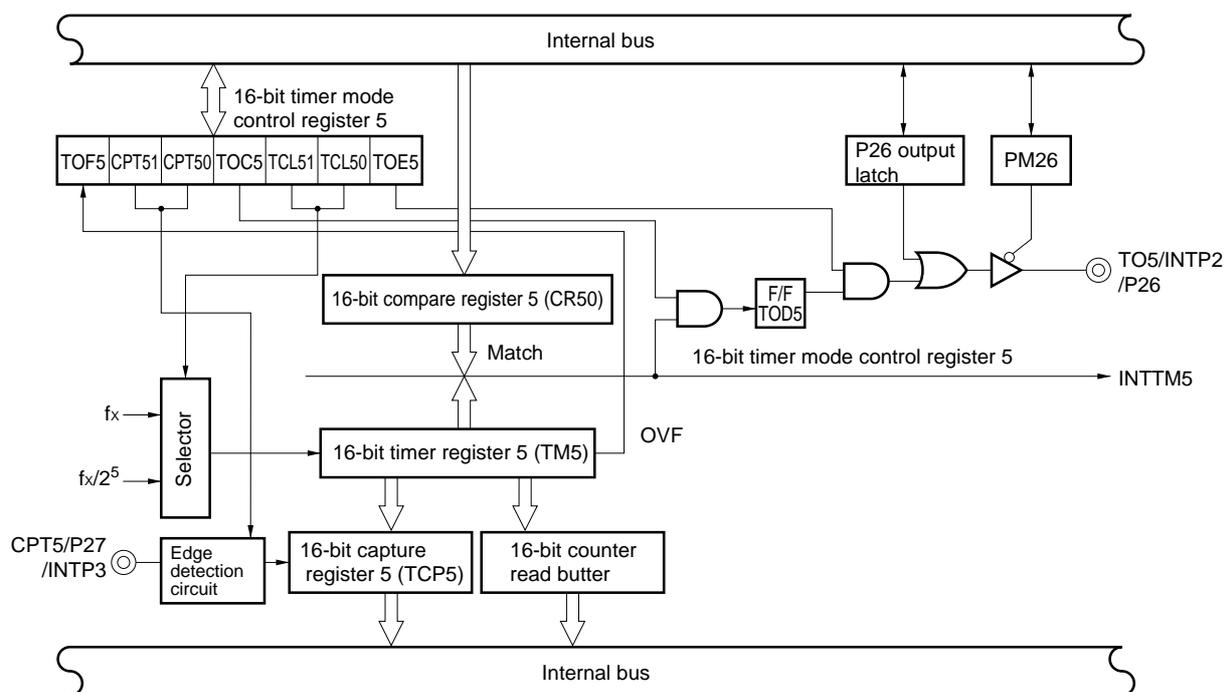
(1) 16-bit compare register 5 (CR50)

A value specified in CR50 is compared with the count in 16-bit timer register 5 (TM5). If they match, an interrupt request (INTTM5) is issued.

CR50 is set using an 8-bit or 16-bit memory manipulation instruction. Any value from 0000H to FFFFH can be set.

A $\overline{\text{RESET}}$ input loads FFFFH into CR50.

> **Cautions 1. CR50 is designed to be manipulated using a 16-bit memory manipulation instruction. It can also be manipulated using 8-bit memory manipulation instructions, however. When an 8-bit memory manipulation instruction is used to set CR50, it must be in a direct addressing access mode.**
> **2. To re-set CR50 during count operation, it is necessary to disable interrupts in advance, using an interrupt mask flag register (MK1). It is also necessary to disable inversion of the timer output data, using 16-bit timer mode control register 5 (TMC5).**

(2) 16-bit timer register 5 (TM5)

TM5 is used to count the number of pulses.

The contents of TM5 are read using an 8-bit or 16-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears TM5 to 0000H.

> **Cautions 1. The count becomes undefined when STOP mode is deselected, because the count operation is performed before oscillation settles.**
> **2. TM5 is designed to be manipulated using a 16-bit memory manipulation instruction. It can also be manipulated using 8-bit memory manipulation instructions, however. When an 8-bit memory instruction is used to manipulate TM5, it must be in a direct addressing access mode.**
> **3. When an 8-bit memory manipulation instruction is used to manipulate TM5, the lower and upper bytes must be read as a pair, in this order.**

(3) 16-bit capture register 5 (TCP5)

TCP5 captures the contents of 16-bit timer 5 (TM5).

It is set using an 8-bit or 16-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input makes TCP5 undefined.

> **Caution TCP5 is designed to be manipulated using a 16-bit memory manipulation instruction. It can also be manipulated using 8-bit memory manipulation instructions, however. When an 8-bit memory manipulation instruction is used to manipulate TCP5, it must be in a direct addressing access mode.**

(4) 16-bit counter read buffer

This buffer is used to latch and hold the count for 16-bit timer 5 (TM5).

5.3.3 16-bit timer/counter control registers

The 16-bit timer/counter (TM5) is controlled by the following registers.

- 16-bit timer mode control register 5 (TMC5)
- Port mode register 2 (PM2)

(1) 16-bit timer mode control register 5 (TMC5)

TMC5 controls the count clock and capture edge settings.

TMC5 is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears TMC5 to 00H.

Figure 5-12. 16-Bit Timer Mode Control Register 5 Format

Symbol	7	⑥	5	4	3	2	1	⓪	Address	When reset	R/W
TMC5	TOD5	TOF5	CPT51	CPT50	TOC5	TCL51	TCL50	TOE5	FF48H	00H	R/W[Note 1]

TOD5	Causes the 16-bit timer output data to be held.

TOF5	Overflow flag control
0	Reset or cleared by software
1	Set when the 16-bit timer overflows

CPT51	CPT50	Capture edge selection
0	0	Capture operation disabled
0	1	Captured at the rising edge at the CPT5 pin
1	0	Captured at the falling edge at the CPT5 pin
1	1	Captured at both the rising and falling edges at the CPT5 pin

TOC5	Timer output data inversion control
0	Inversion disabled
1	Inversion enabled

TCL51	TCL50	16-bit timer register 5 count clock selection
0	0	f_X (5.0 MHz)[Note 2]
0	1	$f_X/2^5$ (156.3 kHz)[Note 3]
Other settings		Not to be specified

TOE5	16-bit timer/counter 5 output control
0	Output disabled (port mode)
1	Output enabled

Notes 1. Bit 7 is read-only.

    2. If the count clock is set to f_X (TCL51 = 0, TCL50 = 0), the capture function cannot be used. To read the timer output, the CPU clock must be set to the main system clock high-speed mode (PCC1 = 0, CSS0 = 0). (See **Figure 5-8.**)

    3. To read the timer output, the CPU clock must be set to the main system clock (PCC1 = 0, CSS0 = 0 or PCC1 = 1, CSS0 = 0). (See **Figure 5-8.**)

Remarks 1. f_X: Main system clock oscillation frequency

     2. The parenthesized values apply to operation at f_X = 5.0 MHz.

(2) Port mode register 2 (PM2)

PM2 specifies whether each bit of port 2 is used for input or output.

To use the P26/INTP2/TO5 pin for timer output, the PM26 and P26 output latches must be reset to 0.

PM2 is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input loads FFH into PM2.

Figure 5-13. Port Mode Register 2 Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PM26	P26 pin input/output mode selection
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

5.4 8-Bit Timer/Event Counter

5.4.1 8-bit timer/event counter functions

Devices of the μPD789417 subseries have two timer/event counters (TM0 and TM1) and one timer counter (TM2). Readers who are seeking a description of TM2 should read the term "timer/event counter" as "timer counter."

The 8-bit timer/event counters (TM0, TM1, and TM2) have the following functions.

(1) 8-bit interval timer

This timer causes interrupts to be issued at specified intervals.

(2) External event counter (TM0 and TM1)

This counter is used to count the number of pulses input from an external source.

(3) Square wave output (TM2 only)

A square wave of any frequency can be output.

Table 5-6. 8-Bit Timer/Event Counter Types and Functions

		TM0	TM1	TM2
Type	Interval timer	One channel	One channel	One channel
	External event counter	○	○	×
Function	Timer output	×	×	○
	Interrupt request	○	○	○

5.4.2 8-bit timer/event counter configuration

The 8-bit timer/event counter consists of the following hardware.

Table 5-7. 8-Bit Timer/Event Counter Configuration

Item	Configuration
Timer register	8 bits × 3 (TM0, TM1, TM2)
Register	Compare registers: 8 bits × 3 (CR00, CR10, CR20)
Timer output	1 (TO2)
Control register	8-bit timer mode control registers 0, 1, 2 (TMC0, TMC1, TMC2) Port mode register 2 (PM2)

Figure 5-14. 8-Bit Timer/Event Counters 0 and 1 (TM0 and TM1) Block Diagram
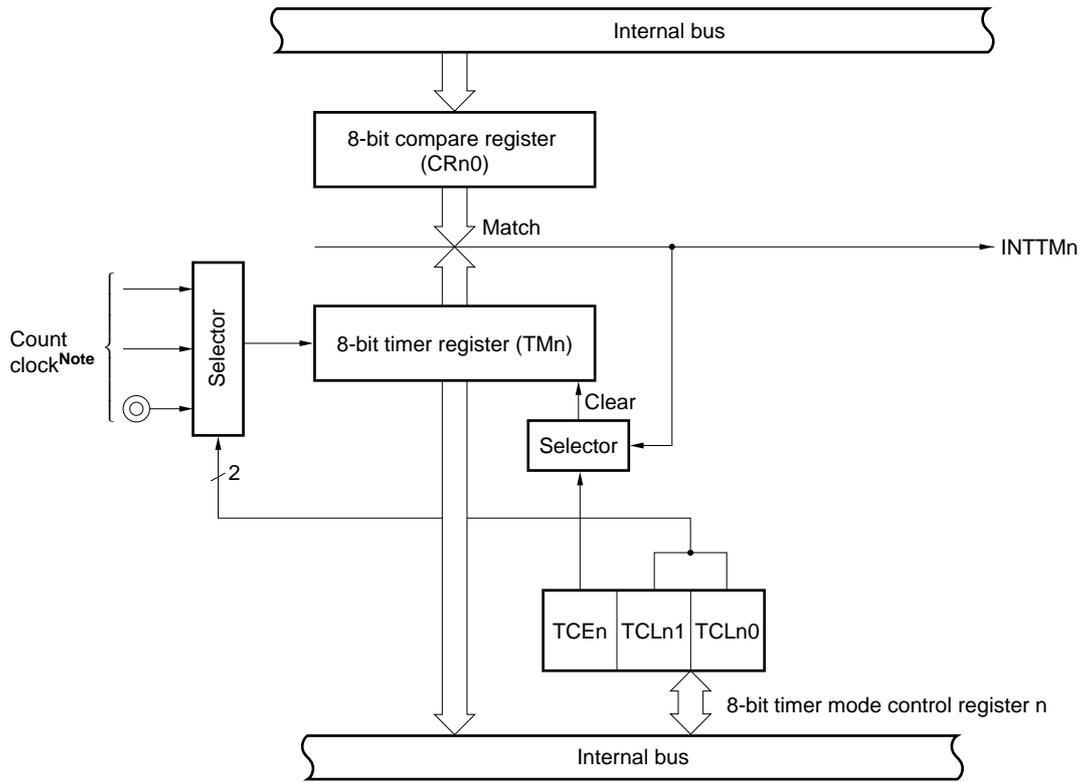
Note $f_X/2^6$, $f_X/2^9$, TI0/P24/INTP0 for TM0
$f_X/2^4$, $f_X/2^8$, TI1/P25/INTP1 for TM1

Remark   n = 0 or 1

Figure 5-15. 8-Bit Timer Counter 2 (TM2) Block Diagram

Note See **Section 5.8** for details of the comparator.

(1) 8-bit compare register n (CRn0)

A value specified in CRn0 is compared with the count in 8-bit timer register n (TMn). If they match, an interrupt request (INTTMn) is issued.

CRn0 is set using an 8-bit memory manipulation instruction. Any value from 00H to FFH can be set.

A $\overline{\text{RESET}}$ input makes CRn0 undefined.

Remark n = 0 to 2

(2) 8-bit timer register n (TMn)

TMn is used to count the number of pulses.

Its contents are read using an 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears TMn to 00H.

Remark n = 0 to 2

5.4.3 8-bit timer/event counter control registers

The 8-bit timer/event counter is controlled by the following registers.

- 8-bit timer mode control registers 0, 1, and 2 (TMC0, TMC1, and TMC2)
- Port mode register 2 (PM2)

(1) 8-bit timer mode control register 0 (TMC0)

TMC0 determines whether to enable or disable 8-bit timer register 0 (TM0) and specifies the count clock for TM0.

TMC0 is set using a 1-bit or 8-bit memory manipulation instruction.

A RESET input clears TMC0 to 00H.

Figure 5-16. 8-Bit Timer Mode Control Register 0 Format

Symbol	⑦	6	5	4	3	2	1	0	Address	When reset	R/W
TMC0	TCE0	0	0	0	0	TCL01	TCL00	0	FF53H	00H	R/W

TCE0	8-bit timer register 0 operation control
0	Operation disabled (TM0 is cleared to 0.)
1	Operation enabled

TCL01	TCL00	8-bit timer register 0 count clock selection
0	0	$f_X/2^6$ (78.1 kHz)
0	1	$f_X/2^9$ (9.77 kHz)
1	0	Rising edge of TI0
1	1	Falling edge of TI0

Caution Always stop the timer before setting TMC0.

Remarks 1. f_X: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_X = 5.0 MHz.

(2) 8-bit timer mode control register 1 (TMC1)

TMC1 determines whether to enable or disable 8-bit timer register 1 (TM1) and specifies the count clock for TM1.

TMC1 is set using a 1-bit or 8-bit memory manipulation instruction.

A RESET input clears TMC1 to 00H.

Figure 5-17. 8-Bit Timer Mode Control Register 1 Format

Symbol	⑦	6	5	4	3	2	1	0	Address	When reset	R/W
TMC1	TCE1	0	0	0	0	TCL11	TCL10	0	FF57H	00H	R/W

TCE1	8-bit timer register 1 operation control
0	Operation disabled (TM1 is cleared to 0.)
1	Operation enabled

TCL11	TCL10	8-bit timer register 1 count clock selection
0	0	$f_x/2^4$ (312.5 kHz)
0	1	$f_x/2^8$ (19.5 kHz)
1	0	Rising edge of TI1
1	1	Falling edge of TI1

Caution   Always stop the timer before setting TMC1.

Remarks 1. f_x: Main system clock oscillation frequency
   2. The parenthesized values apply to operation at f_x = 5.0 MHz.

(3) 8-bit timer mode control register 2 (TMC2)

TMC2 determines whether to enable or disable 8-bit timer register 2 (TM2) and specifies the count clock for TM2. It also controls the operation of the output control circuit of 8-bit timer counter 2.

TMC2 is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears TMC2 to 00H.

Figure 5-18. 8-Bit Timer Mode Control Register 2 Format

Symbol	⑦	6	5	4	3	2	1	⓪	Address	When reset	R/W
TMC2	TCE2	0	0	0	0	TCL21	TCL20	TOE2	FF5BH	00H	R/W

TCE2	8-bit timer register 2 operation control
0	Operation disabled (TM2 is cleared to 0.)
1	Operation enabled

TCL21	TCL20	8-bit timer register 2 count clock selection
0	0	$f_X/2^3$ (625 kHz)
0	1	$f_X/2^7$ (39.1 kHz)
1	0	f_{XT} (32.768 kHz)
1	1	Not to be specified

TOE2	8-bit timer counter 2 output control
0	Output disabled (port mode)
1	Output enabled

Caution   Always stop the timer before setting TMC2.

Remarks 1. f_X : Main system clock oscillation frequency

2. f_{XT}: Subsystem clock oscillation frequency

3. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

(4) Port mode register 2 (PM2)

PM2 specifies whether each bit of port 2 is used for input or output.

To use the P23/CMPTOUT0/TO2 pin for timer output, the PM23 and P23 output latches must be reset to 0.

PM2 is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input loads FFH into PM2.

Figure 5-19. Port Mode Register 2 Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PM23	P23 pin input/output mode selection
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

5.5 Clock Timer

5.5.1 Clock timer functions

The clock timer has the following functions.

- Clock timer
- Interval timer

The clock and interval timers can be used at the same time.
Figure 5-20 is a block diagram of the clock timer.

Figure 5-20. Clock Timer Block Diagram
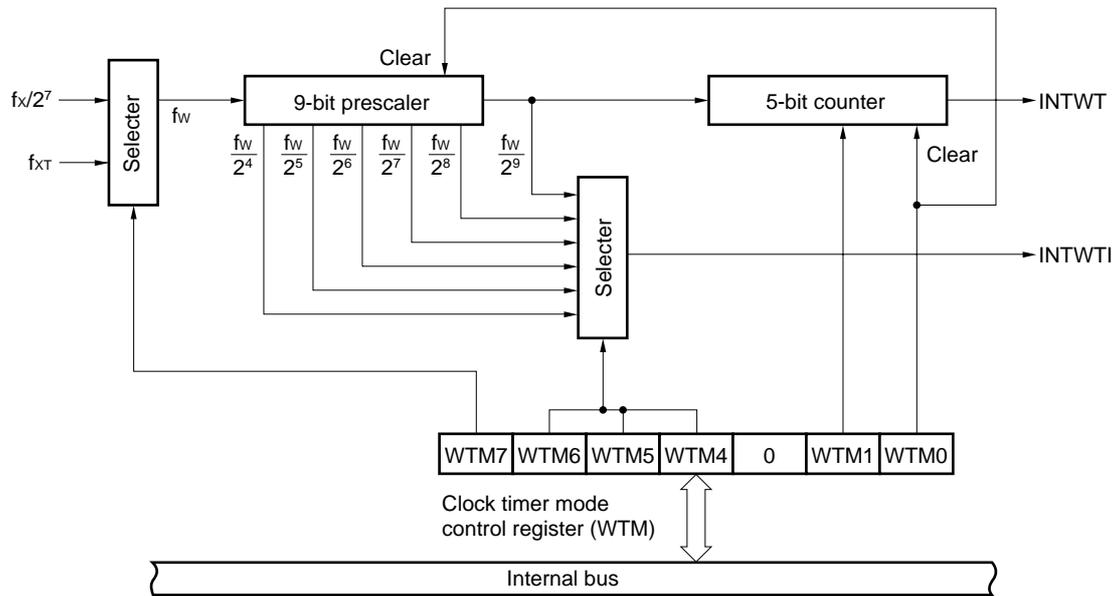
(1) Clock timer

The 4.19-MHz main system clock or 32.768-kHz subsystem clock is used to issue an interrupt request (INTWT) at 0.5-second intervals.

Caution When the main system clock is operating at 5.0 MHz, it cannot be used to generate a 0.5-second interval. In this case, the subsystem clock, which operates at 32.768 kHz, should be used instead.

(2) Interval timer

The interval timer is used to generate an interrupt request (INTWT) at specified intervals.

Table 5-8. Interval Generated Using the Interval Timer

Interval	Operation at f_X = 5.0 MHz	Operation at f_X = 4.19 MHz	Operation at f_{XT} = 32.768 kHz
$2^4 \times 1/f_W$	409.6 μs	489 μs	488 μs
$2^5 \times 1/f_W$	819.2 μs	978 μs	977 μs
$2^6 \times 1/f_W$	1.64 ms	1.96 ms	1.95 ms
$2^7 \times 1/f_W$	3.28 ms	3.91 ms	3.91 ms
$2^8 \times 1/f_W$	6.55 ms	7.82 ms	7.81 ms
$2^9 \times 1/f_W$	13.1 ms	15.6 ms	15.6 ms

Remark f_W : Clock timer clock frequency ($f_X/2^7$ or f_{XT})

f_X : Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

5.5.2 Clock timer configuration

The clock timer consists of the following hardware.

Table 5-9. Clock Timer Configuration

Item	Configuration
Counter	5 bits
Prescaler	9 bits
Control register	Clock timer mode control register (WTM)

5.5.3 Register for controlling the clock timer

The clock timer mode control register (WTM) is used to control the clock timer.

- Clock timer mode control register (WTM)

   The WTM selects a count clock for the clock timer and specifies whether to enable clocking of the timer. It also specifies the prescaler interval and how the 5-bit counter is controlled.

   The WTM is manipulated using a 1-bit or 8-bit memory manipulation instruction.

   A $\overline{\text{RESET}}$ input clears the WTM to 00H.

Figure 5-21. Clock Timer Mode Control Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
WTM	WTM7	WTM6	WTM5	WTM4	0	0	WTM1	WTM0	FF4AH	00H	R/W

WTM7	Clock timer count clock selection
0	$f_X/2^7$ (39.1 kHz)
1	f_{XT} (32.768 kHz)

WTM6	WTM5	WTM4	Prescaler interval selection
0	0	0	$2^4/f_W$ (488 μs)
0	0	1	$2^5/f_W$ (977 μs)
0	1	0	$2^6/f_W$ (1.95 ms)
0	1	1	$2^7/f_W$ (3.91 ms)
1	0	0	$2^8/f_W$ (7.81 ms)
1	0	1	$2^9/f_W$ (15.6 ms)
Other settings			Not to be set

WTM1	Control of 5-bit counter operation
0	Cleared after stop
1	Started

WTM0	Clock timer operation
0	Operation disabled (both prescaler and timer cleared)
1	Operation enabled

Remarks 1. f_W : Clock timer clock frequency ($f_X/2^7$ or f_{XT})

   2. f_X : Main system clock oscillation frequency

   3. f_{XT}: Subsystem clock oscillation frequency

   4. The parenthesized values apply to operation at f_X = 5.0 MHz or f_W = 32.768 kHz.

5.6 Watchdog Timer

5.6.1 Watchdog timer functions
The watchdog timer has the following functions.

(1) Watchdog timer
The watchdog timer is used to detect unintended program loops. If an unintended program loop is detected, a nonmaskable interrupt or $\overline{\text{RESET}}$ signal is generated.

(2) Interval timer
The interval timer is used to generate interrupts at specified intervals.

5.6.2 Watchdog timer configuration
The watchdog timer consists of the following hardware.

Table 5-10. Watchdog Timer Configuration

Item	Configuration
Control register	Timer clock selection register 2 (TCL2) Watchdog timer mode register (WDTM)

Figure 5-22. Watchdog Timer Block Diagram
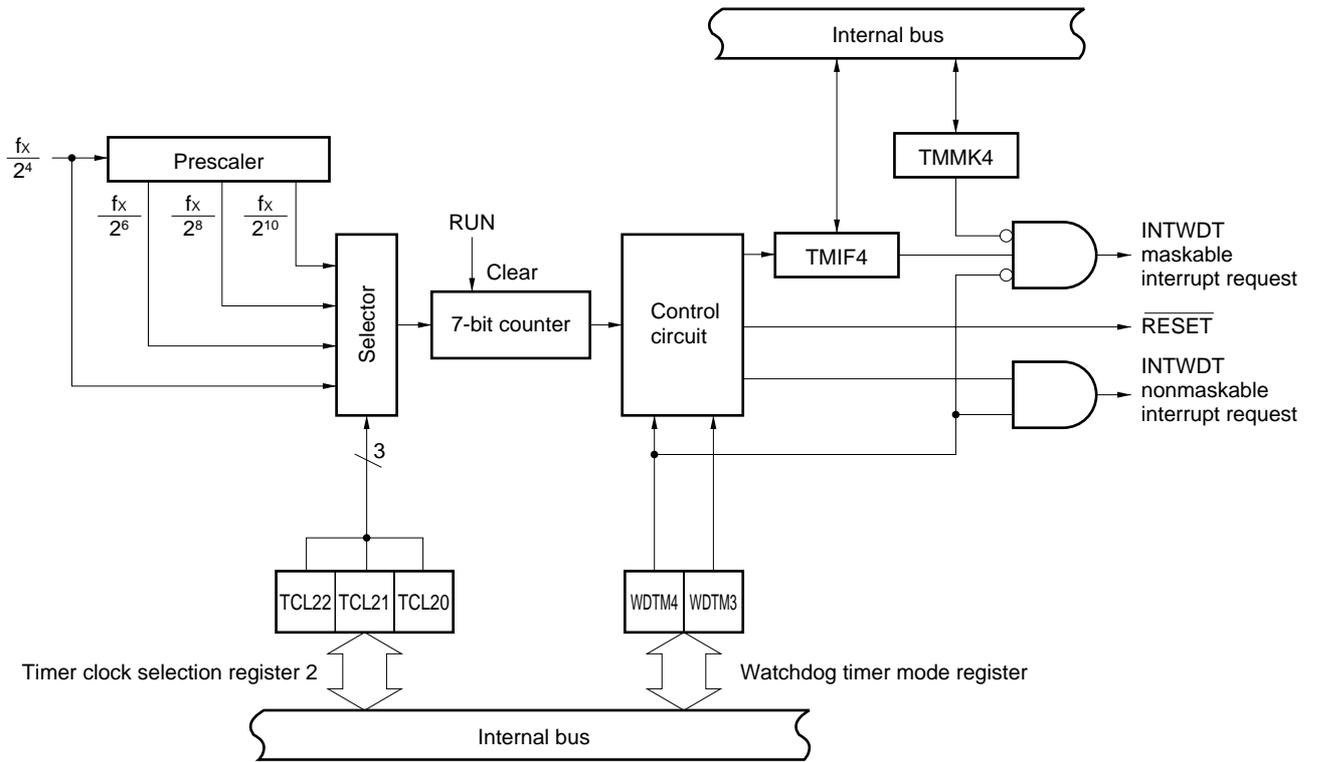
5.6.3 Watchdog timer control registers

The watchdog timer is controlled by the following registers.

- Timer clock selection register 2 (TCL2)
- Watchdog timer mode register (WDTM)

(1) Timer clock selection register 2 (TCL2)

TCL2 specifies the count clock for the watchdog timer.

TCL2 is set using an 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears TCL2 to 00H.

Figure 5-23. Timer Clock Selection Register 2 Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
TCL2	0	0	0	0	0	TCL22	TCL21	TCL20	FF42H	00H	R/W

TCL22	TCL21	TCL20	Watchdog timer count clock selection	Interval time
0	0	0	$f_x/2^4$ (312.5 kHz)	$2^{11}/f_x$ (410 μs)
0	1	0	$f_x/2^6$ (78.1 kHz)	$2^{13}/f_x$ (1.64 ms)
1	0	0	$f_x/2^8$ (19.5 kHz)	$2^{15}/f_x$ (6.55 ms)
1	1	0	$f_x/2^{10}$ (4.88 kHz)	$2^{17}/f_x$ (26.2 ms)
Other settings			Not to be specified	

Remarks 1. f_x: Main system clock oscillation frequency

2. The parenthesized values apply to operation at f_x = 5.0 MHz.

(2) Watchdog timer mode register (WDTM)

The WDTM specifies the watchdog timer operation mode and whether to enable or disable counting.

The WDTM is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the WDTM to 00H.

Figure 5-24. Watchdog Timer Mode Register Format

Symbol	⑦	6	5	4	3	2	1	0	Address	When reset	R/W
WDTM	RUN	0	0	WDTM4	WDTM3	0	0	0	FFF9H	00H	R/W

RUN	Watchdog timer operation selection[Note 1]
0	Stops counting.
1	Clears the counter and causes it start.

WDTM4	WDTM3	Watchdog timer operation mode selection[Note 2]
0	0	Operation disabled
0	1	Internal timer mode (When an overflow occurs, a maskable interrupt is issued.)[Note 3]
1	0	Watchdog timer mode 1 (When an overflow occurs, a nonmaskable interrupt is issued.)
1	1	Watchdog timer mode 2 (When an overflow occurs, a reset operation is started.)

Notes 1. Once the RUN bit has been set (1), it is impossible to zero-clear it by software. So, once counting begins, it cannot be stopped by any means other than a $\overline{\text{RESET}}$ input.

2. Once WDTM3 and WDTM4 have been set (1), it is impossible to zero-clear them by software.

3. The interval timer starts operating when the RUN bit is set to 1.

Cautions 1. If the RUN bit is set to 1, and the watchdog timer is cleared, the actual overflow time becomes 0.8 % (maximum) less than the time specified in timer clock selection register 2.

2. To use watchdog timer mode 1 or 2, ensure that the interrupt request flag (TMIF4) is set to 0, before setting WDTM4 to 1. If TMIF4 is set to 1, selecting mode 1 or 2 causes a nonmaskable interrupt to be issued at the instant rewriting ends.

5.7   10-Bit A/D Converter

5.7.1   10-bit A/D converter functions

   The 10-bit A/D converter converts input analog voltages to digital signals with an 10-bit resolution. It can control up to seven analog input channels (ANI0 to ANI6).

   A/D conversion can be started only by software.

   One of analog inputs ANI0 to ANI6 is selected for A/D conversion. A/D conversion is performed repeatedly, with an interrupt request (INTAD) being issued each time an A/D session is completed.

5.7.2   Configuration of the 10-bit A/D converter

   The A/D converter consists of the following hardware.

Table 5-11. 10-Bit A/D Converter Configuration

Item	Configuration
Analog input	7 channels (ANI0 to ANI6)
Register	Successive approximation register (SAR) A/D conversion result register (ADCR)
Control register	A/D converter mode register (ADM) A/D input selection register (ADS)

Figure 5-25. A/D Converter Block Diagram
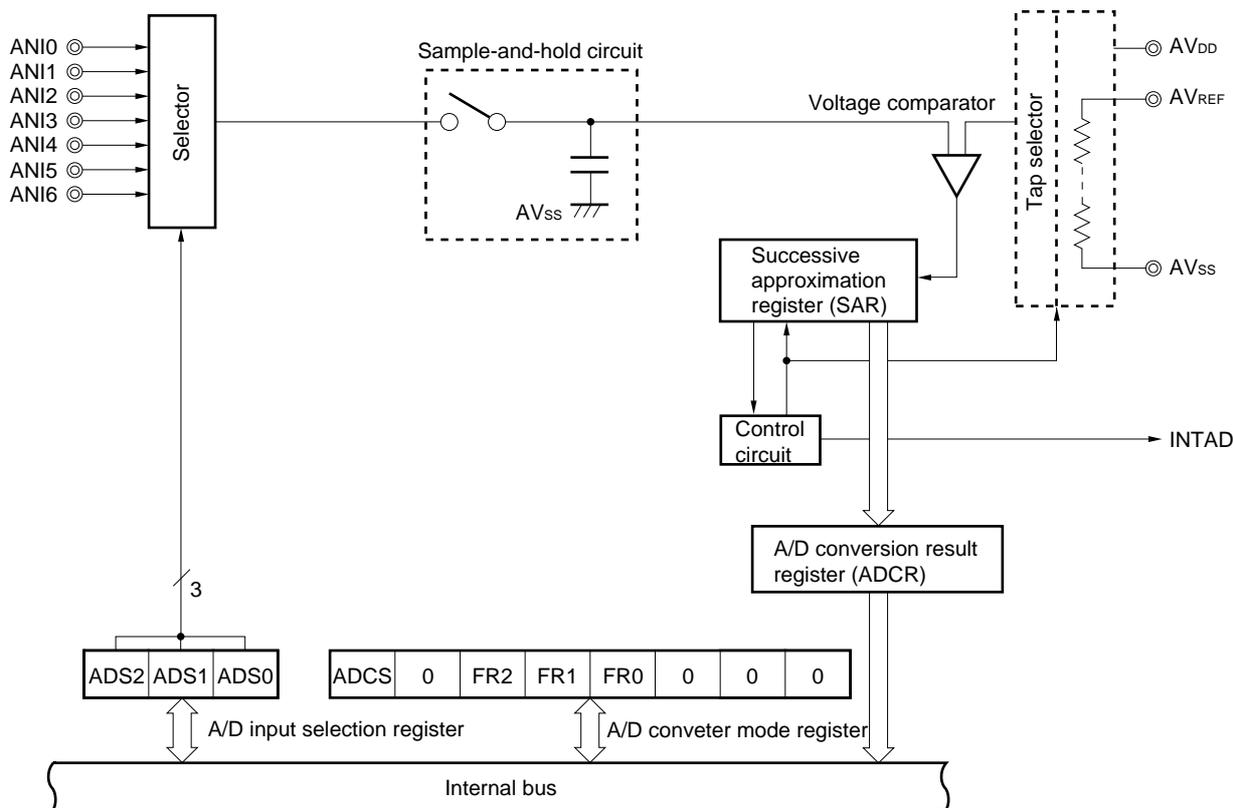
(1) Successive approximation register (SAR)

The SAR receives the result of comparing an analog input voltage and a voltage at a voltage tap (comparison voltage), received from the serial resistor string, starting from the most significant bit (MSB).

Upon receiving all the bits, down to the least significant bit (LSB), that is, upon the completion of A/D conversion, the SAR sends its contents to the A/D conversion result register.

(2) A/D conversion result register (ADCR)

The ADCR holds the result of A/D conversion. Each time A/D conversion ends, the conversion result received from the successive approximation register is loaded into the ADCR.

The ADCR can be manipulated using a 16-bit memory manipulation instruction.

The value of this register becomes unpredictable upon the input of a $\overline{\text{RESET}}$ signal.

Caution   When read with an 8-bit memory manipulation instruction, the eight high-order bits of the 10-bit conversion result are read.

(3) Sample-and-hold circuit

The sample-and-hold circuit samples consecutive analog inputs from the input circuit, one by one, and sends them to the voltage comparator. The sampled analog input voltage is held during A/D conversion.

(4) Voltage comparator

The voltage comparator compares an analog input with the voltage output by the serial resistor string.

(5) Serial resistor string

The serial resistor string is configured between AV_{REF} and AV_{SS}. It generates the reference voltages against which analog inputs are compared.

(6) ANI0 to ANI6 pins

Pins ANI0 to ANI6 are analog input pins for the A/D converter. They are used to receive the analog signals to be subject to A/D conversion.

> **Caution Do not supply pins ANI0 to ANI6 with voltages that fall outside the rated range. If a voltage greater than AV_{REF} or less than AV_{SS} (even if within the absolute maximum rating) is supplied to any of these pins, the conversion value for the corresponding channel will be undefined. Furthermore, the conversion values for the other channels may also be affected.**

(7) AV_{REF} pin

The AV_{REF} pin is a reference voltage pin for the A/D converter.

Signals received at pins ANI0 to ANI6 are converted to digital signals while referencing the voltage across the AV_{REF} and AV_{SS} pins.

(8) AV_{SS} pin

The AV_{SS} pin is a ground potential pin for the A/D converter. This pin must be held at the same potential as the V_{SS0} pin, even while the A/D converter is not being used.

(9) AV_{DD} pin

The AV_{DD} pin is an analog power supply pin for the A/D converter. This pin must be held at the same potential as the V_{DD0} pin, even while the A/D converter is not being used.

5.7.3 10-bit A/D converter control registers

The following two registers are used to control the 10-bit A/D converter.

- A/D converter mode register (ADM)
- A/D input selection register (ADS)

(1) A/D converter mode register (ADM)

The ADM specifies the conversion time for analog inputs. It also specifies whether to enable conversion.

The ADM can be manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the ADM to 00H.

Figure 5-26. A/D Converter Mode Register Format

Symbol	⑦	6	5	4	3	2	1	0	Address	When reset	R/W
ADM	ADCS	0	FR2	FR1	FR0	0	0	0	FF80H	00H	R/W

ADCS	A/D conversion control
0	Conversion disabled
1	Conversion enabled

FR2	FR1	FR0	A/D conversion time selection[Note 1]
0	0	0	144/fx (28.8 μs)
0	0	1	120/fx (24 μs)
0	1	0	96/fx (19.2 μs)
1	0	0	72/fx (14.4 μs)
1	0	1	60/fx (not to be set[Note 2])
1	1	0	48/fx (not to be set[Note 2])
Other settings			Not to be set

Notes 1. The specifications of FR2, FR1, and FR0 must be such that the A/D conversion time is at least 14 μs.

     2. These bit combinations must not be used, as the A/D conversion time will fall below 14 μs.

Caution   The result of conversion performed immediately after bit 7 (ADCS) is set is undefined.

Remarks 1. fx: Main system clock oscillation frequency

       2. The parenthesized values apply to operation at fx = 5.0 MHz.

(2) A/D input selection register (ADS)

The ADS register specifies the port used to input the analog voltages to be converted to a digital signal. The ADS can be manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the ADS to 00H.

Figure 5-27. A/D Input Selection Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
ADS	0	0	0	0	0	ADS2	ADS1	ADS0	FF84H	00H	R/W

ADS2	ADS1	ADS0	Analog input channel specification
0	0	0	ANI0
0	0	1	ANI1
0	1	0	ANI2
0	1	1	ANI3
1	0	0	ANI4
1	0	1	ANI5
1	1	0	ANI6
1	1	1	Not to be set

5.8 Comparator

5.8.1 Comparator functions
The comparator has the following functions.

(1) Input voltage comparison
The comparator compares an input voltage at the reference voltage input pin (CMPREF0) with an input voltage at the comparator input pin (CMPIN0).   The comparison result can be read using memory manipulation instructions.

(2) Interrupt generation
The comparator output (selectable with a rising and/or falling edge) is used to generate an interrupt request signal (INTCMP).

(3) Clock output
When CMPREF0 > CMPIN0, the output of 8-bit timer counter 2 (TM2) is directed to the CMPTOUT0 pin.

(4) Open-drain output selection
Comparator mode register 0 (CMPRM0) is used to specify a port as an N-ch open-drain output.

5.8.2   Comparator configuration
The comparator consists of the following hardware.

(1) CMPIN0
This is the comparator input pin.

(2) CMPTOUT0
This is the comparator output pin.

(3) CMPREF0
This is the comparator reference voltage input pin.

Figure 5-28 is a block diagram of the comparator.

Figure 5-28. Comparator Block Diagram
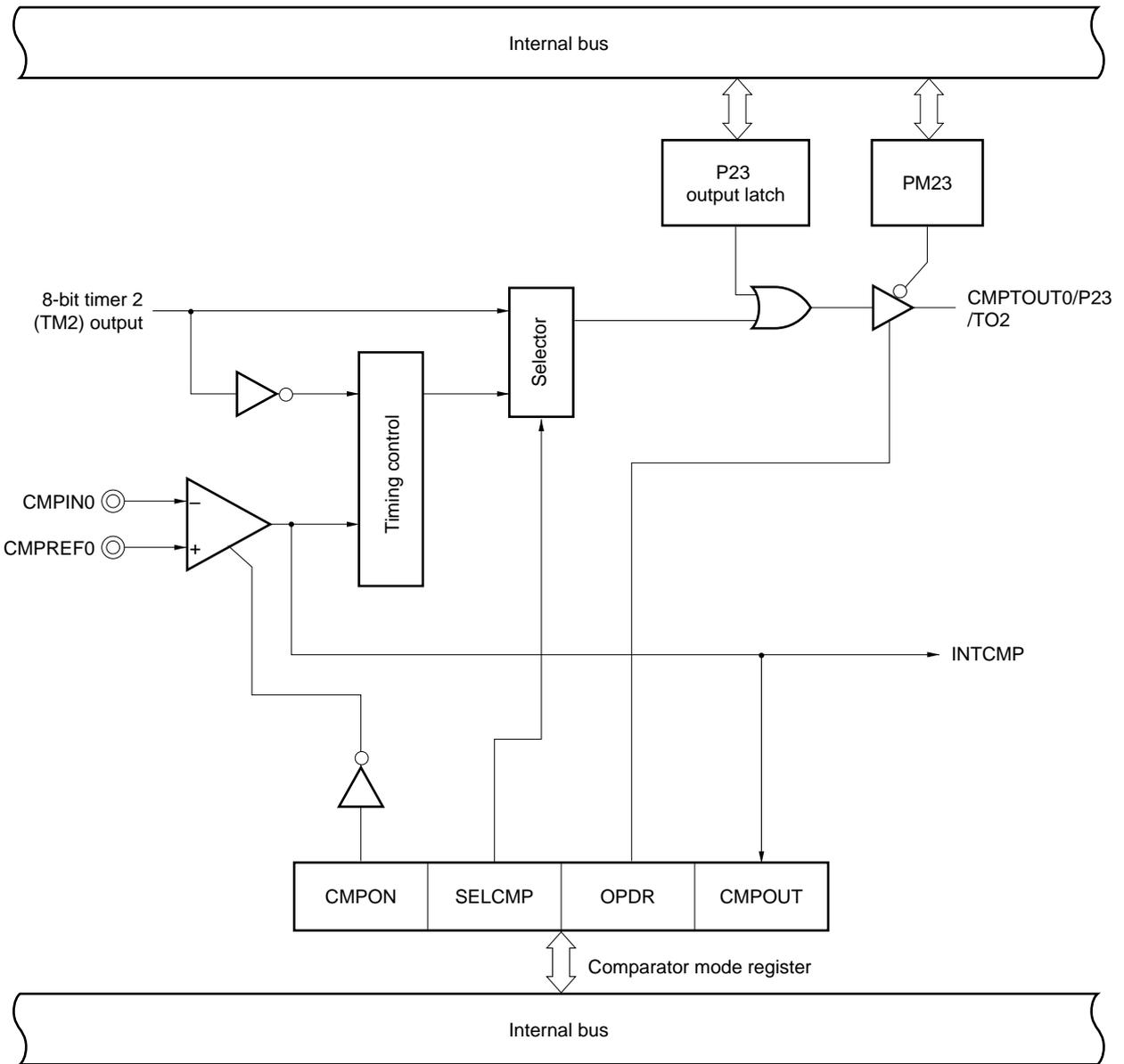
5.8.3 Comparator control register

The comparator is controlled by the following register.

(1) Comparator mode register 0 (CMPRM0)

CMPRM0 controls the power supply and output of the comparator. It also selects an open drain output for the comparator.

CMPRM0 is set using a 1-bit or 8-bit memory manipulation instruction.

A RESET input clears CMPRM0 to 00H.

Figure 5-29. Comparator Mode Register 0 Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
CMPRM0	0	0	0	0	CMPON	SELCMP	OPDR	CMPOUT	FF4EH	00H	R/W**Note**

CMPON	Comparator power supply ON/OFF control
0	Comparator power supply OFF
1	Comparator power supply ON

SELCMP	Clock output control
0	8-bit timer counter (TM2) output
1	8-bit timer counter 2 (TM2) output if CMPREF0 > CMPIN0

OPDR	Open-drain output selection
0	CMOS output
1	N-ch open-drain output

CMPOUT	The comparator output is read.

Note Bit 0 is read-only.

Cautions 1. Bits 4 to 7 must be fixed to 0.
      2. If the comparator is enabled (CMPON = 1), noise may be induced. If it is necessary to generate an interrupt request signal (INTCMP) from the output of the comparator, enable the comparator (CMPON = 1) then clean the interrupt request flag (CMPIF) to 0, before enabling interrupts.
      3. Similarly, if it is necessary to direct the output of the comparator to the port, enable the comparator (CMPON = 1) in advance.

5.9 Serial Interface Channel 0

5.9.1 Functions of serial interface channel 0

Serial interface channel 0 has the following three modes.
- Operation stopped mode
- Asynchronous serial interface (UART) mode
- Three-wire serial I/O mode

(1) Operation stopped mode

This mode is used when serial transfer is not performed. Power consumption is minimized in this mode.

(2) Asynchronous serial interface (UART) mode

This mode is used to send and receive the one byte of data that follows a start bit. It supports full-duplex communication.

Serial interface channel 0 contains a dedicated UART baud rate generator, enabling communication over a wide range of baud rates. It is also possible to define baud rates by dividing the frequency of the input clock pulse at the ASCK pin.

(3) Three-wire serial I/O mode (switchable between MSB-first and LSB-first transmission)

This mode is used to transmit 8-bit data, using three lines: a serial clock ($\overline{SCK}$) line and two serial data lines (SI and SO).

As it supports simultaneous transmission and reception, three-wire serial I/O mode requires less processing time for data transmission than asynchronous serial interface mode.

Because, in three-wire serial I/O mode, it is possible to select whether 8-bit data transmission begins with the MSB or LSB, channel 0 can be connected to any device regardless of whether that device is designed for MSB-first or LSB-first transmission.

Three-wire serial I/O mode is useful for connecting peripheral I/O circuits and display controllers having conventional clock synchronous serial interfaces, such as those of the 75X/XL, 78K, and 17K series devices.

5.9.2 Serial interface channel 0 configuration

Serial interface channel 0 consists of the following hardware.

Table 5-12. Serial Interface Channel 0 Configuration

Item	Configuration
Register	Transmission shift register (TXS) Reception shift register (RXS) Reception buffer register (RXB)
Control register	Serial operation mode register 0 (CSIM0) Asynchronous serial interface mode register (ASIM) Asynchronous serial interface status register (ASIS) Baud rate generator control register (BRGC)

Figure 5-30. Serial Interface Channel 0 Block Diagram
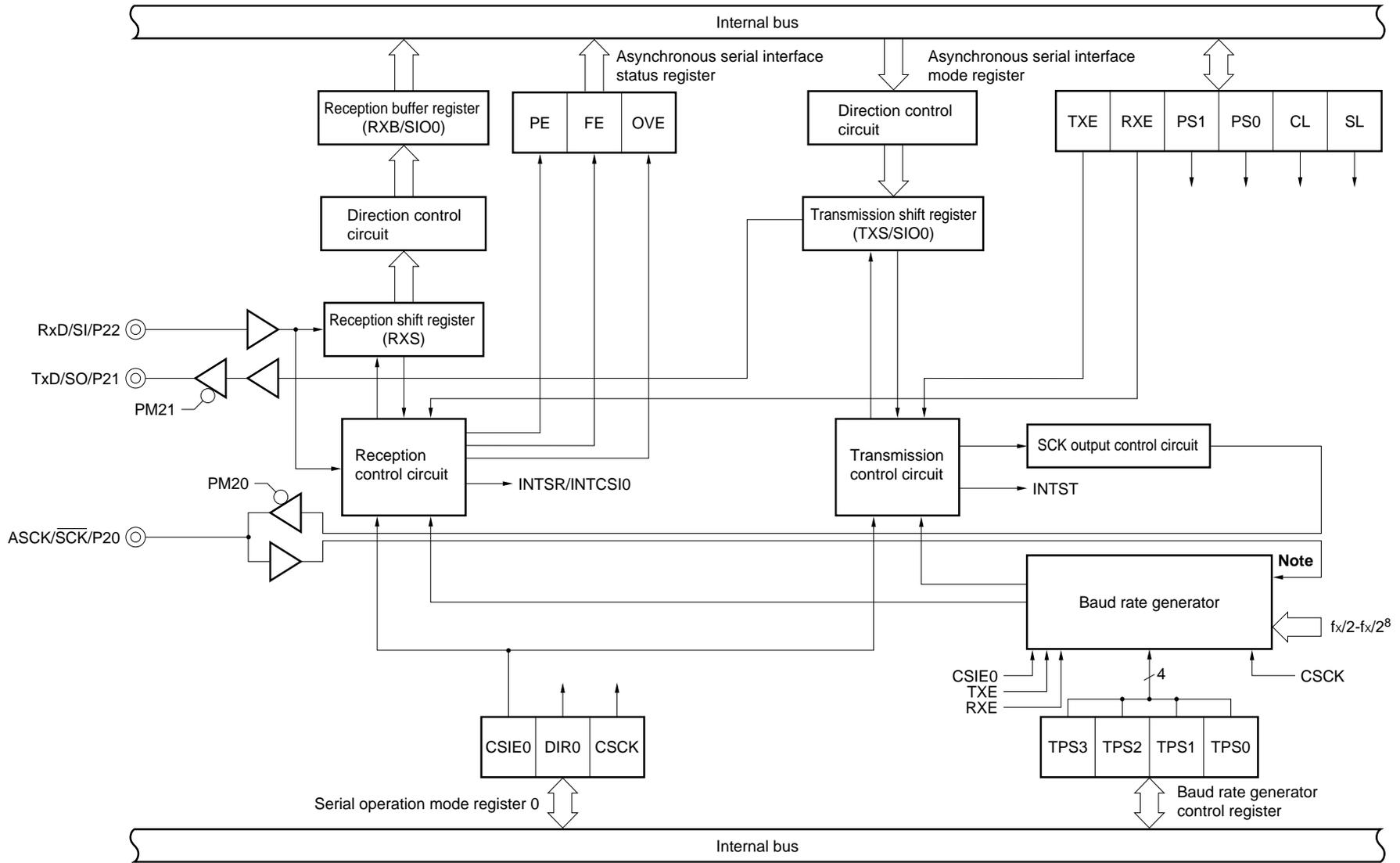
Note See **Figure 5-31** for the configuration of the baud rate generator.

Figure 5-31. Baud Rate Generator Block Diagram
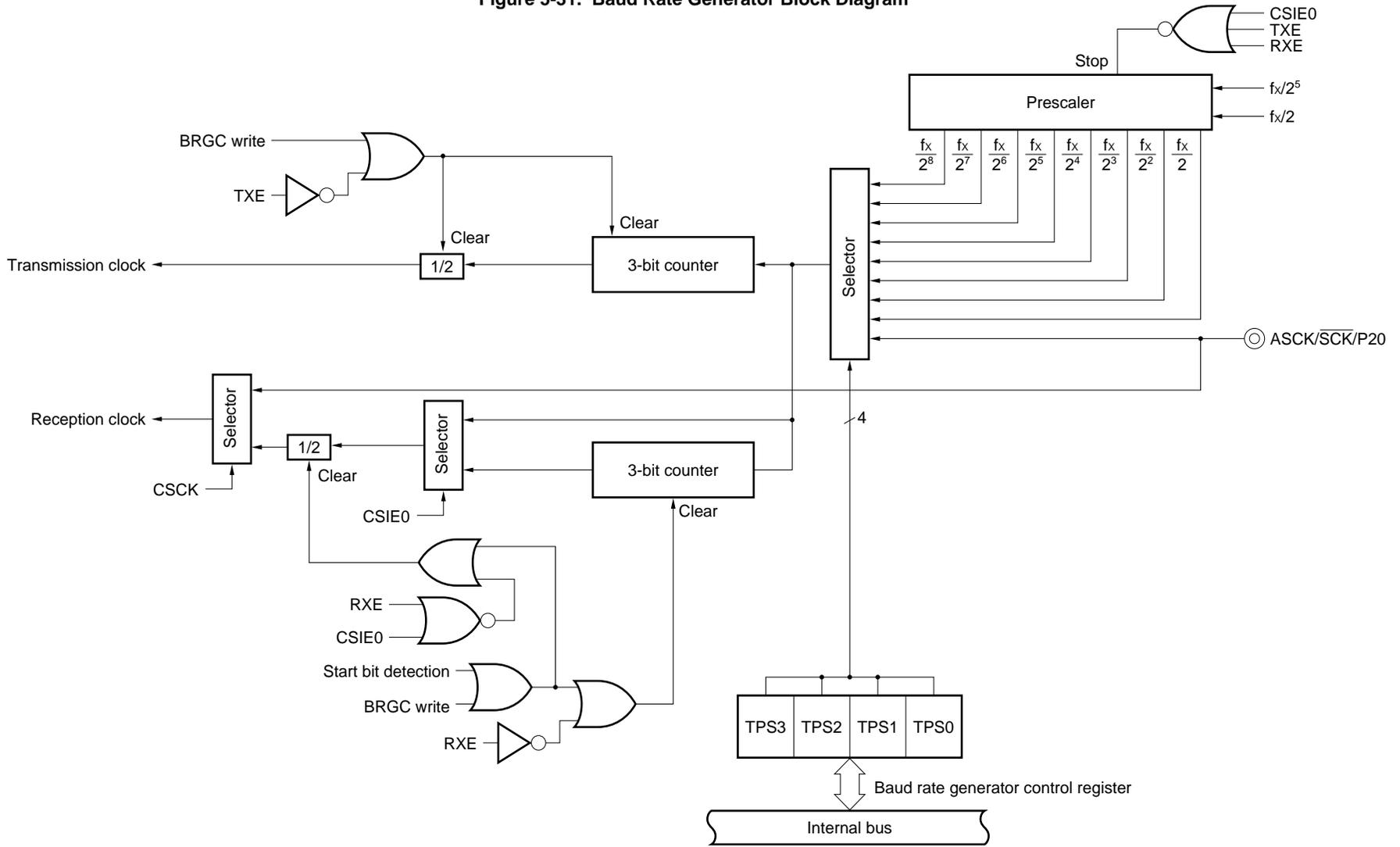
(1) Transmission shift register (TXS)

The TXS is a register in which transmission data is prepared. The transmission data is output from the TXS bit-serially.

When the data length is seven bits, bits 0 to 6 of the data in the TXS will be transmission data. Writing data to the TXS triggers transmission.

The TXS can be write-accessed, using an 8-bit memory manipulation instruction, but cannot be read-accessed. A $\overline{\text{RESET}}$ input loads FFH into the TXS.

Caution   Do not write to the TXS during transmission.
The TXS and the reception buffer register (RXB) are mapped at the same address, such that any attempt to read from the TXS results in a value being read from the RXB.

(2) Reception shift register (RXS)

The RXS is a register in which serial data, received at the RxD pin, is converted to parallel data. Once one entire   byte has been received, the RXS feeds the reception data to the reception buffer register (RXB).

The RXS cannot be manipulated directly by a program.

(3) Reception buffer register (RXB)

The RXB is used to hold reception data. Once the RXS has received one entire byte of data, it feeds that data into the RXB.

When the data length is seven bits, the reception data is sent to bits 0 to 6 of the RXB, in which the MSB is fixed to 0.

The RXB can be read-accessed, using an 8-bit memory manipulation instruction, but cannot be write-accessed. A $\overline{\text{RESET}}$ input makes the RXB undefined.

Caution   The RXB and the transmission shift register (TXS) are mapped at the same address, such that any attempt to write to the RXB results in a value being written to the TXS.

(4) Transmission control circuit

The transmission control circuit controls transmission. For example, it adds start, parity, and stop bits to the data in the transmission shift register (TXS), according to the setting of the asynchronous serial interface mode register (ASIM).

(5) Reception control circuit

The reception control circuit controls reception according to the setting of the asynchronous serial interface mode register (ASIM). It also checks for errors, such as parity errors, during reception. If an error is detected, the asynchronous serial interface status register (ASIS) is set according to the status of the error.

5.9.3 Serial interface channel 0 control registers

Serial interface channel 0 is controlled by the following registers.

- Serial operation mode register 0 (CSIM0)
- Asynchronous serial interface mode register (ASIM)
- Asynchronous serial interface status register (ASIS)
- Baud rate generator control register (BRGC)

(1) Serial operation mode register 0 (CSIM0)

CSIM0 is used to make the settings related to three-wire serial I/O mode.

CSIM0 is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears CSIM0 to 00H.

Figure 5-32. Serial Operation Mode Register 0 Format

Symbol	⑦	6	5	4	3	2	1	0	Address	When reset	R/W
CSIM0	CSIE0	0	0	0	0	DIR0	CSCK	0	FF72H	00H	R/W

CSIE0	Three-wire serial I/O mode operation control
0	Operation disabled
1	Operation enabled

DIR0	First-bit specification
0	MSB
1	LSB

CSCK	Three-wire serial I/O mode clock selection
0	External clock pulse input to the $\overline{\text{SCK0}}$ pin
1	Output of the dedicated baud rate generator

Cautions 1. Bit 0 and bits 3 to 6 must be fixed to 0.

2. CSIM0 must be cleared to 00H, if UART mode is selected.

(2) Asynchronous serial interface mode register (ASIM)

The ASIM is used to make the settings related to asynchronous serial interface mode.

The ASIM is set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the ASIM to 00H.

Figure 5-33. Asynchronous Serial Interface Mode Register Format

Symbol	⑦	⑥	5	4	3	2	1	0	Address	When reset	R/W
ASIM	TXE	RXE	PS1	PS0	CL	SL	0	0	FF70H	00H	R/W

TXE	Transmission control
0	Transmission disabled
1	Transmission enabled

RXE	Reception control
0	Reception disabled
1	Reception enabled

PS1	PS0	Parity bit specification
0	0	No parity
0	1	At transmission, the parity bit is fixed to 0.
		At reception, a parity check is not made; no parity error is reported.
1	0	Odd parity
1	1	Even parity

CL	Character length specification
0	7 bits
1	8 bits

SL	Transmission data stop bit length
0	1 bit
1	2 bits

Cautions 1. Bits 0 and 1 must be fixed to 0.

2. If three-wire serial I/O mode is selected, the ASIM must be cleared to 00H.

3. Before switching from one mode to another, stop both serial transmission and reception.

Table 5-13. Serial Interface Channel 0 Operation Mode Settings

(1) Operation stopped mode

ASIM		CSIM0			PM22	P22	PM21	P21	PM20	P20	First bit	Shift clock	P22/SI/RxD pin function	P21/SO/TxD pin function	P20/SCK/ASCK pin function
TXE	RXE	CSIE0	DIR0	CSCK											
0	0	0	×	×	×[Note 1]	×[Note 1]	×[Note 1]	×[Note 1]	×[Note 1]	×[Note 1]	–	–	P22	P21	P20
Other settings											Not to be specified				

(2) Three-wire serial I/O mode

ASIM		CSIM0			PM22	P22	PM21	P21	PM20	P20	First bit	Shift clock	P22/SI/RxD pin function	P21/SO/TxD pin function	P20/SCK/ASCK pin function
TXE	RXE	CSIE0	DIR0	CSCK											
0	0	1	0	0	1[Note 2]	×[Note 2]	0	1	1	×	MSB	External clock	SI0[Note2]	SO0 (CMOS output)	$\overline{SCK0}$ input
				1					0	1		Internal clock			$\overline{SCK0}$ output
		1	1	0					1	×	LSB	External clock			$\overline{SCK0}$ input
				1					0	1		Internal clock			$\overline{SCK0}$ output
Other settings											Not to be specified				

(3) Asynchronous serial interface mode

ASIM		CSIM0			PM22	P22	PM21	P21	PM20	P20	First bit	Shift clock	P22/SI/RxD pin function	P21/SO/TxD pin function	P20/SCK/ASCK pin function
TXE	RXE	CSIE0	DIR0	CSCK											
1	0	0	0	0	×[Note 1]	×[Note 1]	0	1	1	×	LSB	External clock	P22	TxD (CMOS output)	ASCK input
									×[Note 1]	×[Note 1]		Internal clock			P20
0	1	0	0	0	1	×	×[Note 1]	×[Note 1]	1	×		External clock	RxD	P21	ASCK input
									×[Note 1]	×[Note 1]		Internal clock			P20
1	1	0	0	0	1	×	0	1	1	×		External clock		TxD (CMOS output)	ASCK input
									×[Note 1]	×[Note 1]		Internal clock			P20
Other settings											Not to be specified				

Notes 1. These pins can be used for port functions.

2. When only transmission is used, these pins can be used as P22 (CMOS input/output).

Remark ×: Don't care.

(3) Asynchronous serial interface status register (ASIS)

The ASIS is used to display the type of a reception error, if it occurs while asynchronous serial interface mode is set.

The ASIS is set using an 8-bit memory manipulation instruction.

The contents of the ASIS are undefined in three-wire serial I/O mode.

A $\overline{\text{RESET}}$ input clears the ASIS to 00H.

Figure 5-34. Asynchronous Serial Interface Status Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
ASIS	0	0	0	0	0	PE	FE	OVE	FF71H	00H	R

PE	Parity error flag
0	No parity error has occurred.
1	A parity error has occurred (parity mismatch in transmission data).

FE	Framing error flag
0	No framing error has occurred.
1	A framing error has occurred (no stop bit detected).**Note 1**

OVE	Overrun error flag
0	No overrun error has occurred.
1	An overrun error has occurred.**Note 2** (Before data was read from the reception buffer register, the subsequent reception sequence was completed.)

Notes 1. Even if 2 is specified for the number of stop bits (using bit 2 (SL) of the ASIM), only one stop bit is detected at reception.

2. After an overrun occurs, read-access the reception buffer register (RXB). Otherwise, the overrun error will recur each time data is received.

(4) Baud rate generator control register (BRGC)

The BRGC is used to specify the serial clock for serial interface channel 0.

The BRGC is set using an 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears the BRGC to 00H.

Figure 5-35. Baud Rate Generator Control Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
BRGC	TPS3	TPS2	TPS1	TPS0	0	0	0	0	FF73H	00H	R/W

TPS3	TPS2	TPS1	TPS0	3-bit counter source clock selection	n
0	0	0	0	$f_X/2$ (2.5 MHz)	1
0	0	0	1	$f_X/2^2$ (1.25 MHz)	2
0	0	1	0	$f_X/2^3$ (625 kHz)	3
0	0	1	1	$f_X/2^4$ (313 kHz)	4
0	1	0	0	$f_X/2^5$ (156 kHz)	5
0	1	0	1	$f_X/2^6$ (78.1 kHz)	6
0	1	1	0	$f_X/2^7$ (39.1 kHz)	7
0	1	1	1	$f_X/2^8$ (19.5 kHz)	8
1	0	0	0	External clock pulse input at the ASCK pin[Note]	–
Other settings				Not to be specified	

Note An external clock can be used only in UART mode.

Cautions 1. Any attempt to write to the BRGC during communication adversely affects the output of the baud rate generator, thus hampering normal operation. Therefore, do not write to the BRGC during communication.

2. Do not select n = 1 during operation at f$_X$ = 5.0 MHz, as n = 1 causes the rated baud rate to be exceeded.

Remarks 1. f_X : Main system clock oscillation frequency

2. n : Value specified in TPS0 to TPS3 ($1 \le n \le 8$)

3. The parenthesized values apply to operation at f_X = 5.0 MHz.

The transmission and reception clock pulses used to generate the baud rate are obtained by dividing the frequency of the main system clock pulse or a signal input to the ASCK pin.

(a) Generating transmission and reception clock pulses for baud rates based on the main system clock

The frequency of the main system clock is divided to generate the transmission and reception clock pulses. The baud rate generated based on the main system clock is determined using the following expression.

$$[\text{Baud rate}] = \frac{f_X}{2^{n+1} \times 8} \quad [\text{Hz}]$$

f_X : Main system clock oscillation frequency

n : Value specified at TPS0 to TPS3 ($2 \le n \le 8$)

Table 5-14. Relationships between Main System Clock Frequencies and Baud Rates (Example)

Baud rate (bps)	BRGC setting	Error (%)	
		fx = 5.0 MHz	fx = 4.9152 MHz
1 200	70H	1.73	0
2 400	60H		
4 800	50H		
9 600	40H		
19 200	30H		
38 400	20H		
76 800	10H		

(b) Generating transmission and reception clock pulses for baud rates based on an external clock pulse received at the ASCK pin

The frequency of an external clock pulse received at the ASCK pin is used to generate the transmission and reception clock pulses. The baud rate generated based on the external clock pulse received at the ASCK pin is determined using the following expression.

$$[\text{Baud rate}] = \frac{f_{ASCK}}{16} \ [\text{Hz}]$$

f_{ASCK}: Frequency of clock pulse received at the ASCK pin

Table 5-15. Relationships between ASCK Pin Input Frequencies and Baud Rates (When BRGC = 80H)

Baud rate (bps)	ASCK pin input frequency (kHz)
75	1.2
150	2.4
300	4.8
600	9.6
1 200	19.2
2 400	38.4
4 800	76.8
9 600	153.6
19 200	307.2
31 250	500.0
38 400	614.4

5.10 LCD Controller/Driver

5.10.1 LCD controller/driver functions

The functions of the LCD controller/driver of the μPD789415, μPD789416, and μPD789417 are as follows:

(1) Automatic output of segment and common signals based on automatic display data memory read
(2) Five different display modes:
   - Static
   - 1/2 duty (1/2 bias)
   - 1/3 duty (1/2 bias)
   - 1/3 duty (1/3 bias)
   - 1/4 duty (1/3 bias)
(3) Four different frame frequencies, selectable in each display mode
(4) Up to 28 segment signal outputs (S0 to S27) and four common signal outputs (COM0 to COM3)
   Of these segment signal outputs, 12 outputs can be switched to input/output ports in 2-output units (P80/S27 to P87/S20 and P90/S19 to P93/S16).
(5) Voltage divider resistors (for LCD drive voltage generation) that a port itself can contain if so specified with a mask option
(6) Operation with a subsystem clock

Table 5-16 lists the maximum number of pixels that can be displayed in each display mode.

Table 5-16. Maximum Number of Pixels

Bias mode	Number of time slices	Common signals used	Maximum number of pixels
–	Static	COM0 (COM1-COM3)	28 (28 segment signals, 1 common signal)[Note 1]
1/2	2	COM0, COM1	56 (28 segment signals, 2 common signals)[Note 2]
	3	COM0-COM2	84 (28 segment signals, 3 common signals)[Note 3]
1/3	3	COM0-COM2	
	4	COM0-COM3	112 (28 segment signals, 4 common signals)[Note 4]

Notes **1.** Three-digit LCD panel, each digit having an 8-segment β. configuration.
      2. Seven-digit LCD panel, each digit having a 4-segment β. configuration.
      3. Nine-digit LCD panel, each digit having a 3-segment β. configuration.
      4. Fourteen-digit LCD panel, each digit having a 2-segment β. configuration.

5.10.2 LCD controller/driver configuration

The LCD controller/driver consists of the following hardware.

Table 5-17. LCD Controller/Driver Configuration

Item	Configuration
Display output	28 segment signals (16 dedicated segment signals and 12 segment and input/output port signals) 4 common signals (COM0 to COM3)
Control register	LCD display mode register (LCDM) LCD port selector (LPS) LCD clock control register (LCDC)

Figure 5-36. LCD Controller/Driver Block Diagram
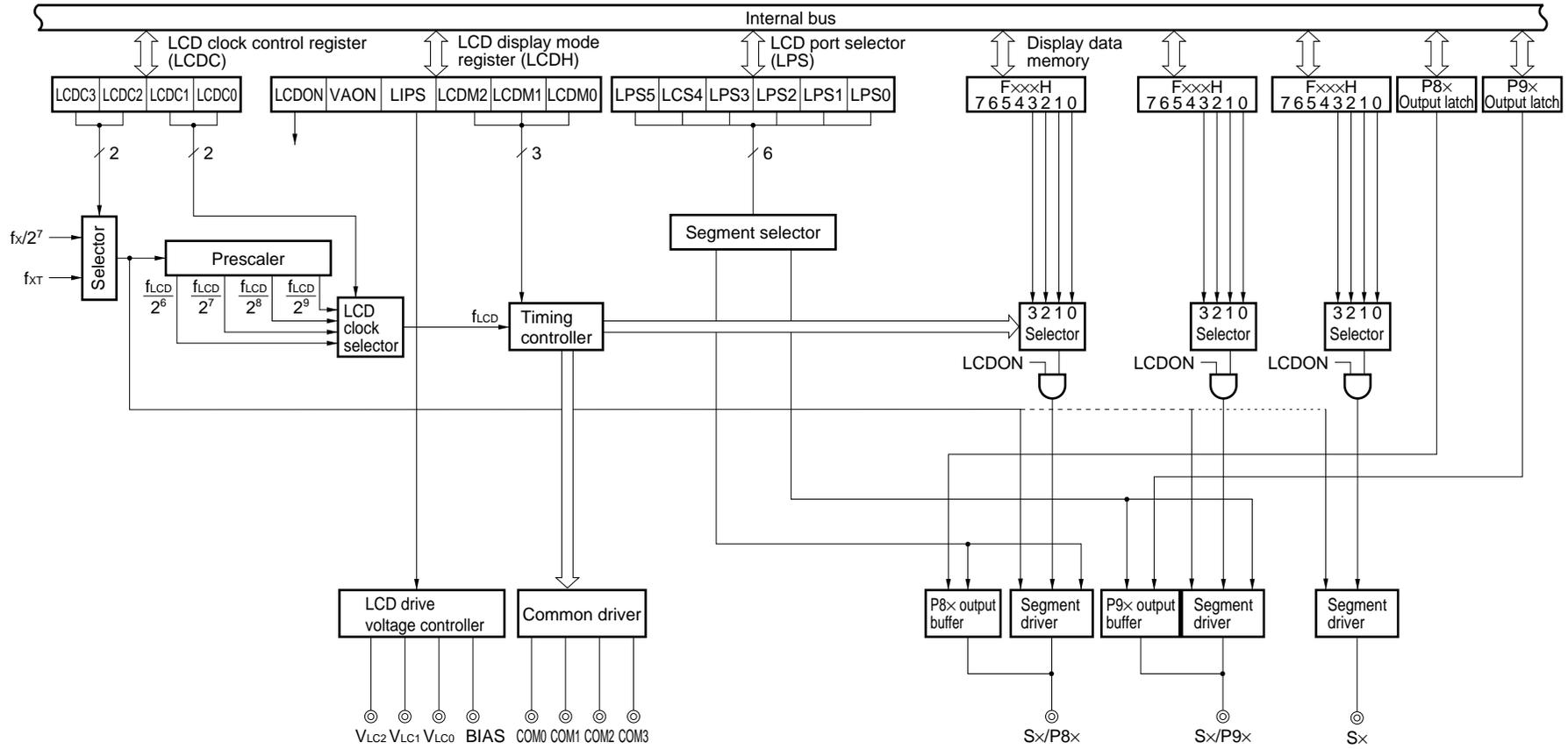
5.10.3 LCD controller/driver control registers

The following three types of registers are used to control the LCD controller/driver.

- LCD display mode register (LCDM)
- LCD port selector (LPS)
- LCD clock control register (LCDC)

(1) LCD display mode register (LCDM)

The LCDM specifies whether to enable display operation. It also specifies the operation mode, LCD drive power supply, and display mode.

The LCDM is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A RESET clears the LCDM to 00H.

Figure 5-37. LCD Display Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
LCDM	LCDON	VAON	0	LIPS	0	LCDM2	LCDM1	LCDM0	FFB0H	00H	R/W

LCDON	Control of LCD display
0	Display OFF (All segment outputs are deselected.)
1	Display ON

VAON	LCD controller/driver operation mode**Note**
0	Normal operation
1	Low-voltage operation

LIPS	LCD drive power supply selection
0	LCD drive power is not supplied.
1	LCD drive power is supplied to the BIAS pin.

LCDM2	LCDM1	LCDM0	LCD controller/driver display mode selection	
			Number of time slices	Bias mode
0	0	0	4	1/3
0	0	1	3	1/3
0	1	0	2	1/2
0	1	1	3	1/2
1	0	0	Static	
Other settings			Not to be set	

Note When the LCD display panel is not used, VAON and LIPS must be fixed to 0 to conserve power.

Caution   Before attempting to manipulate VAON, set LIPS and LCDON to 0 to turn off the LCD.

(2) LCD port selector (LPS)

The LPS controls port and segment signal output switching.

The LPS is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ clears the LPS to 00H.

Figure 5-38. LCD Port Selector Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
LPS	0	0	LPS5	LPS4	LPS3	LPS2	LPS1	LPS0	FFB1H	00H	R/W

	LPS5	LPS4	LPS3	LPS2	LPS1	LPS0
	P93/S16, P92/S17	P91/S18, P90/S19	P87/S20, P86/S21	P85/S22, P84/S23	P83/S24, P82/S25	P81/S26, P80/S27
0	Used as ports (Pmn)					
1	Used as segments (S×)					

Remark m = 8   n = 0 to 7

m = 9   n = 0 to 3

× = 16 to 27

(3) LCD clock control register (LCDC)

The LCDC specifies the LCD clock and frame frequency.

The LCDC is manipulated using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ clears the LCDC to 00H.

Figure 5-39. LCD Clock Control Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
LCDC	0	0	0	0	LCDC3	LCDC2	LCDC1	LCDC0	FFB2H	00H	R/W

LCDC3	LCDC2	LCD clock (f_{LCD}) selection**Note**
0	0	$f_X/2^7$
0	1	f_{XT}
1	0	Not to be set
1	1	

LCDC1	LCDC0	LCD frame frequency selection
0	0	$f_{LCD}/2^6$
0	1	$f_{LCD}/2^7$
1	0	$f_{LCD}/2^8$
1	1	$f_{LCD}/2^9$

Note   Specify an LCD clock (f_{LCD}) frequency of at least 32 kHz.

Table 5-18 lists the frame frequencies used when f_{XT} (32.768 kHz) is supplied to the LCD clock (f_{LCD}).

Table 5-18. Frame Frequencies (Hz)

Frame frequency / Display duty ratio	$f_{XT}/2^9$ (64 Hz)	$f_{XT}/2^8$ (128 Hz)	$f_{XT}/2^7$ (256 Hz)	$f_{XT}/2^6$ (512 Hz)
Static	64	128	256	512
1/2	32	64	128	256
1/3	21	43	85	171
1/4	16	32	64	128

Remark   The parenthesized values apply when f_{XT} (32.768 kHz) is supplied to the LCD clock (f_{LCD}).

6. INTERRUPT FUNCTIONS

6.1 Interrupt Function Types

Two types of interrupt function are supported.

(1) Nonmaskable interrupt

A nonmaskable interrupt request is accepted unconditionally, that is, even when interrupts are disabled. A nonmaskable interrupt takes precedence over all other interrupts; it is not subjected to interrupt priority control.

A nonmaskable interrupt causes the standby release signal to be generated.

The μPD789415, μPD789416, and μPD789417 support one nonmaskable interrupt source namely, the watchdog timer interrupt.

(2) Maskable interrupt

Maskable interrupts are those which are subjected to mask control. If two or more maskable interrupts occur simultaneously, the default priority listed in Table 6-1 applies.

The maskable interrupts cause the standby release signal to be generated.

The maskable interrupts supported by the μPD789415, μPD789416, and μPD789417 include 4 external interrupt sources and 12 internal interrupt sources.

6.2 Interrupt Sources and Configuration

The μPD789415, μPD789416, and μPD789417 each support a total of 17 maskable and nonmaskable interrupt sources. (See **Table 6-1**.)

Table 6-1. Interrupt Sources

Interrupt type	Default priority[Note 1]	Interrupt source		Internal/external	Vector table address	Basic configuration type[Note 2]
		Name	Trigger			
Nonmaskable interrupt	–	INTWDT	Watchdog timer overflow (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when the interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR	End of UART reception on serial interface channel 0	Internal	000EH	(B)
		INTCSI0	End of three-wire SIO transfer reception on serial interface channel 0			
	6	INTST	End of UART transmission on serial interface channel 0		0010H	
	7	INTWT	Clock timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM0	Generation of match signal for 8-bit timer/event counter 0		0016H	
	10	INTTM1	Generation of match signal for 8-bit timer/event counter 1		0018H	
	11	INTTM2	Generation of match signal for 8-bit timer counter 2		001AH	
	12	INTTM5	Generation of match signal for 16-bit timer counter 5		001CH	
	13	INTKR	Key return signal detection		001EH	
	14	INTAD	A/D conversion completion signal		0020H	
	15	INTCMP	Comparator signal		0022H	

Notes 1. The default priority regulates which maskable interrupt is higher, when two or more maskable interrupts are requested simultaneously. Zero signifies the highest priority, while 15 is the lowest.
    2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Functions

(A) Internal nonmaskable interrupt
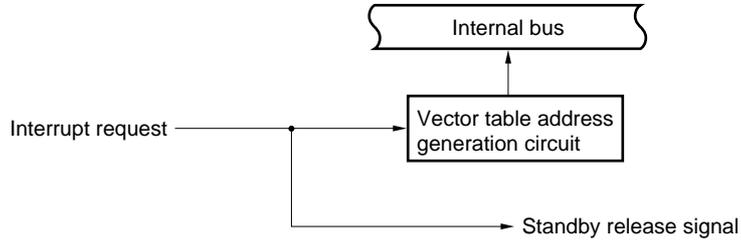
(B) Internal maskable interrupt
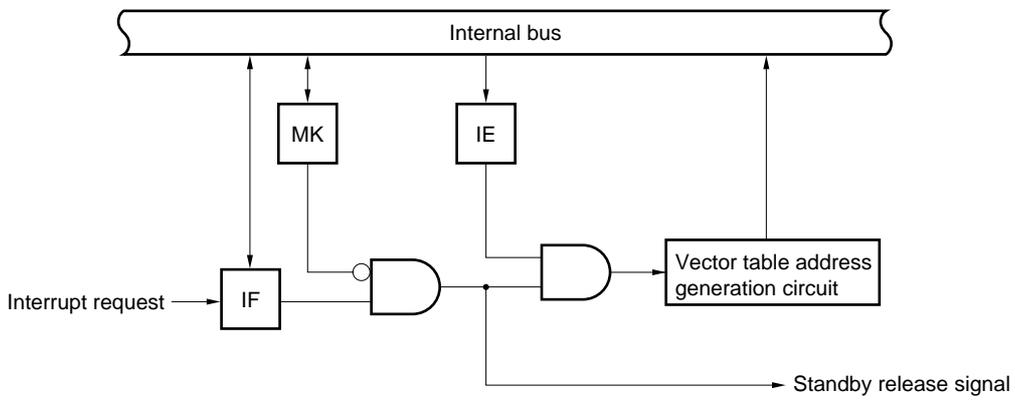
(C) External maskable interrupt
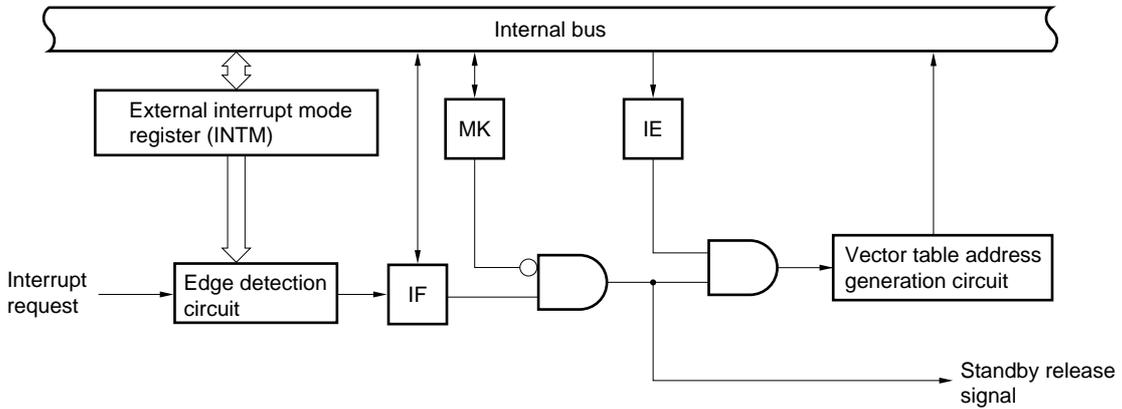
IF : Interrupt request flag

IE : Interrupt enable flag

MK : Interrupt mask flag

6.3 Interrupt Function Control Registers

The interrupt functions are controlled by the following registers.

- Interrupt request flag registers (IF0 and IF1)
- Interrupt mask flag registers (MK0 and MK1)
- External interrupt mode registers (INTM0 and INTM1)
- Program status word (PSW)
- Key return mode register (KRM)

Table 6-2 lists interrupt requests, the corresponding interrupt request flags, and interrupt mask flags.

Table 6-2. Interrupt Request Signals and Corresponding Flags

Interrupt request signal	Interrupt request flag	Interrupt mask flag
INTWDT	TMIF4	TMMK4
INTP0	PIF0	PMK0
INTP1	PIF1	PMK1
INTP2	PIF2	PMK2
INTP3	PIF3	PMK3
INTSR/INTCSI0	SRIF	SRMK
INTST	STIF	STMK
INTWT	WTIF	WTMK
INTWTI	WTIFI	WTMKI
INTTM0	TMIF0	TMMK0
INTTM1	TMIF1	TMMK1
INTTM2	TMIF2	TMMK2
INTTM5	TMIF5	TMMK5
INTKR	KRIF	KRMK
INTAD	ADIF	ADMK
INTCMP	CMPIF	CMPMK

(1) Interrupt request flag registers (IF0 and IF1)

An interrupt request flag is set (1), when the corresponding interrupt request is issued, or when the related instruction is executed. It is cleared (0), when the interrupt request is accepted, when a $\overline{\text{RESET}}$ signal is input, or when a related instruction is executed.

IF0 and IF1 are set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears IF0 and IF1 to 00H.

Figure 6-2. Interrupt Request Flag Register Format

Symbol	⑦	⑥	⑤	④	③	②	①	⓪	Address	When reset	R/W
IF0	WTIF	STIF	SRIF	PIF3	PIF2	PIF1	PIF0	TMIF4	FFE0H	00H	R/W
	⑦	⑥	⑤	④	③	②	①	⓪			
IF1	CMPIF	ADIF	KRIF	TMIF5	TMIF2	TMIF1	TMIF0	WTIFI	FFE1H	00H	R/W

XXIFX	Interrupt request flag
0	No interrupt request signal has been issued.
1	An interrupt request signal has been issued; an interrupt request has been made.

Cautions 1. The TMIF4 flag can be read- and write-accessed only when the watchdog timer is being used as an interval timer. It must be cleared to 0 if the watchdog timer is used in watchdog timer mode 1 or 2.

2. When port 2 is being used as an output port, and its output level is changed, an interrupt request flag is set, because this port is also used as an external interrupt input. To use port 2 in output mode, therefore, the interrupt mask flag must be set to 1 in advance.

(2) Interrupt mask flag registers (MK0 and MK1)

The interrupt mask flags are used to enable and disable the corresponding maskable interrupts.

MK0 and MK1 are set using a 1-bit or 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input loads FFH into MK0 and MK1.

Figure 6-3. Interrupt Mask Flag Register Format

Symbol	⑦	⑥	⑤	④	③	②	①	⓪	Address	When reset	R/W
MK0	WTMK	STMK	SRMK	PMK3	PMK2	PMK1	PMK0	TMMK4	FFE4H	FFH	R/W
	⑦	⑥	⑤	④	③	②	①	⓪			
MK1	CMPMK	ADMK	KRMK	TMMK5	TMMK2	TMMK1	TMMK0	WTMKI	FFE5H	FFH	R/W

XXMKX	Interrupt handling control
0	Enable interrupt handling.
1	Disable interrupt handling.

Cautions 1. When the watchdog timer is being used in watchdog timer mode 1 or 2, any attempt to read TMMK4 flag results in an undefined value being detected.

2. When port 2 is being used as an output port, and its output level is changed, an interrupt request flag is set, because this port is also used as an external interrupt input. To use port 2 in output mode, therefore, the interrupt mask flag must be set to 1 in advance.

(3) External interrupt mode register 0 (INTM0)

INTM0 is used to specify an effective edge for INTP0 to INTP2.

INTM0 is set using an 8-bit memory manipulation instruction.

A RESET input clears INTM0 to 00H.

Figure 6-4. External Interrupt Mode Register 0 Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
INTM0	ES21	ES20	ES11	ES10	ES01	ES00	0	0	FFECH	00H	R/W

ES21	ES20	INTP2 effective edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Not to be specified
1	1	Both rising and falling edges

ES11	ES10	INTP1 effective edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Not to be specified
1	1	Both rising and falling edges

ES01	ES00	INTP0 effective edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Not to be specified
1	1	Both rising and falling edges

Cautions 1. Bits 0 and 1 must be fixed to 0.

2. Before setting INTM0, set the corresponding interrupt mask flag register to 1 to disable interrupts.

To enable interrupts, clear (0) the corresponding interrupt request flag, then the corresponding interrupt mask flag register.

(4) External interrupt mode register 1 (INTM1)

INTM1 is used to specify an effective edge for INTP3 and INTCMP.

INTM1 is set using an 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input clears INTM1 to 00H.

Figure 6-5. External Interrupt Mode Register 1 Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
INTM1	ES61	ES60	0	0	0	0	ES31	ES30	FFEDH	00H	R/W

ES61	ES60	INTCMP effective edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Not to be specified
1	1	Both rising and falling edges

ES31	E30	INTP3 effective edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Not to be specified
1	1	Both rising and falling edges

Cautions 1. Bits 2 to 5 must be fixed to 0.

      2. Before setting INTM1, set the corresponding interrupt mask flag register to 1 to disable interrupts.

         To enable interrupts, clear (0) the corresponding interrupt request flag, then the corresponding interrupt mask flag register.

(5) Program status word (PSW)

The program status word is used to hold the instruction execution result and the current status of the interrupt requests. The IE flag, used to enable and disable maskable interrupts, is mapped to the PSW.

The PSW can be read- and write-accessed in 8-bit units, as well as in 1-bit units when using bit manipulation instructions and dedicated instructions (EI and DI). When a vector interrupt is accepted, the PSW is automatically saved to a stack, and the IE flag is reset (0).

An $\overline{\text{RESET}}$ input loads 02H into the PSW.

Figure 6-6. Program Status Word Configuration

Symbol	7	6	5	4	3	2	1	0	When reset
PSW	IE	Z	0	AC	0	0	1	CY	02H

→ Used in the execution of ordinary instructions

IE	Whether to enable/disable interrupt acceptance
0	Disable
1	Enable
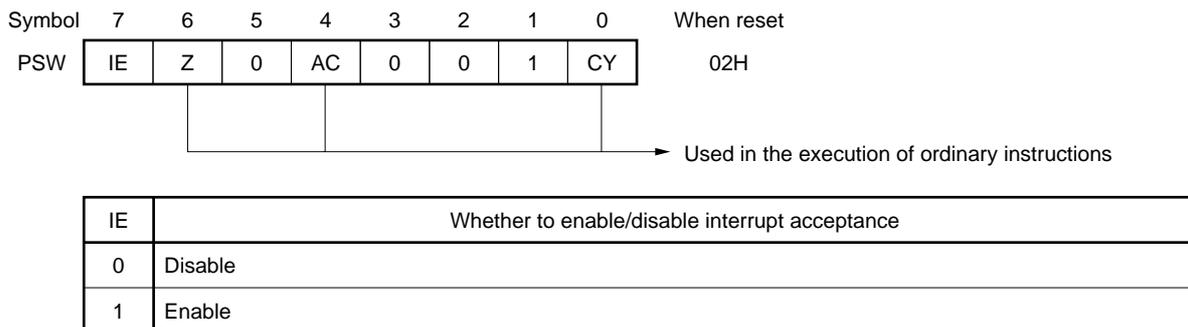
(6) Key return mode register (KRM)

The KRM is used to specify the pin at which a key return signal is detected.

The KRM is set using a 1-bit or 8-bit memory manipulation instruction.

Bit 0 (KRM0) is set in 4-bit units for the KR0/P40 to KR3/P43 pins. Bits 4 and 5 (KRM4 and KRM5) are set in 1-bit units for the KR4/P44 and KR5/P45 pins, respectively.

A $\overline{\text{RESET}}$ input clears the KRM to 00H.

Figure 6-7. Key Return Mode Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
KRM	0	0	KRM5	KRM4	0	0	0	KRM0	FFF5H	00H	R/W

KRMn	Key return signal detection selection
0	Undetected
1	Detected (at the falling edge of port 4)
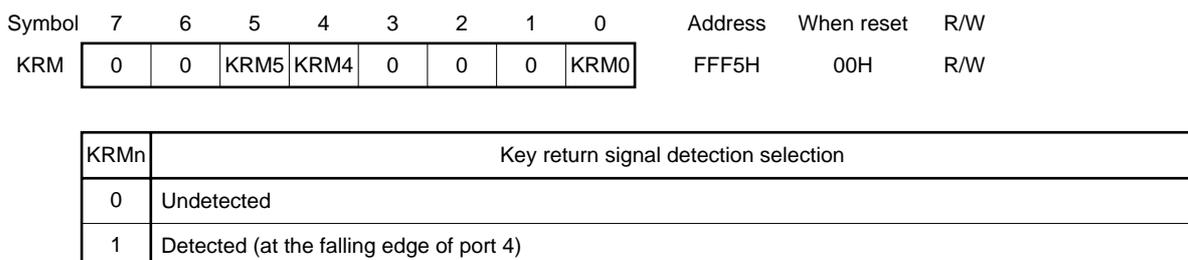
Cautions 1. **Bits 1, 2, 3, 6, and 7 must be fixed to 0.**
2. **When KRM is set (1), the corresponding output pin is connected to a pull-up resistor unless it is in output mode. In output mode, the pull-up resistor is not connected.**
3. **Before setting the KRM, set bit 5 of MK1 (KRMK = 1) to disable interrupts.**
To enable interrupts, clear bit 5 of IF1 (KRIF = 0), then bit 5 of MK1 (KRMK = 0).

Figure 6-8. Falling Edge Detection Circuit
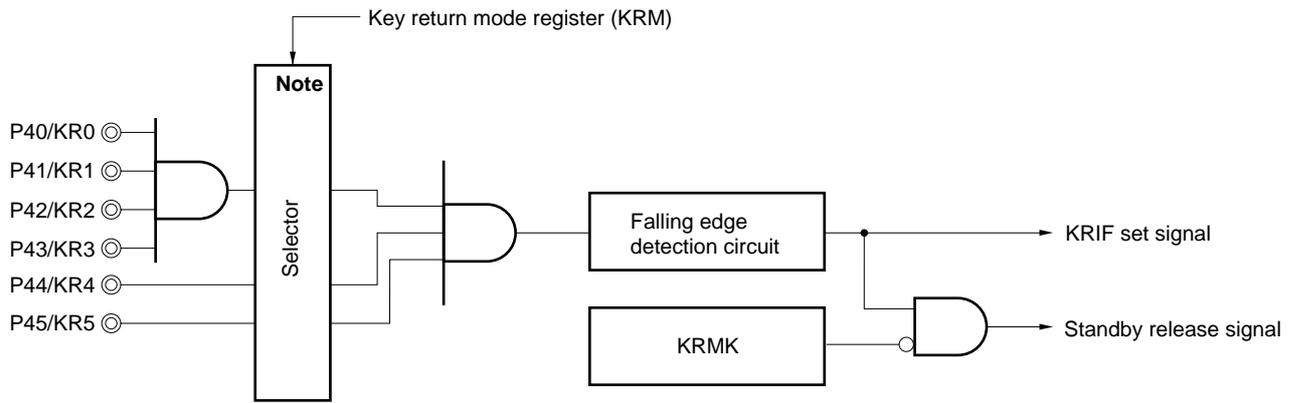
Note Selector used to select the pin to be used for falling edge input

7. STANDBY FUNCTION

7.1 Standby Function

The standby function is supported to minimize the system's power consumption. There are two standby modes: HALT and STOP.

HALT and STOP modes are selected using the HALT and STOP instructions, respectively.

(1) HALT mode
In HALT mode, the CPU clock is stopped. Interleaving normal mode with HALT mode can reduce the average power consumption.

(2) STOP mode
In STOP mode, the main system clock is stopped. As a result, main system clock-based operation is also stopped, thus minimizing power consumption.

> **Caution**   **Before shifting to STOP mode, first stop the operation of the hardware, then execute the STOP instruction.**

Table 7-1. Operation Statuses in HALT Mode

Item	HALT mode operation status while the main system clock is running		HALT mode operation status while the subsystem clock is running	
	While the subsystem clock is running	While the subsystem clock is not running	While the main system clock is running	While the main system clock is not running
Clock generator	Can operate with the main system clock.			Does not run.
CPU	Does not run.			
Port (output latch)	Remains in the state existing before the selection of HALT mode.			
16-bit timer counter (TM5)	Operation enabled			Does not run.
8-bit timer/event counter (TM0 and TM1)	Operation enabled			Operation enabled[Note 1]
8-bit timer counter (TM2)	Operation enabled	Operation enabled[Note 2]	Operation enabled	Operation enabled[Note 3]
Clock timer	Operation enabled	Operation enabled[Note 2]	Operation enabled	Operation enabled[Note 3]
Watchdog timer	Operation enabled			Operation disabled
Serial interface	Operation enabled			Operation enabled[Note 4]
A/D converter	Operation disabled			
LCD controller/driver	Operation enabled	Operation enabled[Note 2]	Operation enabled	Operation enabled[Note 3]
Comparator	Operation enabled[Note 5]			
External interrupt	Operation enabled[Note 6]			

Notes 1. Operation is enabled only when TI0 or TI1 is selected as the count clock.

2. Operation is enabled while the main system clock is selected.

3. Operation is enabled while the subsystem clock is selected.

4. Operation is enabled in both three-wire serial I/O and UART modes while an external clock is being used.

5. Operation is enabled while TM2 is operating, or as an external interrupt.

6. Maskable interrupt that is not masked

Table 7-2. Operation Statuses in Stop Mode

Item	STOP mode operation status while the main system clock is running	
	While the subsystem clock is running	While the subsystem clock is not running
Clock generator	Does not operate with the main system clock.	
CPU	Does not run.	
Port (output latch)	Remains in the state existing before the selection of STOP mode.	
16-bit timer counter (TM5)	Does not run.	
8-bit timer/event counter (TM0 and TM1)	Operation enabled[Note 1]	
8-bit timer counter (TM2)	Operation enabled[Note 2]	Does not run.
Clock timer	Operation enabled[Note 2]	Does not run.
Watchdog timer	Does not run.	
Serial interface	Operation enabled[Note 3]	
A/D converter	Does not run.	
LCD controller/driver	Operation enabled[Note 2]	Does not run.
Comparator	Operation enabled[Notes 5 and 6]	Operation enabled[Note 6]
External interrupt	Operation enabled[Note 4]	

Notes 1. Operation is enabled only when TI0 or TI1 is selected as the count clock.

      2. Operation is enabled while the subsystem clock is selected.

      3. Operation is enabled in both three-wire serial I/O and UART modes while an external clock is being used.

      4. Maskable interrupt that is not masked

      5. Operation is enabled while TM2 is running.

      6. Operation is enabled as an external interrupt.

7.2 Standby Function Control Register

The oscillation settling time selection register (OSTS) is used to control the wait time, from the time the STOP mode is deselected by an interrupt request, until oscillation settles.

The OSTS is manipulated using an 8-bit memory manipulation instruction.

A $\overline{\text{RESET}}$ input loads 04H into the OSTS. If a $\overline{\text{RESET}}$ input is used to deselect STOP mode, the time required for oscillation to settle will be $2^{15}/f_X$, rather than $2^{17}/f_X$.

Figure 7-1. Oscillation Settling Time Selection Register Format

Symbol	7	6	5	4	3	2	1	0	Address	When reset	R/W
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	FFFAH	04H	R/W

OSTS2	OSTS1	OSTS0	Oscillation settling time selection
0	0	0	$2^{12}/f_X$ (819 μs)
0	1	0	$2^{15}/f_X$ (6.55 ms)
1	0	0	$2^{17}/f_X$ (26.2 ms)
Other settings			Not to be set

Caution   The wait time required to deselect STOP mode does not include the time ("a" in the following chart) required for the clock oscillation to settle after STOP mode is deselected, regardless of whether STOP mode is deselected by a $\overline{\text{RESET}}$ input or interrupt.
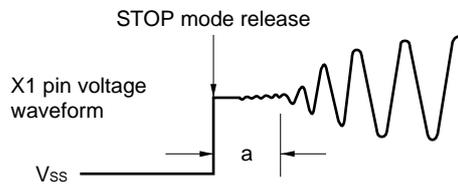
Remarks 1. f_X: Main system clock oscillation frequency
       2. The parenthesized values apply to operation at f_X = 5.0 MHz.

8. RESET FUNCTIONS

The μPD789415, μPD789416, and μPD789417 can be reset using the following signals.

(1) External reset signal input to the $\overline{\text{RESET}}$ pin
(2) Internal reset signal generated upon the elapse of the period set in the watchdog timer, used for detecting an unintended program loop

The external and internal reset signals are functionally equivalent. When $\overline{\text{RESET}}$ is input, they cause program execution to begin at the addresses indicated at addresses 0000H and 0001H, respectively.

If a low level signal is applied to the $\overline{\text{RESET}}$ pin, or if the watchdog timer overflows, a reset occurs, causing each piece of the hardware to enter the states listed in Table 8-1. While a reset signal is being input, or while the oscillation frequency is settling immediately after the end of a reset sequence, each pin remains in the high-impedance state.

If a high level signal is applied to the $\overline{\text{RESET}}$ pin, a reset sequence is terminated, and program execution begins once the oscillation settling time ($2^{15}/f_x$) elapses. A watchdog timer overflow-based reset sequence is terminated automatically. Similarly, program execution begins upon the elapse of the oscillation settling time ($2^{15}/f_x$).

Cautions 1. To use an external reset sequence, supply a low level signal to the $\overline{\text{RESET}}$ pin and maintain the signal for at least 10 μs.

2. When a reset is used to deselect STOP mode, the information related to the STOP mode is held during the reset sequence, that is, while the reset signal is applied. The port pins remain in the high-impedance state, however.

Figure 8-1. Reset Function Block Diagram
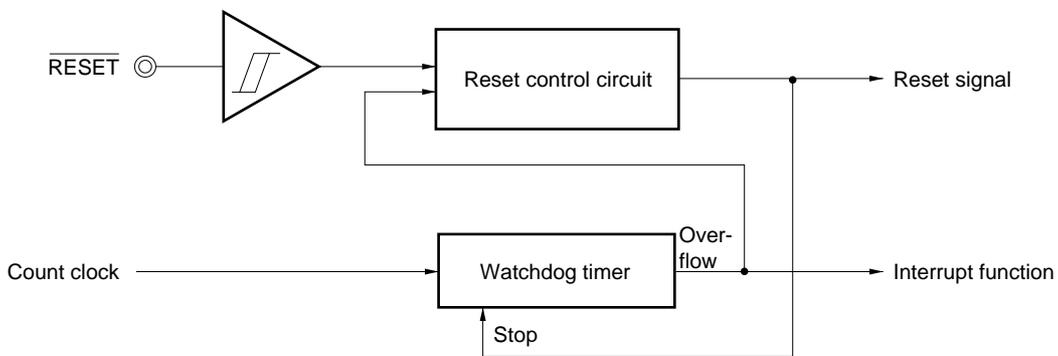
Table 8-1. State of the Hardware after a Reset

Hardware		State after reset
Program counter (PC)[Note 1]		Loaded with the contents of the reset vector table (0000H, 0001H)
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose register	Undefined[Note 2]
Ports (P0, P2, P4, P5, P8, P9) (output latch)		00H
Port mode registers (PM0, PM2, PM4, PM5, PM8, PM9)		FFH
Pull-up resistor option registers (PU0 to PU2)		00H
Processor clock control register (PCC)		02H
Subsystem clock oscillation mode register (SCKM)		00H
Subclock control register (CSS)		00H
Oscillation settling time selection register (OSTS)		04H
16-bit timer/counter 5	Timer register (TM5)	0000H
	Compare register (CR50)	FFFFH
	Capture register (TCP5)	Undefined
	Mode control register (TMC5)	00H
8-bit timer/event counters 0 to 2	Timer registers (TM0 to TM2)	00H
	Compare registers (CR00 to CR20)	Undefined
	Mode control registers (TMC0 to TMC2)	00H
Clock timer	Mode control register (WTM)	00H
Watchdog timer	Timer clock selection register (TCL2)	00H
	Mode register (WDTM)	00H
A/D converter	Mode register (ADM)	00H
	A/D converter input selection register (ADS)	00H
	10-bit A/D conversion result register (ADCR)	Undefined
Comparator	Mode register 0 (CMPRM0)	00H
LCD controller/driver	LCD display mode register (LCDM)	00H
	LCD port selector (LPS)	00H
	LCD clock control register (LCDC)	00H
Serial interface	Mode register (CSIM0)	00H
	Asynchronous serial interface mode register (ASIM)	00H
	Asynchronous serial interface status register (ASIS)	00H
	Baud rate generator control register (BRGC)	00H
	Transmission shift register (TXS)	FFH
	Reception buffer register (RXB)	Undefined
Interrupts	Request flag registers (IF0, IF1)	00H
	Mask flag registers (MK0, MK1)	FFH
	External interrupt mode registers (INTM0, INTM1)	00H
	Key return mode register (KRM)	00H

Notes 1. While a reset signal is being input, and during the oscillation settling period, the contents of the PC will be undefined, while the remainder of the hardware will be the same as after the reset.

2. In standby mode, the RAM enters the hold state after a reset.

9. MASK OPTIONS

The *μ*PD789415, *μ*PD789416, and *μ*PD789417 have the following mask options.

- Mask option for P50 to P53
  This option is used to specify whether to incorporate a pull-up resistor, as follows:
  <1> To indicate whether a pull-up resistor is to be incorporated, an individual bit is specified, independently of the other bits.
  <2> The specification of each bit indicates that a pull-up resistor is not to be incorporated.

- Mask option for the V_{LC0} to V_{LC2} pins and BIAS pin
  This option is used to specify whether a voltage division resistor is to be incorporated for the LCD driver, as listed below:

		R_{LC1} ($2 \times R_{LC2}$)		
		None	20 kΩ	200 kΩ
R_{LC2}	None	○	–	–
	10 kΩ	○	○	–
	100 kΩ	○	–	○

○ : Selectable
– : Not selectable
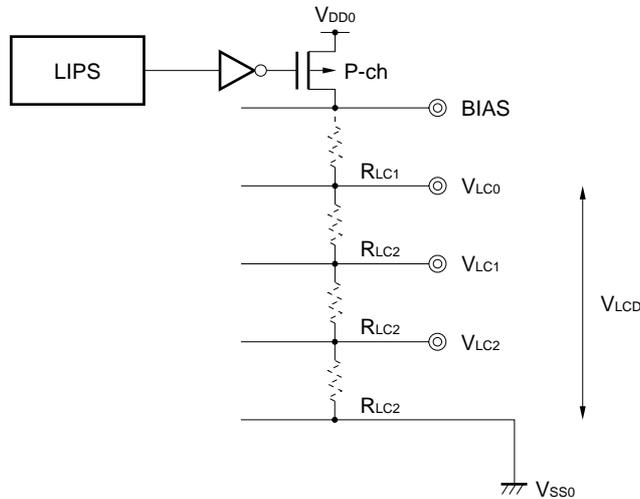
LIPS: Bit 4 of the LCD display mode register (LCDM)

10. INSTRUCTION SET OVERVIEW

The instruction set for the *μ*PD789415, *μ*PD789416, and *μ*PD789417 is listed later.

10.1 Legend

10.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (the details conform with the assembly specification). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and a pair of [and] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows:

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [and]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or a pair of [and].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 10-1).

Table 10-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH: Immediate data or label FE20H to FF1FH: Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH: Immediate data or label (only even address for 16-bit data transfer instructions) 0040H to 007FH: Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

Remark For the special function register symbols, see **Table 4-1**.

10.1.2 Descriptions of the operation field

A	:	A register (8-bit accumulator)
X	:	X register
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
AX	:	AX register pair (16-bit accumulator)
BC	:	BC register pair
DE	:	DE register pair
HL	:	HL register pair
PC	:	Program counter
SP	:	Stack pointer
PSW	:	Program status word
CY	:	Carry flag
AC	:	Auxiliary carry flag
Z	:	Zero flag
IE	:	Interrupt request enable flag
NMIS	:	Flag to indicate that a nonmaskable interrupt is being handled
()	:	Contents of a memory location indicated by a parenthesized address or register name
X_H, X_L	:	Upper and lower 8 bits of a 16-bit register
^	:	Logical product (AND)
∨	:	Logical sum (OR)
⊻	:	Exclusive OR
—	:	Inverted data
addr16	:	16-bit immediate data or label
jdisp8	:	Signed 8-bit data (displacement value)

10.1.3 Description of the flag operation field

(blank)	:	No change
0	:	To be cleared to 0
1	:	To be set to 1
×	:	To be set or cleared according to the result
R	:	To be restored to the previous value

10.2 Operations

Mnemonic	Operand		Byte	Clock	Operation	Flag		
						Z	AC	CY
MOV	r, #byte		3	6	r ← byte			
	saddr, #byte		3	6	(saddr) ← byte			
	sfr, #byte		3	6	sfr ← byte			
	A, r	Note 1	2	4	A ← r			
	r, A	Note 1	2	4	r ← A			
	A, saddr		2	4	A ← (saddr)			
	saddr, A		2	4	(saddr) ← A			
	A, sfr		2	4	A ← sfr			
	sfr, A		2	4	sfr ← A			
	A, !addr16		3	8	A ← (addr16)			
	!addr16, A		3	8	(addr16) ← A			
	PSW, #byte		3	6	PSW ← byte	×	×	×
	A, PSW		2	4	A ← PSW			
	PSW, A		2	4	PSW ← A	×	×	×
	A, [DE]		1	6	A ← (DE)			
	[DE], A		1	6	(DE) ← A			
	A, [HL]		1	6	A ← (HL)			
	[HL], A		1	6	(HL) ← A			
	A, [HL + byte]		2	6	A ← (HL + byte)			
	[HL + byte], A		2	6	(HL + byte) ← A			
XCH	A, X		1	4	A ↔ X			
	A, r	Note 2	2	6	A ↔ r			
	A, saddr		2	6	A ↔ (saddr)			
	A, sfr		2	6	A ↔ (sfr)			
	A, [DE]		1	8	A ↔ (DE)			
	A, [HL]		1	8	A ↔ (HL)			
	A, [HL + byte]		2	8	A ↔ (HL + byte)			
MOVW	rp, #word		3	6	rp ← word			
	AX, saddrp		2	6	AX ← (saddrp)			
	saddrp, AX		2	8	(saddrp) ← AX			
	AX, rp	Note 3	1	4	AX ← rp			
	rp, AX	Note 3	1	4	rp ← AX			

Notes 1. Except when r = A.
2. Except when r = A or X.
3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (fCPU), specified in the processor clock controller register (PCC).

Mnemonic	Operand		Byte	Clock	Operation	Flag		
						Z	AC	CY
XCHW	AX, rp	Note 3	1	8	AX ↔ rp			
ADD	A, #byte		2	4	A, CY ← A + byte	×	×	×
	saddr, #byte		3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r		2	4	A, CY ← A + r	×	×	×
	A, saddr		2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16		3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]		1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]		2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte		2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte		3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r		2	4	A, CY ← A + r + CY	×	×	×
	A, saddr		2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16		3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]		1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]		2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte		2	4	A, CY ← A – byte	×	×	×
	saddr, #byte		3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r		2	4	A, CY ← A – r	×	×	×
	A, saddr		2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16		3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]		1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]		2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte		2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte		3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r		2	4	A, CY ← A – r – CY	×	×	×
	A, saddr		2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16		3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]		1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]		2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte		2	4	A ← A ∧ byte	×		
	saddr, #byte		3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r		2	4	A ← A ∧ r	×		
	A, saddr		2	4	A ← A ∧ (saddr)	×		
	A, !addr16		3	8	A ← A ∧ (addr16)	×		
	A, [HL]		1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]		2	6	A ← A ∧ (HL + byte)	×		

Remark The instruction clock cycle is based on the CPU clock (fCPU), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A, ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r – 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP − 1) ← (PC + 3)$_H$, (SP − 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP − 2			
CALLT	[addr5]	1	8	(SP − 1) ← (PC + 1)$_H$, (SP − 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP − 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP − 1) ← PSW, SP ← SP − 1			
	rp	1	4	(SP − 1) ← rp$_H$, (SP − 2) ← rp$_L$, SP ← SP − 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}), specified in the processor clock controller register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1			
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0			
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B ← B − 1, then PC ← PC + 2 + jdisp8 if B ≠ 0			
	C, $addr16	2	6	C ← C − 1, then PC ← PC + 2 + jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr) ← (saddr) − 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE ← 1 (Enable Interrupt)			
DI		3	6	IE ← 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$), specified in the processor clock controller register (PCC).

11. ELECTRICAL CHARACTERISTICS (TARGET VALUES)

Caution **The ratings listed below are target values for the product, established in the development stage.**

When designing an application system, refer to the following data sheet, which details the formal electrical characteristics:

μ**PD789415, 789416, 789417 Data Sheet: In preparation**

ABSOLUTE MAXIMUM RATINGS (T$_A$ = 25 °C)

(Target values)

Parameter	Symbol	Conditions			Rated value	Unit
Supply voltage	V$_{DD}$				−0.3 to +7.0	V
Input voltage	V$_{I1}$	Pins other than those for port 5			−0.3 to V$_{DD}$ + 0.3	V
	V$_{I2}$	P50-P53	N-channel, open-drain		−0.3 to +13	V
Output voltage	V$_O$				−0.3 to V$_{DD}$ + 0.3	V
Output high current	I$_{OH}$	Each pin		Peak value	−10	mA
				rms	−5	mA
		Total for all pins		Peak value	−30	mA
				rms	−15	mA
Output low current	I$_{OL}$**Note**	Each pin		Peak value	30	mA
				rms	15	mA
		Total for all pins		Peak value	160	mA
				rms	80	mA
Operating ambient temperature	T$_A$				−40 to +85	°C
Storage temperature	T$_{stg}$				−65 to +150	°C

Note Calculate rms with [rms] = [peak value] $\times$ $\sqrt{\text{duty cycle}}$.

Caution **Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.**

Remark The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

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CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATION CIRCUIT
(T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(Target values)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	IC X2 X1 / R1 / C2 C1	Oscillator frequency (f_X)[Note 1]	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation settling time[Note 2]	After V_{DD} reaches MIN. of the oscillation voltage range			4	ms
Crystal	IC X2 X1 / C2 C1	Oscillator frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation settling time[Note 2]	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock	X2 X1 / μPD74HCU04	X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. Only the characteristic of the oscillation circuit is indicated. See the description of the AC characteristic for the instruction execution time.
2. Time required for oscillation to settle once a reset sequence ends or STOP mode is deselected.

Cautions 1. When using the main system clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.
  • **Keep the wiring as short as possible.**
  • **Do not allow signal wires to cross one another.**
  • **Keep the wiring away from wires that carry a high, non-stable current.**
  • **Keep the grounding point of the capacitors at the same level as V_{SS}.**
  • **Do not connect the grounding point to a grounding wire that carries a high current.**
  • **Do not extract a signal from the oscillation circuit.**
  2. Before switching from the subsystem clock back to the main system clock, always allow sufficient time for the oscillation to settle by specifying it in the program.

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATION CIRCUIT
(T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(Target values)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal	IC XT2 XT1 R2 C4 C3	Oscillator frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation settling time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock	XT2 XT1 μPD74HCU04	XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		14.3		15.6	μs
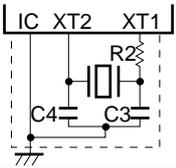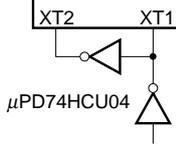
Notes 1. Only the characteristic of the oscillation circuit is indicated. See the description of the AC characteristic for the instruction execution time.

    2. Time required for oscillation to settle after V_{DD} reaches the MIN. value of the oscillation voltage range.

Cautions 1. When using the subsystem clock oscillation circuit, observe the following conditions for the wiring of that section enclosed in dotted lines in the above diagrams, so as to avoid the influence of the wiring capacitance.
- **Keep the wiring as short as possible.**
- **Do not allow signal wires to cross one another.**
- **Keep the wiring away from wires that carry a high, non-stable current.**
- **Keep the grounding point of the capacitors at the same level as V_{SS}.**
- **Do not connect the grounding point to a grounding wire that carries a high current.**
- **Do not extract a signal from the oscillation circuit.**

    2. The subsystem clock oscillation circuit is designed to have a low amplification degree so as to maintain a low current drain. Therefore, it is more likely to malfunction as a result of noise than the main system clock oscillation circuit. When using the subsystem clock, therefore, pay particularly careful attention to how it is wired.

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DC CHARACTERISTICS (T_A =–40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(Target values)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P00-P03, P46, P47, P60-P66, P80-P87, P90-P93	V_{DD} = 2.7 to 5.5 V	$0.7V_{DD}$		V_{DD}	V
				$0.9V_{DD}$		V_{DD}	V
	V_{IH2}	P50-P53	V_{DD} = 2.7 to 5.5 V	$0.7V_{DD}$		12	V
				$0.9V_{DD}$		12	V
	V_{IH3}	$\overline{RESET}$, P20-P27, P40-P45	V_{DD} = 2.7 to 5.5 V	$0.8V_{DD}$		V_{DD}	V
				$0.9V_{DD}$		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	P00-P03, P46, P47, P60-P66, P80-P87, P90-P93	V_{DD} = 2.7 to 5.5 V	0		$0.3V_{DD}$	V
				0		$0.1V_{DD}$	V
	V_{IL2}	P50-P53	V_{DD} = 2.7 to 5.5 V	0		$0.3V_{DD}$	V
				0		$0.1V_{DD}$	V
	V_{IL3}	$\overline{RESET}$, P20-P27, P40-P45	2.7 V $\leq V_{DD} \leq$ 5.5 V	0		$0.2V_{DD}$	V
				0		$0.1V_{DD}$	V
	V_{IL4}	X1, X2		0		0.1	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		V_{DD} = 4.5 to 5.5 V, I_{OH} = –100 μA		V_{DD} – 0.5			V
Low-level output voltage	V_{OL1}	Pins other than those for port 5	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50-P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
High-level input leakage current	L_{LIH1}	V_{IN} = V_{DD}	Pins other than the X1 pin, X2 pin, or those for port 5			3	μA
	L_{LIH2}		X1, X2			20	μA
	L_{LIH3}	V_{IN} = 12 V	P50-P53 (N-channel, open-drain)			20	μA
Low-level input leakage current	L_{LIL1}	V_{IN} = 0 V	Pins other than the X1 pin, X2 pin, or those for port 5			–3	μA
	L_{LIL2}		X1, X2			–20	μA
	L_{LIL3}		P50-P53 (N-channel, open-drain) During input instruction execution			–30	μA
High-level output leakage current	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V				–3	μA

Remark The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(Target values)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Software-specified pull-up resistor	R_1	V_{IN} = 0 V, for pins other than those for ports 5 and 6		50	100	200	kΩ
Mask option-specified pull-up resistor	R_2	V_{IN} = 0 V, P50-P53		15	30	60	kΩ
Power supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operating mode	V_{DD} = 5.0 V $\pm$ 10 %[Note 3]		5.5	16.5	mA
			V_{DD} = 3.0 V $\pm$ 10 %[Note 4]		0.7	2.1	mA
			V_{DD} = 2.0 V $\pm$ 10 %[Note 4]		0.4	1.2	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V $\pm$ 10 %		1.2	3.6	mA
			V_{DD} = 3.0 V $\pm$ 10 %		0.5	1.5	mA
			V_{DD} = 2.0 V $\pm$ 10 %		0.3	0.9	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 2]	V_{DD} = 5.0 V $\pm$ 10 %		100	200	μA
			V_{DD} = 3.0 V $\pm$ 10 %		70	140	μA
			V_{DD} = 2.0 V $\pm$ 10 %		50	100	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 2]	V_{DD} = 5.0 V $\pm$ 10 %		25	55	μA
			V_{DD} = 3.0 V $\pm$ 10 %		5	25	μA
			V_{DD} = 2.0 V $\pm$ 10 %		2.5	12.5	μA
	I_{DD5}	32.768-kHz crystal stop STOP mode	V_{DD} = 5.0 V $\pm$ 10 %		0.1	30	μA
			V_{DD} = 3.0 V $\pm$ 10 %		0.05	10	μA
			V_{DD} = 2.0 V $\pm$ 10 %		0.05	10	μA
	I_{DD6}	5.0-MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V $\pm$ 10 %		6.1	18.3	mA
			V_{DD} = 3.0 V $\pm$ 10 %		1.3	2.9	mA
			V_{DD} = 2.0 V $\pm$ 10 %		1.0	3.0	mA

Notes 1. The power supply current does not include AV_{REF}, AV_{DD}, or the port current (including the current flowing through the built-in pull-up resistor).

    2. When the main system clock is not running.

    3. During high-speed mode operation (when the processor clock control register (PCC) is cleared to 00H.)

    4. During low-speed mode operation (when 02H is loaded into the PCC.)

Remark The characteristic of a dual-function pin does not differ between the port function and the secondary function, unless otherwise stated.

DC CHARACTERISTICS (T$_A$ = –40 to +85 °C, V$_{DD}$ = 1.8 to 5.5 V)

LCD Characteristics

(Target values)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V$_{LCD}$	VAON = 1		1.8		V$_{DD}$	V
		VAON = 0[Note 1]		2.7		V$_{DD}$	V
LCD voltage divider resistor [Note 2]	R$_{LCD1}$			50	100	200	kΩ
	R$_{LCD2}$			5	10	20	kΩ
LCD output voltage deviation[Note 3] (common)	V$_{ODC}$	I$_O$ = ±5 μA	V$_{LCD0}$ = V$_{LCD}$ $\quad$ V$_{LCD1}$ = V$_{LCD}$ × 2/3	0		±0.2	V
LCD output voltage deviation[Note 3] (segment)	V$_{ODS}$	I$_O$ = ±1 μA	2.2 V ≤ V$_{LCD}$ ≤ V$_{DD}$ $\quad$ V$_{LCD2}$ = V$_{LCD}$ × 1/3[Note1]	0		±0.2	V

Notes 1. For an ordinary mode (VAON = 0), T$_A$ = –10 to +85 °C.

2. R$_{LCD1}$, R$_{LCD2}$, or no-resistor can be selected using the mask option.

3. The voltage deviation is the deviation of the segment or common output voltage from the ideal value (V$_{LCDn}$, where n = 0, 1, or 2).

AC CHARACTERISTICS

(1) Basic operations (T$_A$ = −40 to +85 °C, V$_{DD}$ = 1.8 to 5.5 V)

(Target values)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T$_{CY}$	Operation based on the main system clock	V$_{DD}$ = 2.7 to 5.5 V	0.4		32	μs
				1.6		32	μs
		Operation based on the subsystem clock			122		μs
TI0 and TI1 input high/low level width	t$_{TIH}$, t$_{TIL}$	V$_{DD}$ = 2.7 to 5.5 V		0.1			μs
				1.8			μs
TI0 and TI1 input frequency	f$_{TI}$	V$_{DD}$ = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
Interrupt input high/low level width	t$_{INTH}$, t$_{INTL}$	INTP0-INTP3	V$_{DD}$ = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low level width	t$_{RSL}$	V$_{DD}$ = 2.7 to 5.5 V		10			μs
				20			μs

T$_{CY}$ vs V$_{DD}$ (main system clock)
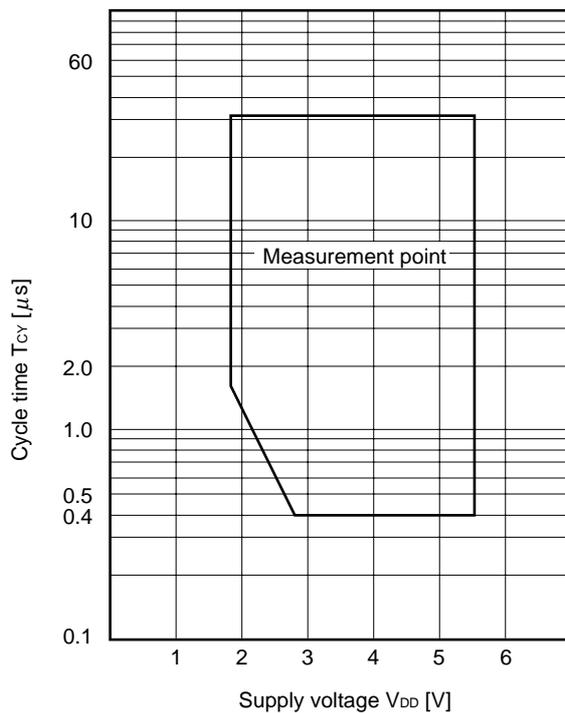
(2) Serial interface (T$_A$ = –40 to +85 °C, V$_{DD}$ = 1.8 to 5.5 V)

(a) Serial interface channel 0

(i) Three-wire serial I/O mode ($\overline{SCK}$...Internal clock output)

(Target values)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t$_{KCY1}$	V$_{DD}$ = 2.7 to 5.5 V		800			ns
				3 200			ns
$\overline{SCK}$ high/low level width	t$_{KH1}$, t$_{KL1}$	V$_{DD}$ = 2.7 to 5.5 V		t$_{KCY1}$/2–50			ns
				t$_{KCY1}$/2–150			ns
SI setup time (for $\overline{SCK}$ ↑)	t$_{SIK1}$	V$_{DD}$ = 2.7 to 5.5 V		150			ns
				500			ns
SI hold time (for $\overline{SCK}$ ↑)	t$_{KSI1}$	V$_{DD}$ = 2.7 to 5.5 V		400			ns
				600			ns
Delay from $\overline{SCK}$↓ to SO output	t$_{KSO1}$	R = 1 kΩ, C = 100 pF**Note**	V$_{DD}$ = 2.7 to 5.5 V	0		250	ns
				0		1 000	ns

Note R and C are the resistance and capacitance of the SO output line, respectively.

(ii) Three-wire serial I/O mode ($\overline{SCK}$...External clock output)

(Target values)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t$_{KCY2}$	V$_{DD}$ = 2.7 to 5.5 V		800			ns
				3 200			ns
$\overline{SCK}$ high/low level width	t$_{KH2}$, t$_{KL2}$	V$_{DD}$ = 2.7 to 5.5 V		400			ns
				1 600			ns
SI setup time (for $\overline{SCK}$ ↑)	t$_{SIK2}$	V$_{DD}$ = 2.7 to 5.5 V		100			ns
				150			ns
SI hold time (for $\overline{SCK}$ ↑)	t$_{KSI2}$	V$_{DD}$ = 2.7 to 5.5 V		400			ns
				600			ns
Delay from $\overline{SCK}$↓ to SO output	t$_{KSO2}$	R = 1 kΩ, C = 100 pF**Note**	V$_{DD}$ = 2.7 to 5.5 V	0		300	ns
				0		1 000	ns

Note R and C are the resistance and capacitance of the SO output line, respectively.

(iii) UART mode (dedicated baud rate generator output)

(Target values)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V$_{DD}$ = 2.7 to 5.5 V			78 125	bps
					19 531	bps

(iv) UART mode (external clock input)

(Target values)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
			3 200			ns
ASCK high/low level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1 600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39 063	bps
					9 766	bps
ASCK rising time, falling time	t_R, t_F				1	μs

AC TIMING MEASUREMENT POINTS (except the X1 and XT1 inputs)

CLOCK TIMING

X1 input

XT1 input

TI TIMING

TI0, TI1
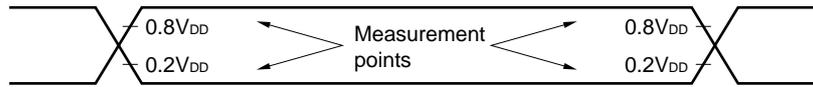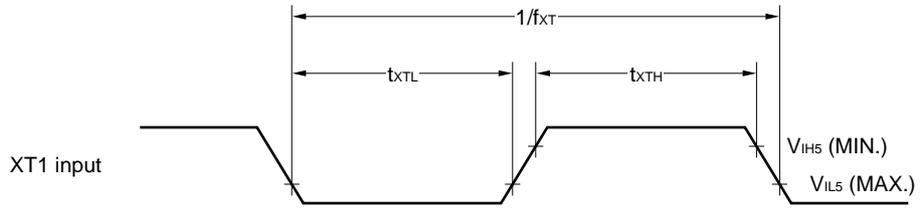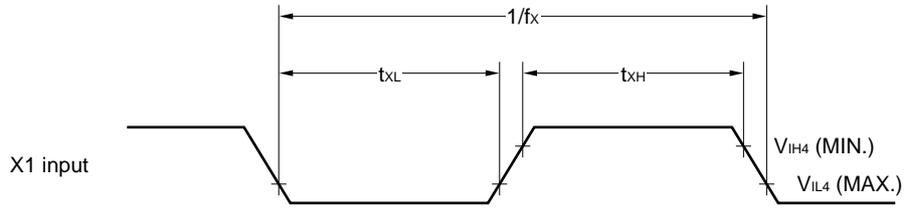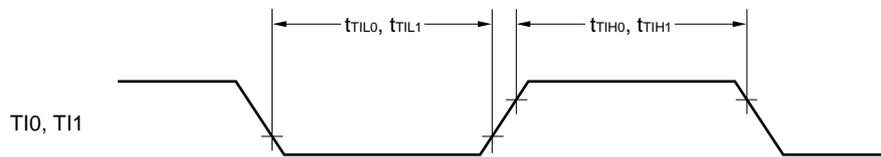
SERIAL TRANSFER TIMING

Three-Wire Serial I/O Mode:
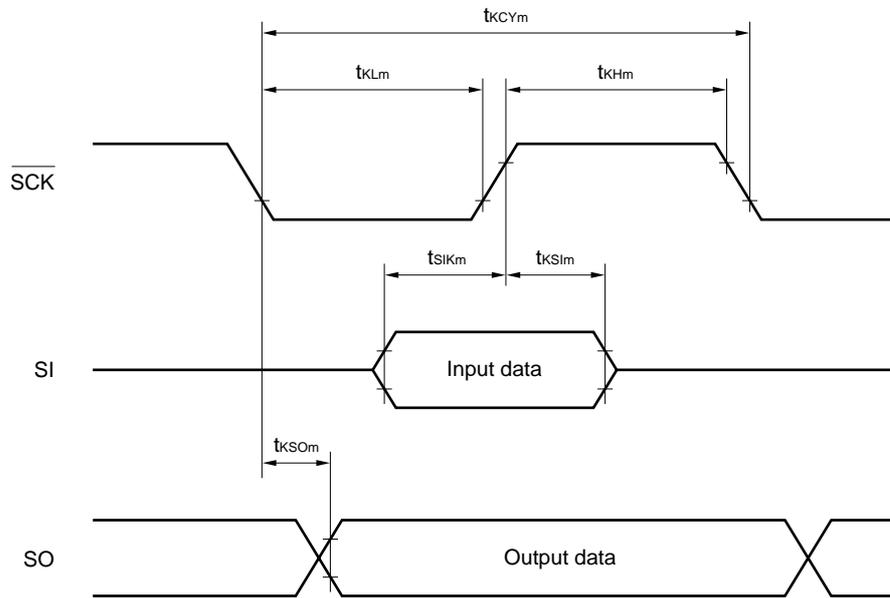
UART Mode (External Clock Input):
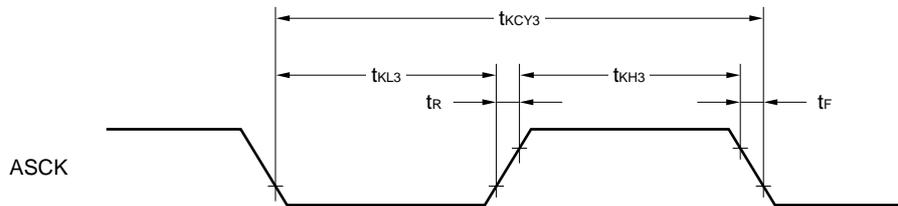
10-BIT A/D CONVERTER CHARACTERISTICS (T$_A$ = –40 to +85 °C, AV$_{DD}$ = V$_{DD}$ = 1.8 to 5.5 V, AV$_{SS}$ = V$_{SS}$ = 0 V)

(Target values)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Total error [Note]		2.7 V ≤ AV$_{DD}$ ≤ 5.5 V			4	LSB
		1.8 V ≤ AV$_{DD}$ ≤ 2.7 V			6	LSB
Conversion time	t$_{CONV}$		14			μs
Analog input voltage	V$_{IAN}$		0		V$_{DD}$	V
Reference voltage	AV$_{REF}$		1.8		V$_{DD}$	V

Note No quantization error (±1/2 LSB) is included.

COMPARATOR CHARACTERISTICS (T$_A$ = –40 to +85 °C, V$_{DD}$ = 1.8 to 5.5 V)

(Target values)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Analog input range	V$_{CIN}$	V$_{DD}$ = 1.8 to 5.5 V	0		V$_{DD}$	V
Reference voltage input range	V$_{CREF}$	V$_{DD}$ = 2.7 to 5.5 V	1.1	1.4	1.7	V
		V$_{DD}$ = 1.8 to 2.7 V	1.1	1.2	1.3	V
Precision		V$_{DD}$ = 1.8 to 5.5 V			±100	mV

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA HOLD CHARACTERISTICS (T$_A$ = –40 to +85 °C)

(Target values)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data hold supply voltage	V$_{DDDR}$		1.8		5.5	V
Release signal set time	t$_{SREL}$		0			μs
Oscillation settling time	t$_{WAIT}$	Reset by $\overline{\text{RESET}}$		2^{15}/f$_X$		ms
		Reset by interrupt		**Note**		ms

Note 2^{12}/f$_X$, 2^{15}/f$_X$, or 2^{17}/f$_X$ can be selected according to the setting of bits 0 to 2 (OSTS0 to OSTS2) of the oscillation settling time selection register.

Remark f$_X$: Main system clock oscillation frequency

DATA HOLD TIMING (STOP mode release by $\overline{\text{RESET}}$)

Internal reset operation

HALT mode

STOP mode

Operating mode

Data hold mode

V_{DD}

V_{DDDR}

t_{SREL}

STOP instruction execution

$\overline{\text{RESET}}$

t_{WAIT}
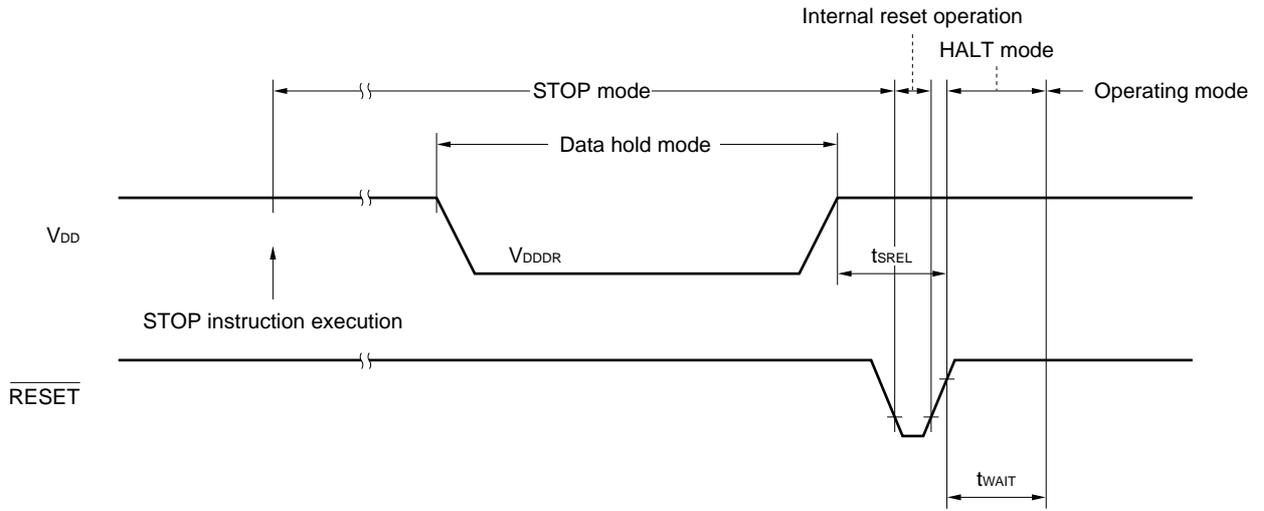
DATA HOLD TIMING (standby release signal: STOP mode release by interrupt signal)

HALT mode

STOP mode

Operating mode

Data hold mode

V_{DD}

V_{DDDR}

t_{SREL}

STOP instruction execution

Standby release signal
(interrupt request)

t_{WAIT}

115
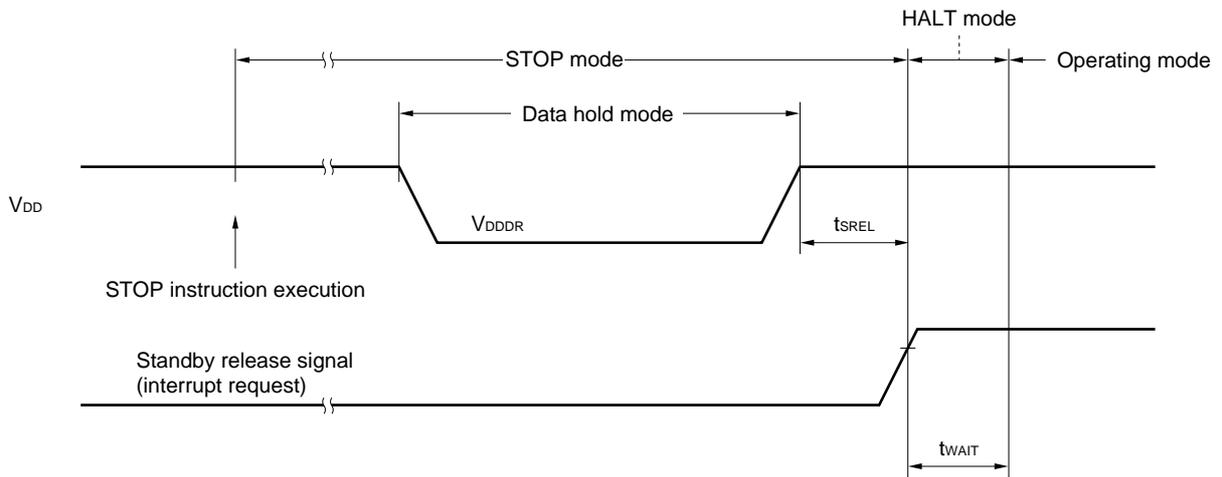
INTERRUPT INPUT TIMING

INTP0-INTP3

t_{INTL} t_{INTH}
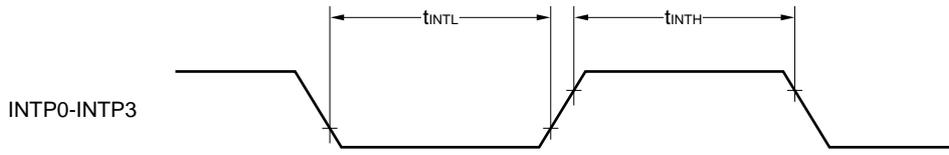
$\overline{\text{RESET}}$ **INPUT TIMING**

$\overline{\text{RESET}}$

t_{RSL}
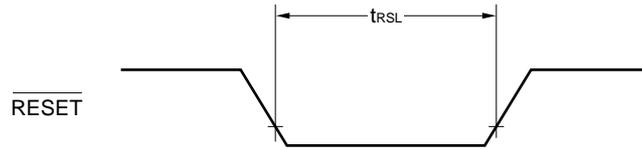
12. PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14×14)

detail of lead end
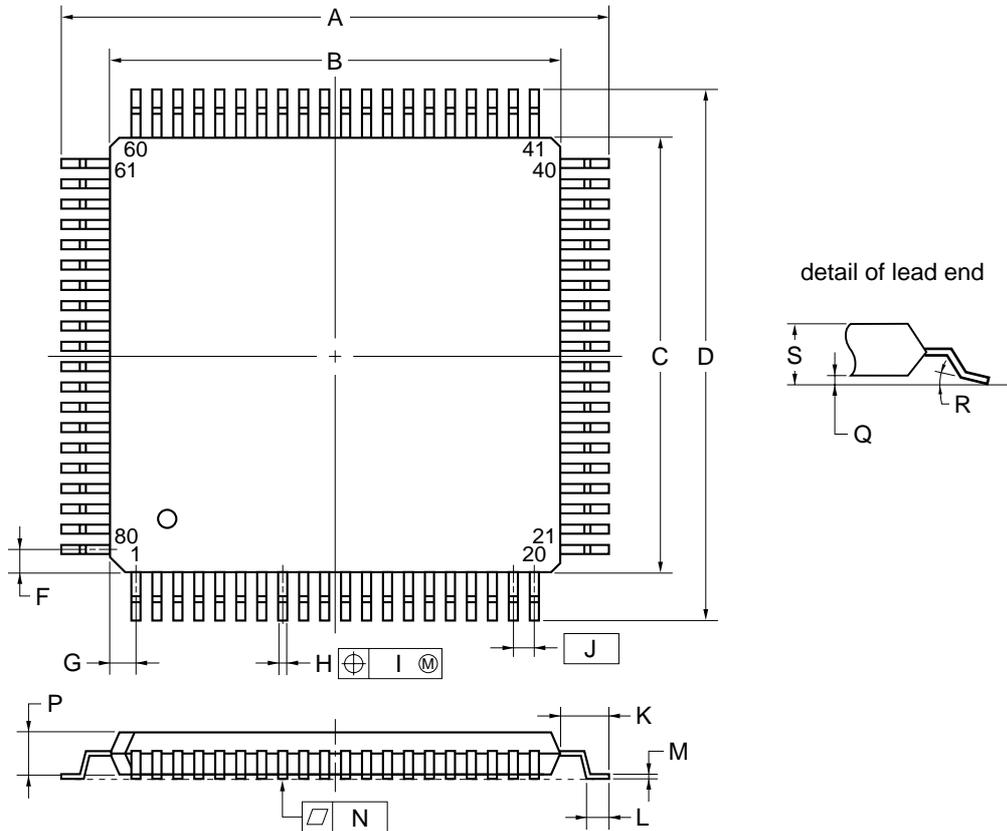
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (□12)

detail of lead end
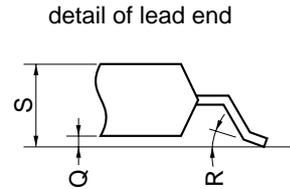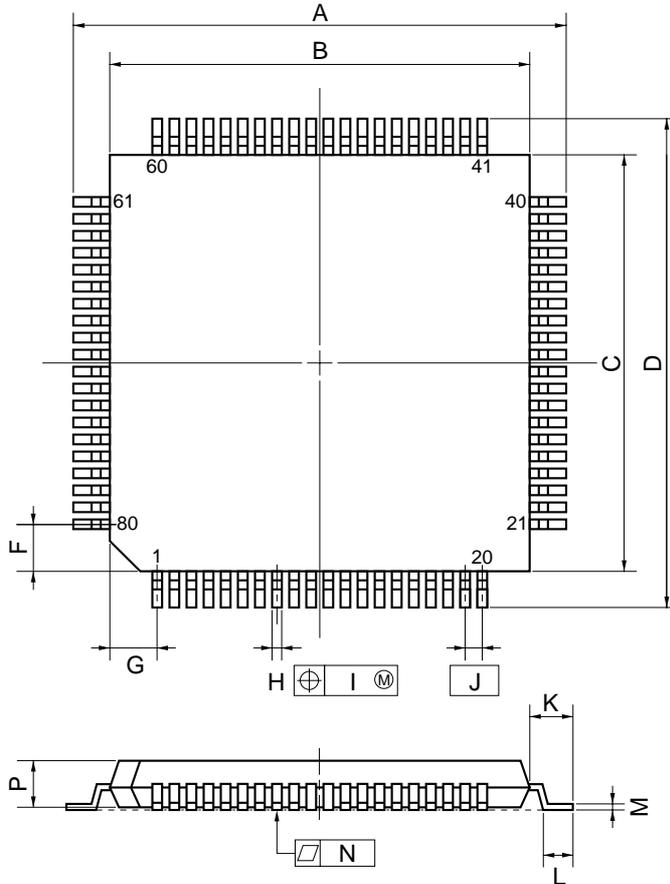
NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5¡±5¡	5¡±5¡
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD789415, μPD789416, and μPD789417.

LANGUAGE PROCESSING SOFTWARE

RA78K0S[Notes 1, 2, 3]	Assembler package common to the 78K/0S series
CC78K0S[Notes 1, 2, 3]	C compiler package common to the 78K/0S series
DF789417[Notes 1, 2, 3, 7]	Device file for the μPD789417 sub-series
CC78K0S-L[Notes 1, 2, 3, 7]	C compiler library source file common to the 78K/0S series

FLASH MEMORY WRITE TOOLS

Flashpro II[Note 4]	Dedicated flash writer (formerly, Flashpro)
FA-80GC[Note 4]	Flash memory write adapter
FA-80GK[Note 4]	

DEBUGGING TOOLS

ND-K904[Notes 4, 7]	In-circuit emulator for the μPD789417 sub-series The ND-K904 incorporates the NS-78K9 screen debugger.
IF-98D[Note 4]	This is an interface board, required when a PC-9800 series (other than a notebook type) are used as the host machine for the ND-K904.
IF-PCD[Note 4]	This is an interface board, required when an IBM PC/AT or compatible (other than a notebook type) is used as the host machine for the ND-K904.
IF-CARD[Note 4]	This is an interface board, required when a PC-9800 notebook, IBM PC/AT notebook, or compatible is used as the host machine for the ND-K904.
NP-80GC[Note 4]	Emulator probe for the 80-pin plastic QFP (GC-8BT type)
NP-80GK[Note 4]	Emulator probe for the 80-pin plastic TQFP (GK-BE9 type)
NJ-535[Note 4]	100/120 VAC adapter
NJ-550W[Note 4]	100-240 VAC adapter
SM78K0S[Notes 5, 6]	System emulator common to all 78K/0S series units
DF789417[Notes 5, 6, 7]	Device file for the μPD789417 sub-series

REAL-TIME OS

MX78K0S[Notes 1, 2, 7]	OS for the 78K/0S series

Notes 1. Based on the PC-9800 series (MS-DOS™)
   2. Based on the IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS)
   3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™), and NEWS™ (NEWS-OS™)
   4. Product manufactured by and available from Naito Densei Machida Seisakusho Co., Ltd. (044-822-3813).
   5. Based on the PC-9800 series (MS-DOS + Windows™)
   6. Based on the IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows)
   7. Under development

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789417.

APPENDIX B RELATED DOCUMENTS

DOCUMENTS RELATED TO DEVICES

Document name	Document No.	
	Japanese	English
μPD789415, 789416, 789417 Preliminary Product Information	U12302J	This manual
μPD78F9418 Preliminary Product Information	U12321J	To be created
μPD789407, 789417 Sub-Series User's Manual	To be released soon	To be created
78K/0 Series User's Manual 78K/0S Series − Instruction	U11047J	U11047E
78K/0S Series Instruction Summary Sheet	To be created	−
78K/0S Series Instruction Set	To be created	−
μPD789417 Sub-Series Special Function Registers	To be created	−

DOCUMENTS RELATED TO DEVELOPMENT TOOLS (USER'S MANUAL)

Document name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K/0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows Base	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E

DOCUMENTS RELATED TO SOFTWARE TO BE INCORPORATED INTO THE PRODUCT (USER'S MANUAL)

Document name	Document No.	
	Japanese	English
OS for 78K/0S Series MX78K0S	To be created	To be created

Caution   **The above documents may be revised without notice. Use the latest versions when you design application systems.**

OTHER DOCUMENTS

Document name	Document No.	
	Japanese	English
IC PACKAGE MANUAL	C10943X	
SMD Surface Mount Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	–
Guide to Quality Assurance for Semiconductor Device	C11893J	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	U11416J	–

**Caution The above documents may be revised without notice. Use the latest versions when you design
application systems.**

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability

- Ordering information

- Product release schedule

- Availability of related technical literature

- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Milton Keynes, UK
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