Digital Step Attenuator 75Ω DC-2000 MHz

15.5 dB, 0.5 dB Step
5 Bit, Parallel Control Interface, Dual Supply Voltage

Product Features

- Dual supply voltage: V_{DD}=+3V, V_{SS}=-3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Parallel control interface
- Fast switching control frequency, 1MHz Typ
- Low Insertion Loss
- High IP3, +52 dBm typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm

Typical Applications

- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

DAT-15575-PN+
DAT-15575-PN

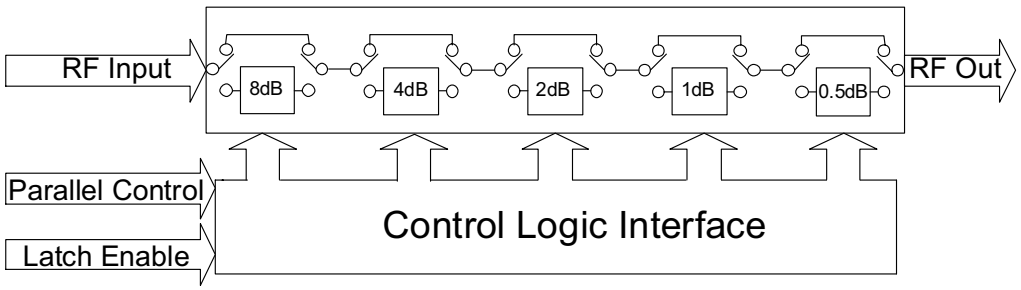
+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

General Description

The DAT-15575-PN is a 75Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps. The control is a 5-bit parallel interface, operating on dual supply voltage: V_{DD}=+3V, V_{SS}=-3V. The DAT-15575-PN is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



RF Electrical Specifications, DC-2000 MHz, T_{AMB}=25°C, V_{DD}=+3V, V_{SS}=-3V

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ **0.5 dB** Attenuation Setting	DC-1.2	—	0.03	0.17	dB
	1.2-2.0	—	0.05	0.18	dB
Accuracy @ **1 dB** Attenuation Setting	DC-1.2	—	0.03	0.19	dB
	1.2-2.0	—	0.1	0.2	dB
Accuracy @ **2 dB** Attenuation Setting	DC-1.2	—	0.07	0.23	dB
	1.2-2.0	—	0.15	0.25	dB
Accuracy @ **4 dB** Attenuation Setting	DC-1.2	—	0.05	0.25	dB
	1.2-2.0	—	0.15	0.35	dB
Accuracy @ **8 dB** Attenuation Setting	DC-1.2	—	0.1	0.25	dB
	1.2-2.0	—	0.24	0.55	dB
Insertion Loss(note1) @ all attenuator set to 0dB	DC-1.2	—	1.2	1.8	dB
	1.2-2.0	—	1.6	2.1	dB
Input IP3(note 2) (at Min. and Max. Attenuation)	DC-2.0	—	+52	—	dBm
Input Power @ 0.2dB Compression* (at Min. and Max. Attenuation)	DC-2.0	—	+24	—	dBm
VSWR	DC-1.2	—	1.6	2.0	—
	1.2-2.0	—	1.7	2.0	—

Notes:
1. I. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.40dB @1200MHz, 0.55dB @2000MHz, 0.75dB @4000MHz)
2. Input IP3 and 1dB compression degrades below 1 MHz

DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
V_{DD}, Supply Voltage	2.7	3	3.3	V
V_{SS}, Supply Voltage	-3.3	-3	-2.7	V
I_{DD} (I_{SS}), Supply Current	—	—	100	μA
Control Input Low	—	—	0.3xV_{DD}	V
Control Input High	0.7xV_{DD}	—	—	V
Control Current	—	—	1	μA

Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	μSec
Switching Control Frequency	—	1.0	—	MHz

Absolute Maximum Ratings

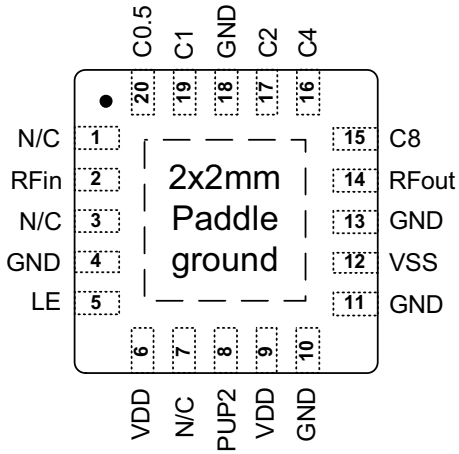
Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
V_{DD}	-0.3V Min., 4V Max.
V_{SS}	-4V Min., 0.3V Max.
Voltage on any input	-0.3V Min., V_{DD}+0.3V Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm

Pin Description

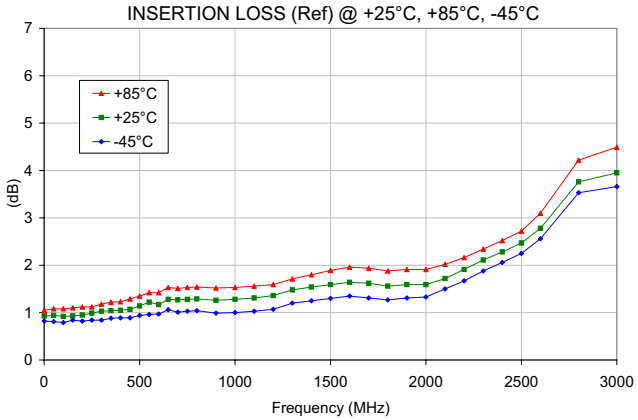
Function	Pin Number	Description
N/C	1	Not connected (Note 3)
RF in	2	RF in port (Note 1)
N/C	3	Not connected (Note 3)
GND	4	Ground connection
LE	5	Latch Enable Input (Note 2)
V_{DD}	6	Positive Supply Voltage
N/C	7	Not connected
PUP2	8	Power up selection bit
V_{DD}	9	Positive Supply Voltage
GND	10	Ground connection
GND	11	Ground connection
V_{SS}	12	Negative supply voltage
GND	13	Ground connection
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB
C4	16	Control for attenuation bit, 4 dB
C2	17	Control for attenuation bit, 2 dB
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB
C0.5	20	Control for attenuation bit, 0.5 dB
GND	Paddle	Paddle ground (Note 4)

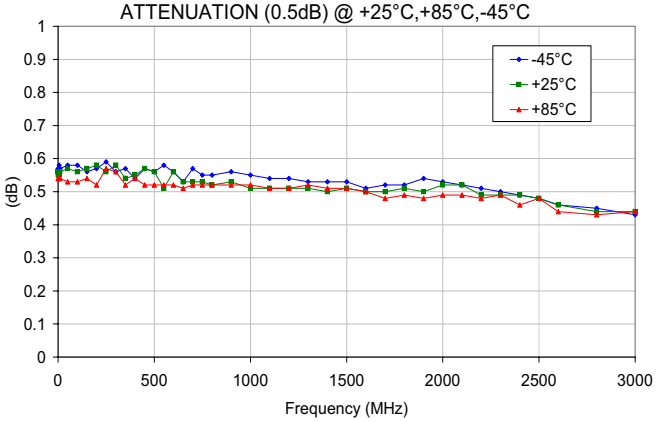
Notes:
1. Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
2. Latch Enable (LE) has an internal 100KΩ resistor to V_{DD}.
3. Place a shunt 10KΩ resistor to GND.
4. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation.

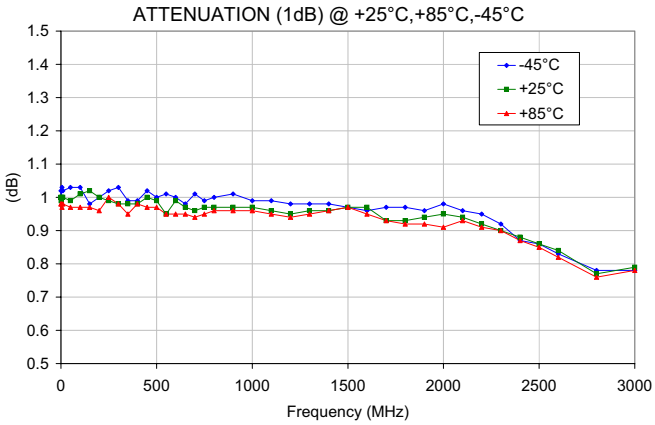
Pin Configuration (Top View)

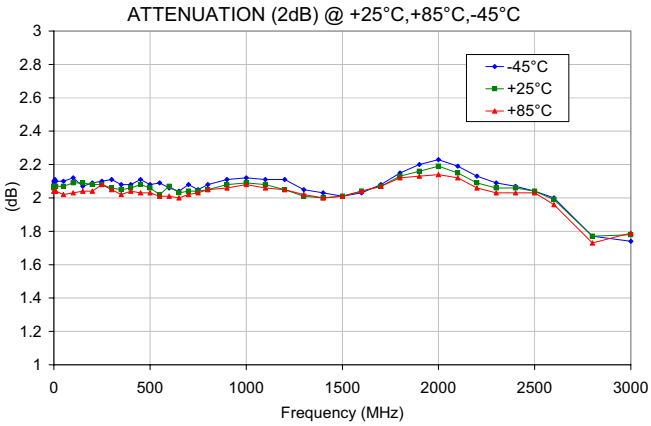


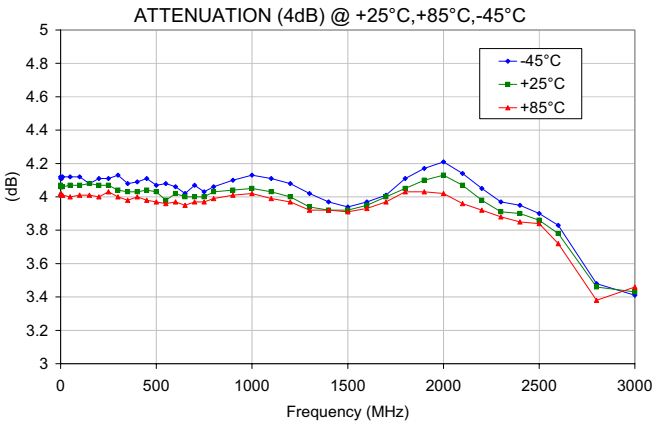
Typical Performance Curves

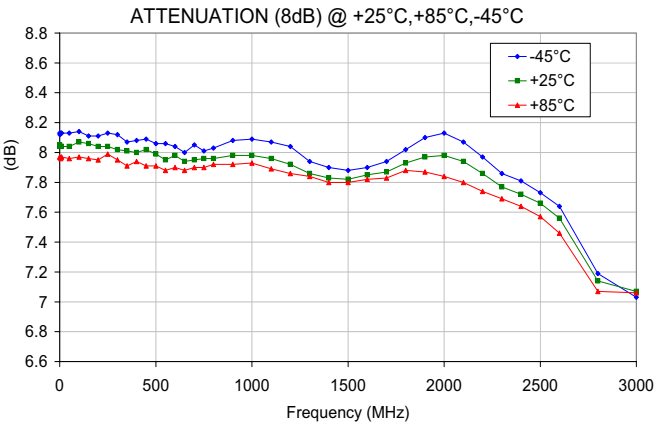




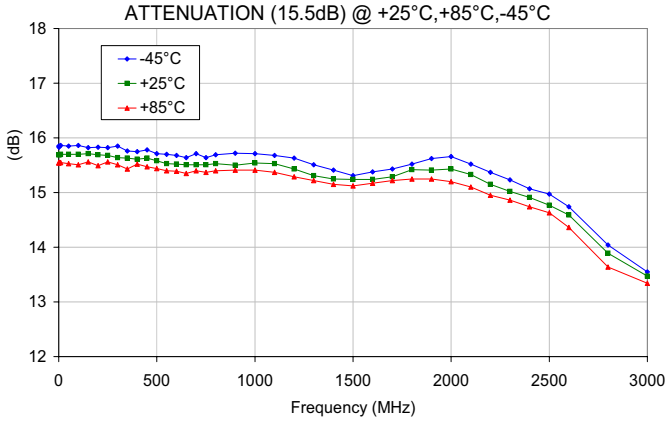


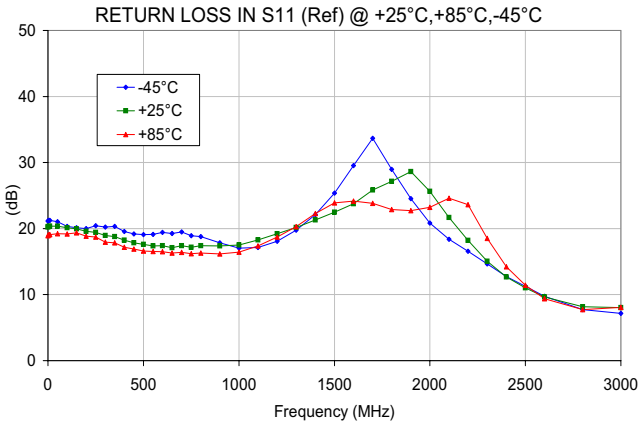


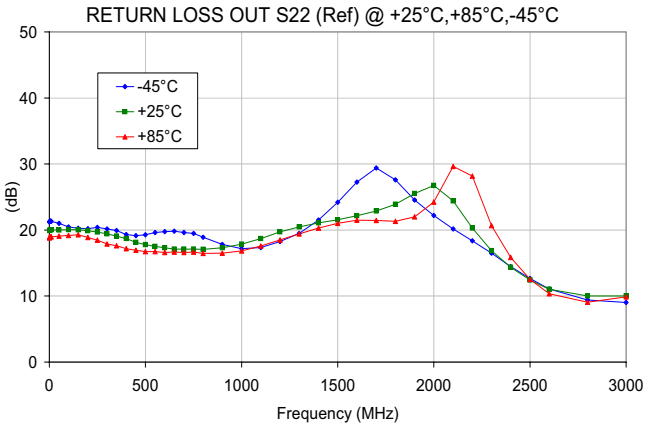


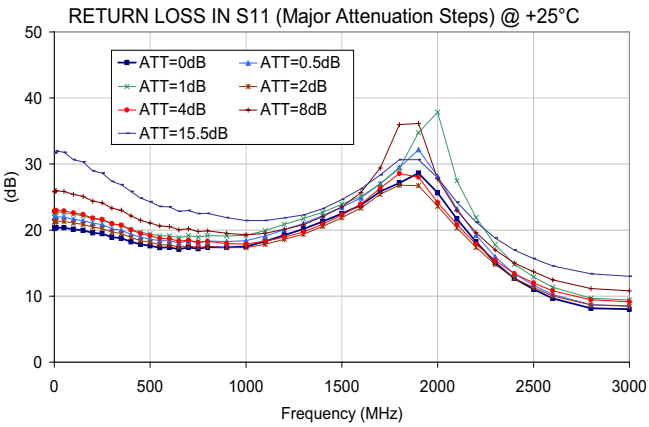


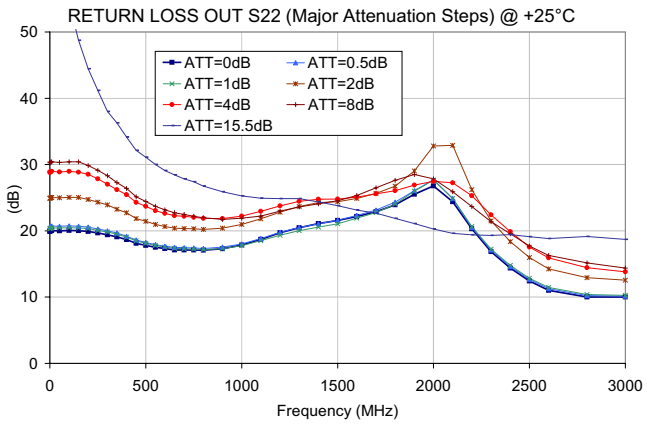
Typical Performance Curves



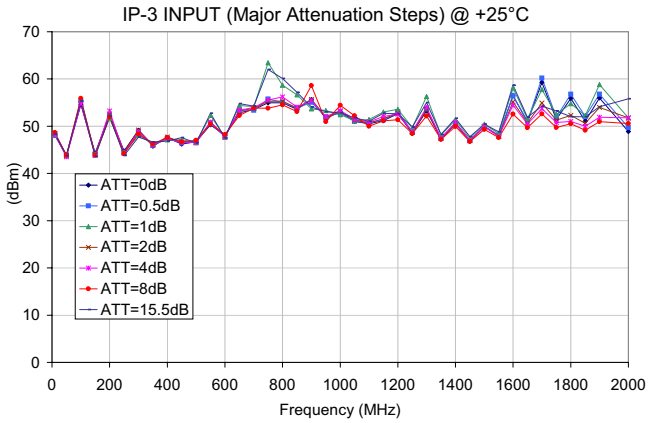


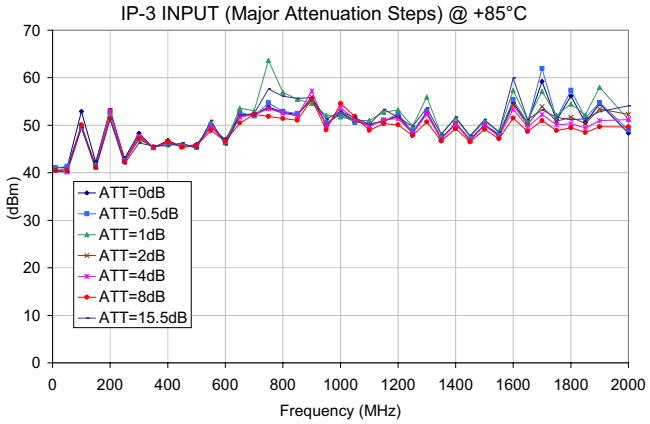


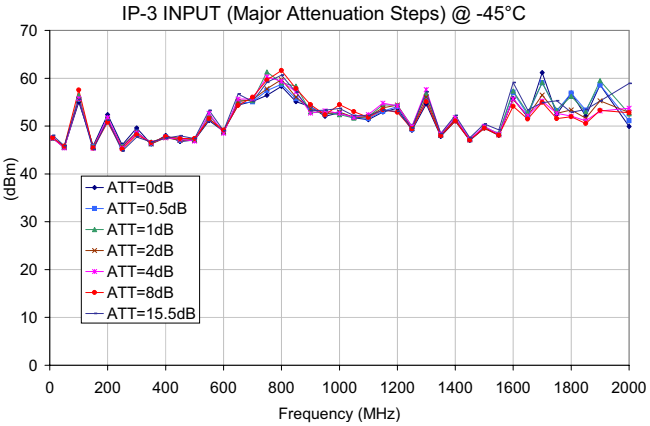


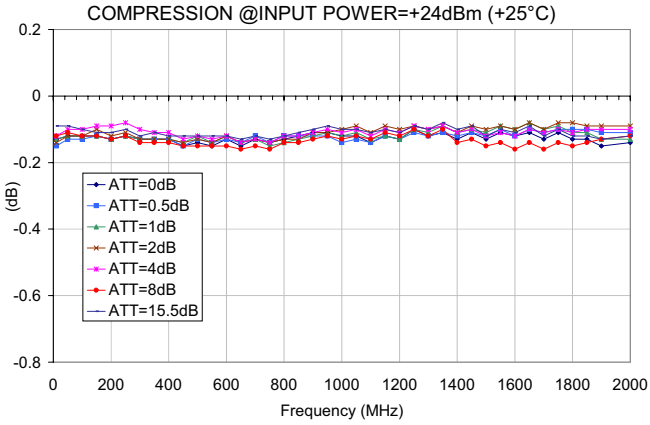


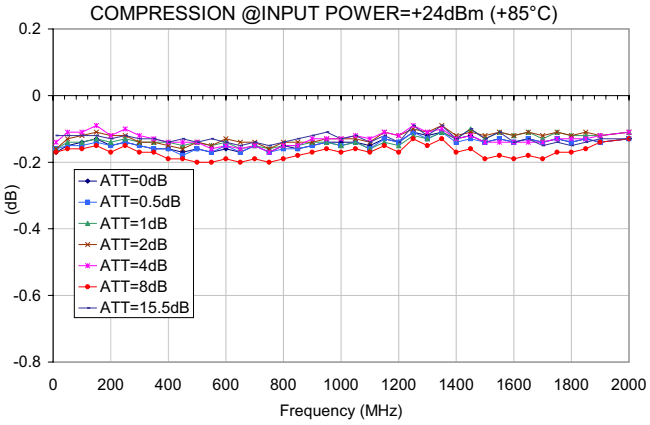
Typical Performance Curves

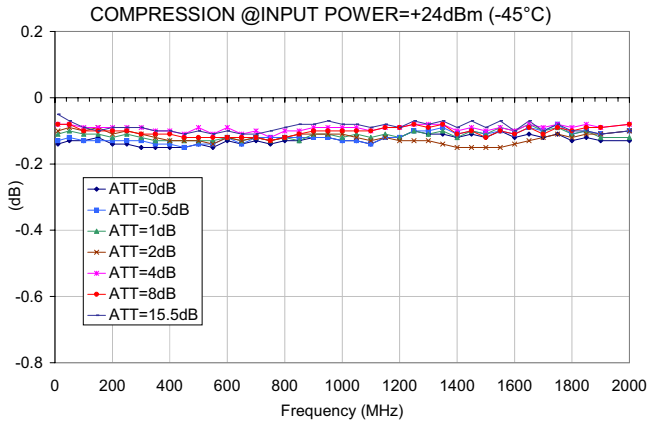




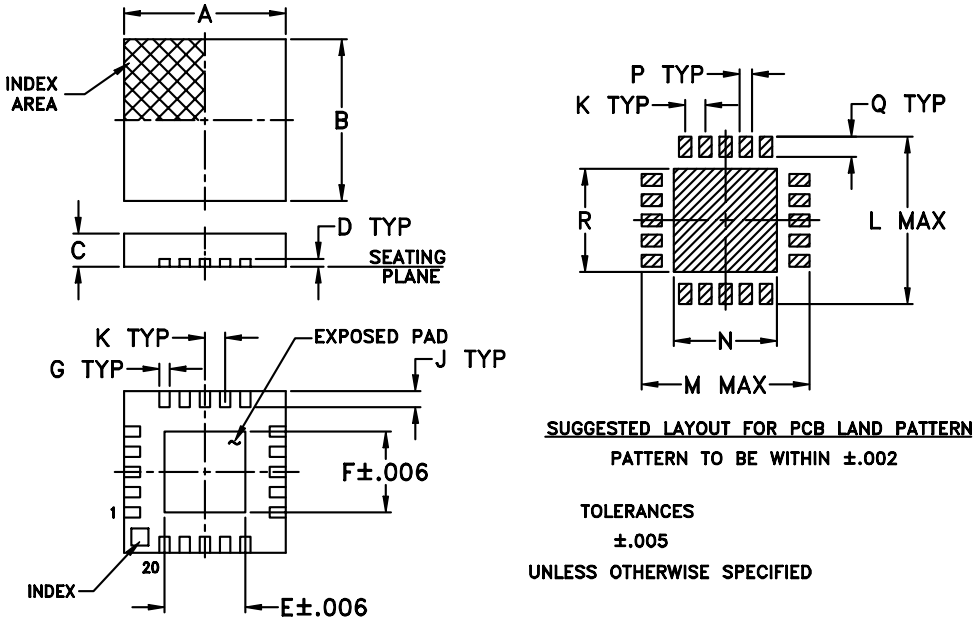




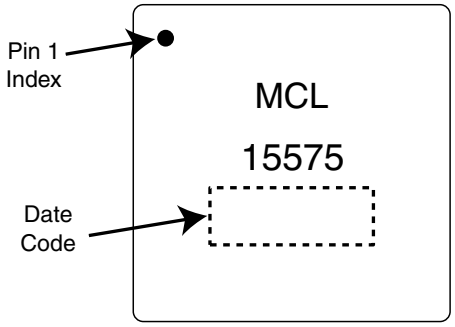




Outline Drawing (DG983-1)



Device Marking

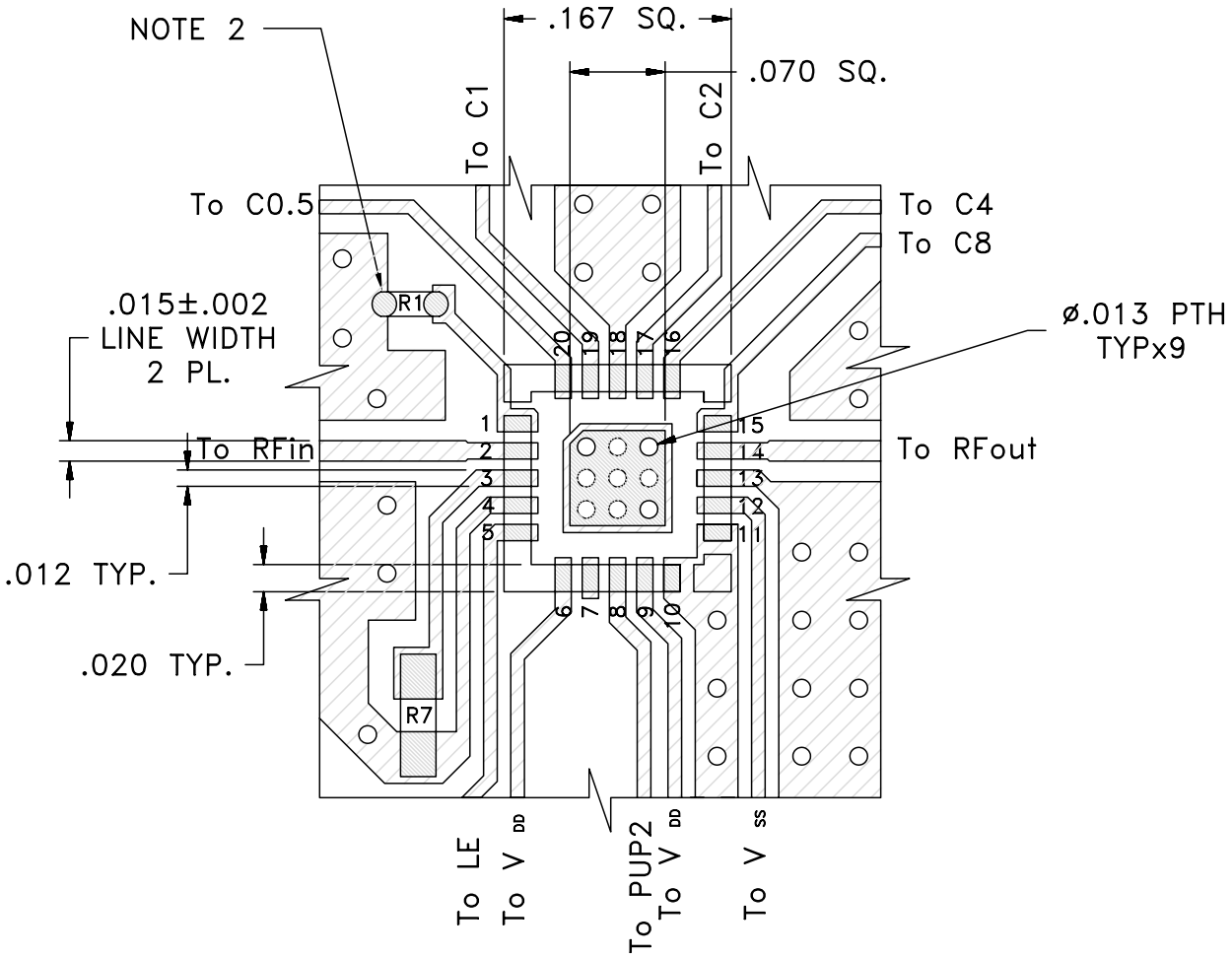


Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	WT. GRAMS
.157	.157	.035	.008	.081	.081	.010	—	.022	.020	.166	.166	.070	.012	.020	.070	.04
4.00	4.00	0.90	0.20	2.06	2.06	0.25	—	0.56	0.50	4.22	4.22	1.78	0.31	0.51	1.78	

Suggested Layout for PCB Design (PL-200)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1, R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



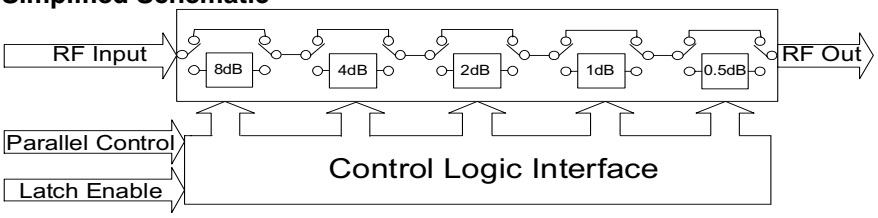
NOTE:

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS. .025"±.002". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603, 0402 SIZES CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SOMBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDERMASK

Simplified Schematic



The DAT-15575-PN parallel interface consists of 5 control bits that select the desired attenuation state, as shown in **Table 1**: Truth Table

Table 1. Truth Table

Attenuation State	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0
0.5 (dB)	0	0	0	0	1
1 (dB)	0	0	0	1	0
2 (dB)	0	0	1	0	0
4 (dB)	0	1	0	0	0
8 (dB)	1	0	0	0	0
15.5 (dB)	1	1	1	1	1

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

The parallel interface timing requirements are defined by Figure 1 (Parallel Interface Timing Diagram) and Table 2 (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenunation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Figure 1: Parallel Interface Timing Diagram

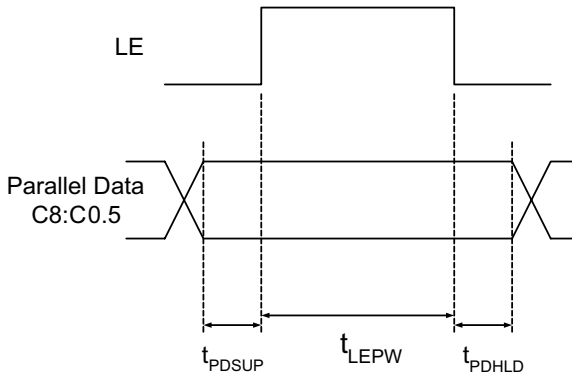


Table 2. Parallel Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{LEPW}	LE minimum pulse width	30		ns
t_{PDSUP}	data set-up time before clock rising edge of LE	10		ns
t_{PDHLD}	data hold time after clock falling edge of LE	10		ns

Pin 1 must always be low to prevent the attenuator from entering an unknown state.

Power-up Control Settings

The DAT-15575-PN always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided.

When the attenuator powers up with LE=0, the control bits are automatically set to one of two possible values. These two values are selected by the power-up control bit, PUP2, as shown in Table 3: (Power-Up Truth Table, Parallel Mode).

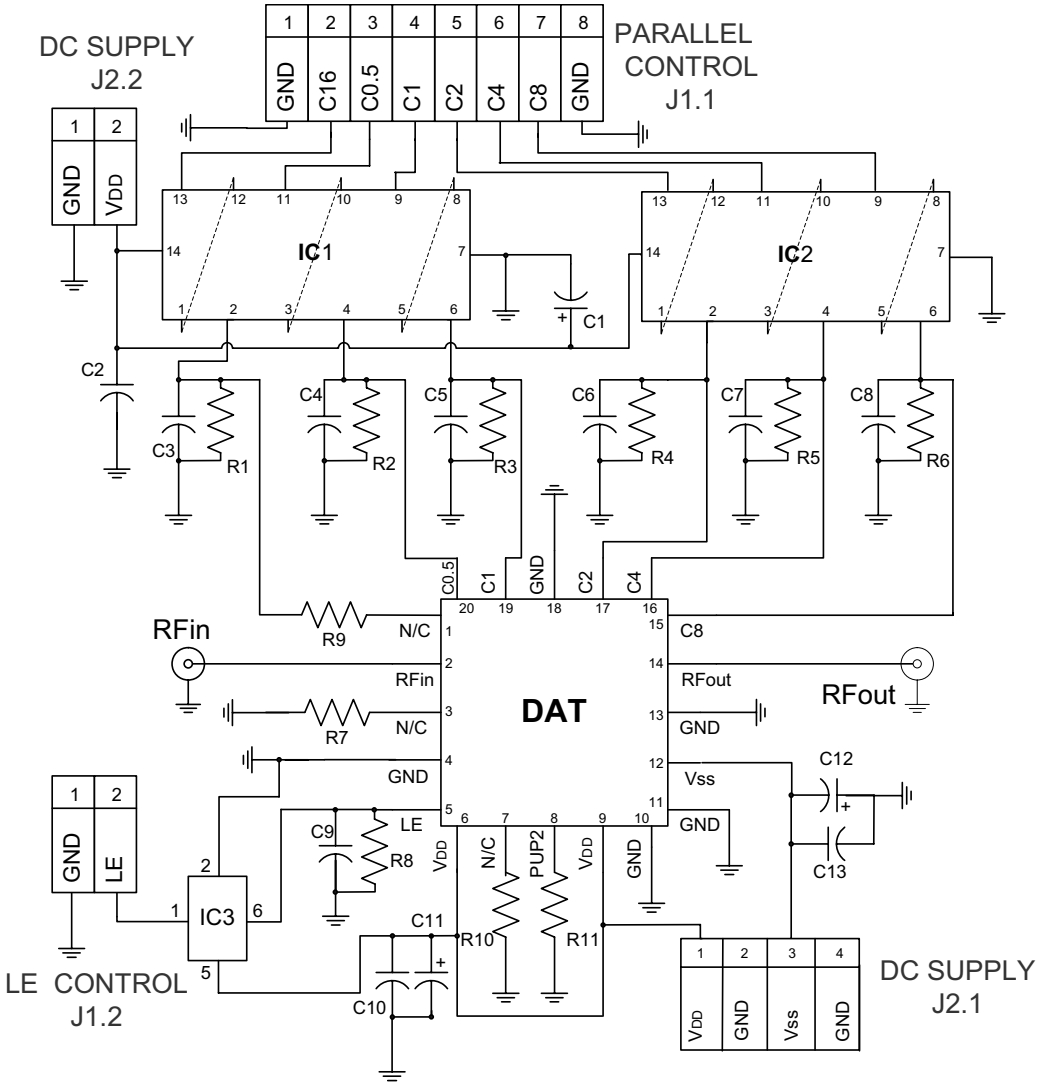
Table 3. Power-Up Truth Table, Parallel Mode

Attenuation State	PUP2	LE
Reference	0	0
8 (dB)	1	0
Defined by C0.5-C8 (See Table 1-Truth Table)	X (Note 1)	1

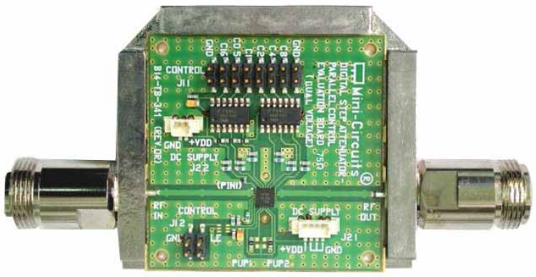
Note 1: PUP2 Connection may be 0, 1, GROUND, or not connect, without effect on attenuation state.

Power-Up with LE=1 provides normal parallel operation with C0.5-C8, and PUP2 is not active.

TB-341 Evaluation Board Schematic Diagram



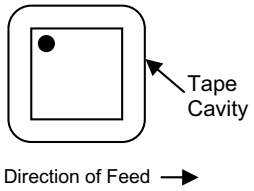
Bill of Materials	
R1 - R8	Resistor 0603 10 KOhm +/- 1%
R10, R11	Resistor 0603 470 Ohm +/- 1%
R9	Resistor 0402 10 KOhm +/- 1%
C2 - C10 & C13	NPO Capacitor 0603 100pF +/- 5%
C1, C11 & C12	Tantalum Capacitor 100 nF +/-10%
IC1, IC2	Hex inverting Schmitt trigger MM74HC14
IC3	Dual non-inverting Schmitt trigger SN74LVC2G17



TB-341

Tape and Reel Packaging Information

Table T&R

TR No.	No. of Devices	Designation Letter	Reel Size	Tape Width	Pitch	Unit Orientation
T-005	1000	K	7 inch	12 mm	8 mm	
	2000	T	13 inch			
	multiples of 10, less than full reel of 1K	PR	7 inch			
	multiples of 10, on tape only	E	not applicable			

Ordering Information

Model No.	Description	Packaging Designation Letter (See Table T&R)	Quantity Min. No. of Units	Price $ Ea.
DAT-15575-PN (+)	Parallel Interface, Dual Voltage (Negative and Positive)	E	10	$3.55
TB-341	Test Board Only	Not Applicable	1	$79.95

How to Order

Example: 1000 pieces of DAT-15575-PN+

1K — Quantity
DAT-15575-PN+ — Model No.
T&R=K — T&R designation letter (see Table T&R)