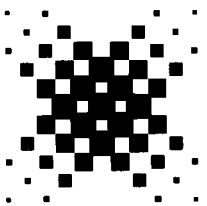
Chapter 1

CP20K Series Field-Programmable Gate Arrays



Introduction to CP20K Series FPGAs

The CP20K Series consists of the industry's first *field-programmable gate arrays* (FPGAs) that are architecturally compatible with standard *mask-programmable gate arrays* (MPGAs). Table 1-1 lists the six different density options included in the product line.

CP20K FPGAs feature transistor-level interconnect programmability resulting in design granularity and a macrocell library equivalent to MPGAs (see Figure 1-1). MPGA design techniques used to improve performance, reduce gate count, etc., are directly applicable to Crosspoint FPGAs. Conversion from an FPGA to MPGA (or vice versa) is therefore very straightforward and predictable.

The CP20K Series consists of six different gate density options, covering the 2,200 to 20,000 gate range. Gate utilization of 60%-85% can be achieved (depending on the nature of the circuit) using the automatic placement and automatic routing capabilities of the Crosspoint Design System (CDS™) (see Figure 1-2). Interactive placement and interactive routing are also provided to allow the designer greater control for fine-tuning critical speed paths and optimizing gate utilization.

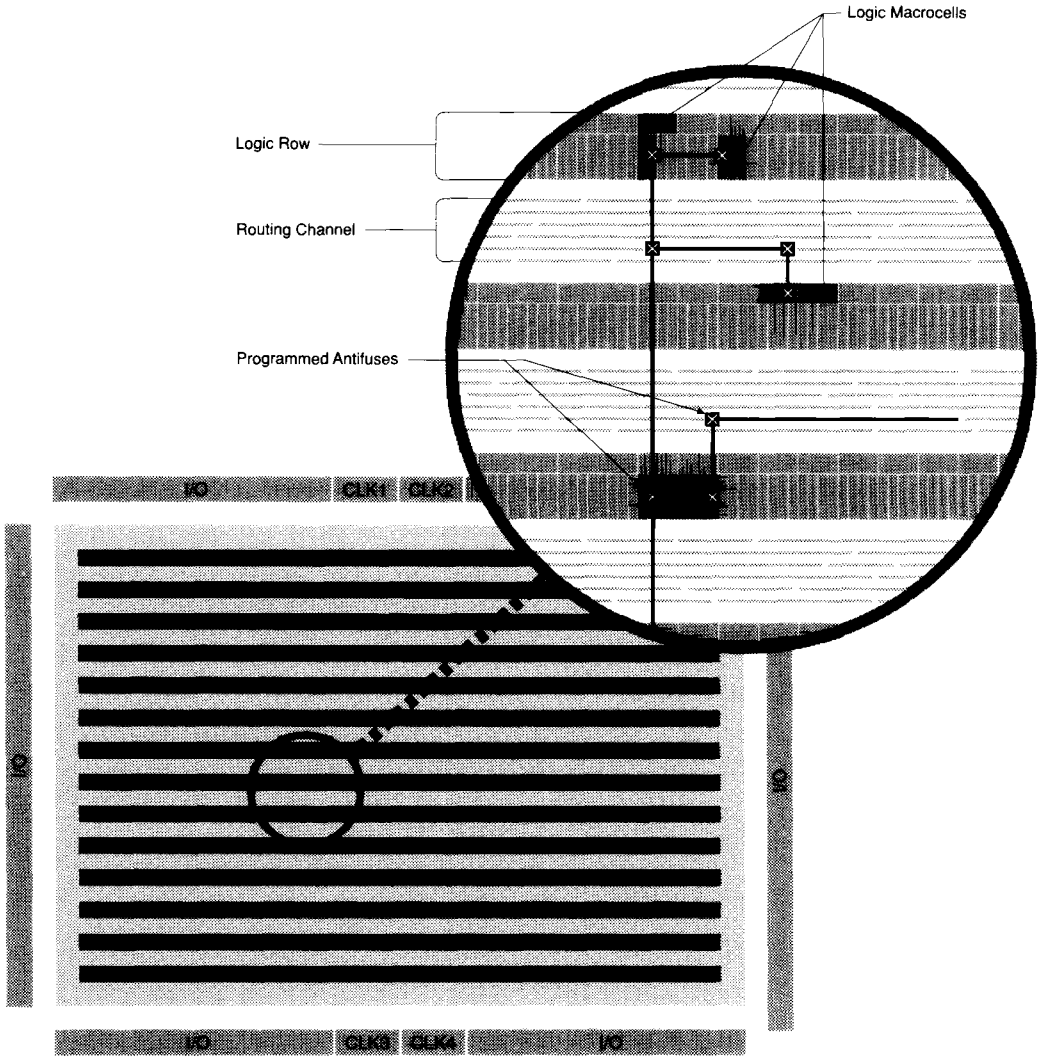
The CP20K Series also features the industry's most flexible I/Os. Each general purpose I/O pad can be configured as an input, output, or bidirectional pad. Additional options are available for each I/O configuration.

Table 1-1 CP20K Product Line*

Part Number	Available Gates	Usable Gates	TPT Count	RLT Count	Maximum I/O Pads	Package Options							
						Chip Carriers	Quad Flat Packs			Pin Grid Arrays			
						84	160	208	240	155	223	299	383
CP20220	2,246	1,300 — 1,900	1,896	474	91	✓							
CP20420	4,245	2,500 — 3,600	3,584	896	130	✓	✓			✓			
CP20840	8,425	5,100 — 7,100	6,740	1,685	180	✓	✓	✓			✓		
CP21200	12,320	7,400 — 10,800	8,960	2,240	203			✓	✓			✓	
CP21600	16,170	9,700 — 13,700	11,760	2,940	250			✓	✓				✓
CP22000	20,262	12,000 — 17,200	14,736	3,684	270			✓	✓				✓

* Contact Crosspoint for availability information on each part and package option.

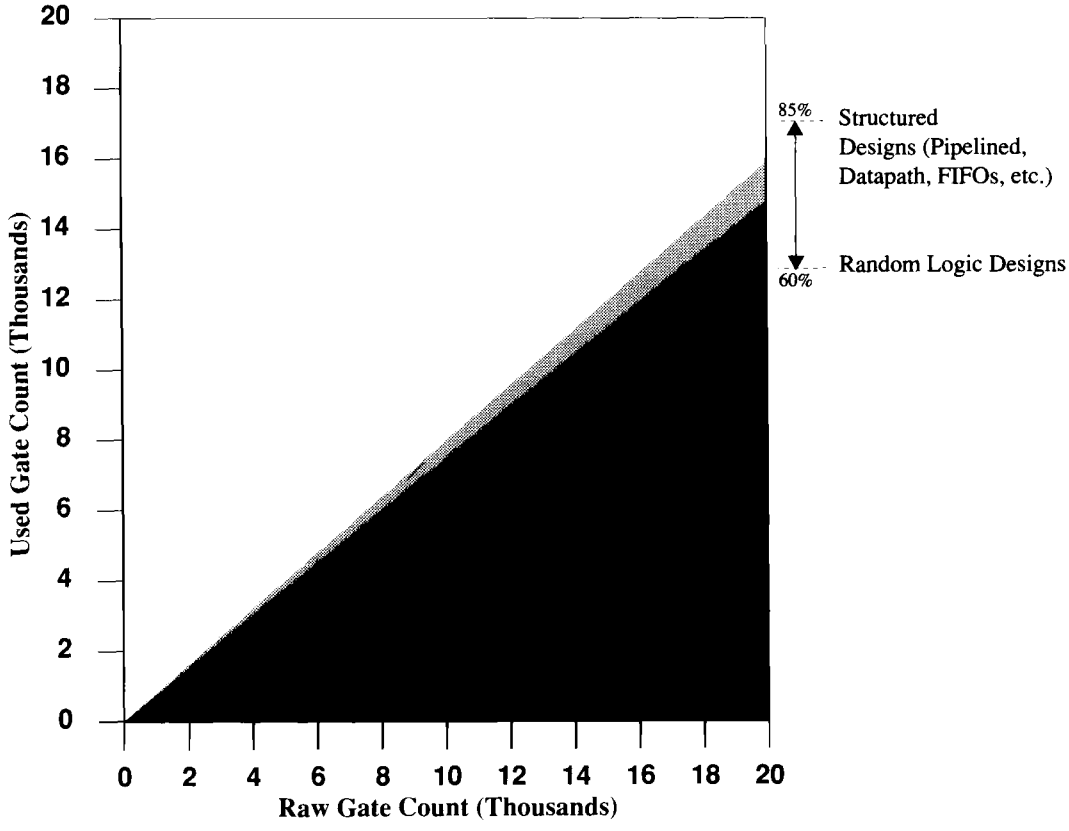
Figure 1-1
CP20K array



Key Features

- True gate array architecture
  - Transistor-level interconnect programmability
  - Gate array macro library
  - Gate array design methodology
- 50% - 100% faster than other *programmable logic devices* (PLDs)/FPGAs
- Field programmability based on a unique and proprietary low-impedance antifuse technology
- Six density options: 2.2K to 20K available gates
- Four independent clock grids to minimize internal clock skew to less than 1.0 ns
- Flexible I/O configuration
  - Input: CMOS or TTL thresholds with or without pull-up; 7 pins also feature Schmitt thresholds
  - Output: 4mA, 8mA or 12mA drive; three-state; programmable slew rate; open-drain and open-source options
  - Bidirectional: Any combination of the above input and output configurations
- High I/O count
- Flexible memory block implementation
- Built-in IEEE 1149.1 (JTAG) interface
- Design entry, simulation, timing analysis, fault simulation, and test pattern generation done with familiar industry-standard EDA tools
- Gate-level-granularity architecture takes maximum advantage of HDL/Synthesis top-down design methodology
- Automatic and interactive place and route capability for maximum flexibility to fine-tune performance and increase gate utilization.

Figure 1-2
CP20K usable gate capacity



The CP20K Series is manufactured using a high-performance, high-density 0.8 µm CMOS process with two-layer metallization. This process, coupled with Crosspoint's gate array architecture and interconnect scheme, yields performance and design flexibility far superior to other programmable logic alternatives.

Central to Crosspoint's process architecture is a proprietary antifuse technology. An antifuse is a programmable element that has a very high impedance (>100MΩ) initially, but exhibits a low resistance (<100Ω) after programming. Crosspoint's unique antifuse fabrication technique provides antifuse elements with very low capacitance when unprogrammed and very low resistance when programmed. This translates

directly to higher speed, since interconnect RC delays are reduced. The programming is permanent (that is, non-volatile) resulting in a one-time programmable (OTP) device.

Developing FPGAs with gate densities in the 20,000 gate range and system speeds of 40-50 MHz and higher requires an advanced development environment. Crosspoint addresses this need by allowing designers to use the familiar EDA tools for ASIC design and coupling them tightly to the CP20K specific tools for placement and routing.

Designers use existing third-party EDA tools for schematic entry, synthesis, simulation, timing analysis, fault analysis, and test vector generation. The Crosspoint Design System (CDS) is then used to place and route the designs. A choice of automatic or interactive place and route features give the designer maximum flexibility to fine-tune performance. Post-layout simulation uses RC-tree back annotation and provides for certified accuracy on third party tools.

When the design is complete, an antifuse map is generated and downloaded to a Crosspoint FPGA Programmer. The Programmer is connected directly to the user's workstation through a SCSI interface. The Programmer programs the FPGA, and also may perform functional testing if desired. Numerous densities and package options are supported via individual socket adapters.

The JTAG boundary scan is a built-in feature of all CP20K parts. This feature is also used by Crosspoint for the programming and functional testing of each FPGA. The JTAG boundary scan implementation is fully IEEE 1149 compliant and enables board level testing.