Features

- 64K x 18 Synchronous Burst Mode SRAM
- 0.5µ CMOS Technology
- Compatible with Pentium™ and i486™ processors
- Supports Pentium™ Address Pipelining
- LVTTL I/O Compatible with common I/O
- Single +3.3 V ± 5% Power Supply and Ground
- Registered Addresses, Data Ins and Control Signals
- 5 V Tolerant I/O
- Asynchronous Output Enable
- Self-Timed Write Operation and Byte Write Capability
- Low Power Dissipation
  - 1.1 W Active at 83MHz
  - 90 mW Standby
- 100 Pin Thin Quad Flat Pack

Description

IBM Microelectronics 1M SRAM is a Synchronous Burstable, high performance CMOS Static RAM that is versatile, wide I/O, and achieves 8 nanosecond access. A single clock is used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the Clock, all Addresses, Data Ins and Control Signals are registered internally. Burst mode operation, is accomplished by integrating input registers, internal 2-bit burst counter and high speed SRAM in a single chip. Burst reads are initiated with either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ being LOW with a valid address during the rising edge of clock. Data from this address plus the three subsequent addresses will be output. The chip is operated with a single +3.3 V power supply and is compatible with LVTTL I/O interfaces.

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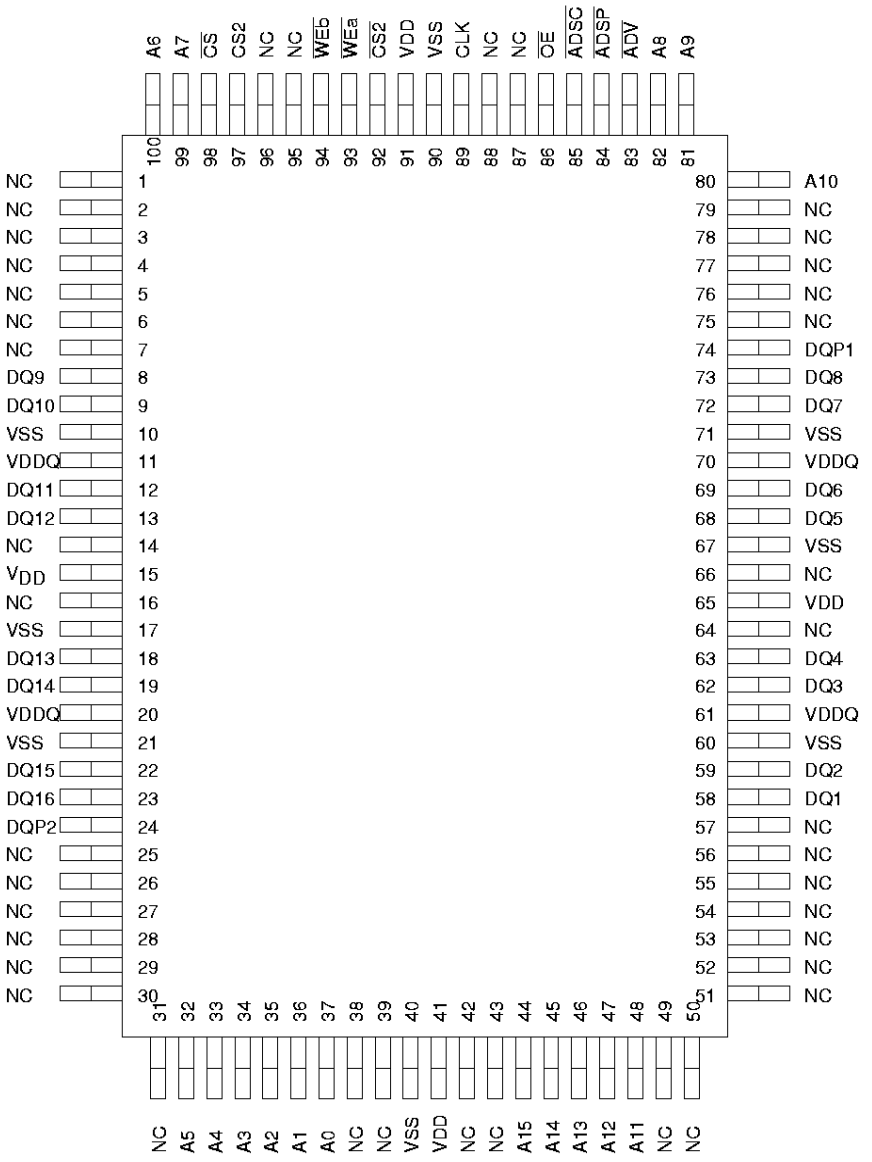
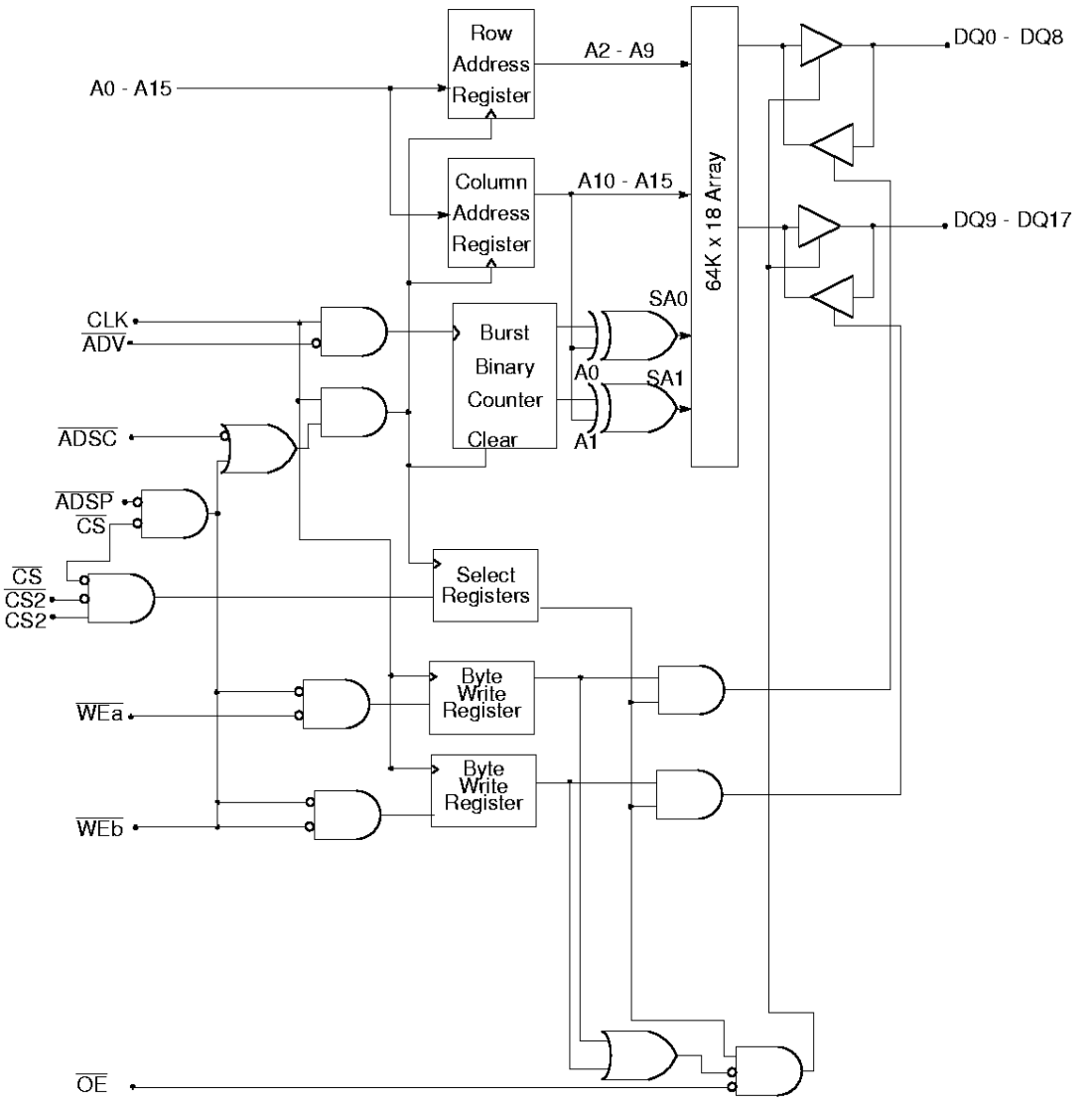
X18 TQFP Pin Array Layout



Pin Description

A0-A15	Address input	$\overline{ADSP}$	Address Status Processor
DQa - DQb	Data Input/Output (1-8 , 9-16)	$\overline{ADSC}$	Address status controller
CLK	Clock	$\overline{ADV}$	Burst Advance Control
$\overline{WEa}$	Write Enable, Byte a (1 to 8 & DQP1)	$\overline{CS}$	$\overline{ADSP}$ - Gated Chip Select
$\overline{WEb}$	Write Enable, Byte b (9 to 16 & DQP2)	V_{DD}	Power Supply (+3.3V)
$\overline{OE}$	Output Enable	V_{SS}	Ground
$\overline{CS2}$, CS2	Chip Selects	V_{DDQ}	Output Power Supply (+3.3V)
DQP1,DQP2	Parity bits for byte a, and byte b.	NC	No Connect

Block Diagram



Ordering Information

Part Number	Organization	Speed	Leads	Notes
IBM041812PQK-8	64K x 18	8 ns Access / 12 ns Cycle	100 pin TQFP	
IBM041812PQK-9	64K x 18	9 ns Access / 12 ns Cycle	100 pin TQFP	
IBM041812PQK-10	64K x 18	10 ns Access / 12 ns Cycle	100 pin TQFP	
IBM041812PQK-11	64K x 18	11 ns Access / 12 ns Cycle	100 pin TQFP	

Burst SRAM Clock Truth Table

CLK	$\overline{CS2}$	CS2	$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	DQ	Operation
L→H	H	X	L	L	X	X	X	X	High-Z	Deselected Cycle
L→H	X	L	L	L	X	X	X	X	High-Z	Deselected Cycle
L→H	H	X	X	X	L	X	X	X	High-Z	Deselected Cycle
L→H	X	L	X	X	L	X	X	X	High-Z	Deselected Cycle
L→H	L	H	L	L	X	X	X	L	Q	Read from External Address, Begin Burst
L→H	L	H	L	L	X	X	X	H	High-Z	Read from External Address, Begin Burst
L→H	L	H	L	H	L	X	H	L	Q	Read from External Address, Begin Burst
L→H	L	H	L	H	L	X	L	X	D	Write to External Address, Begin Burst
L→H	X	X	X	H	H	L	H	L	Q	Read from next Add., Continue Burst
L→H	X	X	X	H	H	L	L	X	D	Write to next Add., Continue Burst
L→H	X	X	X	H	H	H	H	L	Q	Read from Current Add., Suspend Burst
L→H	X	X	X	H	H	H	L	X	D	Write to Current Add., Suspend Burst
L→H	X	X	H	X	L	X	X	X	High-Z	Deselect Cycle
L→H	X	X	H	X	H	L	H	L	Q	Read from next Add., Continue Burst
L→H	X	X	H	X	H	L	L	X	D	Write to next Add., Continue Burst
L→H	X	X	H	X	H	H	H	L	Q	Read from current Add., Suspend Burst
L→H	X	X	H	X	H	H	L	X	D	Write to current Add., Suspend Burst

1. For a write operation preceded by a read cycle, $\overline{OE}$ must be HIGH early enough to allow Input Data Setup, and must be kept HIGH through Input Data Hold Time.
2. $\overline{WE}$ refers to $\overline{WEa}$, $\overline{WEb}$.
3. $\overline{ADSP}$ is gated by $\overline{CS}$, and $\overline{CS}$ is used to block $\overline{ADSP}$ when $\overline{CS} = V_{IH}$, as required in applications using Processor Address Pipelining.
4. All Addresses, Data In and Control signals are registered on the rising edge of CLK.

Burst Sequence Truth Table

External Address	A15-A2	(A1,A0)				Notes
		(0,0)	(0,1)	(1,0)	(1,1)	
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)	
2nd Access	A15-A2	(0,1)	(0,0)	(1,1)	(1,0)	
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)	
4th Access	A15-A2	(1,1)	(1,0)	(0,1)	(0,0)	

Write Enable Truth Table

$\overline{WEa}$	$\overline{WEb}$	Byte Written	Notes
H	H	Read All Bytes	
L	L	Write All Bytes	
L	H	Write Byte A (D_{IN} 0 - 8)	
H	L	Write Byte B (D_{IN} 9 - 17)	

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage	V_{DD}	-0.5 to 4.6	V	1
Input Voltage	V_{IN}	-0.5 to 6.0	V	1
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5	V	1
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Power Dissipation	P_D	2.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.465	V	1, 4
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2, 4
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3, 4
Output Current	I_{OUT}	—	5	8	mA	4

1. All voltages referenced to V_{SS}. All V_{DD} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)
4. Input Voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 nanosecond set-up and hold times.

Capacitance (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, f=1MHz)

Parameter	Symbol	Test Condition	Max	Units	Notes
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF	
Data I/O Capacitance (DQ0-DQ17)	C_{OUT}	V_{OUT} = 0V	5	pF	

DC Electrical Characteristics (T_A= 0 to +70°C, V_{DD}=3.3V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{DD12}	—	300	mA	2, 3
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH} or CS2 = V_{IL} or $\overline{CS}$ = V_{IL} All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0 Clock @ 83MHz)	I_{SB}	—	25	mA	1, 3
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}	—	+1	µA	4
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}	—	+1	µA	
Output High Level Output "H" Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4	—	V	
Output Low Level Output "L" Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}	—	0.4	V	

1. I_{SB} = Stand-by Current
2. I_{DD} = Selected Current
3. I_{OUT} = Chip Output Current
4. The input leakage current for 5.5V input is 200 µA for Clk, Chip Selects, and Output Enable. Other inputs have 100 µA of leakage current at 5.5V.

AC Test Conditions (T_A=0 to +70°C, V_{DD}=3.3V ± 5%)

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	V_{IH}	3.0	V	
Input Pulse Low Level	V_{IL}	0.0	V	
Input Rise Time	T_R	2.0	ns	
Input Fall Time	T_F	2.0	ns	
Input and Output Timing Reference Level		1.5	V	
Output Load Conditions				1

1. See AC Test Loading figure on page 8.

AC Characteristics (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, Units in nsec)

Parameter	Symbol	-8		-9		-10		-11		Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	12.0	—	12.0	—	12.0	—	12.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	8.0	—	9.0	—	10.0	—	11.0	3
Address Status Controller Setup Time	t_{ADSCS}	2.5	—	2.5	—	2.5	—	2.5	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	0.5	—	0.5	—	
Address Status Processor Setup Time	t_{ADSPS}	2.5	—	2.5	—	2.5	—	2.5	—	
Address Status Processor Hold Time	t_{ADSPH}	0.5	—	0.5	—	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.5	—	2.5	—	2.5	—	2.5	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.5	—	2.5	—	2.5	—	2.5	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.5	—	2.5	—	2.5	—	2.5	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.5	—	2.5	—	2.5	—	2.5	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.5	—	2.5	—	2.5	—	2.5	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	3.0	—	3.0	—	3
Clock High to Output High Z	t_{CHZ}	—	5.0	—	5.0	—	5.5	—	5.5	1, 2, 4
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	2.5	—	2.5	—	1, 2, 4
Output Enable to High Z	t_{OHZ}	2.0	5.0	2.0	5.5	2.0	6.0	2.0	6.5	1, 4
Output Enable to Low Z	t_{OLZ}	0.25	—	0.25	—	0.25	—	0.25	—	1, 4
Output Enable to Output Valid	t_{OQ}	—	4.0	—	5.0	—	5.0	—	6.0	3

1. Transitions are measured ± 200 mV from steady state voltage.
2. At any given voltage and temperature, T_{CHZ} (max) is always less than T_{CLZ} (min) for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from High-Z to new RAM data.
3. See AC Test Loading figure 1 on page 8.
4. See AC Test Loading figure 2 on page 8.

AC Test Loading

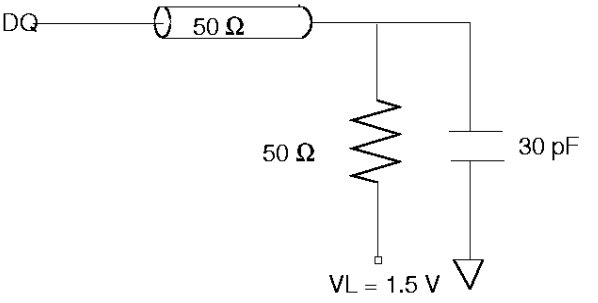


Fig. 1 Test Equivalent Load

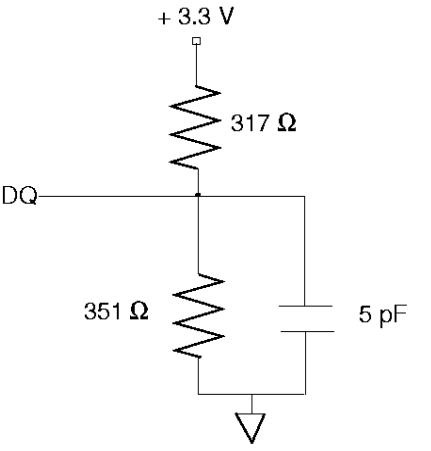
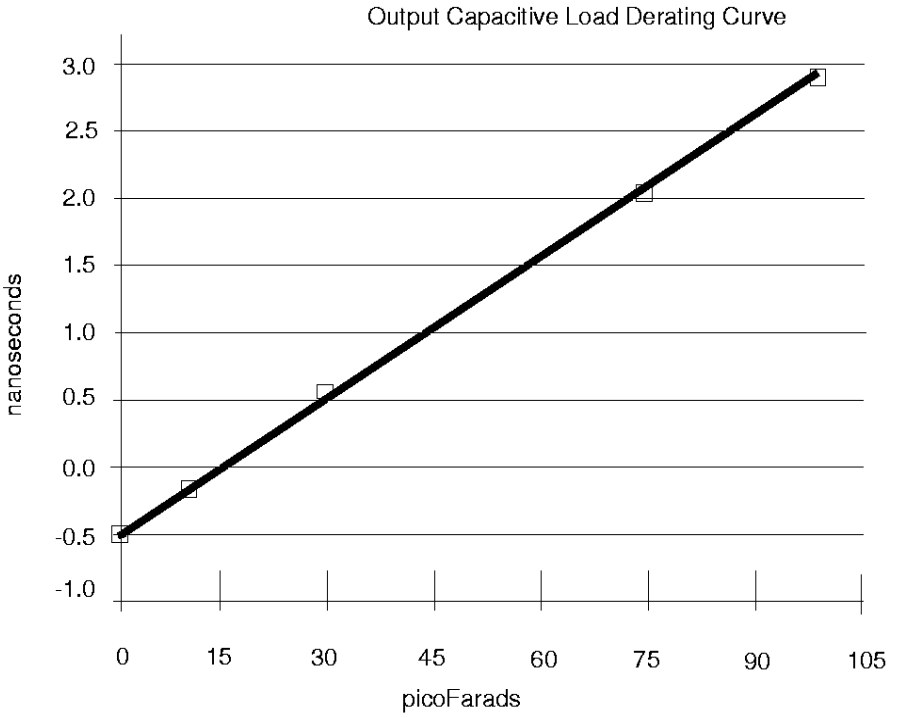
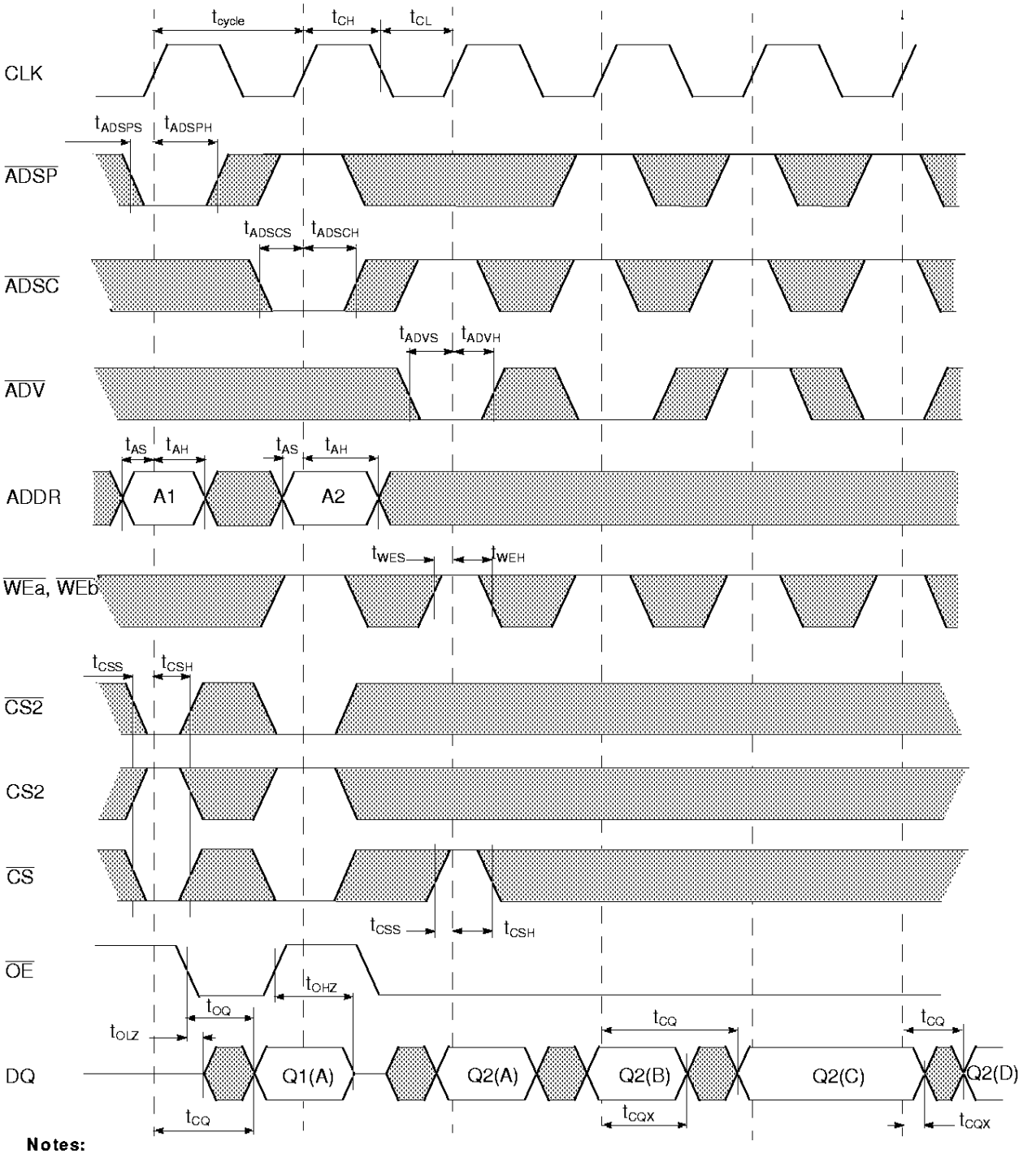


Fig. 2 Test Equivalent Load



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 8ns access time will behave as though it has an 8.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access times guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters Vcc = 3.14 V, Ta = 70° C.

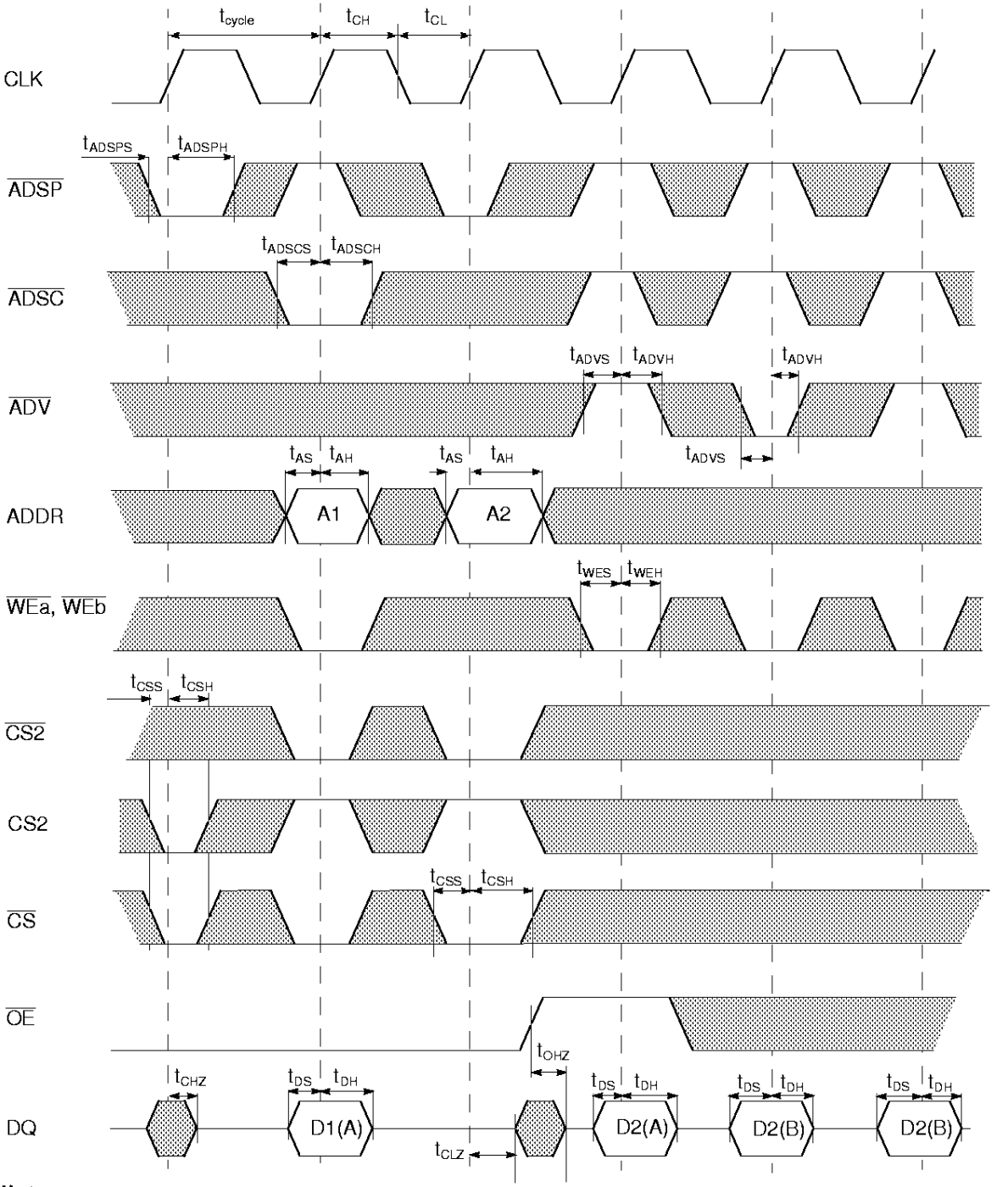
Timing Diagram (Burst Read)



Notes:

1. Q1(A) and Q2(A) refer to data written to address A1 and A2.
2. Q2(B), Q2(C) and Q2(D) refer to data written to subsequent internal burst counter addresses.

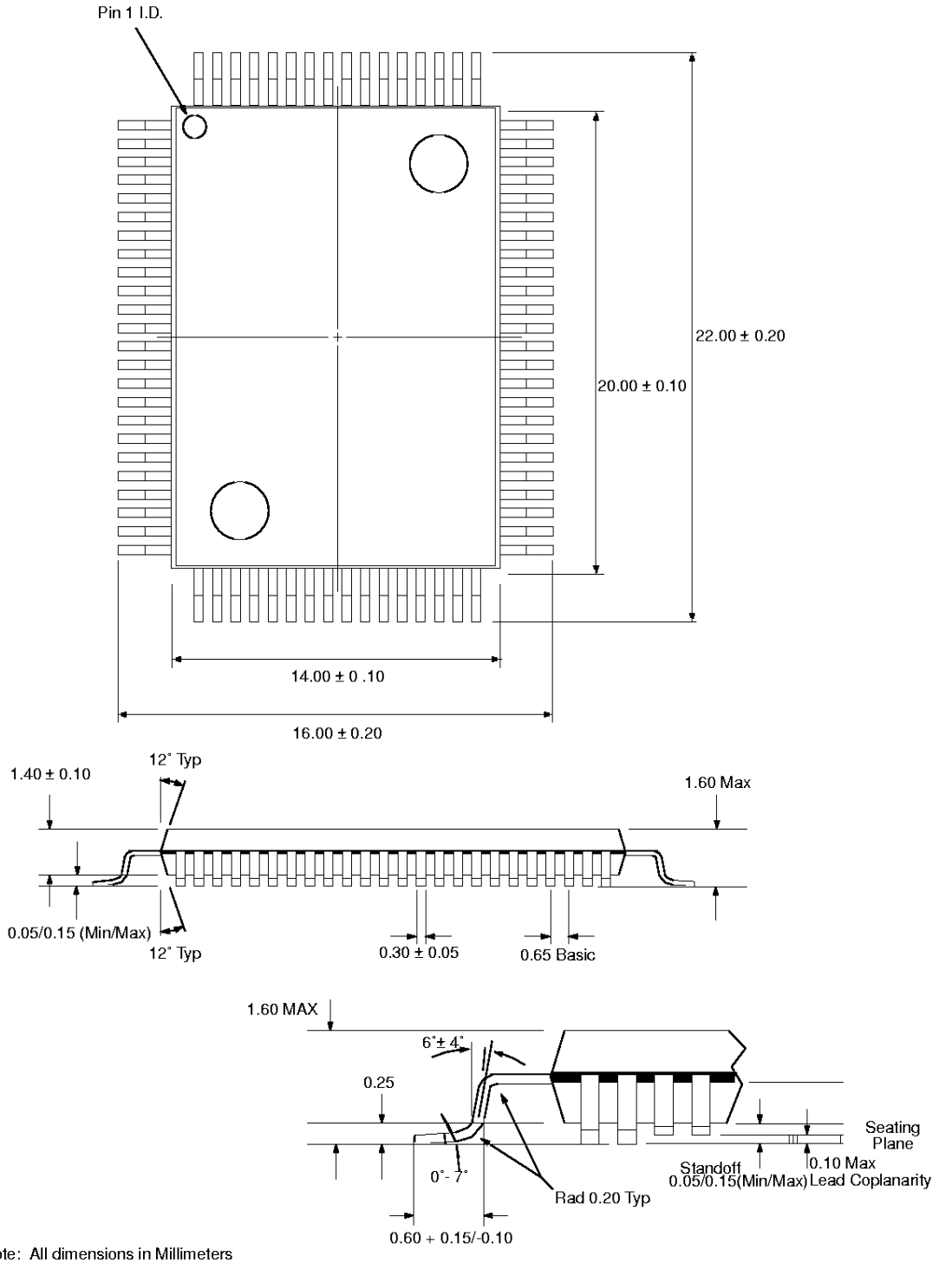
Timing Diagram (Burst Write)



Notes:

1. D1(A) and D2(A) refer to data written to address A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3. $\overline{WEa}$, $\overline{WEb}$ are don't cares when ADSP is sampled LOW.

100 Pin TQFP Package Diagram



Note: All dimensions in Millimeters

Connect Compatibility for 64K x18 and Future 64K x 16 & 64K x 18

TQFP PIN #	Current Connections (x18)	Future Connections (x16 & x18)	Function
4,27,54,77	NC	V_{DDQ}	Output Power Supply
5,26,55,76	NC	V_{SS}	Ground
14	NC	Low or High, NC for most vendors but Low or High to comply to the JEDEC standard.	$\overline{FT}$, Flow thru or Pipeline function, tie Low for flow thru, High for Pipeline
24	DQP2	NC or DQ in x18	Parity bit for second byte
31	NC	Low or High	$\overline{LBO}$, Linear Burst Order, This pin must be tied low for linear(PowerPC), High for Interleave (Pentium)
64	NC	Low or High. Low allows normal operation.	$\overline{ZZ}$, Asynchronous Sleep Mode, Tie to ground for normal function, V_{DDQ} for sleep mode (Low power state)
74	DQP1	NC or DQ in x18	Parity bit for first byte
87	NC	Low or $\overline{BWE}$, Tie low if function not used	Byte Write Enable, Allows individual bytes to be written.
88	NC	Low or $\overline{GW}$, Tie High if function not used	Global Write Enable, Allows write of all bytes to occur with single pin.

The IBM041812PQK has the pins connected in the manner indicated in the Current Connections (x18) and is also JEDEC complaint. Future Connections refers to the evolution on the JEDEC standard for subsequent part numbers.

Revision Log

Rev	Contents of Modification
7/95	Initial Release of the 64K x 18 (8/9/10/11) TQFP BURST MODE Application Spec.

For more information contact your IBM Microelectronics sales representative or
visit us on World Wide Web at http://www.chips.ibm.com