8K x 8 Bit Static RAM

FEATURES

- **Fast Access Time : 70, 100, 120ns (Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 10μW (typ) L.Version
  : 5μW (typ) LL.Version
  Operating:55mW/1MHz
- **Single 5V±10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - No clock or refresh required
- **Three state Output**
- **Low Data Retention Voltage : 2V (Min.)**
- **JEDEC Standard pin coniguration**
  KM6264BLP/BLP-L : 28-DIP-600B
  KM6264BLS/BLS-L : 28-DIP-300
  KM6264BLG/BLG-L : 28- SOP-450

GENERAL DESCRIPTION

The KM6264BL/BL-L is 65,536-bit high-speed Static Random Access Memory organized as 8, 192 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM6264 BL/BL-L has an output enable input for precise control of the data outputs.
It also has chip select inputs for the minimum current power down mode.
The KM6264 BL/BL-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up non-volatile memory applications

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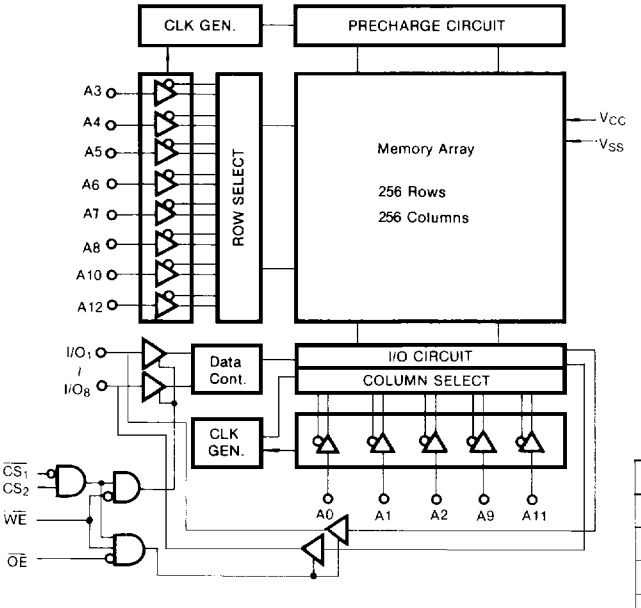
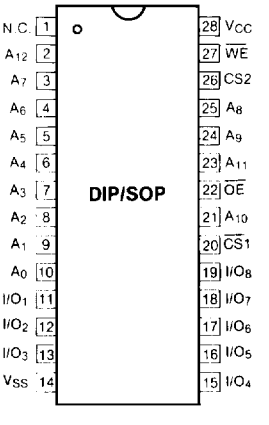
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Pin Name	Pin Function
A_0-A_{12}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{OE}$	Output Enable Input
I/O_1-I/O_8	Data Inputs/Outputs
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C
Soldering Temperature and Time	T_{solder}	260° C, 10 sec(Lead only)	—

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min)=-3.0V for $\leq$ 50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Typ*	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS1}$=V_{IN} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}		-2	—	2	μA
Operation Power Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, $\overline{CS2}$=V_{IH} V_{IN}=V_{IH} or V_{IL} $I_{I/O}$=0mA		—	—	15	mA
Average Operating Current	I_{CC1}	Cycle Time=1μS, 100% Duty $\overline{CS1}\leq$0.2V, $\overline{CS2}\geq V_{CC}$-0.2V $V_{IL}\leq$0.2V $V_{IH}\geq V_{CC}$-0.2V, $I_{I/O}$=0mA		—	—	10	mA
	I_{CC2}	Min Cycle. 100% Duty $\overline{CS1}$=V_{IL},	70ns	—	—	55	mA
		$\overline{CS2}$=V_{IH}, V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA	100/120ns	—	—	45	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$=V_{IH} or $\overline{CS2}$=V_{IL}		—	0.2	2	mA
	I_{SB1}	$\overline{CS1}\geq V_{CC}$-0.2V, $\overline{CS2}\leq$0.2V or $\overline{CS2}\geq V_{CC}$-0.2V,	L	—	2	100	μA
		$V_{IN}\geq V_{CC}$-0.2 or $V_{IN}\leq$0.2V	LL	—	1	10	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4	—	—	V

*Typ: V_{CC}=5V, T_A=25° C

CAPACITANCE ($f = 1MHz$, $T_A = 25°C$)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF

* Note: Capacitance is sampled and not 100% tested.

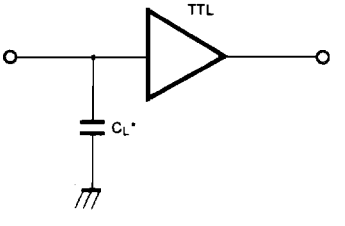
AC CHARACTERISTICS

TEST CONDITIONS ($Ta = 0$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$^*C_L = 100$ pF + 1 TTL

*C_L=30pF for KM6264BL-7/7L

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM6264BL-7 KM6264BL-7L		KM6264BL-10 KM6264BL-10L		KM6264BL-12 KM6264BL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		100		120		ns
Address Access Time	t_{AA}		70		100		120	ns
Chip Select to Output	t_{CO1}, t_{CO2}		70		100		120	ns
Output Enable to Valid Output	t_{OE}		35		50		60	ns
Chip Enable to Low-Z Output	t_{LZ1}, t_{LZ2}	5		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ1}, t_{HZ2}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t_{OHZ}	0	30	0	35	0	40	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

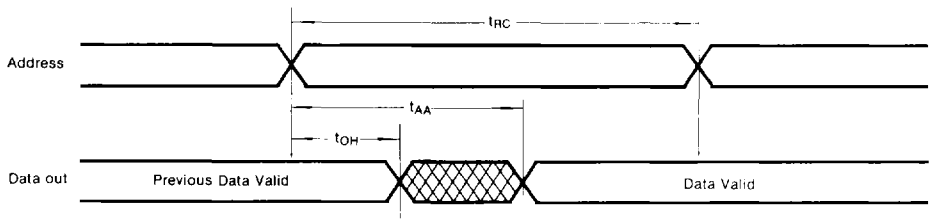
WRITE CYCLE

Parameter	Symbol	KM6264BL-7 KM6264BL-7L		KM6264BL-10 KM6264BL-10L		KM6264BL-12 KM6264BL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		120		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Write Pulse Width	t_{WP}	40		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		10		ns

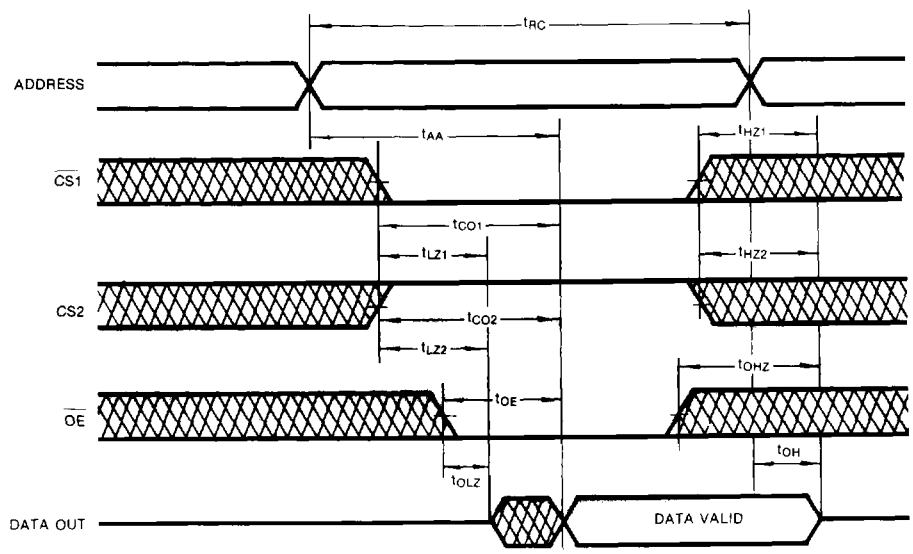
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO. 1

($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$)



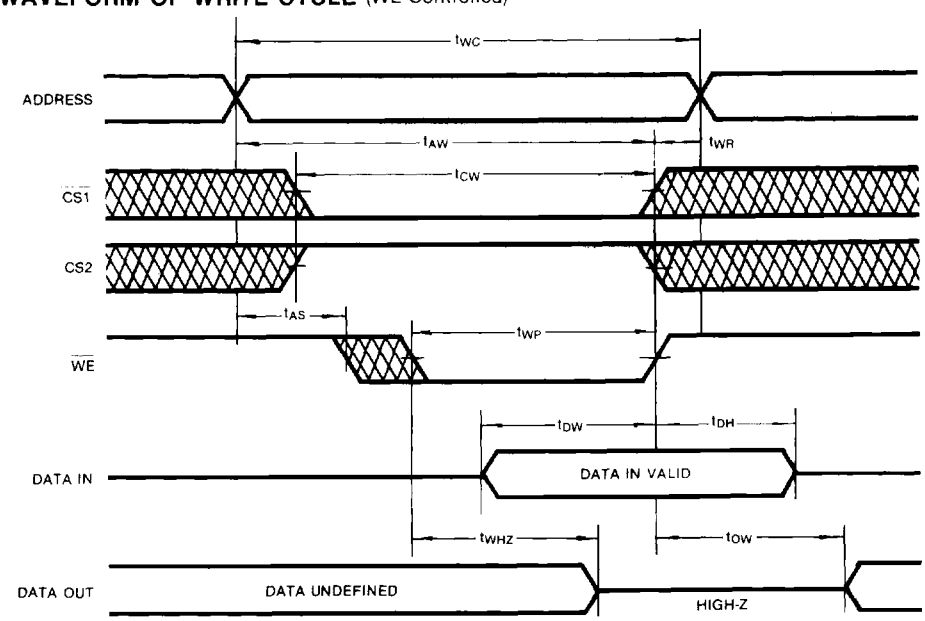
TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{WE}$ = V_{IH})



Note (READ CYCLE)

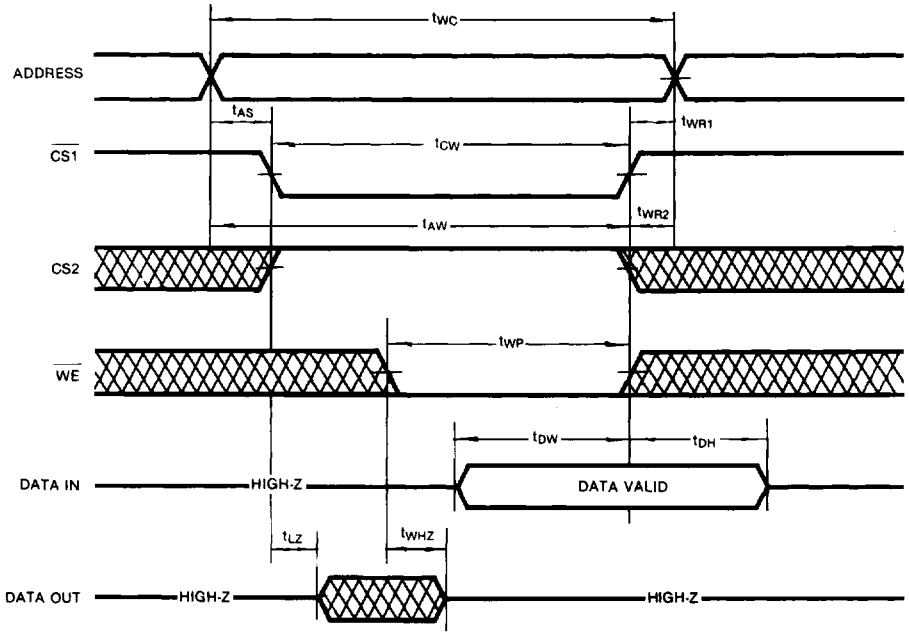
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ}(min) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)

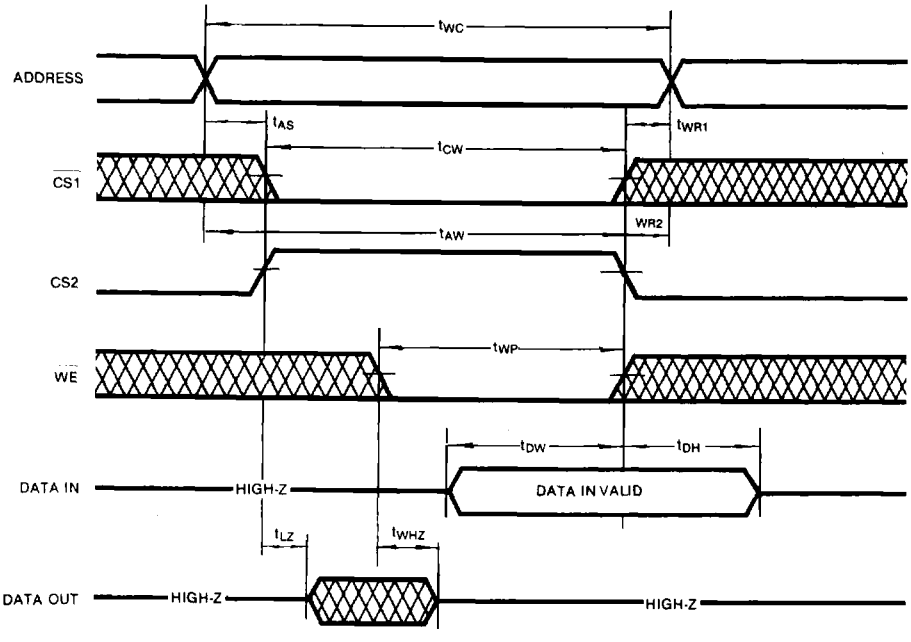


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or $\overline{WE}$ going high, t_{WR2} applied in case a write ends at CS2 going low.
5. If $\overline{OE}$, CS2 and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and CS2 is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

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FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
X*	L	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

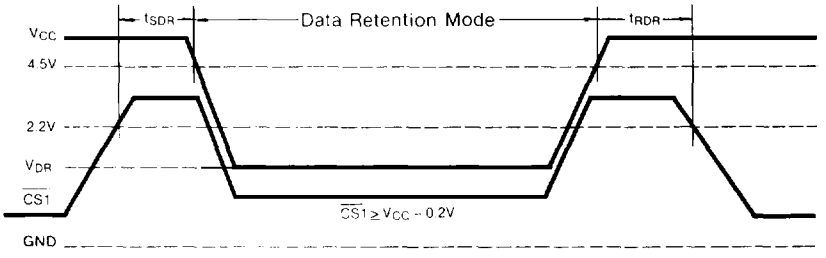
* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC} - 0.2V$*		2.0		5.5	V
Data Retention Current	I_{DR}	V_{CC} = 3V $\overline{CS1} \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	L		1	50	μA
			LL		0.5	5**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)		0			ns
Recovery Time	t_{RDR}			t_{RC}***			ns

* $\overline{CS1} \geq V_{CC}$-0.2V, CS2 $\geq V_{CC}$-0.2V ($\overline{CS1}$ Controlled) or CS2 $\leq$ 0.2V (CS2 Controlled)
** 1μA (max.) at 0°C~40°C
*** t_{RC} = Read cycle time

DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)