*MEMORY Mobile FCRAM*TM

CMOS

32M Bit (2 M word × 16 bit)
Mobile Phone Application Specific Memory

MB82DPS02183B-85/-85L

CMOS 2,097,152-WORD x 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

The Fujitsu MB82DPS02183B is a CMOS Fast Cycle Random Access Memory (FCRAM*) with asynchronous Static Random Access Memory (SRAM) interface containing 33,554,432 storages accessible in a 16-bit format. This MB82DPS02183B is suited for mobile applications such as Cellular Handset and PDA.
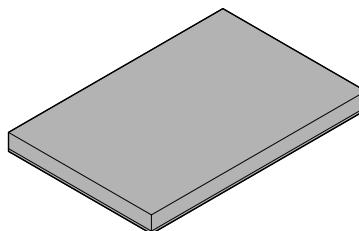
*: FCRAM is a trademark of Fujitsu Limited, Japan

■ FEATURES

- Asynchronous SRAM Interface
- Fast Access Cycle Time : t_{CE} = 85 ns Max
- 8 words Page Access Capability : t_{PAA} = 25 ns Max
- Low Voltage Operating Condition : V_{DD} = + 1.65 V to + 1.95 V
- Wide Operating Temperature : T_A = −30 °C to + 85 °C
- Byte Control by $\overline{LB}$ and $\overline{UB}$
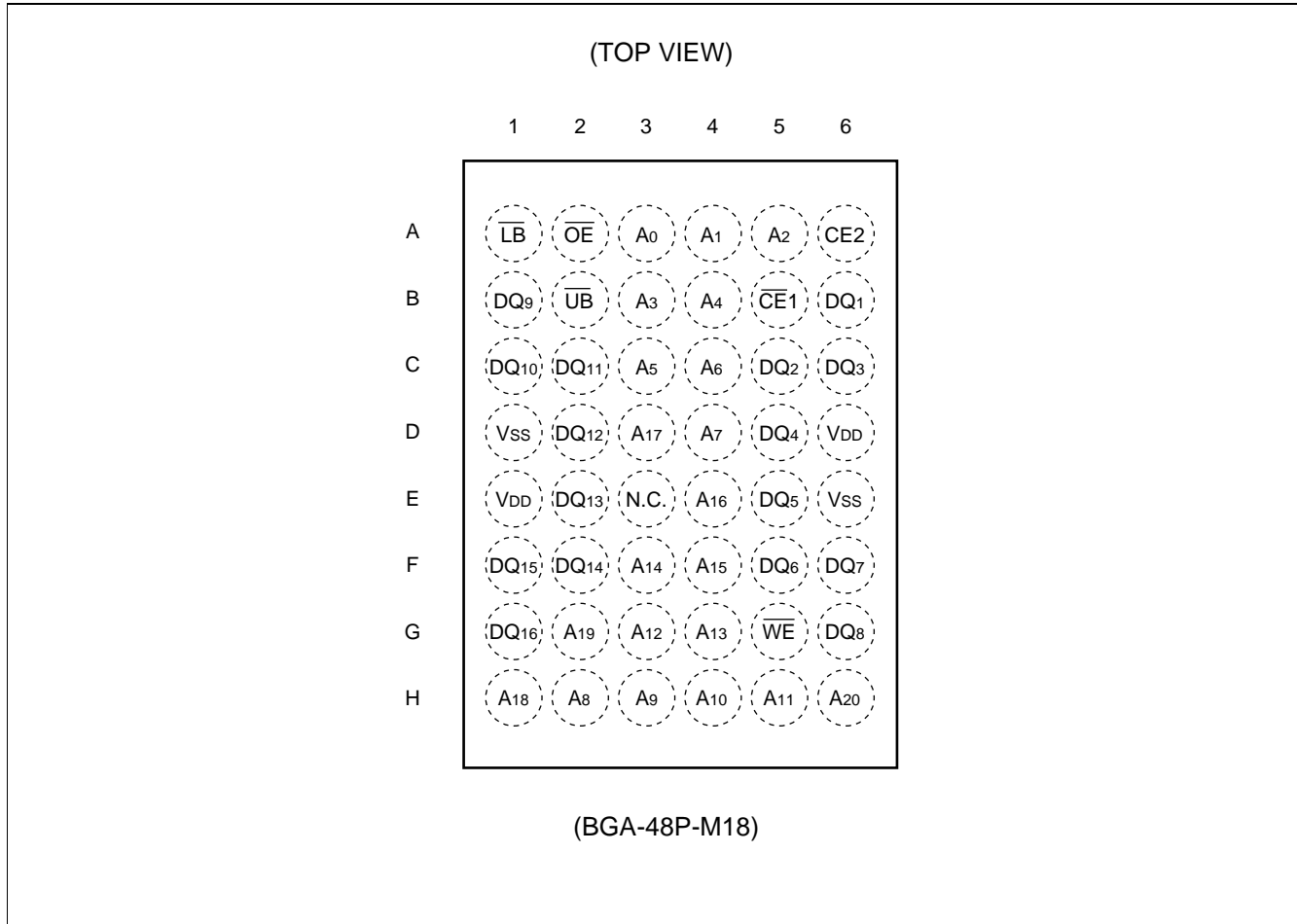
(Continued)

■ PACKAGE

48-ball Plastic FBGA

(BGA-48P-M18)

FUJITSU

(Continued)

- Low Power Consumption : I_{DDA1} = 25 mA Max

  I_{DDS1} = 200 μA Max

  100 μA Max (L version)

- Various Partial Power Down mode : Sleep

  4 M-bit Partial

  8 M-bit Partial

  16 M-bit Partial

■ **PIN ASSIGNMENT**

(TOP VIEW)

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2
B	DQ_9	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	DQ_1
C	DQ_{10}	DQ_{11}	A_5	A_6	DQ_2	DQ_3
D	V_{SS}	DQ_{12}	A_{17}	A_7	DQ_4	V_{DD}
E	V_{DD}	DQ_{13}	N.C.	A_{16}	DQ_5	V_{SS}
F	DQ_{15}	DQ_{14}	A_{14}	A_{15}	DQ_6	DQ_7
G	DQ_{16}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	DQ_8
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{20}

(BGA-48P-M18)

■ **PIN DESCRIPTION**

Pin Name	Description
A_{20} to A_0	Address Input
$\overline{CE1}$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ_8 to DQ_1	Lower Byte Data Input/Output
DQ_{16} to DQ_9	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
N.C.	No Connection

■ BLOCK DIAGRAM
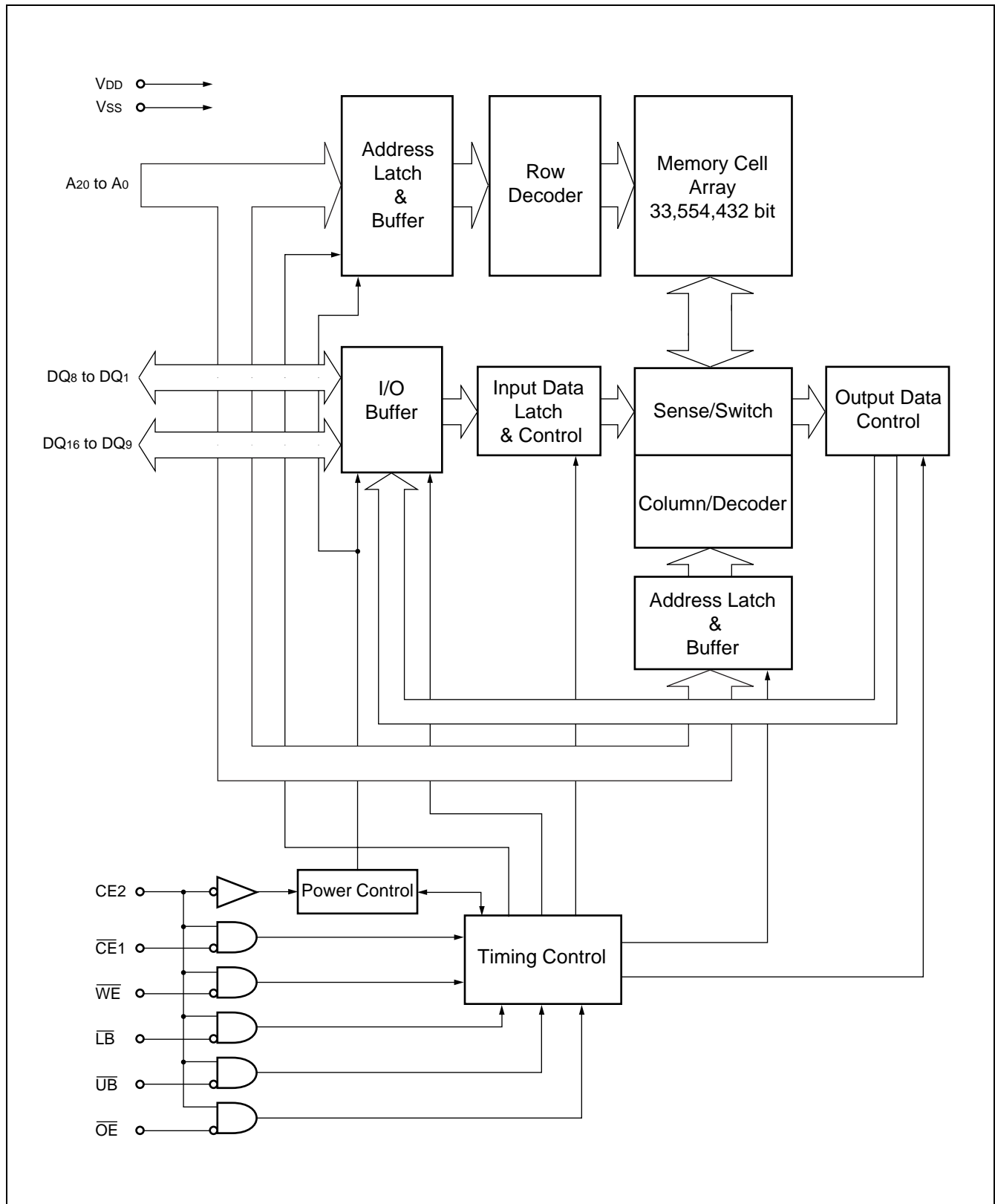
■ FUNCTION TRUTH TABLE

Mode	CE2	$\overline{CE1}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{20} to A_0	DQ_8 to DQ_1	DQ_{16} to DQ_9
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z
Output Disable[1]	H	L	H	H	X	X	*3	High-Z	High-Z
Output Disable (No Read)	H	L	H	L	H	H	Valid	High-Z	High-Z
Read (Upper Byte)	H	L	H	L	H	L	Valid	High-Z	Output Valid
Read (Lower Byte)	H	L	H	L	L	H	Valid	Output Valid	High-Z
Read (Word)	H	L	H	L	L	L	Valid	Output Valid	Output Valid
No Write	H	L	L	H*4	H	H	Valid	Invalid	Invalid
Write (Upper Byte)	H	L	L	H*4	H	L	Valid	Invalid	Input Valid
Write (Lower Byte)	H	L	L	H*4	L	H	Valid	Input Valid	Invalid
Write (Word)	H	L	L	H*4	L	L	Valid	Input Valid	Input Valid
Power Down[2]	L	X	X	X	X	X	X	High-Z	High-Z

Notes : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

*1 : Should not be kept this logic condition longer than 1 μs.

*2 : Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.
Data retention depends on the selection of Power Down Program.
Refer to "Power Down Program" for the detail.

*3 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*4 : $\overline{OE}$ can be V_{IL} during Write operation if the following conditions are satisfied;
  (1) Write pulse is initiated by $\overline{CE1}$ (refer to $\overline{CE1}$ Controlled Write timing) , or cycle time of the previous operation cycle is satisfied.
  (2) $\overline{OE}$ stays V_{IL} during Write cycle.

■ POWER DOWN

Power Down

The Power Down is to enter low power idle state when CE2 stays Low.
The MB82DPS02183B has four power down mode, Sleep, 4 M Partial, 8 M Partial, and 16 M Partial.
These can be programmed by series of read/write operation. Each mode has following features.

Mode	Data Retention	Retention Address
Sleep (default)	No	N/A
4 M Partial	4 M bit	00000h to 3FFFFh
8 M Partial	8 M bit	00000h to 7FFFFh
16 M Partial	16 M bit	00000h to FFFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to program to Sleep mode after power-up.

Power Down Program Sequence

The program requires total 6 read/write operation with unique address and data. Between each read/write operation requires that device be in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	1FFFFFh (MSB)	Read Data (RDa)
2nd	Write	1FFFFFh	RDa
3rd	Write	1FFFFFh	RDa
4th	Write	1FFFFFh	0000h
5th	Write	1FFFFFh	Data Key
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB) .
The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the program is cancelled and the data written by the second or third cycle is valid as a normal write operation.
The forth and fifth cycle is to write the data key for program. The data of forth cycle must be all 0's and data of fifth cycle is a data key for mode selection. If the forth or fifth cycle is written into different address, the program is also cancelled but write data may not be written as normal write operation.
The last cycle is to read from specific address key for mode selection. The both data key written by fifth cycle and address key must be the same mode for proper programming.

Once this program sequence is performed from a Partial mode to other Partial mode, the write data may be lost. So, it should perform this program prior to regular read/write operation if Partial mode is used.

Address Key

The address key has following format.

Mode	Address			
	A_{20}	A_{19}	A_{18} to A_0	Binary
Sleep (default)	1	1	1	1FFFFFh
4 M Partial	0	1	1	0FFFFFh
8 M Partial	1	0	1	17FFFFh
16 M Partial	0	0	1	07FFFFh

Data Key

The data key has following format.

Mode	Data			
	DQ$_{16}$ to DQ$_9$	DQ$_8$ to DQ$_2$	DQ$_1$	DQ$_0$
Sleep (default)	0	0	1	1
4 M Partial	0	0	1	0
8 M Partial	0	0	0	1
16 M Partial	0	0	0	0

The upper byte of data code may be ignored and it is just for recommendation to write 0's to upper byte for future compatibility.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value		Unit
		Min	Max	
Voltage of V_{DD} Supply Relative to Vss	V_{DD}	−0.5	+3.6	V
Voltage at Any Pin Relative to Vss	V_{IN}, V_{OUT}	−0.5	+3.6	V
Short Circuit Output Current	I_{OUT}	−50	+50	mA
Storage Temperature	T_{STG}	−55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage*1	V_{DD}	1.65	1.95	V
	V_{SS}	0	0	V
High Level Input Voltage *1, *2	V_{IH}	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage *1, *3	V_{IL}	−0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	−30	+85	°C

*1 : All voltage are referenced to Vss.

*2 : Maximum DC voltage on input and I/O pins are V_{DD} + 0.2 V. During voltage transitions, inputs may overshoot to V_{DD} + 1.0 V for periods of up to 5 ns.

*3 : Minimum DC voltage on input or I/O pins is −0.3 V. During voltage transitions, inputs may undershoot V_{SS} to −1.0 V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ **PIN CAPACITANCE**

(f = 1 MHz, T_A = + 25 °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	$C_{I/O}$	V_{IO} = 0 V	—	—	8	pF

■ ELECTRICAL CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

1. DC CHARACTERISTICS

Parameter		Symbol	Test conditions		Value		Unit
					Min	Max	
Input Leakage Current		I_{LI}	$V_{SS} \leq V_{IN} \leq V_{DD}$		−1.0	+1.0	μA
Output Leakage Current		I_{LO}	$0\,V \leq V_{OUT} \leq V_{DD}$, Output Disable		−1.0	+1.0	μA
Output High Voltage Level		V_{OH}	$V_{DD} = V_{DD}$ Min, $I_{OH} = -0.5$ mA		1.4	—	V
Output Low Voltage Level		V_{OL}	$I_{OL} = 1$ mA		—	0.4	V
V_{DD} Power Down Current		I_{DDPS}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $CE2 \leq 0.2$ V	SLEEP	—	30	μA
	L version				—	10	μA
		I_{DDP4}		4 M partial	—	80	μA
	L version				—	45	μA
		I_{DDP8}		8 M partial	—	100	μA
	L version				—	55	μA
		I_{DDP16}		16 M partial	—	130	μA
	L version				—	70	μA
V_{DD} Standby Current		I_{DDS}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = CE2 = V_{IH}$		—	5	mA
	L version				—	1.5	mA
		I_{DDS1}	$V_{DD} = V_{DD}$ Max, $V_{IN} \leq 0.2$ V or $V_{IL} \geq V_{DD} - 0.2$ V, $\overline{CE}1 = CE2 \geq V_{DD} - 0.2$ V		—	200	μA
	L version				—	100	μA
V_{DD} Active Current		I_{DDA1}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA	$t_{RC}/t_{WC} =$ minimum	—	25	mA
		I_{DDA2}		$t_{RC}/t_{WC} = 1\ \mu s$	—	3	mA
V_{DD} Page Read Current		I_{DDA3}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and $CE2 = V_{IH}$, $I_{OUT} = 0$ mA, $t_{PRC} =$ Min		—	10	mA

Notes : • All voltages are referenced to Vss.
• DC Characteristics are measured after following POWER-UP timing.
• I_{OUT} depends on the output load conditions.

2. AC CHARACTERISTICS

(1) READ OPERATION

Parameter	Symbol	-85/-85L Min	-85/-85L Max	Unit	Notes
Read Cycle Time	t_{RC}	85	1000	ns	*1, *2
$\overline{CE}1$ Access Time	t_{CE}	—	85	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	50	ns	*3
Address Access Time	t_{AA}	—	85	ns	*3, *5
$\overline{LB}/\overline{UB}$ Access Time	t_{BA}	—	35	ns	*3
Page Address Access Time	t_{PAA}	—	25	ns	*3, *6
Page Read Cycle Time	t_{PRC}	30	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{LB}/\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*3
$\overline{LB}/\overline{UB}$ High to Output High-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}1$ Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	12	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *8
Address Hold Time from $\overline{CE}1$ High	t_{CHAH}	–5	—	ns	*9
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without change of address input of A_{20} to A_3.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*4 : The output load 5 pF without any other load.

*5 : Applicable to A_{20} to A_3 when $\overline{CE}1$ is kept at Low.

*6 : Applicable only to A_2, A_1 and A_0 when $\overline{CE}1$ is kept at Low for the page address access.

*7 : In case Page Read Cycle is continued with keeping $\overline{CE}1$ stays Low, $\overline{CE}1$ must be brought to High within 4 μs. In other words, Page Read Cycle must be closed within 4 μs.

*8 : Applicable when at least two of address inputs among applicable are switched from previous state.

*9 : t_{RC} (Min) and t_{PRC} (Min) must be satisfied.

(2) WRITE OPERATION

Parameter	Symbol	-85/-85L		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	85	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*2
$\overline{CE}1$ Write Pulse Width	t_{CW}	50	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	50	—	ns	*3
$\overline{LB}/\overline{UB}$ Write Pulse Width	t_{BW}	50	—	ns	*3
$\overline{LB}/\overline{UB}$ Byte Mask Setup Time	t_{BS}	–5	—	ns	*4
$\overline{LB}/\overline{UB}$ Byte Mask Hold Time	t_{BH}	5	—	ns	*5
$\overline{CE}1$ Write Recovery Time	t_{WRC}	15	—	ns	*6
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*6
$\overline{LB}/\overline{UB}$ Write Recovery Time	t_{BR}	15	1000	ns	*6
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*7
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*8
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	20	—	ns	
$\overline{CE}1$ High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}) .

*3 : Write pulse is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$, or $\overline{LB}/\overline{UB}$, whichever occurs last.

*4 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs last.

*5 : Applicable for byte mask only. Byte mask hold time is defined from Low to High transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs first.

*6 : Write recovery is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$, or $\overline{LB}/\overline{UB}$, whichever occurs first.

*7 : If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other words, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}1$ is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

*8 : If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other words, $\overline{OE}$ must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

(3) POWER DOWN PARAMETERS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	85	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	μs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	1	—	μs	*2
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	

*1 : Applicable also to power-up.

*2 : Applicable when 4 M, 8 M, and 16 M Partial mode is programmed.

(4) OTHER TIMING PARAMETERS

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	μs	
Input Transition Time	t_{T}	1	25	ns	*2

*1 : Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

*2 : The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.

(5) AC TEST CONDITIONS

Description	Symbol	Test Setup	Value	Unit	Note
Input High Level	V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low Level	V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level	V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	t_{T}	Between V_{IL} and V_{IH}	5	ns	

VDD × 0.5 V

VDD ○————•———————————⌇ 50 Ω

0.1 μF ⊣⊢   Device under
              Test   •————○ Output

VSS ○————•

                            ⊣⊢ 50 pF
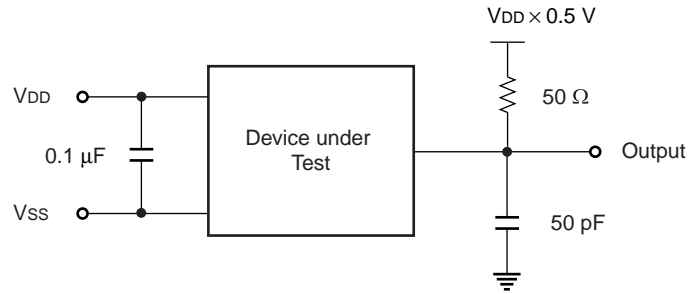
AC MEASUREMENT OUTPUT LOAD CIRCUIT

■ TIMING DIAGRAMS

(1) READ Timing #1 (Basic Timing)

Note : CE2 and $\overline{WE}$ must be High for entire read cycle.
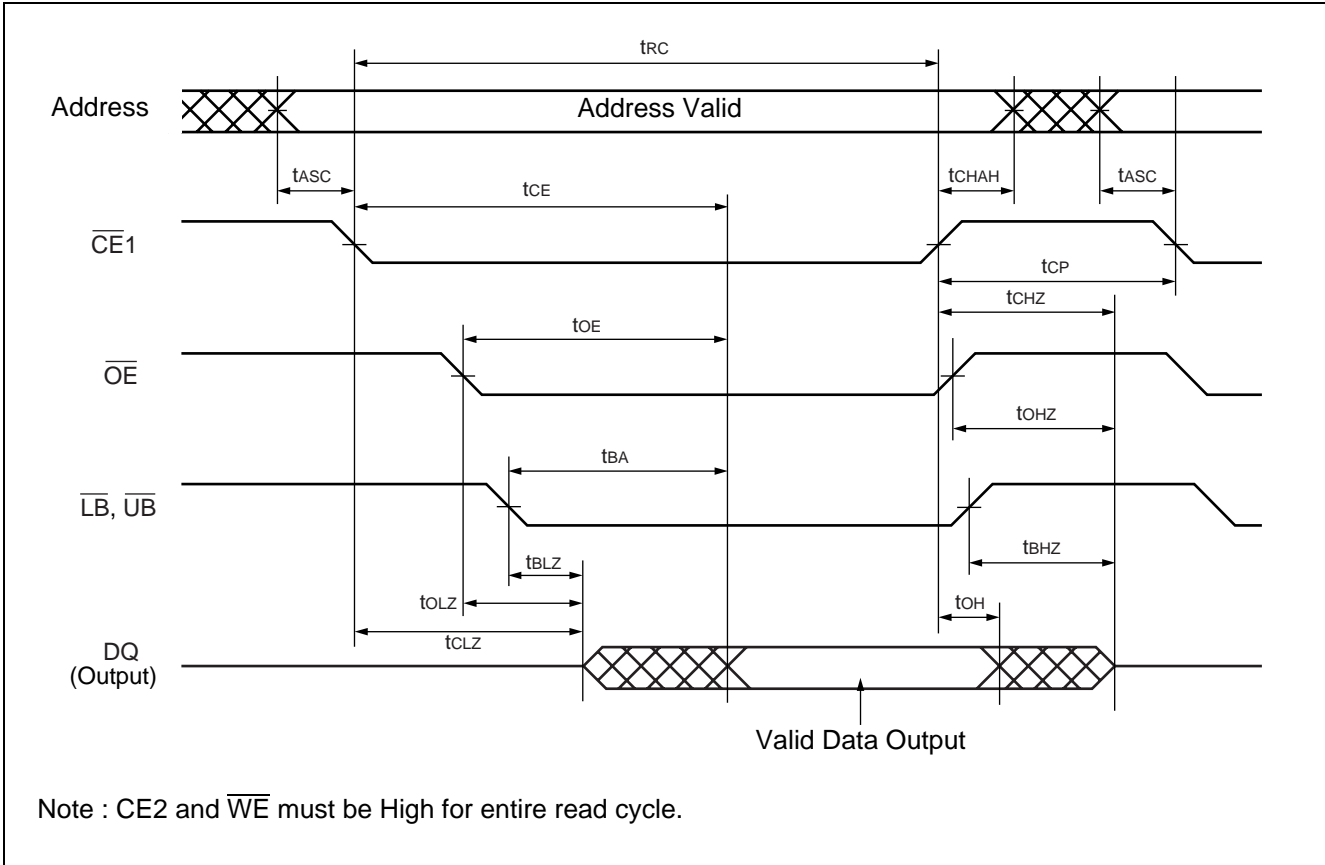
(2) READ Timing #2 ($\overline{OE}$ & Address Access)

Note : CE2 and $\overline{WE}$ must be High for entire read cycle.
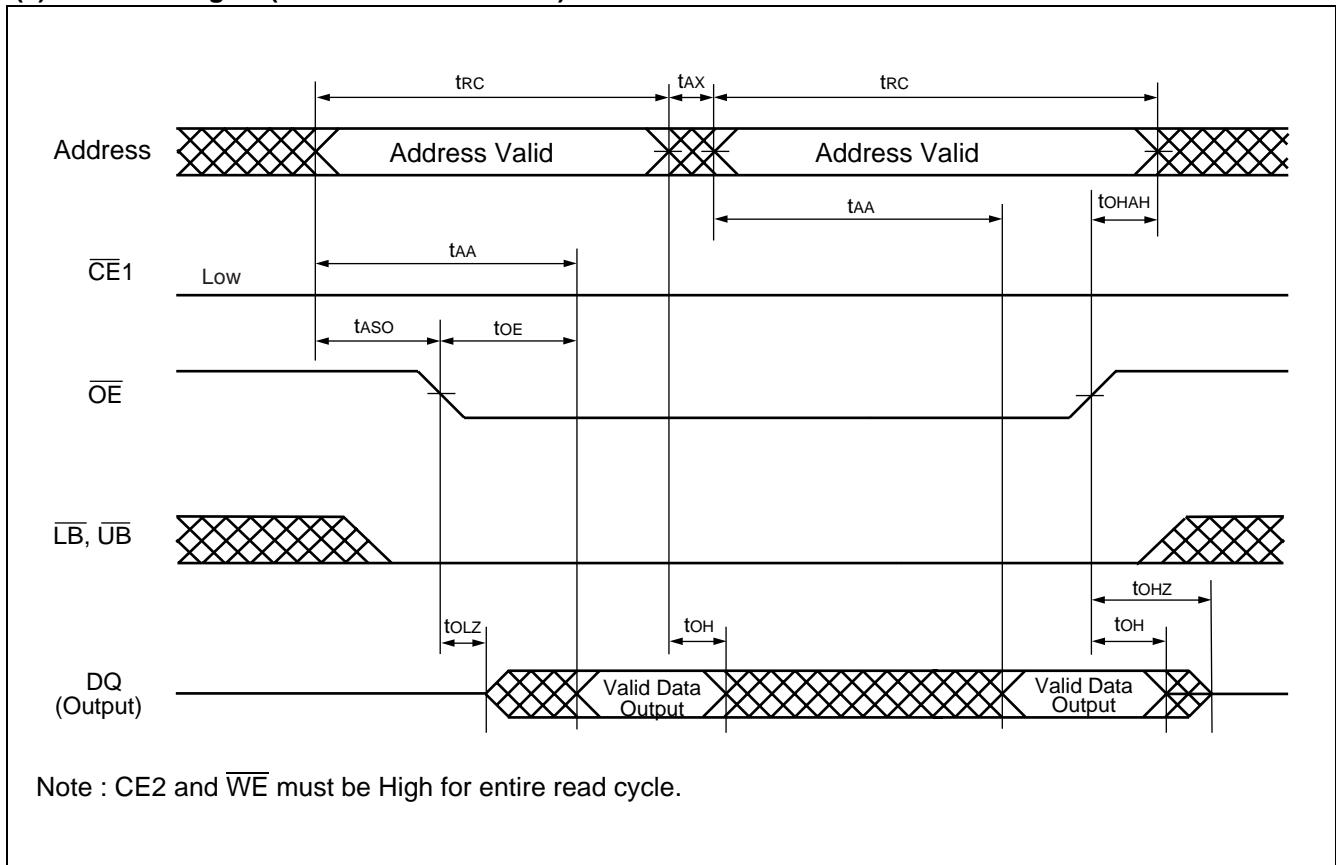
(3) READ Timing #3 (L̄B̄, ŪB̄ Byte Access)

tAX   tRC   tAX

Address   Address Valid

tAA

C̄Ē1, ŌĒ   Low

tBA   tBA

L̄B̄

tBA

ŪB̄

tBHZ   tBHZ

tBLZ   tOH   tBLZ   tOH

DQ8 to DQ1
(Output)

Valid Data Output   Valid Data Output   tBHZ

tBLZ   tOH

DQ16 to DQ9
(Output)

Valid Data Output

Note : CE2 and W̄Ē must be High for entire read cycle.
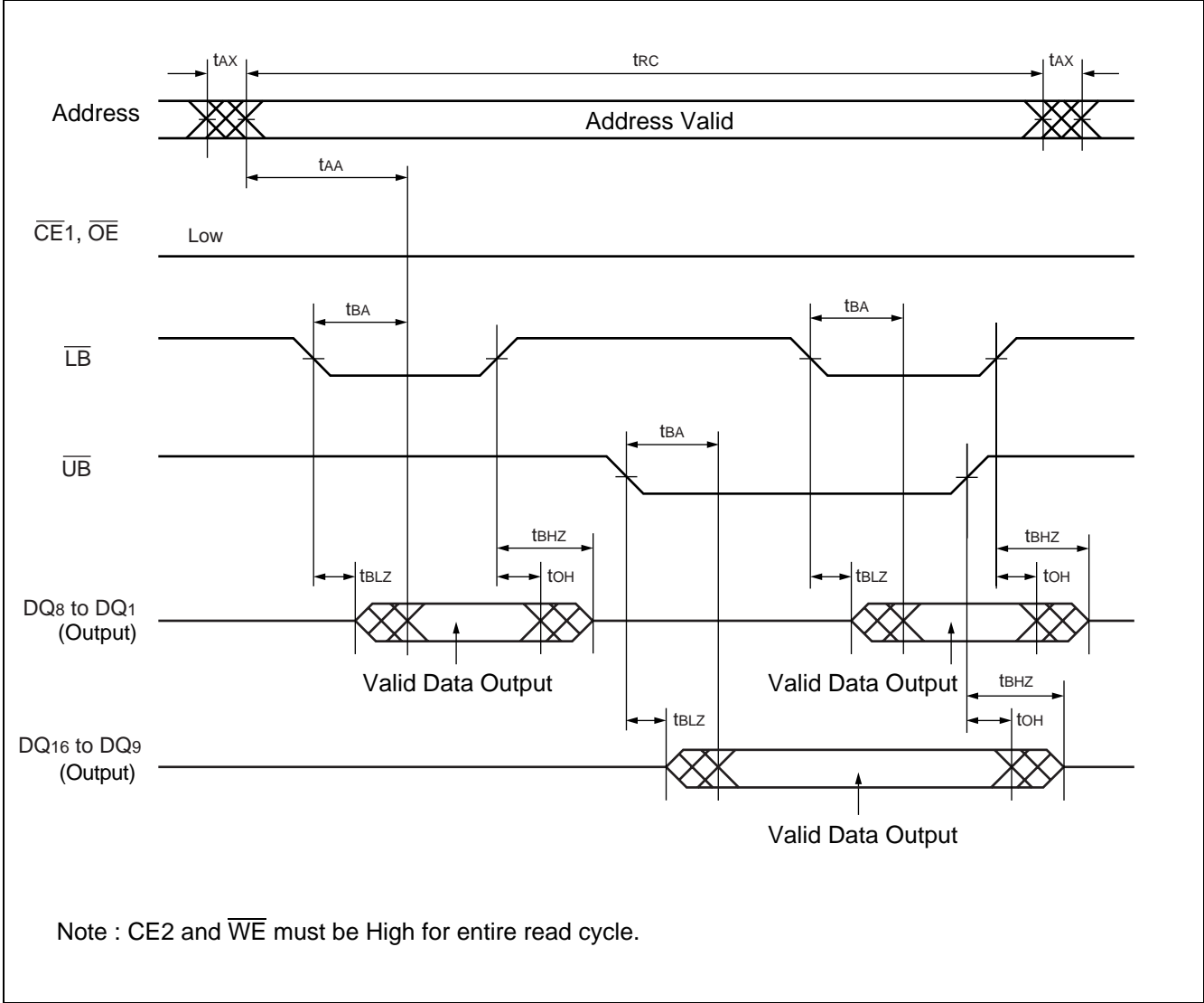
(4) READ Timing #4 (Page Address Access after $\overline{CE}$1 Control Access)

Note : CE2 and $\overline{WE}$ must be High for entire read cycle.
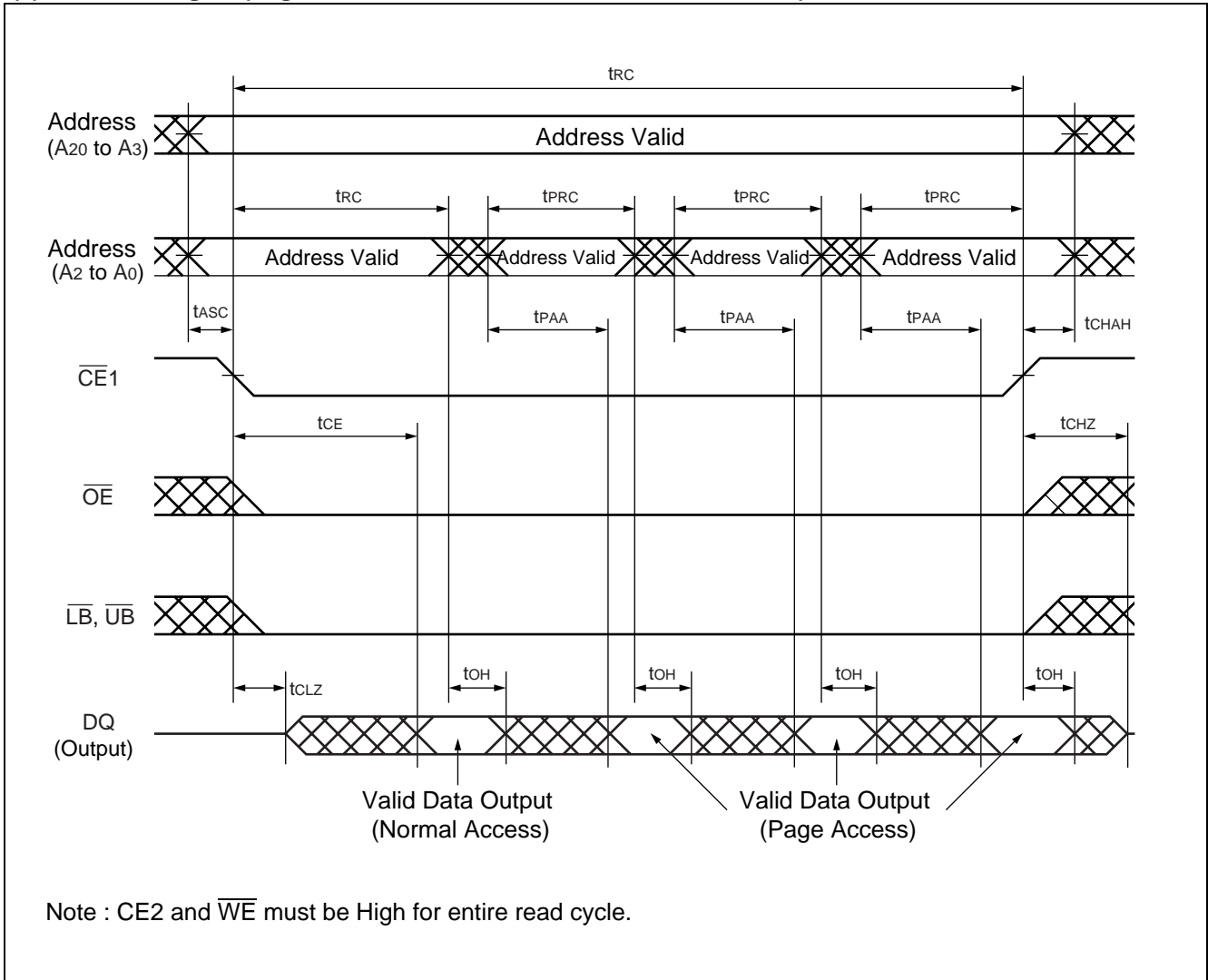
(5) READ Timing #5 (Random and Page Address Access)

	t_{RC}	t_{AX}		t_{RC}	t_{AX}	

Address
(A20 to A3)

Address Valid — Address Valid

t_{RC} t_{PRC} t_{RC} t_{PRC}

Address
(A2 to A0)

Address Valid — Address Valid — Address Valid — Address Valid

t_{AA} t_{PAA} t_{AA} t_{PAA}

$\overline{CE}1$ LOW

t_{ASO} t_{OE}

$\overline{OE}$

t_{BA}

$\overline{LB}, \overline{UB}$

t_{OLZ} t_{OH} t_{OH} t_{OH} t_{OH}
t_{BLZ}

DQ
(Output)

Valid Data Output
(Normal Access)

Valid Data Output
(Page Access)

Notes : • CE2 and $\overline{WE}$ must be High for entire read cycle.
• Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}1$ and $\overline{OE}$ are Low.
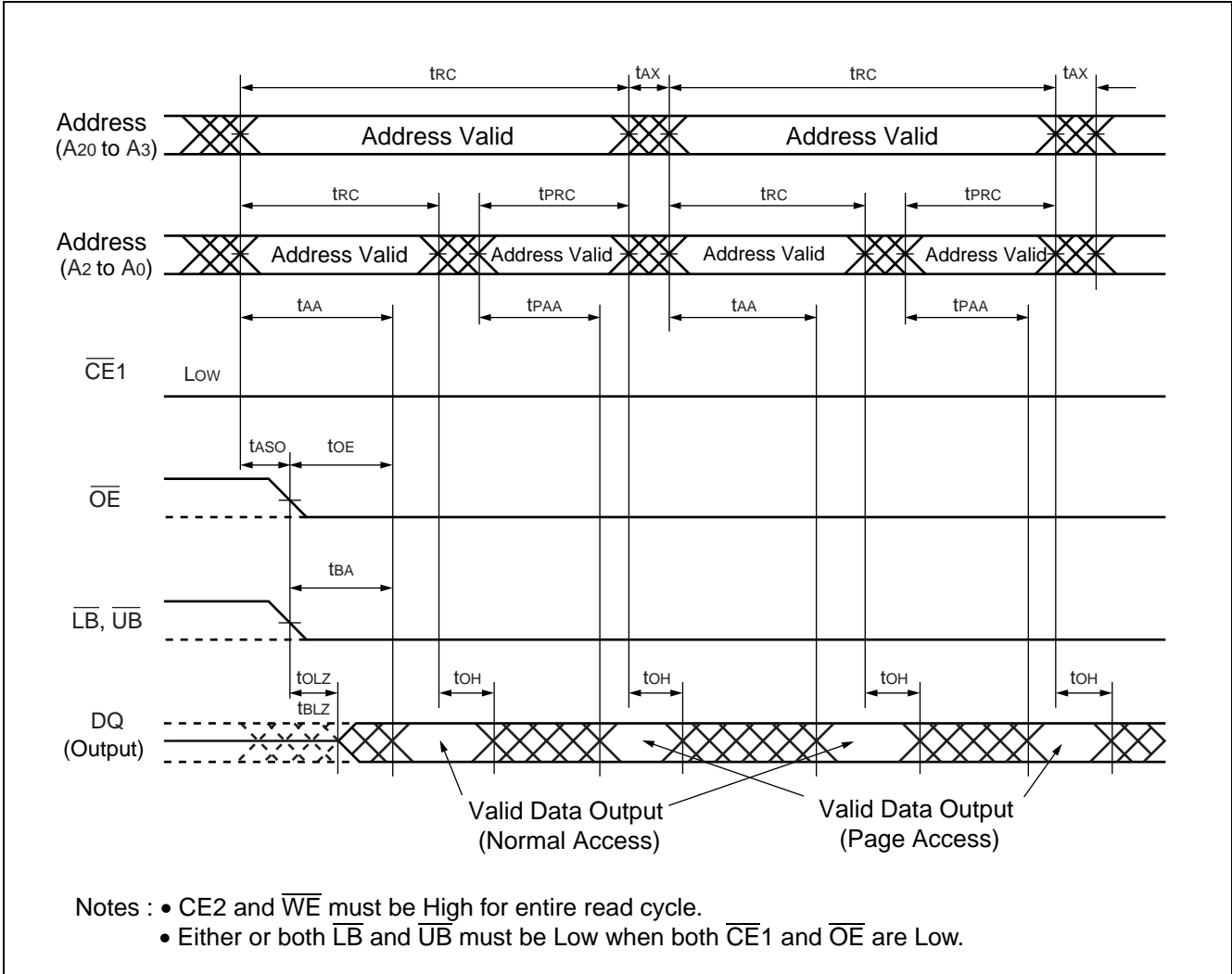
(6) WRITE Timing #1 (Basic Timing)

Note : CE2 must be High for write cycle.
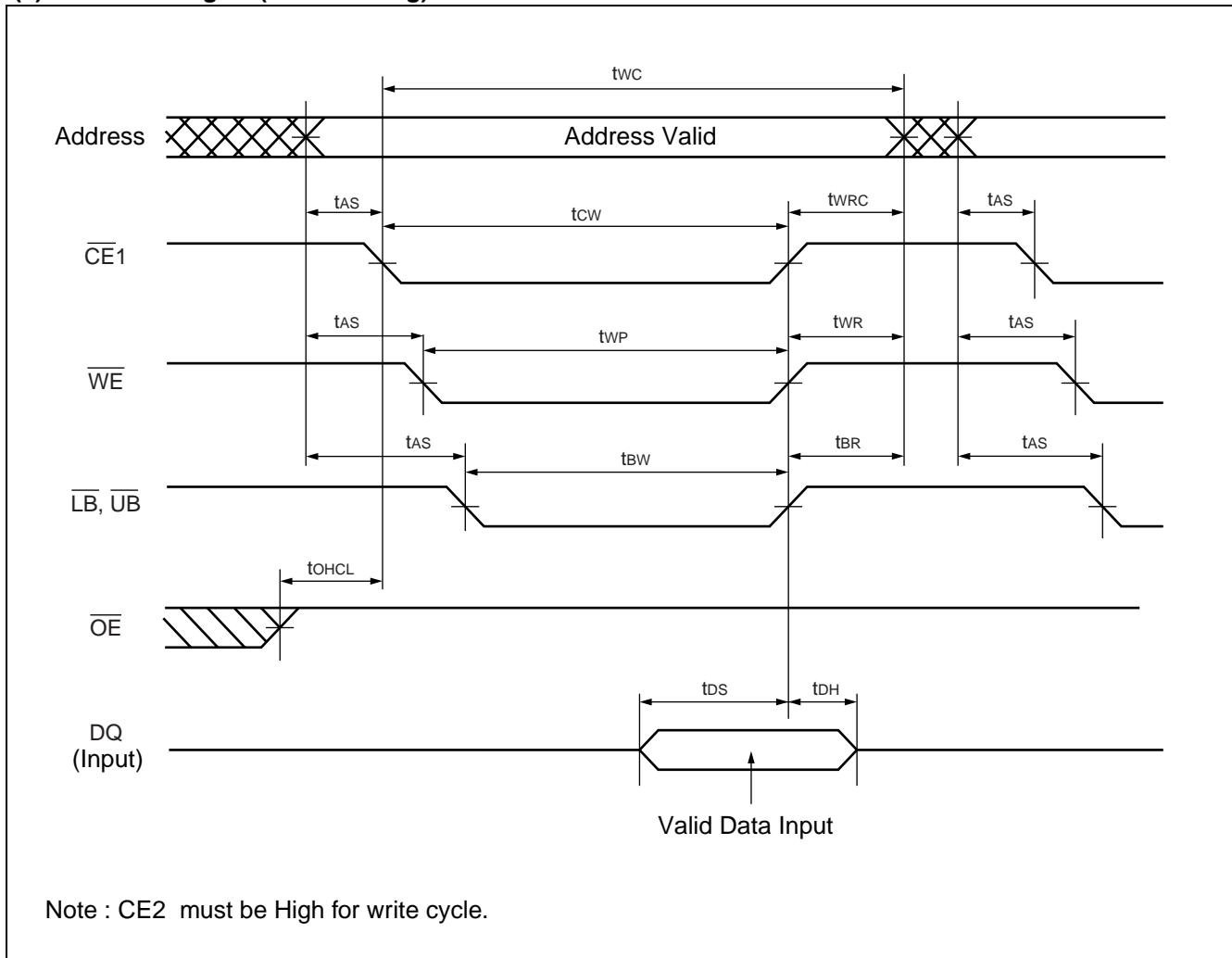
(7) WRITE Timing #2 (WE Control)

Note : CE2 must be High for write cycle.
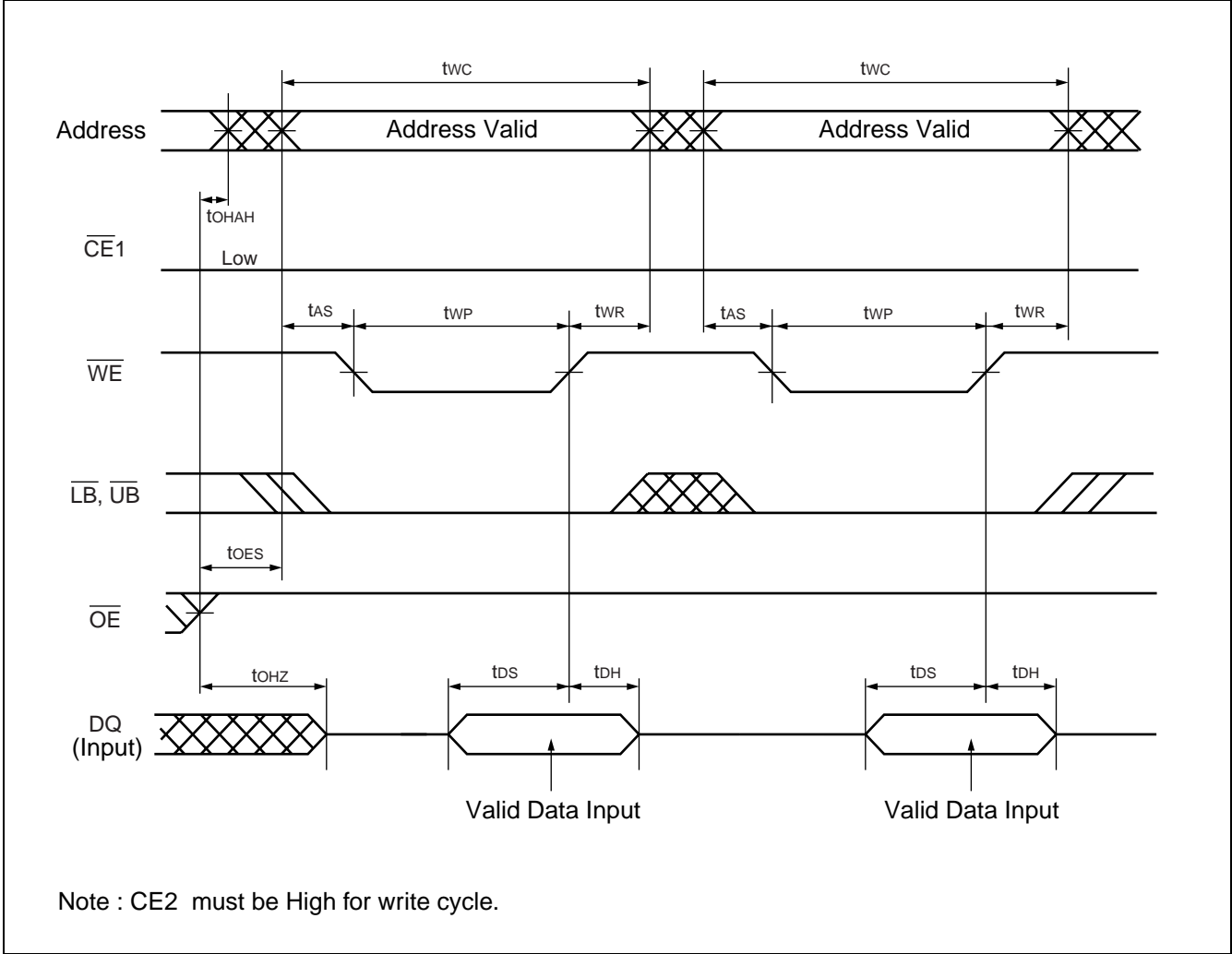
(8) WRITE Timing #3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)

Note : CE2 must be High for write cycle.
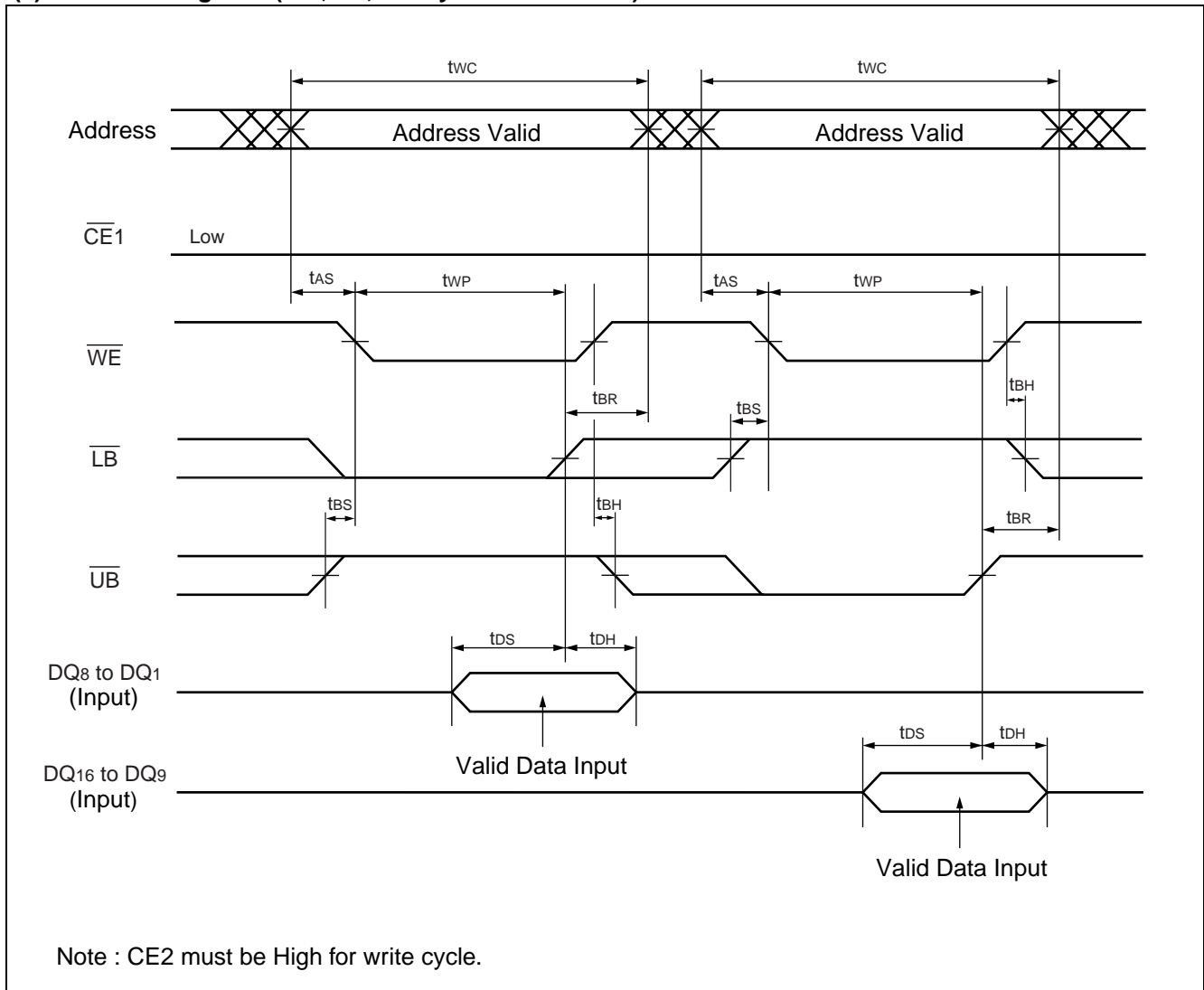
(9) WRITE Timing #3-2 (WE, LB, UB Byte Write Control)

Note : CE2 must be High for write cycle.
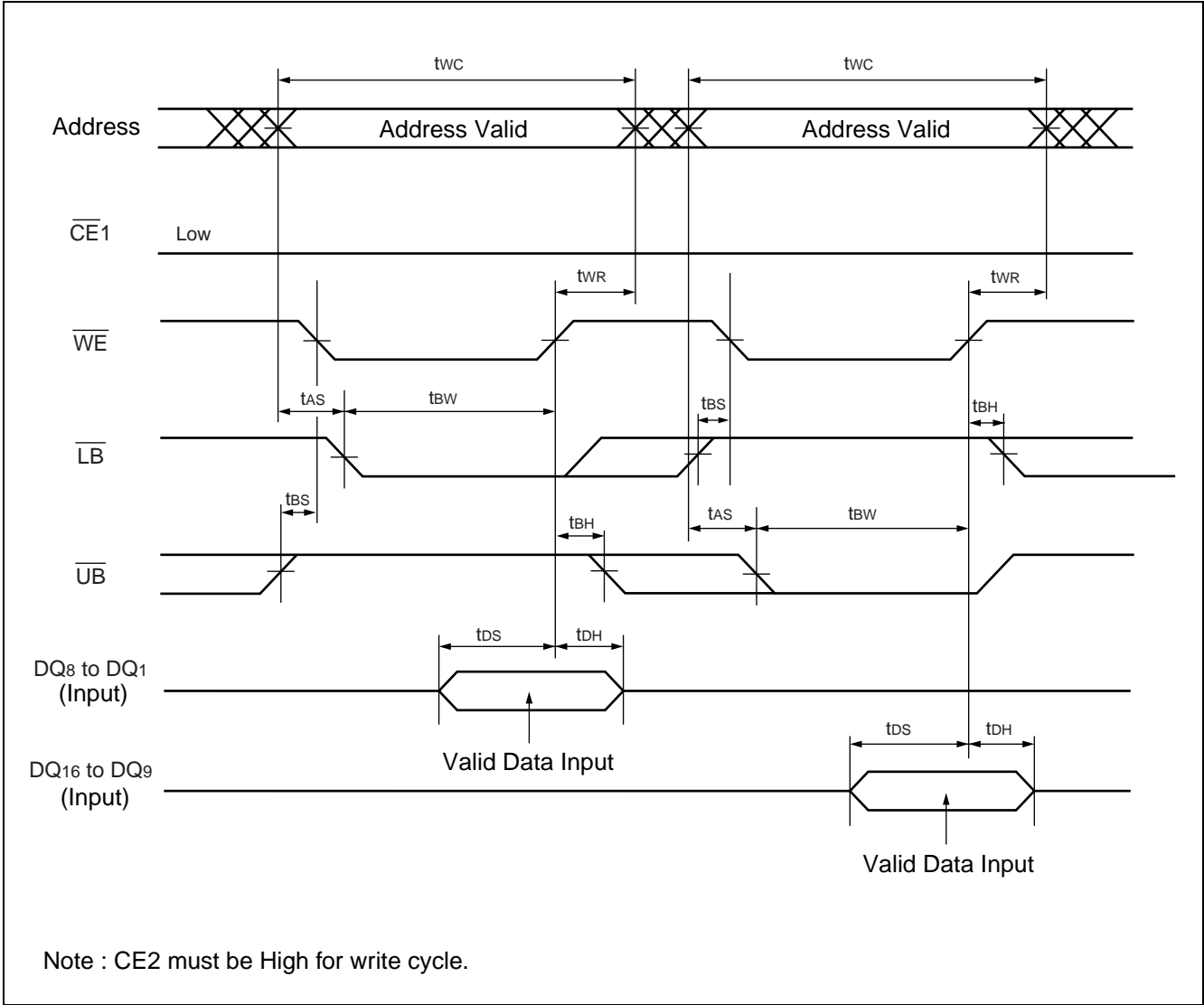
(10) WRITE Timing #3-3 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)

Note : CE2 must be High for write cycle.
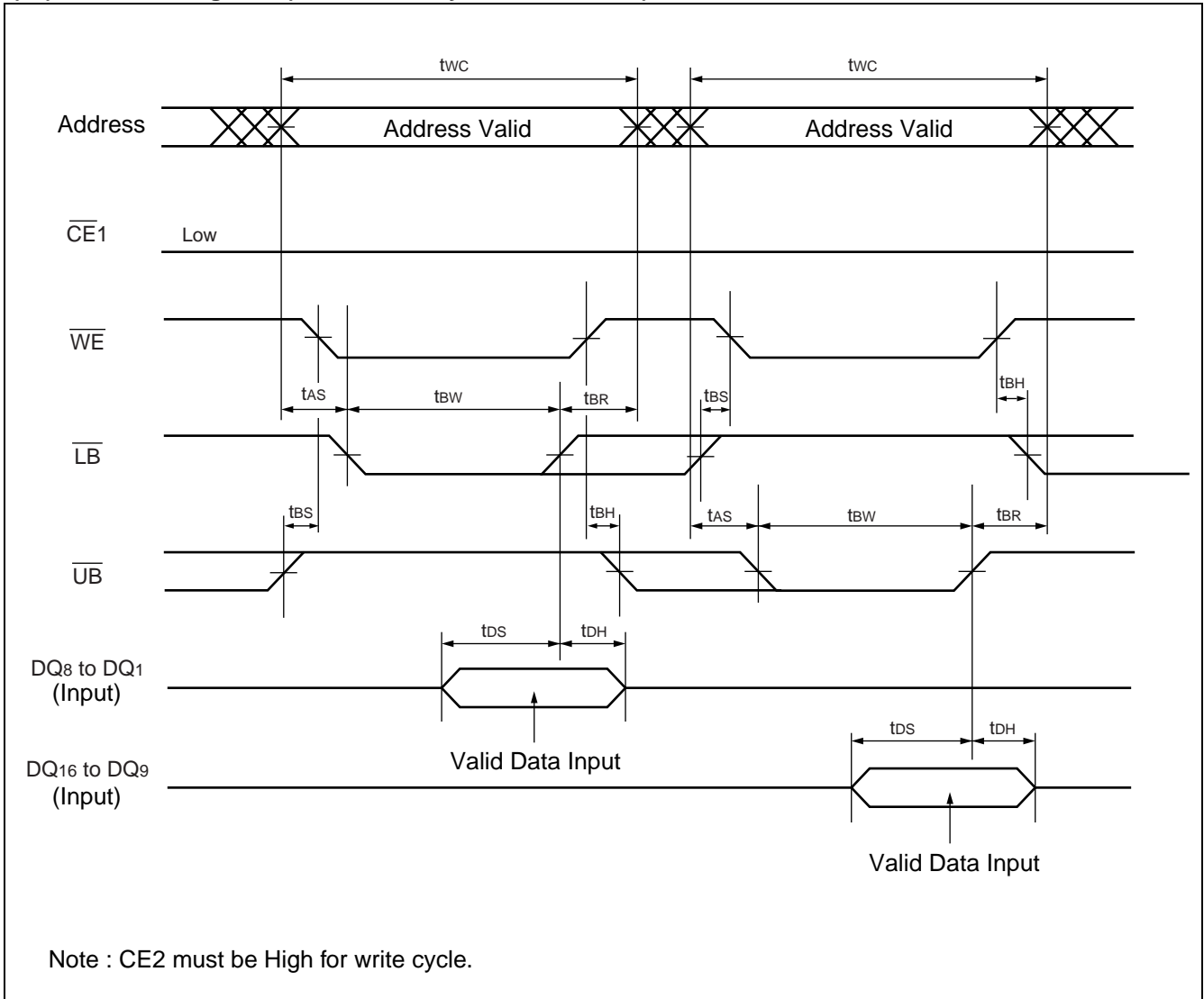
(11) WRITE Timing #3-4 ($\overline{\text{WE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$ Byte Write Control)

Note : CE2 must be High for write cycle.
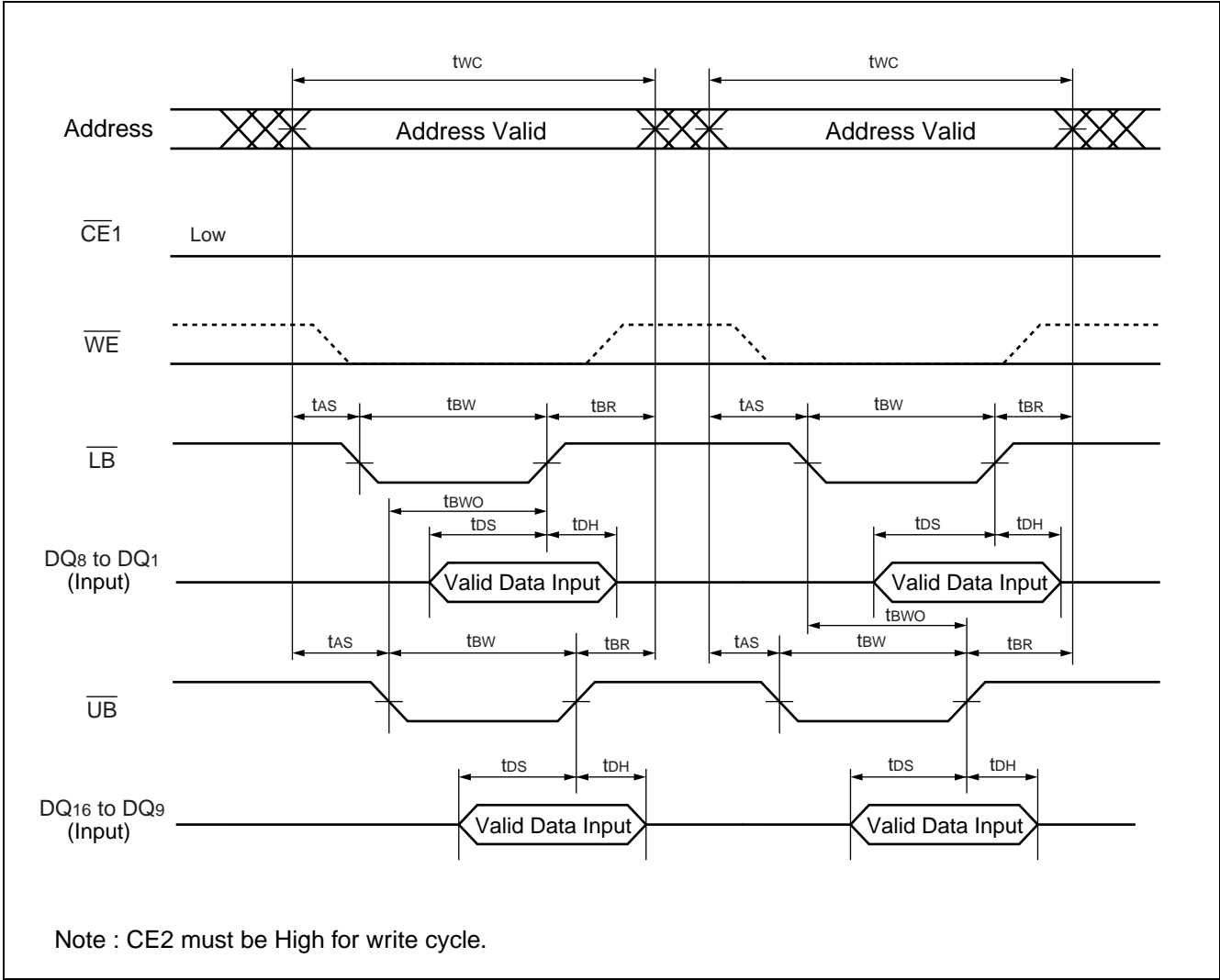
(12) READ / WRITE Timing #1-1 (CE1 Control)
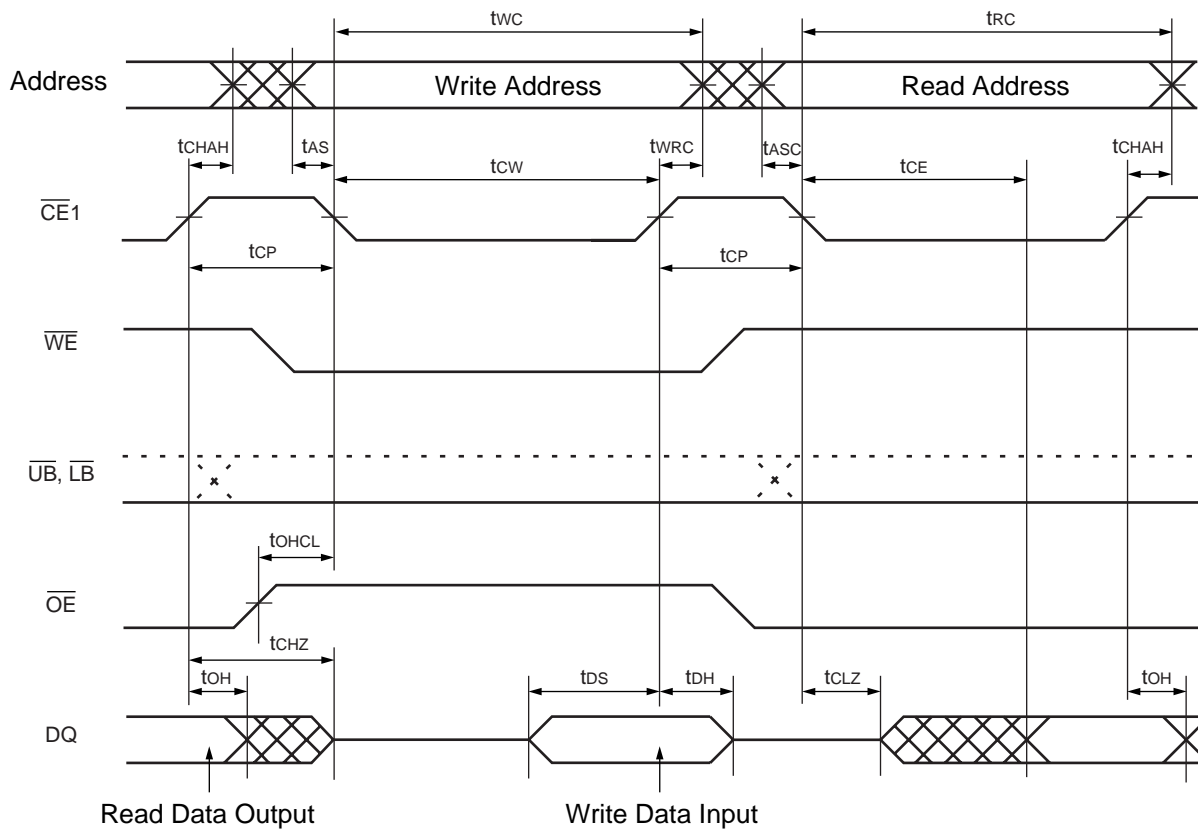
Note : Write address is valid from either CE1 or WE of last falling edge.

(13) READ / WRITE Timing #1-2 ($\overline{CE}1$, $\overline{WE}$, $\overline{OE}$ Control)

Note : $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}1$ controlled write at Read-Write-Read sequence.
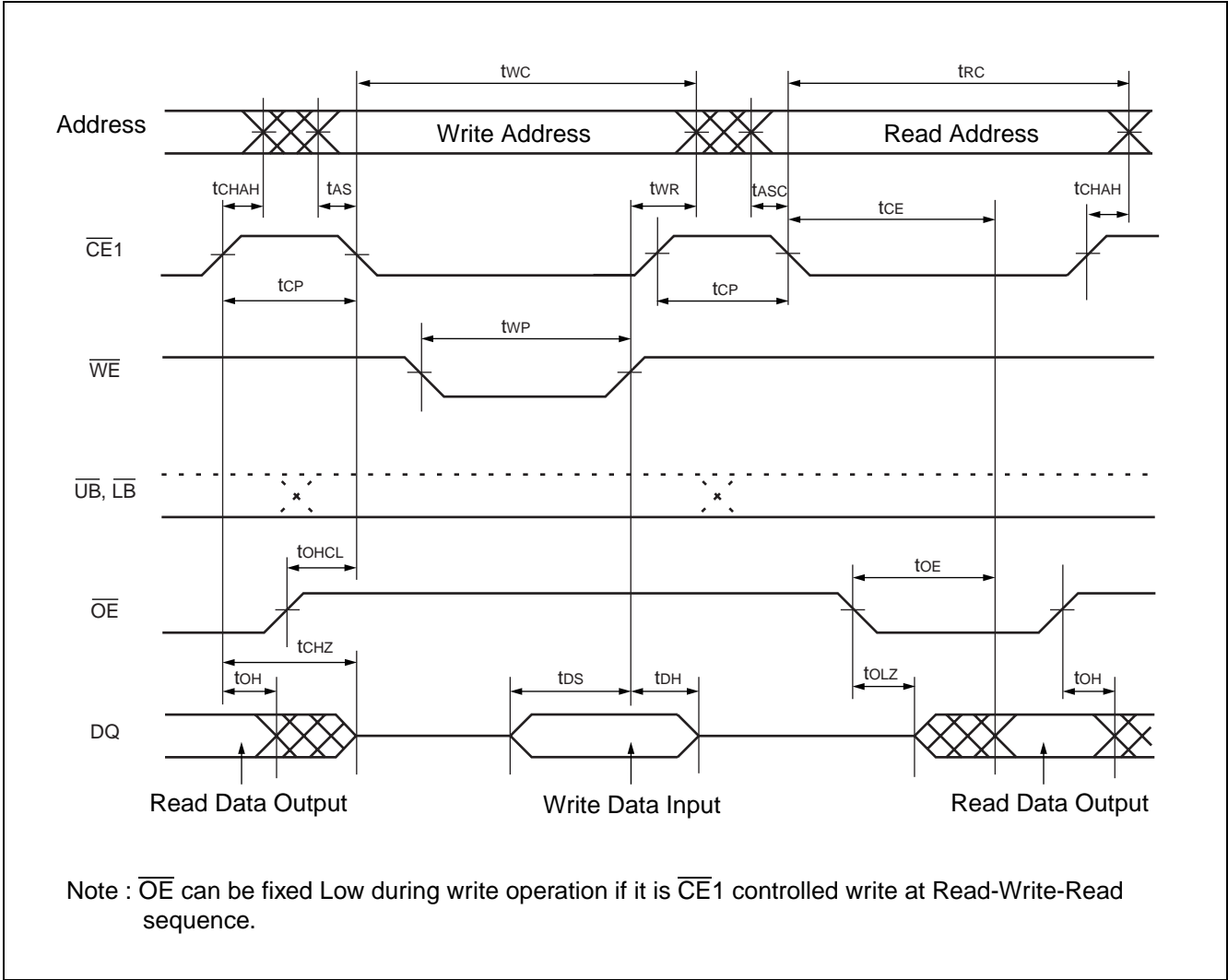
(14) READ / WRITE Timing #2 ($\overline{OE}$, $\overline{WE}$ Control)
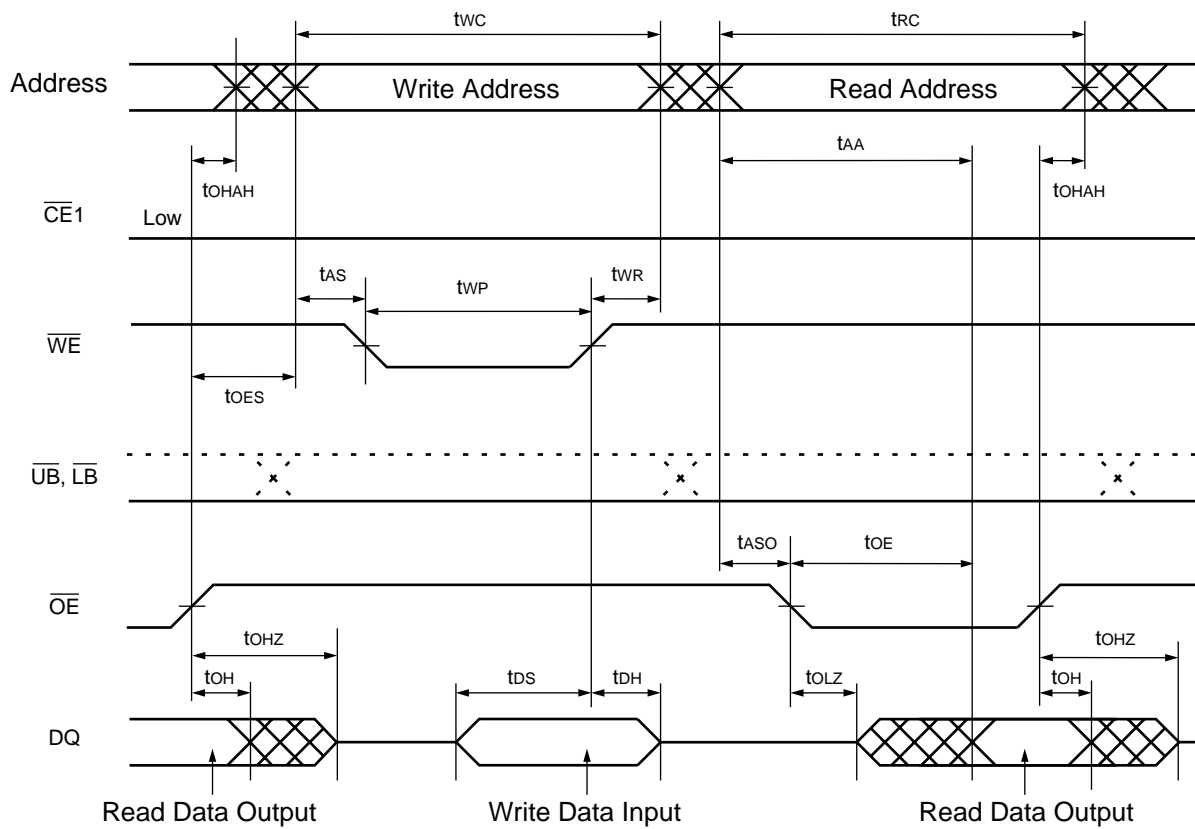
Note : $\overline{CE}1$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(15) READ / WRITE Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)

Note : $\overline{CE}1$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

(16) POWER-UP Timing

Note : The t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable both $\overline{CE}1$ and CE2.
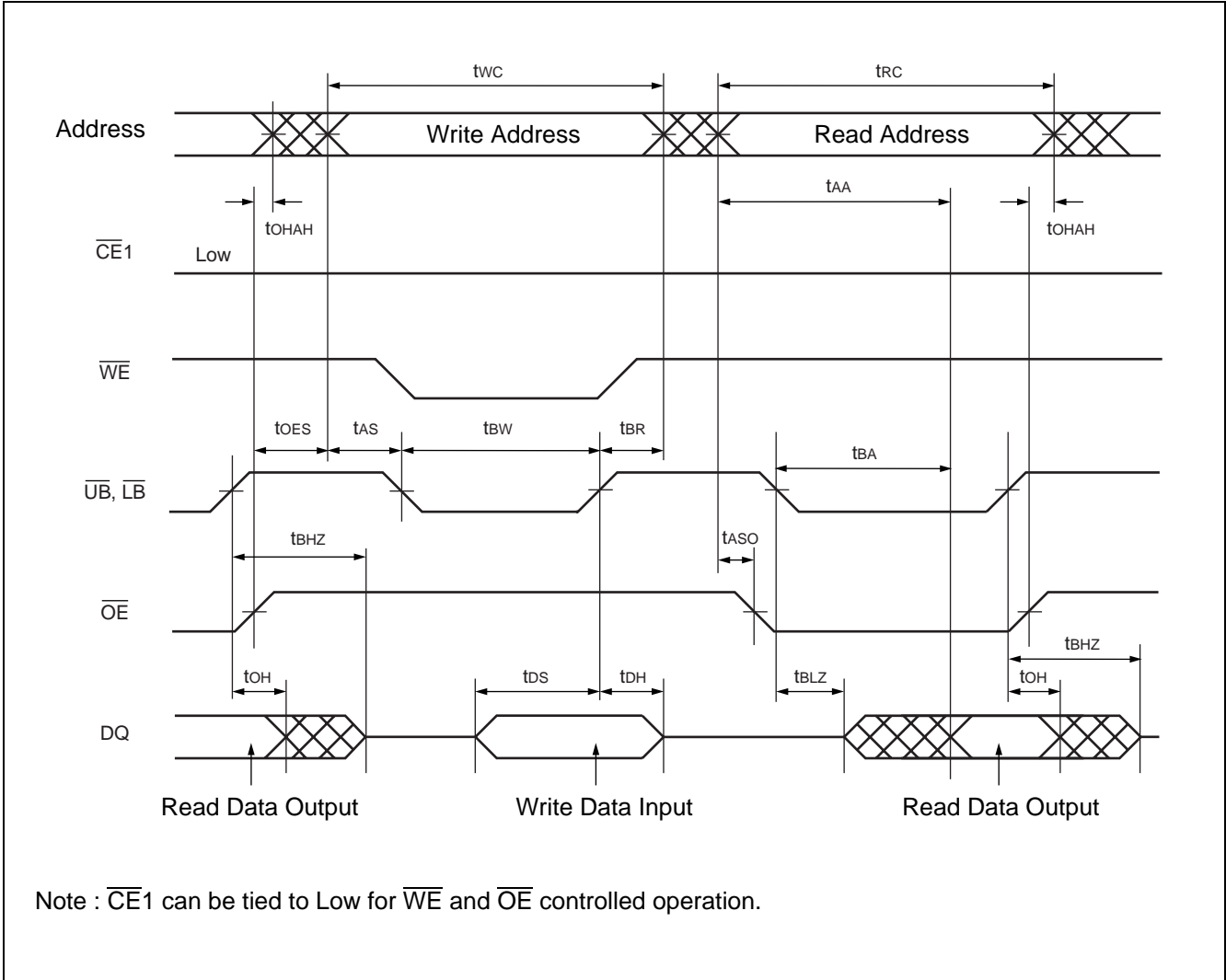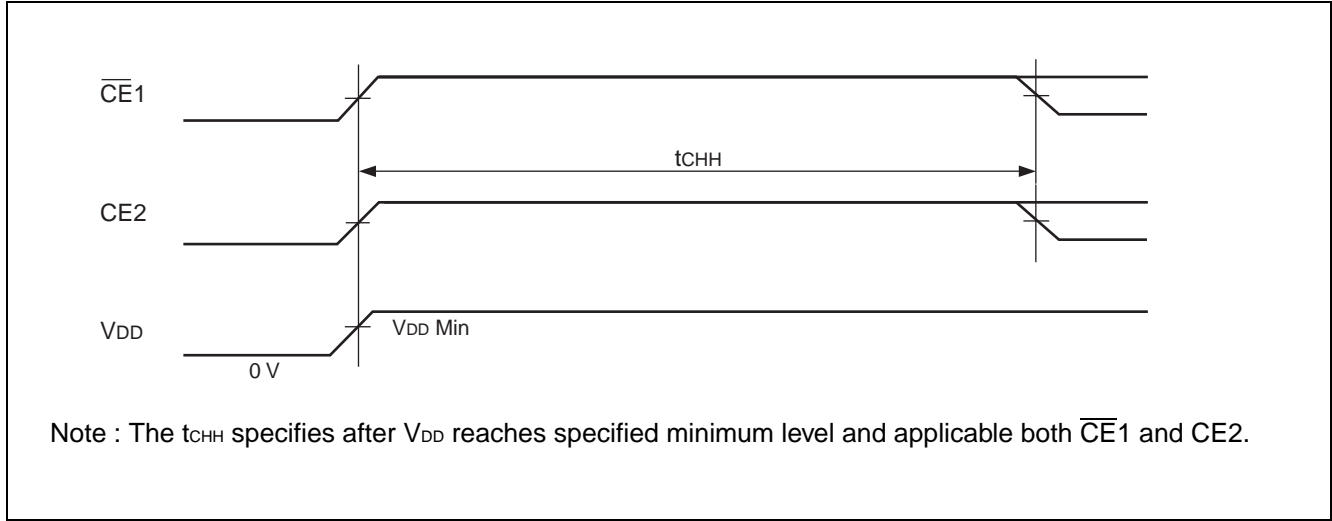
(17) POWER DOWN Entry and Exit Timing
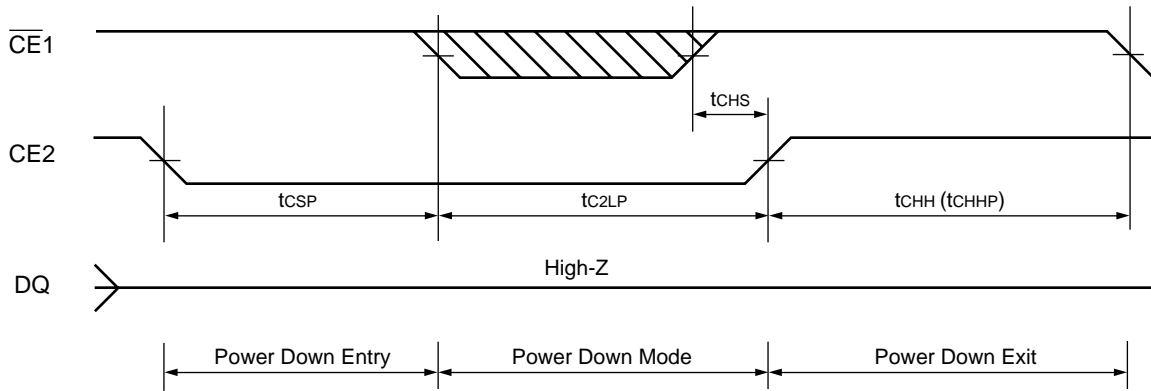
Note : This Power Down mode can be also used as a reset timing if " (16) POWER-UP timing" could not be satisfied and Power Down program was not performed prior to this reset.

(18) Standby Entry Timing after Read or Write
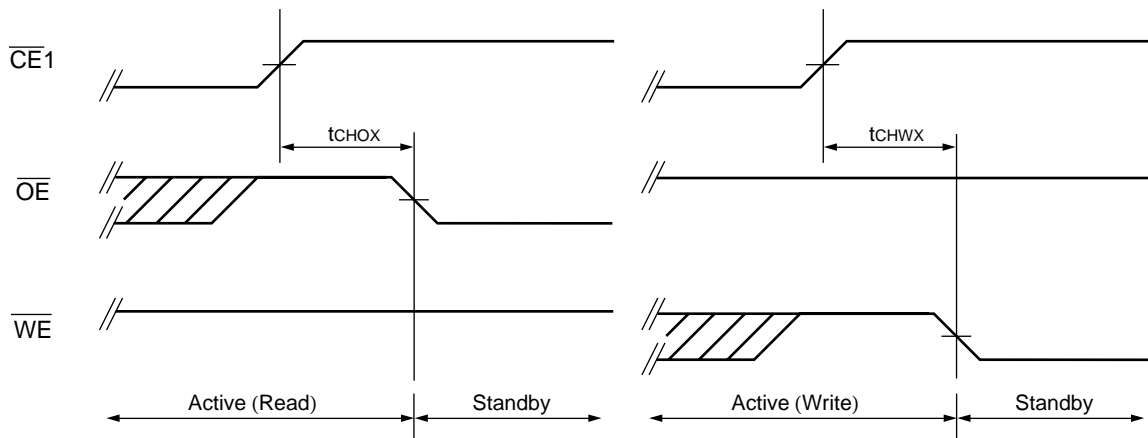
Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (Min) period for Standby mode from $\overline{CE}$1 Low to High transition.

(19) POWER DOWN PROGRAM Timing
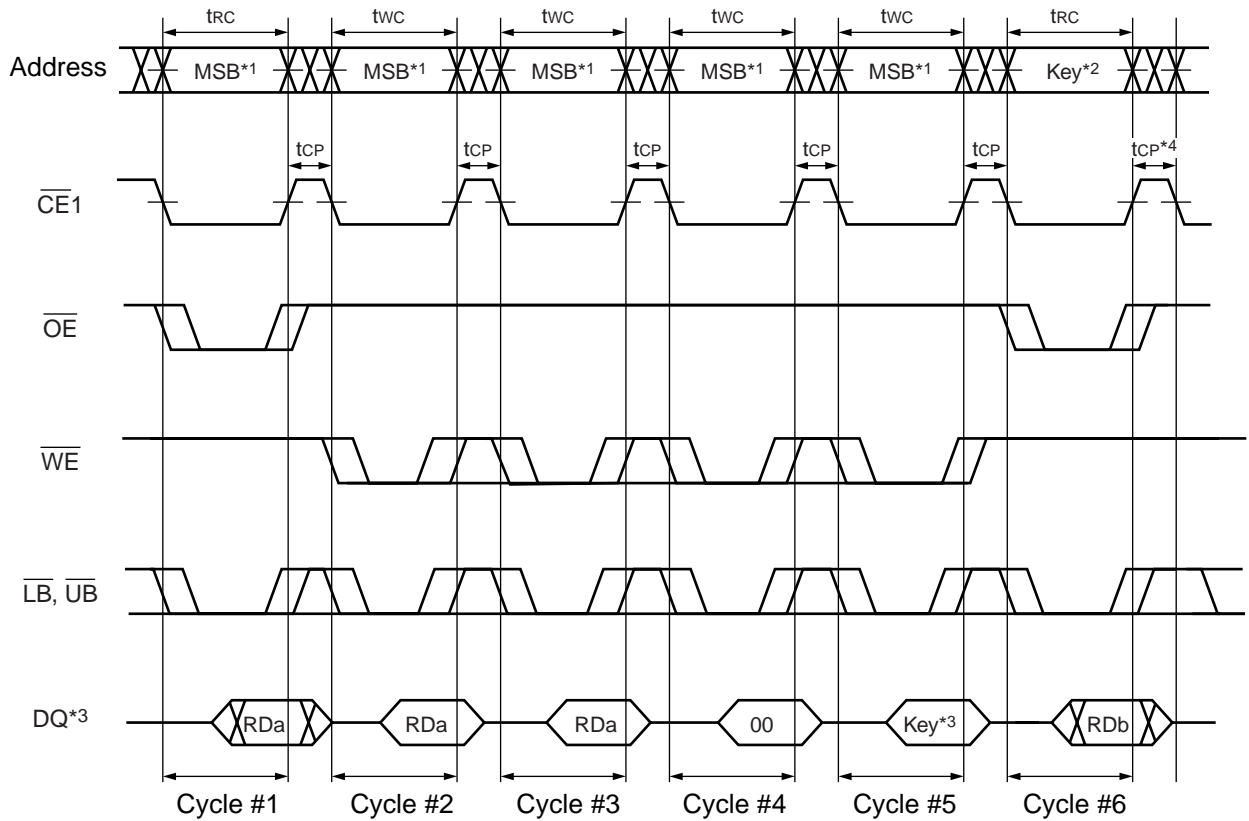
*1 : The all address inputs must be High from Cycle #1 to #5.

*2 : The address key must confirm the format specified in "■ POWER DOWN". If not, the operation and data are not guaranteed.

*3 : The data key must confirm the format specified in "■ POWER DOWN". If not, the operation and data are not guaranteed.

*4 : After t_{CP} following Cycle #6, the Power Down Program is completed and returned to the normal operation.

■ ORDERING INFORMATION

Part No.	Package	Remarks
MB82DPS02183B-85PBN	48-ball plastic FBGA 0.75 mm pitch (BGA-48P-M18)	t_{CE} = 85 ns Max, I_{DDS1} = 200 µA Max
MB82DPS02183B-85LPBN		t_{CE} = 85 ns Max, I_{DDS1} = 100 µA Max

■ PACKAGE DIMENSION

48-ball plastic FBGA
(BGA-48P-M18)

9.00±0.10(.354±.004)

6.00±0.10
(.236±.004)

INDEX AREA

$1.05^{+0.15}_{-0.10}$ (Mounting height)
$\left(.041^{+.006}_{-.004}\right)$

0.25±0.10
(.010±.004) (Stand off)

(5.25(.207))

0.75(.030)
TYP

(3.75(.148))

0.75(.030)
TYP

6
5
4
3
2
1

H G F E D C B A   INDEX MARK

48-ø0.35±0.10   ⊕ | 0.08(.003) Ⓜ
(48-ø.014±.004)

// | 0.20(.008) | S

S

⌒ | 0.10(.004) | S
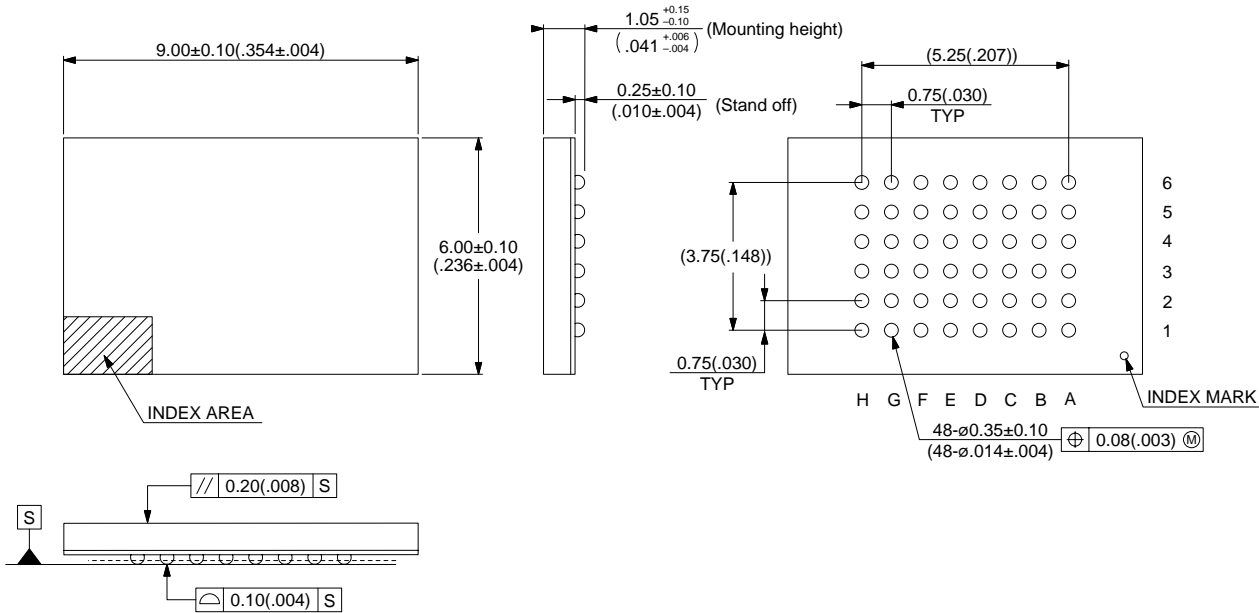
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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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