

3.3V 1:16 LVPECL Fanout Buffer

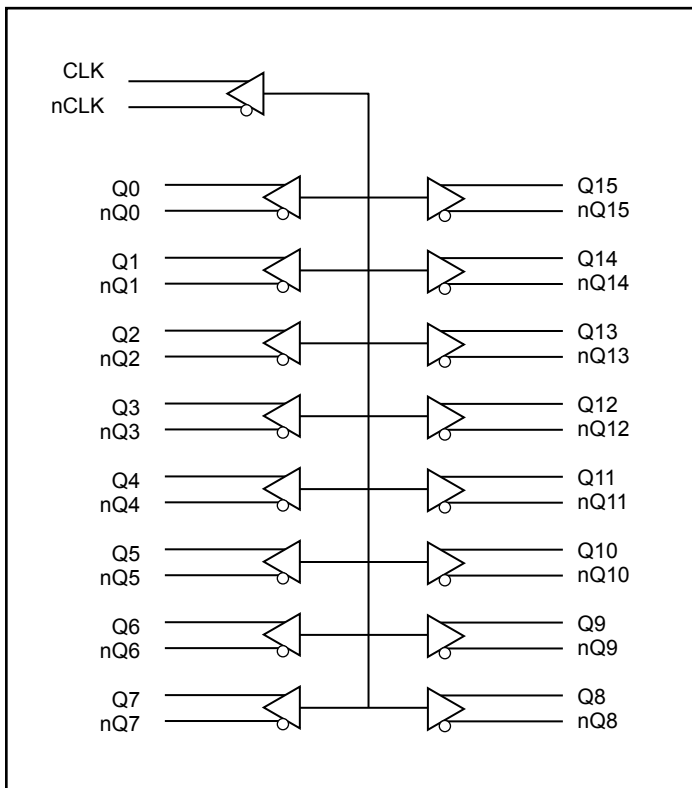
**Features**

- Low voltage operation  $V_{CC} = 3.3V$
- 1:16 fanout
- Differential input can accept the following: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Translates any single-ended input signal to 3.3V LVPECL levels with a resistor bias on nCLK input
- Pin-to-pin compatible to ICS8530-01
- Low Output skew: 75ps
- Part-to-part skew: 250ps
- Propagation Delay: 2ns
- Maximum output frequency: 500MHz
- 3.3V output operating supply
- Packaging (Pb-free & Green available):  
- 48-pin LQFP (FB)

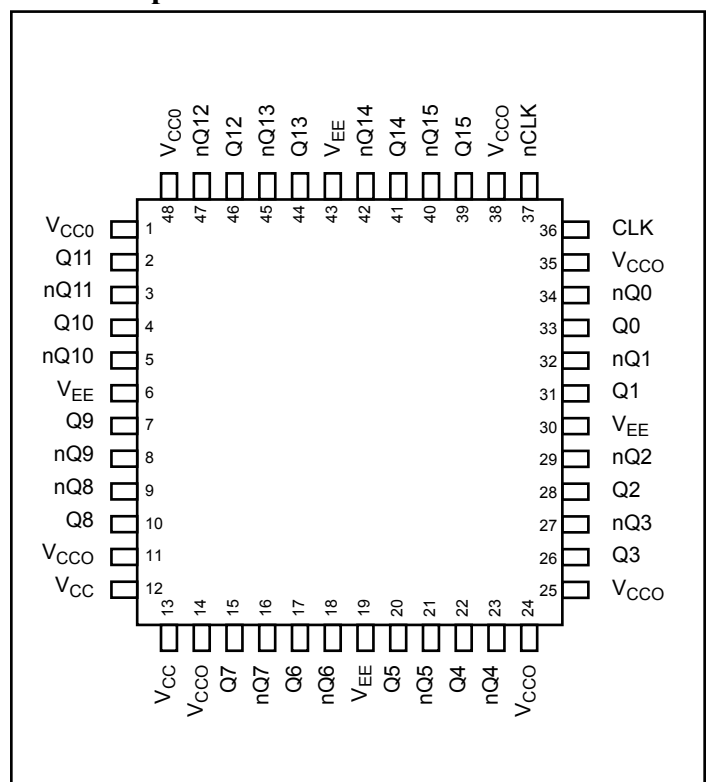
**Description**

The PI6C48530-01 is a high performance low skew LVPECL fanout buffer. PI6C48530-01 features a single differential LVPECL or LVDS or LVHSTL or SSTL or HCSL input, and sixteen 3.3V LVPECL outputs. The input can accept a single-ended signal with external bias circuit. The large fanout from a single input line reduces loading on input clock. PI6C48530-01 is ideal for both single-ended to LVPECL translations and/or LVPECL clock distribution. Typical applications are clock and signal distribution for data-communications and telecommunications.

**Block Diagram**



**Pin Description**



**Pin Description**

Name	Pin #	Type	Description
V <sub>CCO</sub>	1, 11, 14, 24, 25, 35, 38, 48	P	Output supply, connect to 3.3V
Q11, nQ11	2, 3	O	Differential output pair, 3.3V LVPECL interface level.
Q12, nQ12	4, 5	O	Differential output pair, 3.3V LVPECL interface level.
V <sub>EE</sub>	6, 19, 30, 43	P	Ground, connect to negative supply
Q9, nQ9	7, 8	O	Differential output pair, 3.3V LVPECL interface level.
Q8, nQ8	9, 10	O	Differential output pair, 3.3V LVPECL interface level.
V <sub>CC</sub>	12, 13	P	Core power supply, connect to 3.3V.
Q7, nQ7	15, 16	O	Differential output pair, 3.3V LVPECL interface level.
Q6, nQ6	17, 18	O	Differential output pair, 3.3V LVPECL interface level.
Q5, nQ5	20, 21	O	Differential output pair, 3.3V LVPECL interface level.
Q4, nQ4	22, 23	O	Differential output pair, 3.3V LVPECL interface level.
Q3, nQ3	26, 27	O	Differential output pair, 3.3V LVPECL interface level.
Q2, nQ2	28, 29	O	Differential output pair, 3.3V LVPECL interface level.
Q1, nQ1	31, 32	O	Differential output pair, 3.3V LVPECL interface level.
Q0, nQ0	33, 34	O	Differential output pair, 3.3V LVPECL interface level.
CLK	36	I_PD	Non-inverting differential clock input
nCLK	37	I_PU	Inverting differential clock input
Q15, nQ15	39, 40	O	Differential output pair, 3.3V LVPECL interface level.
Q14, nQ14	41, 42	O	Differential output pair, 3.3V LVPECL interface level.
Q13, nQ13	44, 45	O	Differential output pair, 3.3V LVPECL interface level.
Q12, nQ12	46, 47	O	Differential output pair, 3.3V LVPECL interface level.

**Notes:**

1. I = Input, O = Output, P = Power supply connection, I\_PD = Input with pull down, I\_PU = Input with pull up

**Pin Characteristics**

Symbol	Parameter	Conditions	Min	Typical	Max	Units
$C_{IN}$	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		K $\Omega$
R_pulldown	Input Pulldown Resistance			50		K $\Omega$

**Clock Input Function Table**

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; $V_{IN} = V_{CC}/2$	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; $V_{IN} = V_{CC}/2$	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; $V_{IN} = V_{CC}/2$	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; $V_{IN} = V_{CC}/2$	1	LOW	HIGH	Single Ended to Differential	Inverting

### Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CC}, V_{CCO}$	Supply voltage	Referenced to GND			4.6	V
$V_{IN}$	Input voltage	Referenced to GND	-0.5		$V_{CC} + 0.5V$	V
$V_{OUT}$	Output voltage	Referenced to GND	-0.5		$V_{CCO} + 0.5V$	V
$T_{STG}$	Storage temperature		-65		150	°C

#### Notes:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage		3	3.3	3.6	V
$V_{CCO}$	Output Power Supply		3	3.3	3.6	V
$T_A$	Ambient Temperature		0		70	°C
$I_{CC}$	Power Supply Current				120	mA

### Differential Inputs DC Characteristics

$T_A = 0^{\circ}C$  to  $70^{\circ}C$ ,  $V_{CC} = V_{CCO} = 3.0V$  to  $3.6V$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IH}$	Input High Current	nCLK	$V_{IN} = V_{CC} = 3.6V$		5	uA
		CLK	$V_{IN} = V_{CC} = 3.6V$		150	
$I_{IL}$	Input Low Current	nCLK	$V_{CC} = 3.6V, V_{IN} = 0V$	-150		
		CLK	$V_{CC} = 3.6V, V_{IN} = 0V$	-5		
$V_{PP}$	Peak-to-peak Voltage	CLK, nCLK	0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage <sup>(1,2)</sup>	CLK, nCLK	$V_{EE} + 0.05$		$V_{CC} - 0.85$	

#### Notes:

- For single ended applications, the maximum input voltage for CLK and nCLK is  $V_{CC} + 0.3V$
- Common mode voltage is defined as  $V_{IH}$ .

### LVPECL DC Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = V_{CCO} = 3.0\text{V}$  to  $3.6\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage <sup>(3,4)</sup>		$V_{CCO} - 1.4$		$V_{CCO} - 1.0$	V
$V_{OL}$	Output LOW Voltage <sup>(3,4)</sup>		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	
$V_{SWING}$	Peak-to-peak Output Voltage Swing		0.6		0.85	

#### Notes:

- The PI6C48530-01 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket, or mounted on a printed circuit board.
- Q0:Q15 and nQ0:nQ15 outputs are loaded with  $50\Omega$  to  $V_{CCO} - 2\text{V}$ .

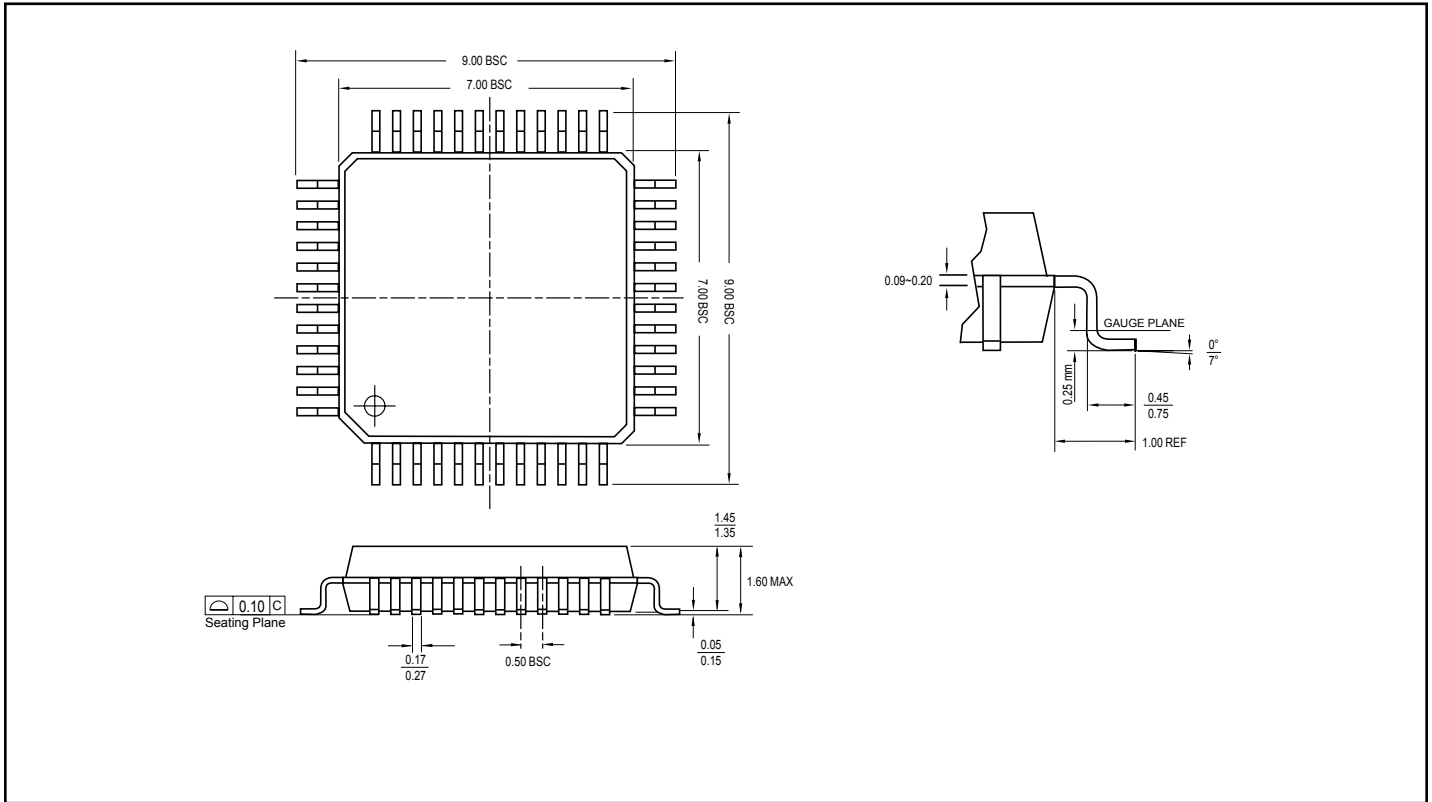
### AC Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = V_{CCO} = 3.0\text{V}$  to  $3.6\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{max}$	Output Frequency				500	MHz
$T_{pd}$	Propagation Delay <sup>(5)</sup>	$F \leq 500\text{MHz}$	1		2	ns
$T_{sk(o)}$	Output-to-output Skew <sup>(6,8)</sup>				75	ps
$T_{sk(pp)}$	Part-to-part Skew <sup>(7,8)</sup>			88	250	
$t_r/t_f$	Output Rise/Fall time	20% - 80% @ 50MHz	300		700	
$t_{dc}$	Output duty cycle		48		52	%

#### Notes:

- Measured from the differential input crossing point to the differential output crossing point
- Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
- Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
- This parameter is defined in accordance with JEDEC Standard
- All parameters are measured at 250MHz unless noted otherwise

**Package Mechanical: 48-pin LQFP (FB)**

**Ordering Information**

Ordering Code	Packaging Code	Package Type
PI6C48530-01FB	FB	48 pin LQFP
PI6C48530-01FBE	FB	Pb-free & Green, 48 pin LQFP

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)