

# SDIO101

## SD/SDIO/MMC/CE-ATA host controller

Rev. 03 — 11 March 2010

Product data sheet

## 1. General description

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The SDIO101 is a SD/SDIO/MMC/CE-ATA host controller with a standard 16-bit asynchronous memory interface. The device conforms to the *SD Host Standard Specification Version 2.0* (see [Ref. 1](#)). The SDIO101 manages the physical layer of SD, SDIO, MMC and CE-ATA protocols and can be used together with SD Host Standard compatible driver software to add SD/SDIO/MMC/CE-ATA host functionality to a variety of microprocessor systems.

The SDIO101 supports both full-speed (< 25 MHz) and high-speed (< 52 MHz) data transmissions on the SD/SDIO/MMC/CE-ATA port. The SDIO101 offers separate pins for SD/SDIO/MMC/CE-ATA port supply voltage, host interface supply voltage and core supply voltage. The SD/SDIO/MMC/CE-ATA port can operate at a wide voltage range (1.8 V to 3.6 V) which allows the device to interface to a large variety of SD, SDIO, MMC or CE-ATA devices. The SDIO101 allows 1-bit and 4-bit SD transactions and 8-bit MMC/CE-ATA transactions. The 16-bit asynchronous memory interface can operate at a 2.5 V to 3.6 V voltage range.

A built-in, 2 kB data buffer allows for a low interrupt latency time and efficient communication with the host processor at high data rates. The SDIO101 provides a DMA request line that can be connected to an external DMA controller to off-load the host processor and increase overall system performance.

An on-board PLL allows a large range of SD/SDIO/MMC/CE-ATA clock speeds to be generated from a single externally available clock source. An additional fractional divider allows the SD clock speed to be fine-tuned with very fine granularity, which enables the user to achieve the maximum desired SD clock speed from the external clock source.

The SDIO101 offers 5 levels of power saving, including a 'Hibernate mode' where the on-board oscillator, PLL and data buffer memories are switched off, and a 'Coma mode' in which supply power to most of the device is internally switched off. This allows the device to be used in very power-critical applications.

## 2. Features

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### 2.1 General

- Provides 1 SD/SDIO/MMC/CE-ATA slot, operating in 1-bit, 4-bit and 8-bit (MMC/CE-ATA) modes
- 2.5 V to 3.3 V host interface
- 1.8 V core supply voltage
- Separate SD supply voltage pin. SD/SDIO/MMC/CE-ATA slot is able to operate at a wide voltage range (1.8 V to 3.3 V).

- Compliant with *SDIO card specification version 2.00* (see [Ref. 2](#))
- Compliant with *SD Host Controller Standard Specification Version 2.0* (see [Ref. 1](#))
- Compliant with *SD Physical Layer Specification version 2.0* (see [Ref. 3](#))
- Compliant with *MMC Specification version 3.31 and 4.2* (see [Ref. 4](#))
- Supports CE-ATA Digital Protocol revision 1.1 (see [Ref. 5](#))
- Supports CE-ATA Digital Protocol commands (CMD60/CMD61)
- Dedicated SD Card Detection input pin (insertion/removal)
- Dedicated SD Card Write Protection input pin
- Full speed (< 25 MHz) and high-speed (< 52 MHz) SD data transmissions
- Supports interrupt and slave-DMA transfer operation
- Built-in 2 kB double data buffer (with 1 kB maximum block size) for efficient communication with host processor
- Supports SDIO features Multi-block, Suspend/Resume, Read Wait and Wake-up Control
- Up to 400 Mbit/s read and write data transfer rates at 50 MHz using MMC 8 data lines
- Up to 208 Mbit/s read and write data transfer rates at 52 MHz using SD 4 data lines
- On-board crystal oscillator and PLL
- 5 levels of power saving, including a 'Hibernate mode' where oscillator, PLL and memories are switched off, and a 'Coma mode' that internally switches off supply power to most of the chip
- Additional on-board fractional clock divider for fine-grained SD clock speed control
- Cyclic Redundancy Check (CRC) for command and data
- Programmable pull-up resistor on SD CMD and SD DATn lines
- Programmable drive strength for SDCLK output to optimize SD/SDIO/MMC/CE-ATA clock speed

## 2.2 Host processor interface

- Supports 16-bit asynchronous memory interface
- Separate host interface power supply pin, able to operate on 2.5 V to 3.3 V
- Programmable open collector or push-pull mode for  $\overline{\text{INT}}$  interrupt pin output

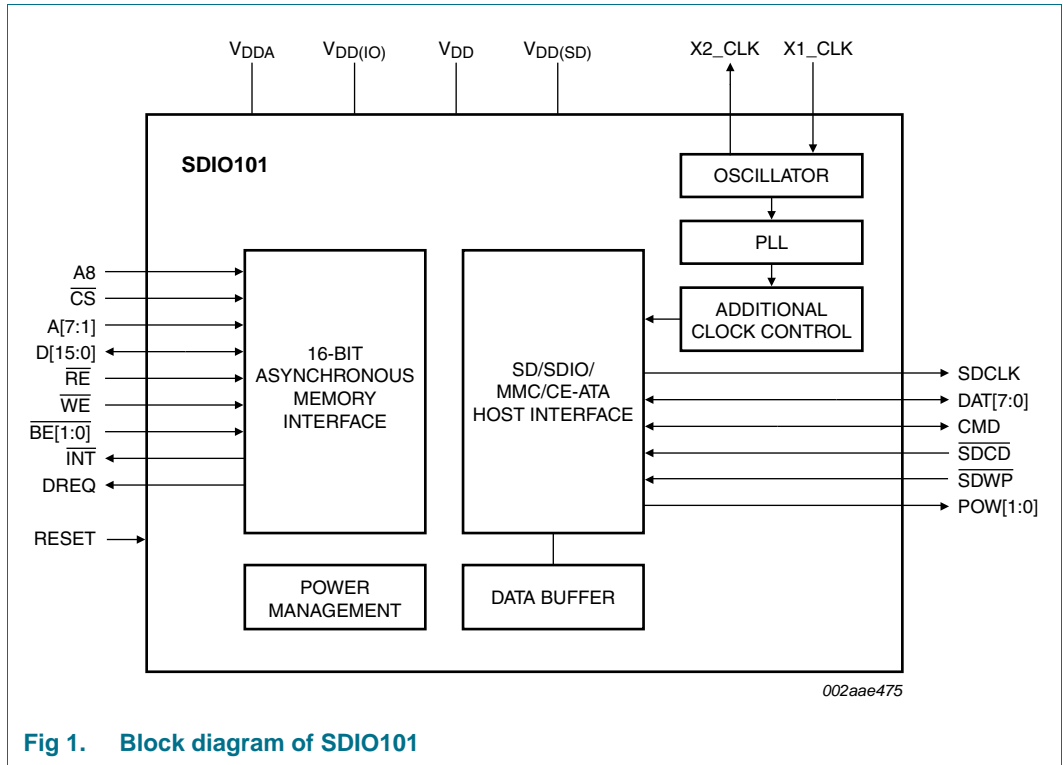
## 3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SDIO101IET <sup>[1]</sup>	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls; body 4 × 4 × 0.8 mm	SOT969-1
SDIO101IHR	HXQFN60U	plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLF based; body 5 × 5 × 0.5 mm	SOT1133-1

[1] Package approved for manufacture, but not currently available for standard ordering. Contact [interface.support.nxp.com](mailto:interface.support.nxp.com).

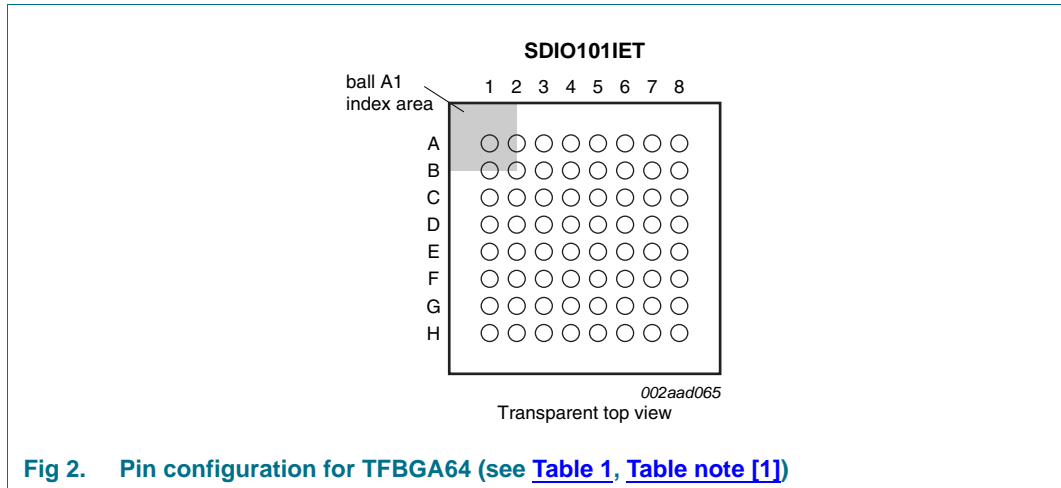
**4. Block diagram**



**Fig 1. Block diagram of SDIO101**

## 5. Pinning information

### 5.1 Pinning

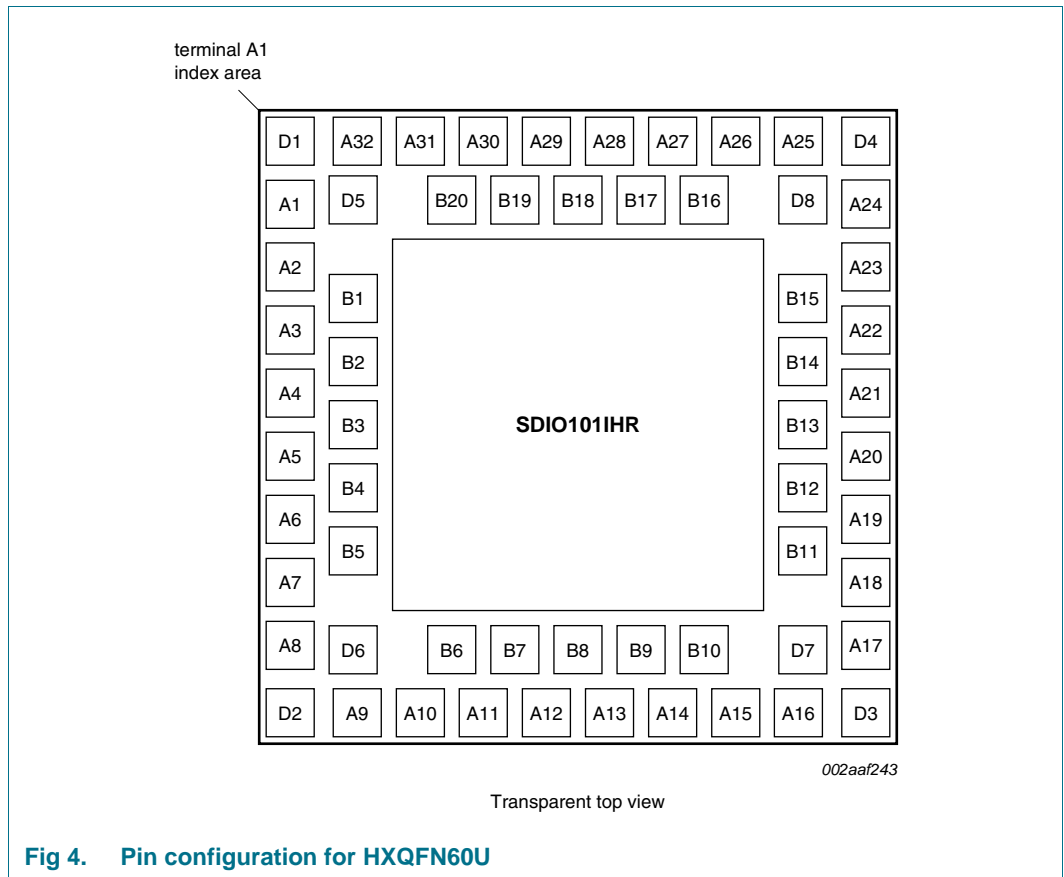


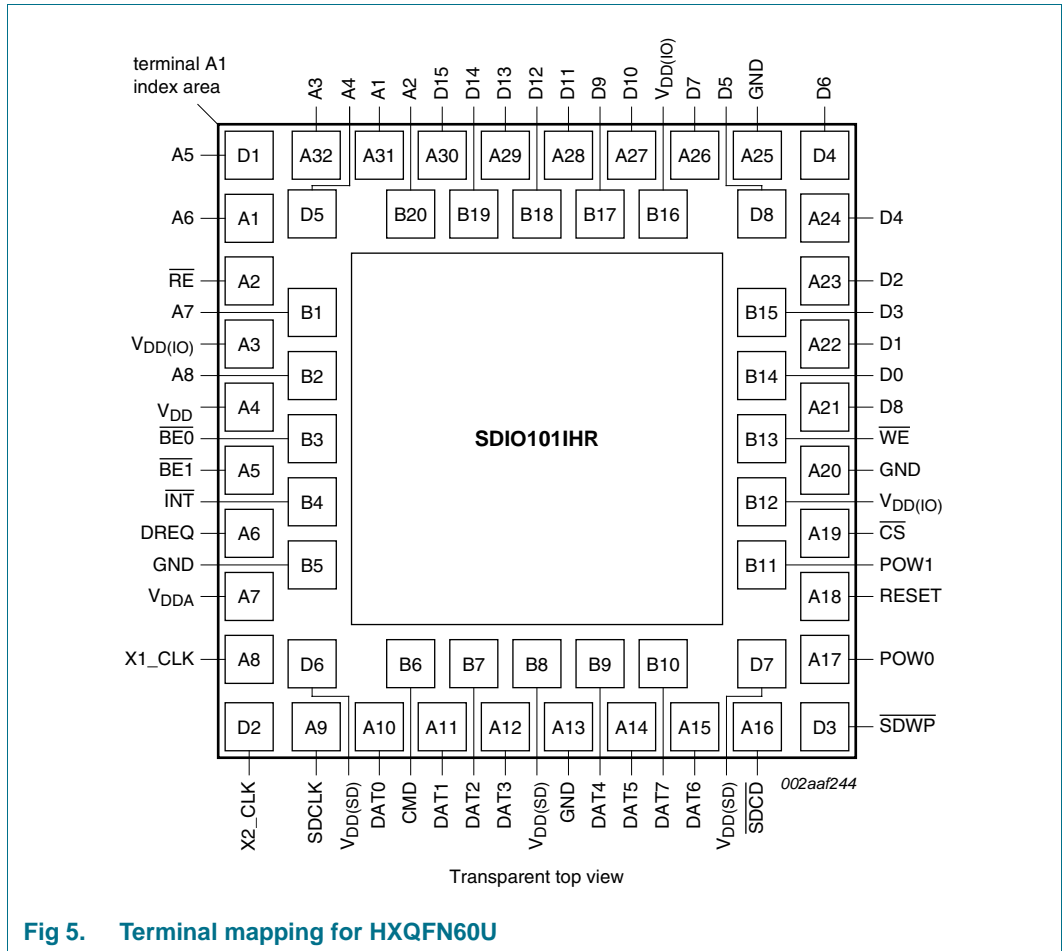
	1	2	3	4	5	6	7	8
A	A5	A3	D15	D13	D10	V <sub>DD(I/O)</sub>	D6	D4
B	A6	A4	A1	D14	D9	GND	D5	D2
C	$\overline{RE}$	A7	A2	D11	D7	D3	D1	D0
D	GND	A8	V <sub>DD(I/O)</sub>	D12	GND	GND	D8	$\overline{WE}$
E	$\overline{INT}$	$\overline{BE1}$	$\overline{BE0}$	V <sub>DD</sub>	DAT3	RESET	$\overline{CS}$	V <sub>DD(I/O)</sub>
F	DREQ	V <sub>DDA</sub>	GND	DAT0	V <sub>DD(SD)</sub>	DAT7	POW0	POW1
G	X1_CLK	X2_CLK	SDCLK	DAT1	DAT4	DAT6	V <sub>DD(SD)</sub>	GND
H	V <sub>DD(SD)</sub>	GND	CMD	DAT2	GND	DAT5	$\overline{SDCD}$	$\overline{SDWP}$

002aad064

Transparent top view.

**Fig 3. Ball mapping for TFBGA64 (see Table 1, Table note [1])**





## 5.2 Pin description

### 5.2.1 Pin description by function

Following are the signal descriptions on the SDIO101 interfaces. Pins are organized by function.

**Table 2. Pin description by function**

*B = bidirectional; I = input; O = output; n.c. = not connected.*

Symbol	Pin		Type	Description
	TFBGA64 <sup>[1]</sup>	HXQFN60U		
<b>SD/SDIO/MMC/CE-ATA interface signals</b>				
SDCLK	G3	A9	O	<b>SD clock output.</b> This output clock is driven by the host controller during read and write transactions.
CMD	H3	B6	B	<b>SD command line.</b> This bidirectional signal is used to transfer commands and responses between the host and the card.
DAT0	F4	A10	B	<b>SD Data bit 0.</b>
DAT1	G4	A11	B	<b>SD Data bit 1.</b>
DAT2	H4	B7	B	<b>SD Data bit 2.</b>
DAT3	E5	A12	B	<b>SD Data bit 3.</b>
DAT4	G5	B9	B	<b>SD Data bit 4.</b>
DAT5	H6	A14	B	<b>SD Data bit 5.</b>
DAT6	G6	A15	B	<b>SD Data bit 6.</b>
DAT7	F6	B10	B	<b>SD Data bit 7.</b>
SDCD	H7	A16	I	<b>SD card detect (active LOW).</b> This pin can be used to detect insertion and removal of SD/SDIO/MMC cards.
SDWP	H8	D3	I	<b>SD write protect (active LOW).</b> This pin can be used to detect if the inserted SD/SDIO/MMC card is write protected.
<b>System interface signals</b>				
X1_CLK	G1	A8	I	<b>Clock input.</b> Must be connected to the system clock which is used to generate the host bus interface (see <a href="#">Section 6.4.3.1</a> ).
X2_CLK	G2	D2	O	<b>Clock output.</b>
RESET	E6	A18	I	<b>Asynchronous reset (active HIGH).</b> This active HIGH input pin unconditionally resets the entire device.
<b>Card power supply control interface signals</b>				
POW[1:0]	F8, F7	B11, A17	O	<b>SD power supply control bits.</b> These bits can be used to control the voltage of an external power supply for the SD/SDIO/MMC/CE-ATA device. See <a href="#">Table 4</a> for details.

**Table 2. Pin description by function ...continued***B = bidirectional; I = input; O = output; n.c. = not connected.*

Symbol	Pin		Type	Description
	TFBGA64[1]	HXQFN60U		
<b>Host Interface control signals</b>				
$\overline{CS}$	E7	A19	I	<b>Chip Select (active LOW).</b>
A[7:1]	C2, B1, A1, B2, A2, C3, B3	B1, A1, D1, D5, A32, B20, A31	I	<b>Address lines.</b> Can be used to address the 256 bytes of the Standard Host register space.
A8	D2	B2	I	<b>Address 8.</b> When accessing SDIO101 transmit or receive buffer under DMA control, this pin must be HIGH. This pin must be LOW when accessing other registers or when accessing transmit or receive buffer under interrupt control.
D[15:0]	A3, B4, A4, D4, C4, A5, B5, D7, C5, A7, B7, A8, C6, B8, C7, C8	A30, B19, A29, B18, A28, A27, B17, A21, A26, D4, D8, A24, B15, A23, A22, B14	B	<b>Data lines.</b> Used to transfer data between host controller and the processor.
$\overline{RE}$	C1	A2	I	<b>Read Enable (active LOW).</b> Initiates a read transaction when active.
$\overline{WE}$	D8	B13	I	<b>Write Enable (active LOW).</b> Initiates a write transaction when active.
$\overline{BE}[1:0]$	E2, E3	A5, B3	I	<b>Byte write enables (active LOW).</b> When $\overline{BE}[0]$ is active, the least significant byte on the data bus can be written. When $\overline{BE}[1]$ is active, the most significant byte on the data bus can be written.
$\overline{INT}$	E1	B4	O	<b>Interrupt request (active LOW).</b> Can be configured as push/pull or open-collector output.
DREQ	F1	A6	O	<b>DMA request.</b>
<b>Power interface signals</b>				
V <sub>DD</sub>	E4	A4	-	<b>Core power supply pin, 1.8 V.</b>
V <sub>DDA</sub>	F2	A7	-	<b>Analog power supply, 1.8 V.</b>
V <sub>DD(SD)</sub>	F5, G7, H1	D6, B8, D7	-	<b>SD power supply pins, 1.8 V to 3.3 V.</b>
V <sub>DD(IO)</sub>	A6, D3, E8	B12, B16, A3	-	<b>Host interface power supply pins, 2.5 V to 3.3 V.</b>
GND	B6, D1, D5, D6, F3, G8, H2, H5	B5, A13, A20, A25	-	<b>Ground.</b>

[1] Refer to [Table 1](#), [Table note \[1\]](#).



## 6. Functional description

The SDIO101 offers the SD Standard Host register set as defined in the *SD Host Standard Specification Version 2.0* (see [Ref. 1](#)), through which the Host Driver software can configure the host controller and initiate transactions to and from an SD/SDIO/MMC/CE-ATA target. On top of the Standard Host registers, 4 extra registers are available in the Host Controller register space, which can be used to control the additional features in the SDIO101. These features are described in detail in [Section 6.4](#). [Section 6.2](#) gives an overview of the SDIO101 register set.

### 6.1 DMA mode

The SDIO101 supports slave DMA where the transferring of data between the host and the SDIO101 is under the control of the host's DMA controller. In this mode, the software can program DMA burst size (number of 16-bit words per DMA cycle) as well as the delay between back-to-back DMA requests from SDIO101.

In DMA mode, Buffer Data Port 0 (0x20) and Buffer Data Port 1 (0x22) are mapped differently than in Interrupt mode—address line A8 must be at logic 1 when Buffer Data Ports are being accessed while the rest of the address lines are ignored by the SDIO101. Once the DMA operation starts, all the accesses to the SDIO101 with A8 set to logic 1 will be considered as Buffer Data Ports access. To access other SDIO101 internal registers, address A8 must be set to logic 0.

The total number of DMA accesses to the Buffer Data Ports must be an even number. The first access from the host will be to Buffer Data Port 0, and the second access will be to Buffer Data Port 1. The SDIO101 will automatically alternate between Buffer Data Port 0 and Buffer Data Port 1 on each access by the host. This scheme allows the SDIO101 Buffer Data Ports to look like a continuous block of memory or FIFO to the DMA controller.

There are two registers that must be programmed for the SDIO101 to support DMA operation:

- Miscellaneous register (0xF8) bit 1 (enable slave DMA) must be set to logic 1.
- DMA burst size and DMA inter delay (back-to-back DREQs) must be programmed through DMA register (0xF4). DMA register bit [8:0] programs the DMA burst size (the number of 16-bit words to be transferred between the DMA controller and the SDIO101), and DMA register bit [15:9] programs the delay time between two back-to-back DMA requests from SDIO101 (the inter delay value in bit [15:9] represents the number of SD clocks).

#### 6.1.1 DMA read

When the receive buffer is empty, DREQ is at LOW state. Once the receive buffer has at least the number of 16-bit words equal to the programmed DMA burst size (DMA register [8:0]) DREQ goes HIGH. The DMA controller then can perform a block read of the receive buffer with the block size equal to the programmed DMA burst size in the DMA register.

The DREQ will go LOW once a block of data has been read from the SDIO101's receive buffer, and DREQ will remain LOW for a period defined by DMA register bit [15:9]. The DREQ signal will go HIGH again if the receive buffer still holds at least the burst size of 16-bit word data.

### 6.1.2 DMA write

When the transmit buffer is empty, DREQ is at HIGH state. The DMA controller then can perform a block write to the receive buffer with the block size equal to the programmed DMA burst size programmed in DMA register [9:0].

The DREQ will go LOW once a block of data has been written to the SDIO101's transmit buffer, and DREQ will remain LOW for a period defined by DMA register bit [15:9]. The DREQ signal will go HIGH again if the transmit buffer still has space to hold at least the burst size of 16-bit word data.

## 6.2 Standard Host register overview

**Table 3. SD Host Controller register map**

Offset	Bits 15:8	Bits 7:0	Offset	Bits 15:8	Bits 7:0
0x02	System Address (high)		0x00	System Address (low)	
0x06	Block Count		0x04	Block Size	
0x0A	Argument1		0x08	Argument0	
0x0E	Command		0x0C	Transfer Mode	
0x12	Response1		0x10	Response0	
0x16	Response3		0x14	Response2	
0x1A	Response5		0x18	Response4	
0x1E	Response7		0x1C	Response6	
0x22	Buffer Data Port1		0x20	Buffer Data Port 0	
0x26	Present State		0x24	Present State	
0x2A	Wake-up Control	Block Gap Control	0x28	Power Control	Host Control
0x2E	Software Reset	Time-out Control	0x2C	Clock Control	
0x32	Error Interrupt Status		0x30	Normal Interrupt Status	
0x36	Error Interrupt Status Enable		0x34	Normal Interrupt Status Enable	
0x3A	Error Interrupt Signal Enable		0x38	Normal Interrupt Signal Enable	
0x3E	reserved		0x3C	Auto CMD12 Error Status	
0x42	Capabilities		0x40	Capabilities	
0x46	Capabilities (reserved)		0x44	Capabilities (reserved)	
0x4A	Maximum Current Capabilities		0x48	Maximum Current Capabilities	
0x4E	Maximum Current Capabilities (reserved)		0x4C	Maximum Current Capabilities (reserved)	
0x52	(reserved)		0x50 <sup>[1]</sup>	IO-cell Configuration	
-	-		-	-	
0xF6 <sup>[1]</sup>	Secondary Clock Control		0xF4 <sup>[1]</sup>	DMA register	
0xFA <sup>[1]</sup>	PLL		0xF8 <sup>[1]</sup>	Miscellaneous	
0xFE	Host Controller Version		0xFC	Slot Interrupt Status	

[1] This register is not part of the Standard Host register set.

### 6.3 Standard Host register set description

The SDIO101 registers that are part of the Standard Host register set are described in detail in [Ref. 1](#). In this paragraph, we will only describe the specific implementation of the Standard register set in the SDIO101 that are different from [Ref. 1](#).

#### 6.3.1 System Address register (offset 0x00)

Since master-DMA functionality is not implemented, all bits in this register will always read zero. Writes to this register will be ignored.

#### 6.3.2 Block Size register (offset 0x04)

Data written to bits R[14:12] will be ignored. The maximum block size that can be programmed is 1 kB. Any block size higher than that will default to 1 kB.

#### 6.3.3 Transfer Mode register (offset 0x0C)

Since master-DMA functionality is not implemented, bit R[00] will always read zero. Writes to this bit will be ignored.

#### 6.3.4 Present State register (offset 0x24)

The SDIO101 supports multiple buffers, that is, the available data buffer space (2 kB) is larger than the Maximum Block Size (1 kB). The Buffer Write Enable bit R[10] indicates that there is room to write at least one more single block length (as specified in the Block Size register) in the data buffer even though previously-written blocks might still be present. Similarly, the Buffer Read Enable R[11] bit indicates that there is at least one single block length (as specified in the Block Size register) available in the data buffer.

#### 6.3.5 Host Control register (offset 0x28)

A separate LED control pin SDLD is **not** supported in the SDIO101. If desired, the user can use a GPIO pin on the Host Processor to implement this functionality. Bit R[00] in the Host Control register will always read zero, and writing to it will have no effect.

#### 6.3.6 Power Control register (offset 0x29)

Bits R[03:00] control the POW[1:0] pins of the SDIO101, which can be used to control an external power supply that powers the SD/SDIO/MMC/CE-ATA device. Two power modes are supported: 'normal' and 'low power'. It is up to the user to decide what voltage to associate with normal and low-power modes, but a typical implementation is 3.3 V for normal and 1.8 V for low power mode. [Table 4](#) shows the relation between the Power Control register and the POW[1:0] pins.

**Table 4. Relation between the Power Control register and the POW[1:0] pins**

Power Control register R[03:00]	POW[1:0]	Description
xxx0b	00b	SD power off
1011b	01b	SD low power (1.8 V) on
1101b	10b	SD normal power (3.3 V) on
1111b	10b	SD normal power (3.3 V) on

**6.3.7 Capabilities register (offset 0x40)**

The SDIO101 Capabilities register contents are shown in [Table 5](#).

**Table 5. Contents of the Capabilities register (offset 0x40)**

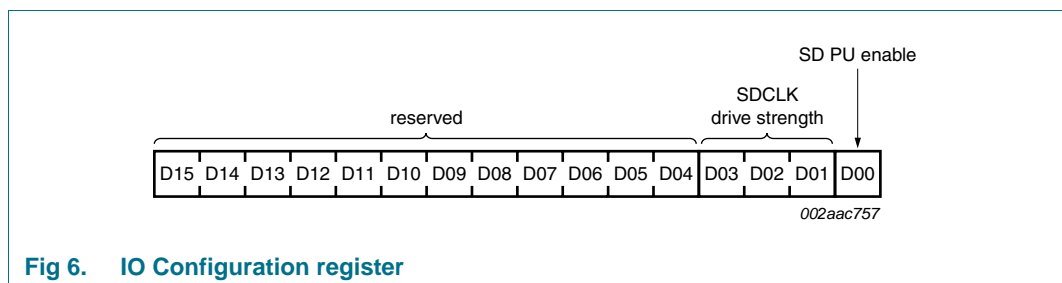
Location	Attribute	Default	Description
63:27	reserved	00h	reserved
26	R	1b	low voltage (1.8 V) supported
25	R	0b	3.0 V not supported (defaults to normal voltage)
24	R	1b	normal voltage (3.3 V) supported
23	R	1b	suspend/resume supported
22	R	0b	master DMA not supported
21	R	1b	high speed SD (> 25 MHz) supported
20:18	reserved	00h	reserved
17:16	R	01b	1 kB maximum block length
15:14	reserved	00h	reserved
13:08	R	00h	get info through other method ( <a href="#">Ref. 1</a> )
07	R	1b	time-out clock unit in MHz
06	reserved	0b	reserved
05:00	R	00h	get info through other method ( <a href="#">Ref. 1</a> )

**6.4 Additional register set description**

The additional registers are not part of the *SD Host Standard Specification Version 2.0* (see [Ref. 1](#)). These registers do not have to be initialized, so Standard Host Driver software does not have to be aware of them.

**6.4.1 IO Configuration register (offset 0x50)**

The IO Configuration register offers three bits to set the drive strength of the IO cell used for driving the SDCLK pin. This way the user can adjust SDCLK rise/fall times according to their system performance requirements. Typically, drive strength should be set to LOW when the SD slot is operating on normal (2.7 V to 3.3 V) voltage, and to HIGH when the SD slot is operating on low voltage (1.8 V). Also, a bit is offered to disable the default pull-up resistors on the SD CMD and SD DATn lines, in case they are not required and the possible leakage current through these resistors is undesired.



**Fig 6. IO Configuration register**

**Table 6. Contents of the IO Configuration register (offset 0x52)**

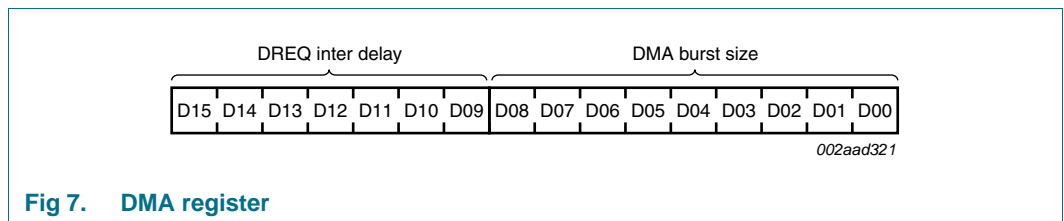
Location	Attribute	Default	Description
15:04	reserved	0h	reserved
03:01	R/W	3h	SDCLK drive strength select. These bits can be used to program the drive strength of the SDCLK IO cell. <a href="#">Table 7</a> shows the possible values.
00	R/W	0b	SD line pull-up. If set to b1, the internal pull-up resistors on the SD CMD and SD DATn lines are switched off.

**Table 7. SDCLK drive strength programming**

IO Configuration register R[03:01]	SDCLK drive strength
000b	low (SD operating on 2.7 V to 3.6 V)
0001b	reserved
010b	reserved
011b	reserved
100b	high (SD operating on 1.8 V)
101b	reserved
110b	reserved
111b	reserved

**6.4.2 DMA register (offset 0xF4)**

The DMA register is located in the Common register area. This register controls the DREQ output. The DREQ LOW and HIGH times are programmed with DMA inter delay and DMA burst size.



**Fig 7. DMA register**

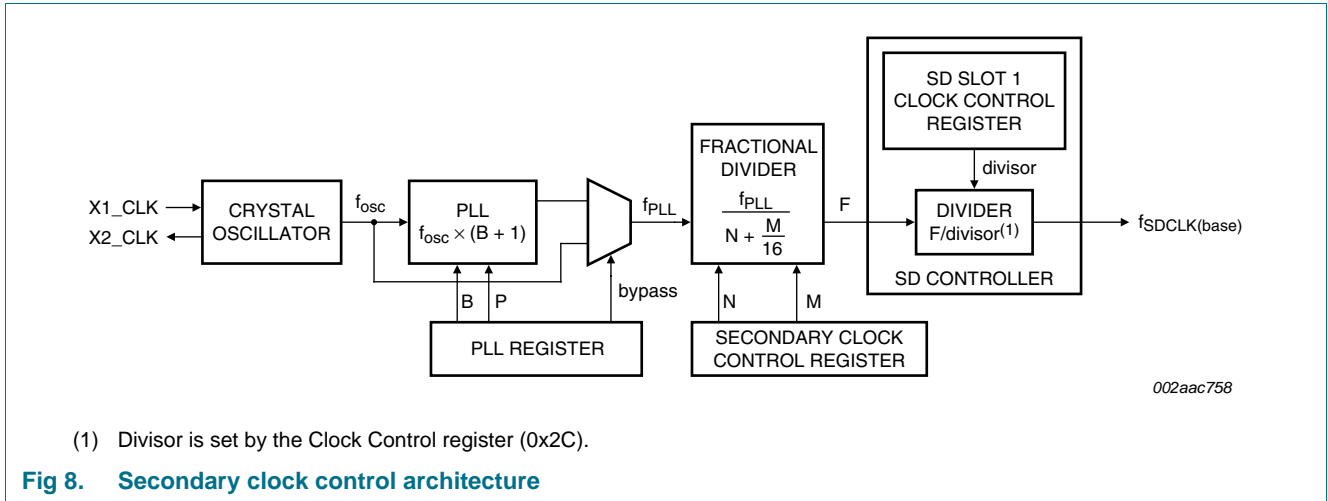
**Table 8. DREQ control programming**

Location	Attribute	Default	Description
15:09	R/W	0h	DREQ delay period (DREQ LOW time) LOW time = value × SD clock cycle time
08:01	R/W	0h	DMA burst size (DREQ HIGH time)

**Remark:** Refer to [Section 6.1](#) for more detailed DMA description.

6.4.3 Secondary Clock Control register (offset 0xF6)

The Secondary Clock Control register is located in the Common register area. This register gives the user more control over the clock generation. An additional fractional divider is offered to program the SDCLK base frequency with higher granularity, allowing the design to use an existing (available) clock rather than an external crystal or oscillator. Figure 8 shows the architecture of the secondary clock control.



The SDCLK base frequency can be calculated with Equation 1:

$$f_{SDCLK(base)} = \frac{f_{PLL}}{divisor \left( N + \frac{M}{16} \right)} \tag{1}$$

Where 'divisor' is the standard divisor as programmed in the Clock Control register; N is the integer divisor as programmed in the Secondary Clock Control register R[07:00]; M is the fractional divisor as programmed in the Secondary Clock Control register R[11:08]. Figure 9 and Table 9 below show the register bits of the Secondary Clock Control register.

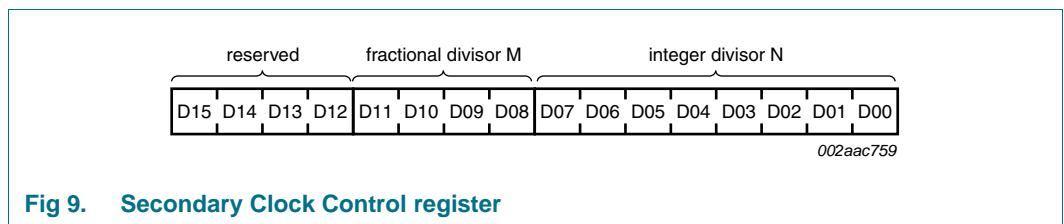


Table 9. Contents of the Secondary Clock Control register (offset 0xF6)

Location	Attribute	Default	Description
15:12	reserved	00h	reserved
11:08	R/W	00h	fractional divisor value M
07:00	R/W	01h	integer divisor value N

6.4.3.1 SDIO101 X1\_CLK input

The SDIO101 SD bus must be synchronized to the host processor read and write operations. The device is designed such that the X1\_CLK input must be connected to the processor's system clock (Figure 10). Or alternatively, the X1\_CLK can be connected to the processor crystal clock output (Figure 11). In either case, the SDIO101 internal PLL can be used to boost up the X1\_CLK input then divided down to the desired SDIO clock by using the internal divider in combination with the built-in fractional divider.

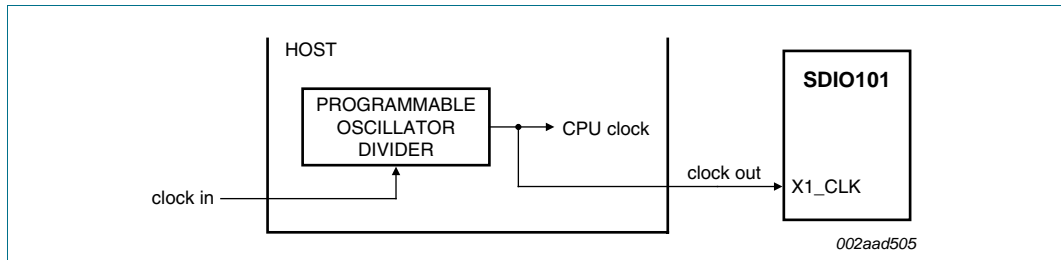


Fig 10. X1\_CLK connected to processor's system clock

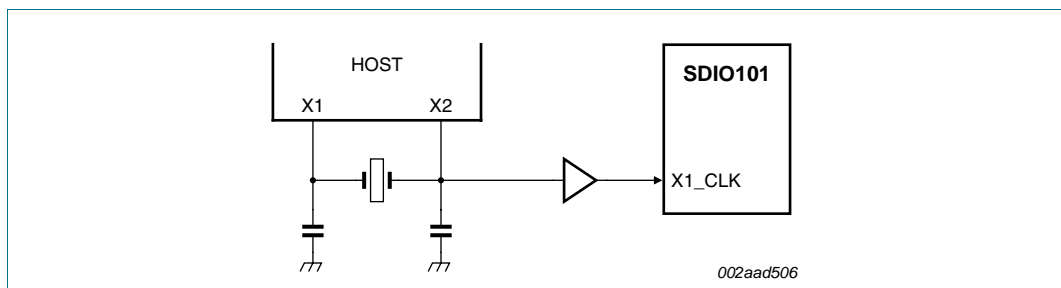


Fig 11. X1\_CLK connected to processor crystal clock output

Figure 12 details a typical scenario where the host processor uses a 13 MHz crystal as its clock source, and the same clock is used by the SDIO101 to operate the SD clock as close to 50 MHz as possible.

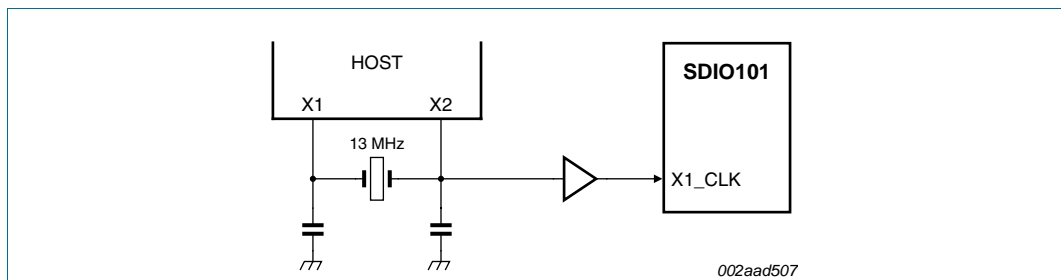


Fig 12. Host processor using 13 MHz crystal as clock source

With its input clock supplies by the processor crystal output, the SDIO101 internal PLL (0xFA) is used to boost the input frequency to 104 MHz, the standard Clock Control register (0x2C) and the fractional divider (0xF6) registers are then used to divide the 104 MHz to about 48.9 MHz to be used as SD clock.

PLL register (0xFA) settings:

- Bit 15 = 0b
- Bit 14 = 0b
- Bit [13:7] = 0000000b
- Bit [6:5] = 01b
- Bit [4:0] = 00111b; B = 7

Fractional divider (0xF6) settings:

- Bit [15:12] = 0000b; reserved bit
- Bit [11:8] = 0010b; M = 1
- Bit [7:0] = 00000001b; N = 1

Clock Control register (0x2C) settings:

- Bit [15:0] = 103h

$$f_{SDCLK(base)} = \frac{f_{PLL}}{divisor \left( N + \frac{M}{16} \right)}$$

$$= (13 \text{ MHz} \times 8) / (2 \times (1 + 2 / 16))$$

$$= 48.9 \text{ MHz}$$

#### 6.4.4 Miscellaneous register (offset 0xF8)

The Miscellaneous register is located in the Common register area. This register can be programmed to put the device in the ‘Coma mode’ or ‘Hibernate mode’, extra-low power-down modes on top of the Standby mode programmable through bit R[00] in the Clock Control register. Also, a bit is offered to disable the DREQ DMA request line on the Host Interface. Lastly, a bit is offered to switch between open-drain and push-pull mode for the  $\overline{\text{INT}}$  interrupt output pin. [Figure 13](#) and [Table 10](#) below show the register bits of the Miscellaneous register.

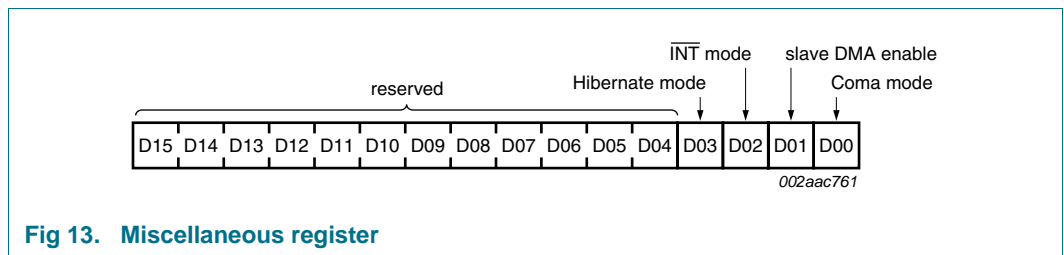


Fig 13. Miscellaneous register



**Table 10. Contents of the Miscellaneous register (offset 0xF8)**

Location	Attribute	Default	Description
15:03	reserved	00h	reserved
02	R/W	0b	INT mode select. When set to 0b, the $\overline{\text{INT}}$ interrupt output pin will be open-drain mode. An external 10 k $\Omega$ pull-up resistor is required in this case. When set to 1b, the INT interrupt output pin will be in push-pull mode.
01	R/W	1b	Slave DMA enable. If programmed to 1b, the DREQ signal will be functional. If programmed to 0b, the DREQ signal will be fixed to zero.
00	R/W	0b	Coma mode. If programmed to 1b, power will internally be switched off to most of the device, resulting in a very low coma mode current. All state in the device will be lost, and no registers can be read or written, with the exception of the 'Software Reset for All' bit in the Software Reset register. Setting this bit will re-instate power to the entire chip, and reset the SDIO101. A hard-reset on the RESET pin will also bring the device back out of Coma mode.

#### 6.4.5 PLL register (offset 0xFA)

The PLL register is located in the Common register area. This register provides control over the Phase-Locked Loop, which is used in the SDIO101 to generate an SD base clock frequency from the crystal oscillator or external clock source. The default values of this register are such that the PLL multiplies the incoming frequency from the crystal oscillator by 5. This means that, if the PLL register is not programmed, the frequency generated by the crystal oscillator or external clock source should be 10.4 MHz in order to generate the 52 MHz maximum SDCLK speed. For the SD base clock frequency generated by the PLL from the Crystal oscillator frequency it holds

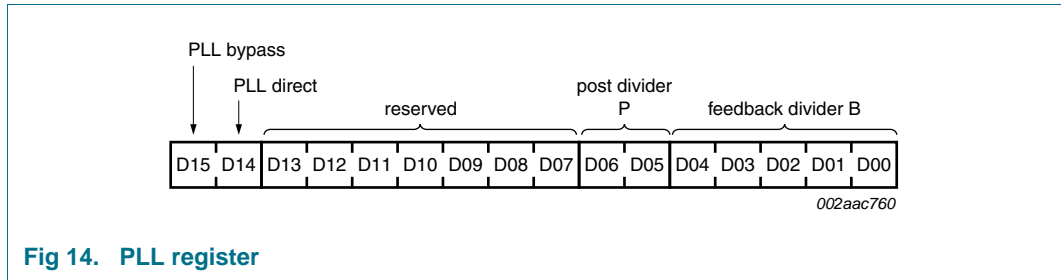
$$f_{PLL} = (B + 1) \times f_{CLK} \quad (2)$$

where B is the feedback divider value as programmed in R[04:00] of the PLL register. The user should determine the desired  $f_{PLL}$ , choose the required value B for the feedback divider based on the available clock source  $f_{osc}$ , and then choose a value for post divider P (as programmed in R[06:05]) such that the following condition gets satisfied:

$$156 \text{ MHz} < 2 \times (P + 1) \times f_{PLL} < 320 \text{ MHz} \quad (3)$$

The post divider setting decided by the value of P does not affect the frequency value (in MHz) of the  $f_{PLL}$ . The only advantage of this post divider is in adjusting the duty cycle of the resulting  $f_{PLL}$  clock. The greater the value of P, the closer the duty cycle will be to 50 % (provided the condition mentioned in [Equation 3](#) is not violated, for a guaranteed behavior).

The PLL register also provides the possibility to bypass the PLL post divider, effectively setting a value of 1 for P. Also, the user can bypass the entire PLL. [Figure 14](#) and [Table 11](#) show the register bits of the PLL register.



**Table 11. Contents of the PLL register (offset 0xFA)**

Location	Attribute	Default	Description
15	R/W	0b	PLL bypass. If this bit is 1b, the PLL is bypassed. The SDCLK base frequency is then equal to the frequency provided by the oscillator, either generated by a crystal or generated by an external clock. If this bit is 0b, the PLL is not bypassed.
14	R/W	0b	PLL direct. If this bit is 1b, the post divider of the PLL is bypassed, effectively setting the post divider value P to 1b. In this mode, the duty cycle out of the PLL can be unequal to 50 %. If set to 0b, the post divider P is used, and its value is determined by R[06:05] of the PLL register.
13:07	reserved	00h	reserved
06:05	R/W	01h	PLL post divider P
04:00	R/W	05h	PLL feedback divider B

**6.4.6 Host Controller Version register (offset 0xFE)**

The SDIO101 Host Controller version is shown in [Table 12](#).

**Table 12. Contents of the Host Controller Version register (offset 0xFE)**

Location	Attribute	Default	Description
15:08	R	01h	SDIO101 version 1.0
07:00	reserved	00h	reserved

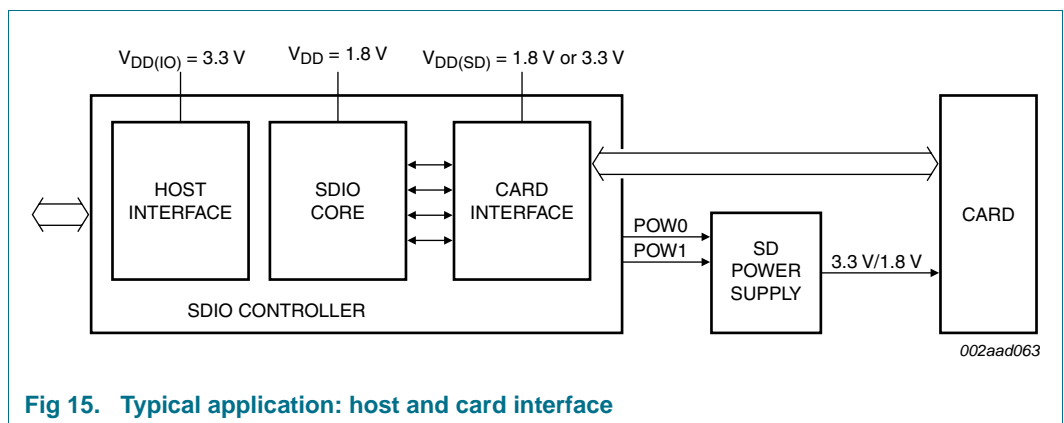
### 6.5 Power-saving modes

The SDIO101 provides 5 power-saving modes that can be used in different situations to minimize the power consumption of the device. [Table 13](#) below describes these modes and their associated register bits that can be programmed to enable them. Idle, Low Power and Standby modes can be used if card interrupts should still be serviced. The Hibernate mode will switch off the power to the SD device and the Coma mode switches off most of the Host Controller, therefore, card interrupts will not be generated. [Table 13](#) shows the 5 power-saving modes.

**Table 13. SDIO101 Power saving modes**

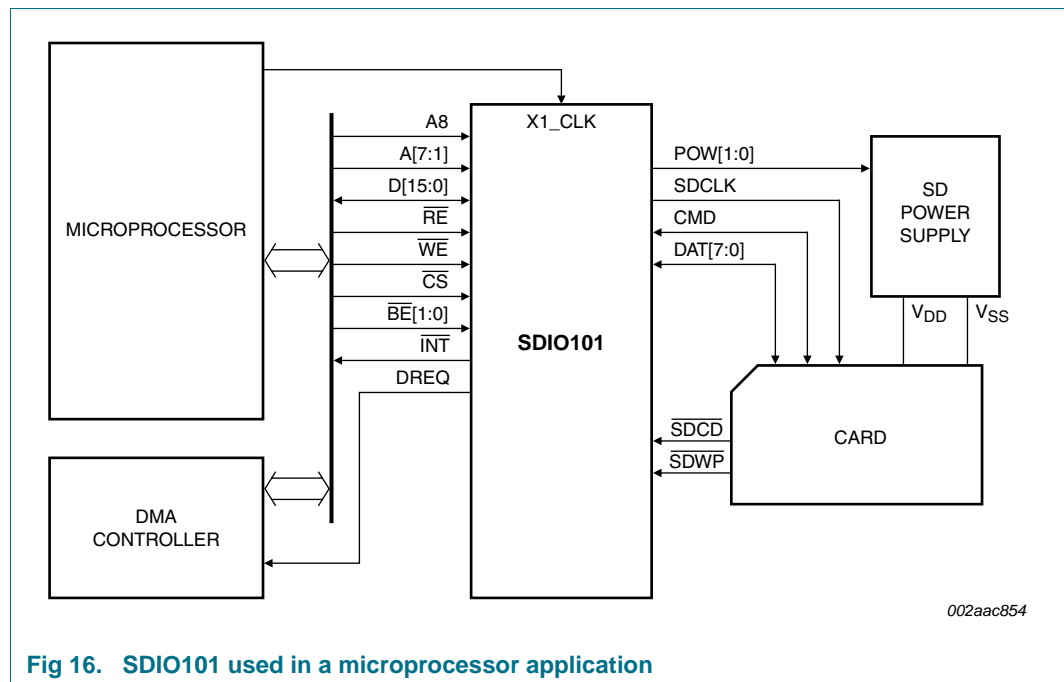
Mode	Associated register bits	Description
Idle mode	Clock Control register R[02]	SD Card clock stopped; oscillator and PLL is active.
Low Power mode	Power Control register R[00]	SD Card power switched off.
Standby mode	Clock Control register R[00]	When the Clock Control register R[00] is set to b0, the SDIO101 internal clock is stopped, the PLL is in Power-down mode, the oscillator is active and all register states are maintained. The device will still respond to card interrupts. When waking up from Standby mode, after writing a b1 in the Clock Control register R[00], the data buffer FIFO pointers will reset to empty.
Coma mode	Miscellaneous register R[00]	When the Miscellaneous register R[00] is set to b1, the SDIO101 internal power is switched off. All device pins are 3-stated, and only a write to the 'Software Reset for All' bit in the Software Reset register or a hard reset on the RESET pin will wake up the device. All device states, including data buffer contents, are lost. Card insertion and removal detection through the SDCD pin is disabled.
Hibernate mode	Miscellaneous register R[03]	The oscillator, PLL and supply to the buffer memory will be switched off. All states are maintained, but data buffer contents are lost. Upon wake-up, the data buffer FIFO pointers will reset to empty. Card insertion and removal detection through the SDCD pin is disabled.

## 7. Application design-in information



## 8. Basic architecture

The SDIO101 provides SD/SDIO/MMC/CE-ATA functionality to a microprocessor system as illustrated in [Figure 16](#). A standard SD/SDIO/MMC/CE-ATA driver running on the host processor will be able to access the standard host register set in the SDIO101 through the 16-bit memory interface, and initiate transactions to and from the SD card. An external SD power supply (controlled by the SDIO101) can be used to supply the SD card.



**Fig 16. SDIO101 used in a microprocessor application**

## 9. Limiting values

**Table 14. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(IO)}$	input/output supply voltage	host interface; in 2.5 V to 3.3 V range	-0.3	+4.6	V
$V_{DD(SD)}$	SD supply voltage	SD interface			
		in 1.8 V range	-0.3	+1.95	V
		in 3.3 V range	-0.3	+3.6	V
$V_{DD}$	supply voltage	core; 1.8 V range	-0.3	+2.4	V
$V_I$	input voltage	on any input pin			
		1.8 V interface	$V_{SS} - 0.3$	$V_{DD} + 0.6$	V
		3.3 V interface	-0.3	+3.6	V
$T_{amb}$	ambient temperature	operating	-40	+85	°C
$T_{stg}$	storage temperature		-65	+150	°C
$V_{ESD}$	electrostatic discharge voltage	SD/MMC/SDIO interface; Human Body Model	-4	+4	kV

## 10. Recommended operating conditions

**Table 15. Operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage	core	1.65	1.8	1.95	V
$V_{DD(IO)}$	input/output supply voltage	host interface	2.25	3.3	3.6	V
$V_{DD(SD)}$	SD supply voltage	SD interface	1.65	3.3	3.6	V
$f_{clk(ext)}$	external clock frequency		<a href="#">[1]</a> 1	-	52	MHz
$I_{DD(AV)}$	average supply current	$f = 13$ MHz; SDCLK = 25 MHz	-	6	-	mA
$I_{DD}$	supply current	Standby mode	-	460	-	μA
		Hibernate mode	-	69	-	μA
		Coma mode	-	5	-	μA
$T_{oper}$	operating temperature		-40	+25	+85	°C

[1] If the PLL is not bypassed, the minimum input frequency is 10 MHz.

## 11. Static characteristics

Table 16. Static characteristics

Symbol	Parameter	Conditions	$V_{DD(IO)} = 2.5\text{ V}$		$V_{DD(IO)} = 3.3\text{ V}$		Unit
			Min	Max	Min	Max	
$V_{IL(\text{clk})}$	clock LOW-level input voltage	X1_CLK [1]	-0.3	+0.6	-0.3	+0.6	V
$V_{IH(\text{clk})}$	clock HIGH-level input voltage	X1_CLK [1]	2.4	$V_{DD}$	2.4	$V_{DD}$	V
$V_{IL}$	LOW-level input voltage		-0.3	+0.65	-0.3	+0.8	V
$V_{IH}$	HIGH-level input voltage		1.6	$V_{DD}$	2.1	$V_{DD}$	V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 2\text{ mA}$	-	0.4	-	0.4	V
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -800\text{ }\mu\text{A}$	1.4	-	2.1	-	V
$I_{LIL}$	LOW-level input leakage current		-	10	-	10	$\mu\text{A}$
$I_{LIH}$	HIGH-level input leakage current		-	10	-	10	$\mu\text{A}$
$I_{L(\text{clk})}$	clock leakage current	X1_CLK	-	30	-	30	$\mu\text{A}$
$C_i$	input capacitance		-	5	-	5	pF
<b>Dynamic average supply current (<math>V_{DD(SD)} = 3.3\text{ V}</math>)</b>							
$I_{DD(AV)}$	average supply current	25 MHz [2]	-	7	-	7	mA
		52 MHz [2]	-	9	-	9	mA
$I_{DD(IO)}$	input/output supply current	25 MHz [3]	-	1.3	-	1.5	mA
		52 MHz [3]	-	1.3	-	1.5	mA
$I_{DD(SD)}$	SD supply current	25 MHz	-	1.5	-	1.5	mA
		52 MHz	-	2.3	-	2.3	mA
<b>Hibernate mode supply current (<math>V_{DD(SD)} = 3.3\text{ V}</math>)</b>							
$I_{DD}$	supply current		[2]	-	130	-	130 $\mu\text{A}$
$I_{DD(IO)}$	input/output supply current	25 MHz [3]	-	20	-	20	$\mu\text{A}$
$I_{DD(SD)}$	SD supply current		-	1.5	-	1.5	$\mu\text{A}$
<b>Standby mode supply current (<math>V_{DD(SD)} = 3.3\text{ V}</math>)</b>							
$I_{DD}$	supply current		[2]	-	4	-	4 mA
$I_{DD(IO)}$	input/output supply current		[3]	-	20	-	20 $\mu\text{A}$
$I_{DD(SD)}$	SD supply current		-	1.5	-	1.5	$\mu\text{A}$
<b>Coma mode supply current (<math>V_{DD(SD)} = 3.3\text{ V}</math>)</b>							
$I_{DD}$	supply current		[2]	-	0.6	-	0.6 $\mu\text{A}$
$I_{DD(IO)}$	input/output supply current		[3]	-	20	-	20 $\mu\text{A}$
$I_{DD(SD)}$	SD supply current		-	0.5	-	0.5	$\mu\text{A}$

[1] X1\_CLK = 3.3 V only.

[2]  $I_{DD}$  is the supply on  $V_{DD}$  and  $V_{DDA}$ .

[3]  $I_{DD(IO)}$  current might be higher or lower depending on the activity of the 16-bit data bus. The numbers specified in the data sheet are measured with no activity on the host controller bus. The data bus, address bus and control signals are pulled HIGH.

## 12. Dynamic characteristics

Table 17. Dynamic characteristics for 16-bit host bus interface

Symbol	Parameter	Conditions	$V_{DD(IO)} = 2.5\text{ V}$		$V_{DD(IO)} = 3.3\text{ V}$		Unit
			Min	Max	Min	Max	
$t_{WL(X1\_CLK)}$	X1_CLK pulse width LOW		9	-	9	-	ns
$t_{WH(X1\_CLK)}$	X1_CLK pulse width HIGH		9	-	9	-	ns
$f_{X1\_CLK}$	frequency on pin X1_CLK		-	52	-	52	MHz
$t_{su(A)}$	address set-up time		5	-	5	-	ns
$t_{h(A)}$	address hold time		10	-	5	-	ns
$t_{h(WE-CS)}$	hold time from $\overline{WE}$ to $\overline{CS}$		0	-	0	-	ns
$t_{d(CSL-WEL)}$	delay time from $\overline{CS}$ LOW to $\overline{WE}$ LOW		0	-	0	-	ns
$t_{w(WE)}$	$\overline{WE}$ pulse width		10	-	20	-	ns
$t_{d(WE)}$	$\overline{WE}$ delay time		10	-	20	-	ns
$t_{su(D-WEH)}$	set-up time from data input to $\overline{WE}$ HIGH		5	-	5	-	ns
$t_{h(WEH-D)}$	data input hold time after $\overline{WE}$ HIGH		5	-	5	-	ns
$t_{su(BEn)}$	set-up time on pin $\overline{BEn}$		5	-	5	-	ns
$t_{h(BEn)}$	hold time on pin $\overline{BEn}$		5	-	5	-	ns
$t_{h(RE-CS)}$	hold time from $\overline{RE}$ to $\overline{CS}$		0	-	0	-	ns
$t_{d(CS-RE)}$	delay time from $\overline{CS}$ to $\overline{RE}$		0	-	0	-	ns
$t_{w(RE)}$	$\overline{RE}$ pulse width		25	-	20	-	ns
$t_{d(RE)}$	$\overline{RE}$ delay time		10	-	10	-	ns
$t_{d(RE-Q)}$	delay time from $\overline{RE}$ to data output	25 pF load	-	20	-	25	ns
$t_{dis(RE-QZ)}$	disable time from $\overline{RE}$ to high-impedance data output	25 pF load	-	20	-	15	ns
$t_{w(RESET)}$	pulse width on pin RESET		10	-	5	-	ns
$t_{d(buf\_full-INTL)}$	delay time from buffer full to $\overline{INT}$ LOW	receive buffer (receive)	-	4XTAL1	-	4XTAL1	ns
$t_{d(int\_clr-INTH)}$	delay time from interrupt clear to $\overline{INT}$ HIGH	receive buffer (read)	-	300	-	300	ns
$t_{d(buf\_emp-INTL)}$	delay time from buffer empty to $\overline{INT}$ LOW	transmit buffer (transmit)	-	4XTAL2	-	4XTAL2	ns
$t_{d(int\_clr-INTH)}$	delay time from interrupt clear to $\overline{INT}$ HIGH	transmit buffer (write)	-	80	-	80	ns
$t_{su(A8)}$	address 8 set-up time		5	-	5	-	ns
$t_{su(A8-CS)}$	set-up time from address 8 to $\overline{CS}$		5	-	5	-	ns
$t_{d(SDCLK-DREQH)}$	delay time from SDCLK to DREQ HIGH		-	20	-	15	ns
$t_{d(CSH-DREQ)W}$	write delay time from $\overline{CS}$ HIGH to DREQ LOW		-	20	-	15	ns
$t_{d(CSH-DREQ)R}$	read delay time from $\overline{CS}$ HIGH to DREQ LOW		-	20	-	15	ns

**Table 18. Dynamic characteristics for MMC/SD/SDIO bus interface** $V_{DD(SD)} = 2.7\text{ V to }3.3\text{ V}$ .

Symbol	Parameter	Conditions	25 MHz		52 MHz		Unit
			Min	Max	Min	Max	
<b>Clock</b>							
t <sub>WL</sub>	clock low time	10 pF max.	12	-	8	-	ns
t <sub>WH</sub>	clock high time	10 pF max.	12	-	8	-	ns
t <sub>w(clk)</sub>	clock pulse width	10 pF max.	40	-	18	-	ns
t <sub>TLH</sub>	clock rise time	10 pF max.	-	10	-	3	ns
t <sub>THL</sub>	clock fall time	10 pF max.	-	10	-	3	ns
<b>Input CMD, DATn</b>							
t <sub>ISU</sub>	input set-up time	10 pF max.	5	-	6	-	ns
t <sub>IH</sub>	input hold time	10 pF max.	5	-	2	-	ns
<b>Output CMD, DATn</b>							
t <sub>ODLY</sub>	output delay time	during data transfer mode; 40 pF max.	0	14	-	14	ns
t <sub>OH</sub>	output hold time		2.5	-	2.5	-	ns

**Table 19. Dynamic characteristics for MMC/SD/SDIO bus interface** $V_{DD(SD)} = 1.70\text{ V to }1.95\text{ V}$ .

Symbol	Parameter	Conditions	25 MHz		52 MHz		Unit
			Min	Max	Min	Max	
<b>Clock</b>							
t <sub>WL</sub>	clock low time	10 pF max.	12	-	8	-	ns
t <sub>WH</sub>	clock high time	10 pF max.	12	-	8	-	ns
t <sub>w(clk)</sub>	clock pulse width	10 pF max.	40	-	18	-	ns
t <sub>TLH</sub>	clock rise time	10 pF max.	-	10	-	3	ns
t <sub>THL</sub>	clock fall time	10 pF max.	-	10	-	3	ns
<b>Input CMD, DATn</b>							
t <sub>ISU</sub>	input set-up time	10 pF max.	5	-	6	-	ns
t <sub>IH</sub>	input hold time	10 pF max.	5	-	2	-	ns
<b>Output CMD, DATn</b>							
t <sub>ODLY</sub>	output delay time	during data transfer mode; 40 pF max.	0	14	-	14	ns
t <sub>OH</sub>	output hold time		2.5	-	2.5	-	ns



12.1 Timing diagrams

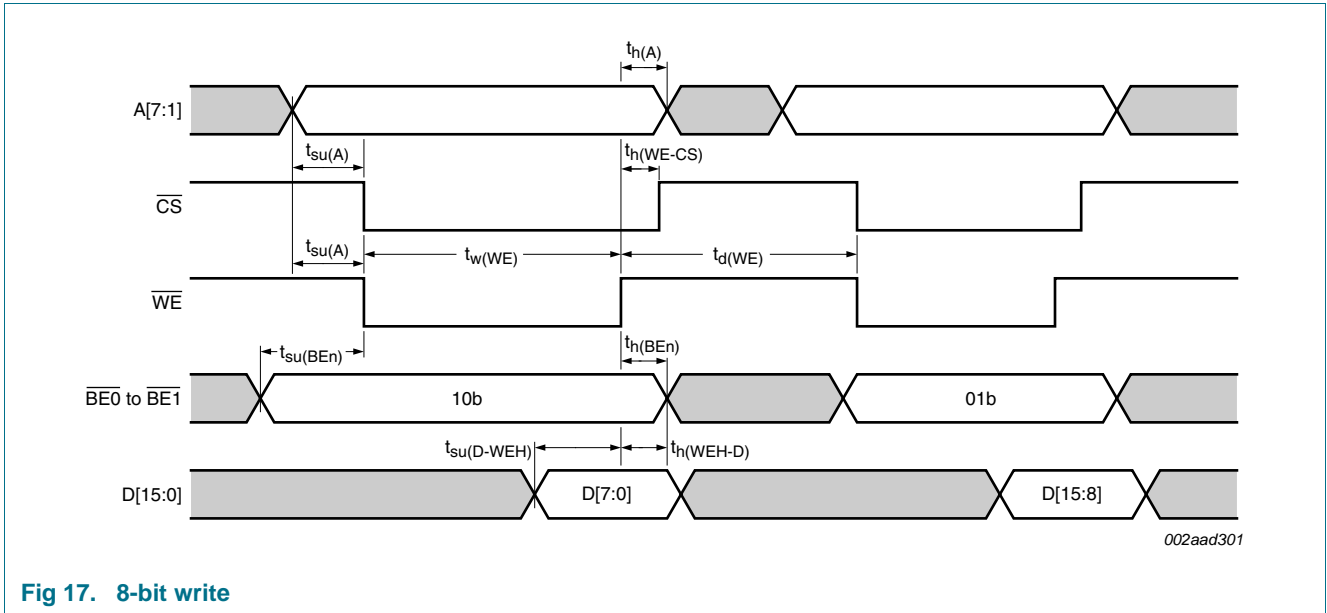


Fig 17. 8-bit write

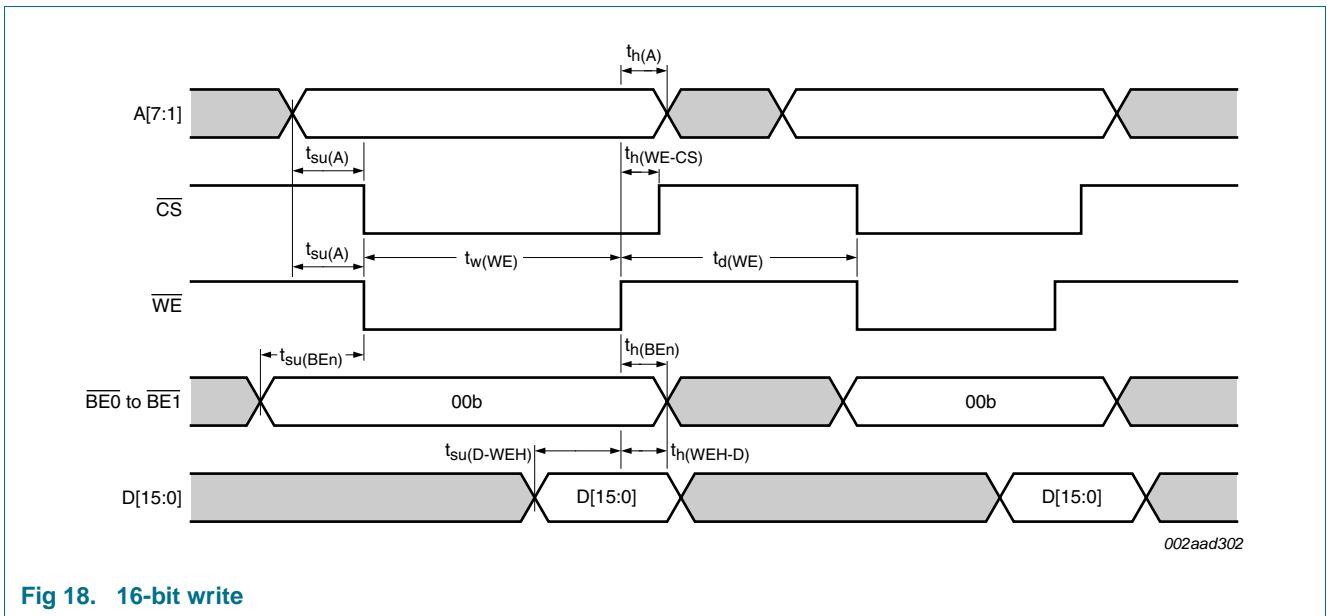


Fig 18. 16-bit write

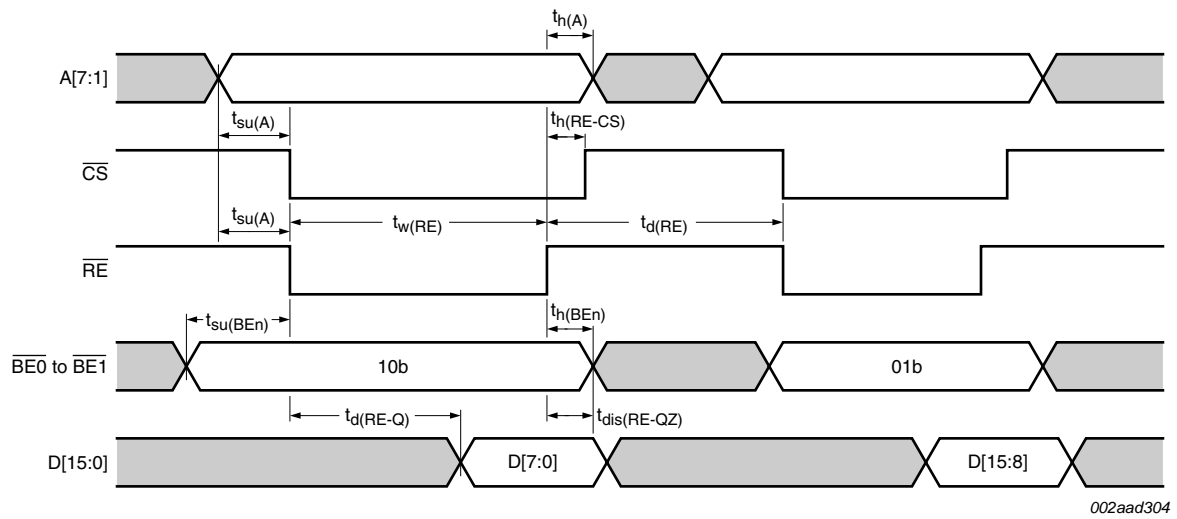


Fig 19. 8-bit read

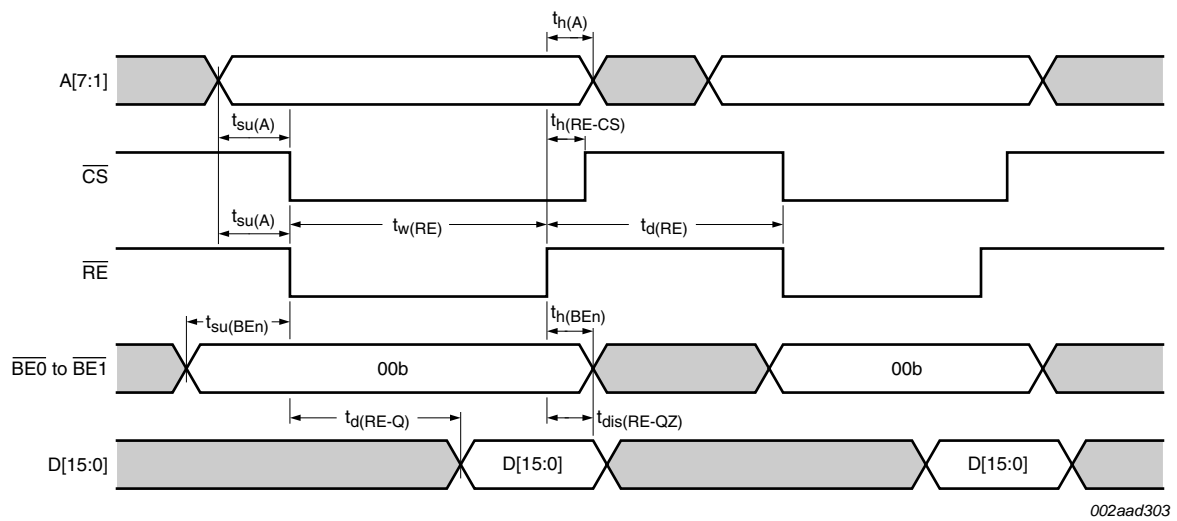


Fig 20. 16-bit read

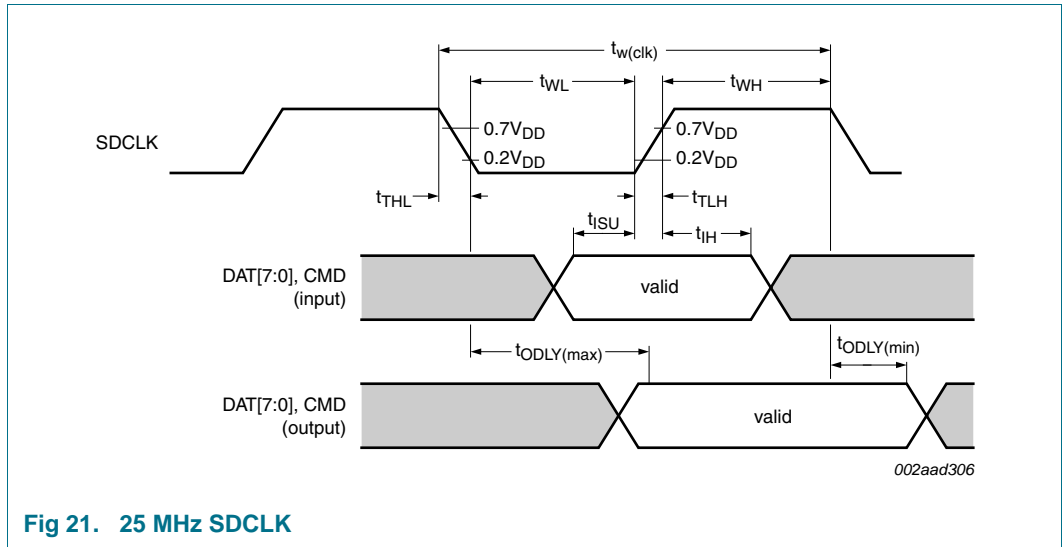


Fig 21. 25 MHz SDCLK

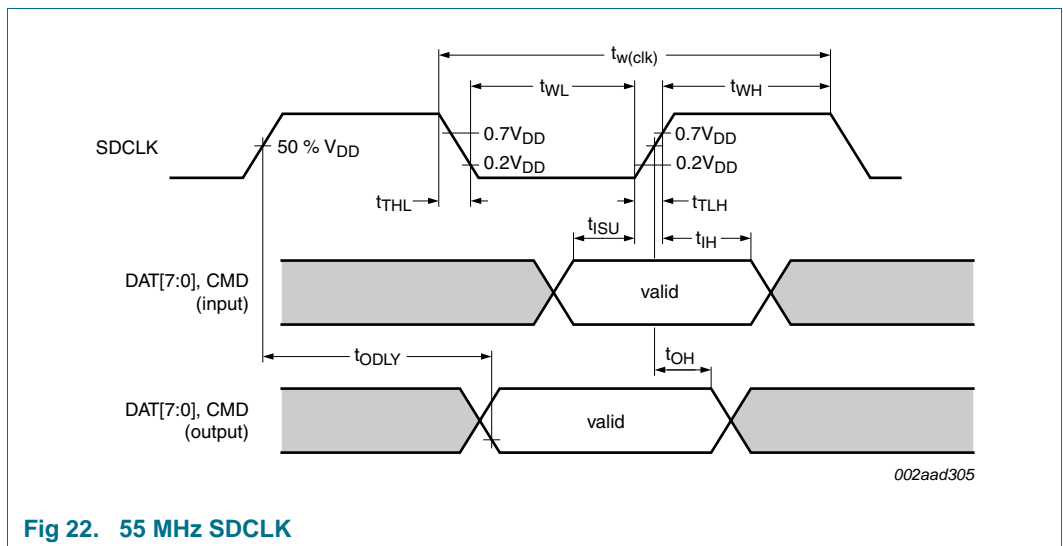


Fig 22. 55 MHz SDCLK

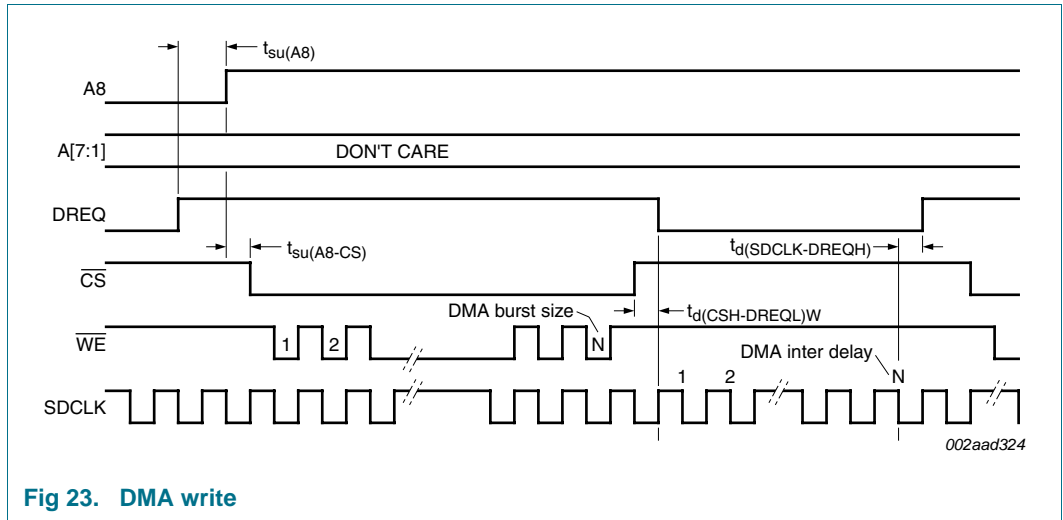


Fig 23. DMA write

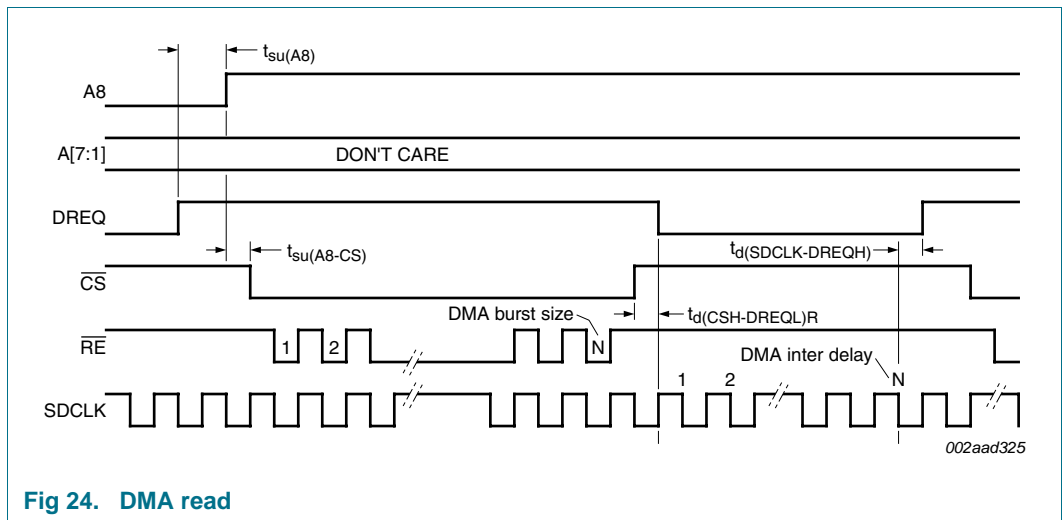


Fig 24. DMA read

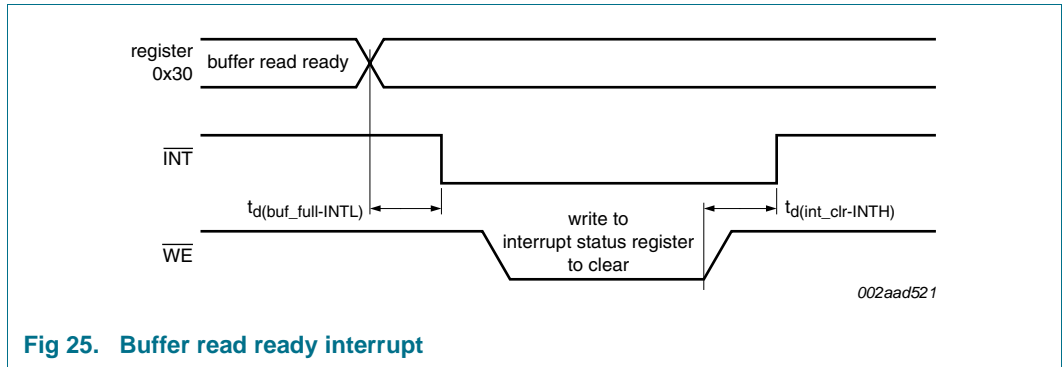


Fig 25. Buffer read ready interrupt

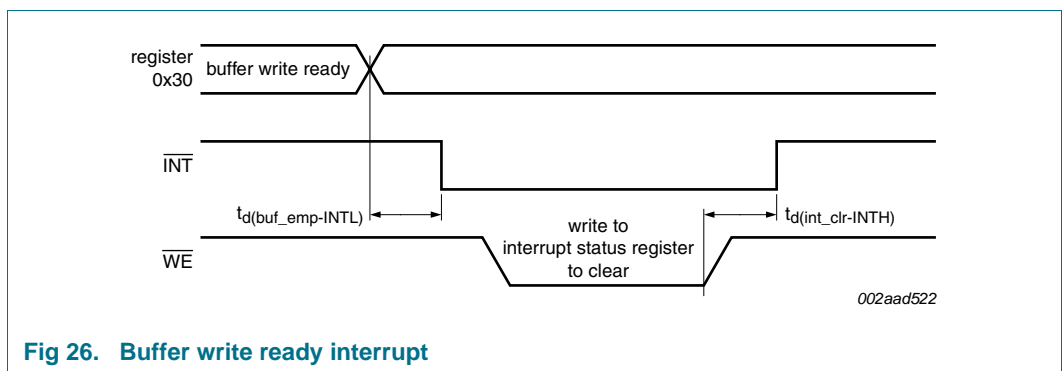


Fig 26. Buffer write ready interrupt

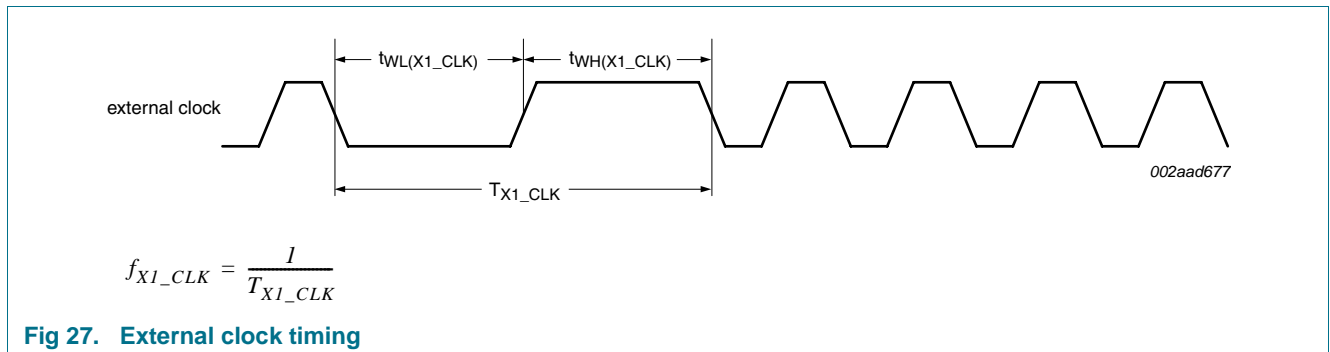


Fig 27. External clock timing

13. Package outline

TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls; body 4 x 4 x 0.8 mm

SOT969-1

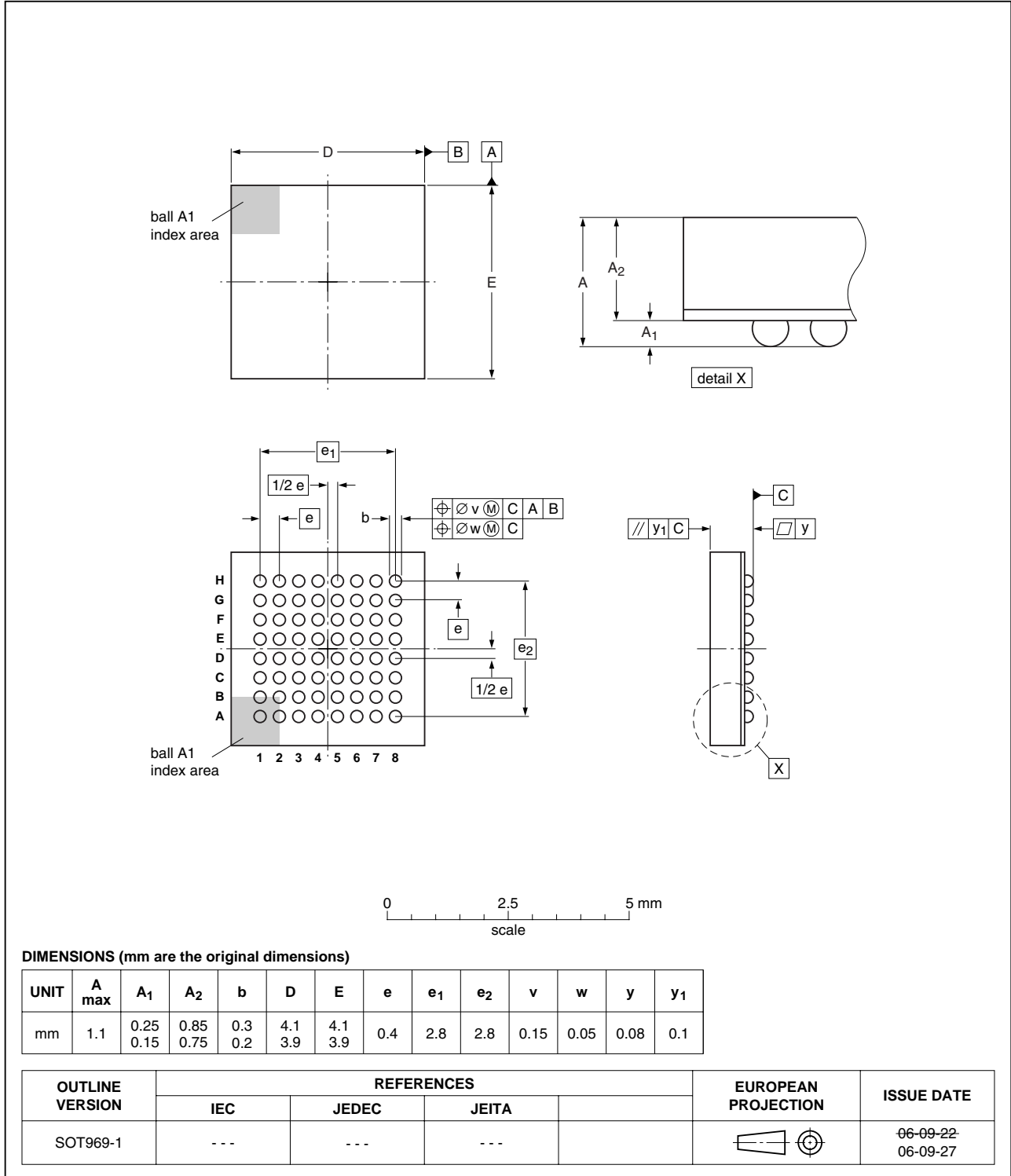


Fig 28. Package outline SOT969-1 (TFBGA64); see Table 1, Table note [1]

HXQFN60U: plastic thermal enhanced extremely thin quad flat package; no leads; 60 terminals; UTLP based; body 5 x 5 x 0.5 mm

SOT1133-1

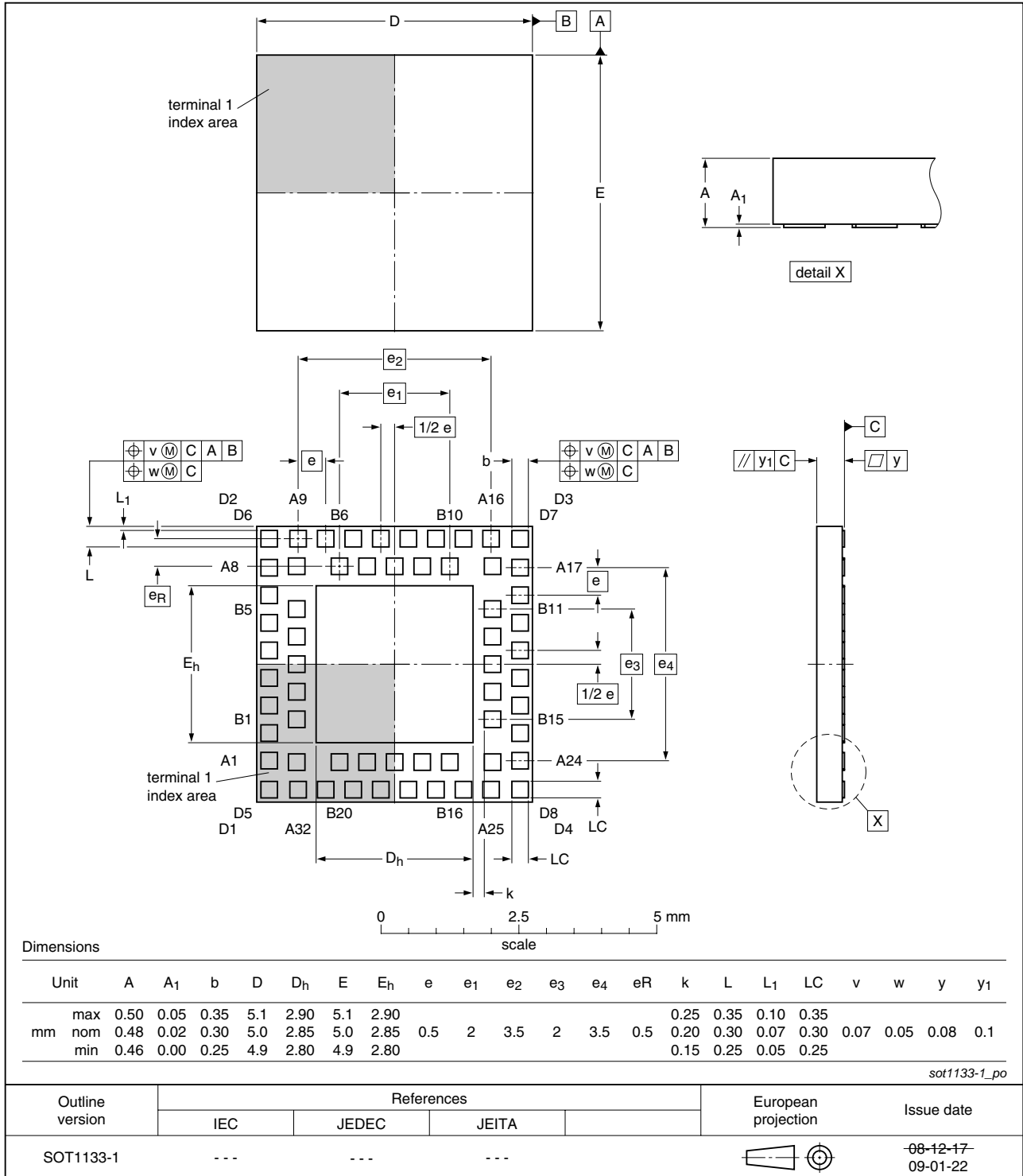


Fig 29. Package outline SOT1133-1 (HXQFN60U)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities



## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 30](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 20](#) and [21](#)

**Table 20. SnPb eutectic process (from J-STD-020C)**

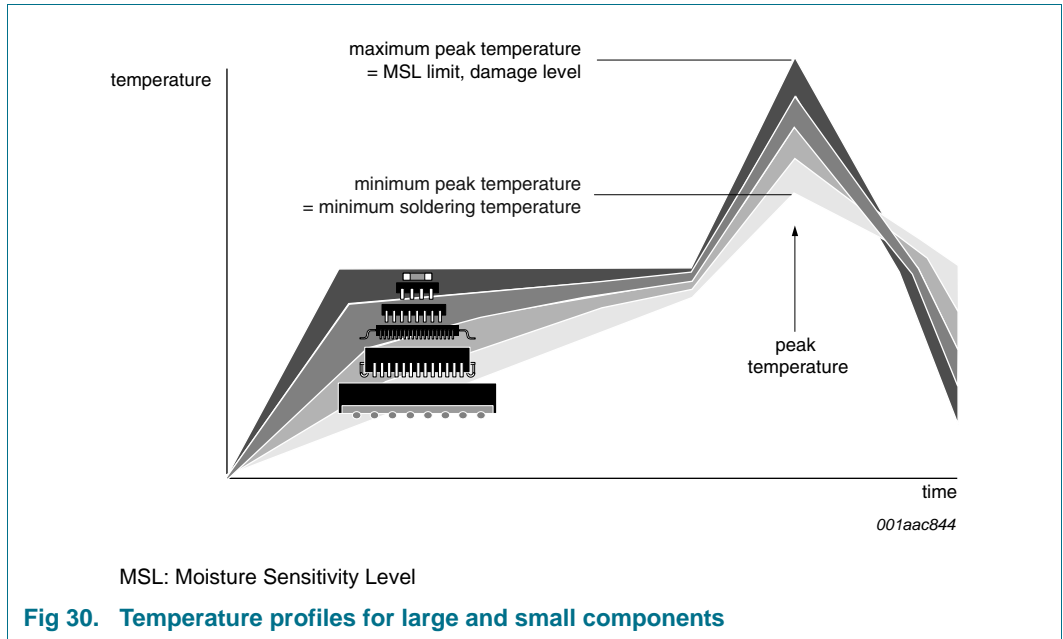
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 21. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 30](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15. Appendix

### 15.1 Errata added 2010-01-07

This errata describes the functional behavior deviation of the SDIO101 from the data sheet Rev. 01.

#### 15.1.1 Card detection in Hibernate mode or Coma mode

Card detection does not work when the device is in Coma mode or Hibernate mode. When put in these modes, the SDIO101 SD supply is powered down. When a card is inserted, the card detection circuit won't be able to detect the card because there is no power.

**Workaround:** If the card is to be put in Hibernate mode or Coma mode, a processor's GPIO pin with a pull-up resistor can be used to do card detect function. The pin is to be programmed as input, and set to interrupt on both edges. When a card is inserted, this GPIO pin will be pulled LOW by the card and an interrupt is generated. When a card is removed, this GPIO pin will be pulled HIGH by the pull-up resistor and an interrupt is generated.

#### 15.1.2 16-bit host interface synchronization

Due to a design synchronization requirement between the host and the SDIO, an external crystal cannot be used as a clock source for the SDIO101. Random interrupt lockups sometimes occur during data read and write to the SDIO101 internal buffers when an external crystal is used between X1\_CLK and X2\_CLK pins.

**Workaround:** A workaround solution is to use one of the processor's clocks as the input clock for the SDIO101 (see data sheet [Section 6.4.3.1](#) for more detail).

#### 15.1.3 SD side data rate limitation at 1.8 V

The current device does not work at 52 MHz when the  $V_{DD(SD)}$  supply is at 1.8 V. When powered at 1.8 V, the SD side works up to about 30 MHz. (Please note that when  $V_{DD(SD)}$  is 2.5 V to 3.3 V, there is no data rate limitation and the device works up to 52 MHz).

**Workaround:** There is no known workaround solution for this issue, if the card is to be used at 52 MHz with 1.8 V supply. To run the card at 52 MHz,  $V_{DD(SD)}$  must be powered at 2.5 V minimum.

#### 15.1.4 High current on $V_{DD}$ pin after power-up

After power-up,  $V_{DD}$  pin draws close to 2 mA then the current slowly drops down to the idle current state at 68  $\mu$ A in about 40 seconds. This issue does not have any effect on the normal operation of the device, and the high current only occurs just after the device is powered up.

**Workaround:** We are investigating this issue to find out what might cause this problem. And, since the issue does not alter the behavior of the device and a root cause has not been identified, there is not a workaround for this issue at this time.

## 16. Abbreviations

Table 22. Abbreviations

Acronym	Description
CE-ATA	Consumer Electronics Advanced Technology Attachment
CPU	Central Processing Unit
DMA	Direct Memory Access
FIFO	First In, First Out
GPIO	General Purpose Input/Output
IO	Input/Output
kB	kiloByte
LED	Light Emitting Diode
MMC	Multi-Media Card
PLL	Phase-Locked Loop
PU	Pull-Up
SD	Secure Digital
SDIO	Secure Digital Input/Output

## 17. References

- [1] *SD Specifications Part A2, SD Host Controller Standard Specification, Version 2.00*, February 2007
- [2] *SD Specifications Part E1, SDIO Specification, Version 2.00*, February 8, 2007
- [3] *SD Specifications Part 1, Physical Layer Specification, Version 2.0*, May 9, 2006
- [4] *The Multimedia Card, System Specification Version 4.1*
- [5] *CE-ATA Digital Protocol, Version 1.1*

## 18. Revision history

Table 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SDIO101_3	20100311	Product data sheet	-	SDIO101_2
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 1 “Ordering information”</a>:               <ul style="list-style-type: none"> <li>– Removed type number SDIO101IHE (HUQFN60U, SOT1008-1).</li> <li>– Added type number SDIO101IHR (HXQFN60U, SOT1133-1).</li> </ul> </li> <li>• <a href="#">Figure 4 “Pin configuration for HXQFN60U”</a> replaces (old) “Pin configuration for HUQFN60U”.</li> <li>• <a href="#">Figure 5 “Terminal mapping for HXQFN60U”</a> replaces (old) “Terminal mapping for HUQFN60U”.</li> <li>• <a href="#">Table 2 “Pin description by function”</a>: 3<sup>rd</sup> column’s heading changed from “HUQFN60U” to “HXQFN60U”.</li> <li>• <a href="#">Figure 29 “Package outline SOT1133-1 (HXQFN60U)”</a> replaces (old) “Package outline SOT1008-1 (HUQFN60U)”.</li> </ul>			
SDIO101_2	20100119	Product data sheet	-	SDIO101_1
Modifications:	<ul style="list-style-type: none"> <li>• Added errata <a href="#">Section 15 “Appendix”</a>.</li> </ul>			
SDIO101_1	20090924	Product data sheet	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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