

MOSFETs Silicon N-Channel MOS (DTMOS II)

TK40J60U

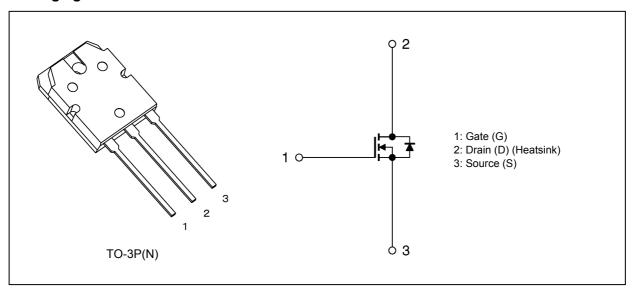
1. Applications

• Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 0.065 \Omega$ (typ.)
- (2) High forward transfer admittance: $|Y_{fs}| = 30 \text{ S (typ.)}$
- (3) Low leakage current: $I_{DSS} = 100 \mu A \text{ (max) (V}_{DS} = 600 \text{ V)}$
- (4) Enhancement mode: $V_{th} = 3.0 \text{ to } 5.0 \text{ V } (V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA})$

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	600	V
Gate-source voltage		V_{GSS}	±30	
Drain current (DC)	(Note 1)	I _D	40	Α
Drain current (pulsed)	(Note 1)	I _{DP}	80	
Power dissipation $(T_c = 25^{\circ}C)$		P _D	320	W
Single-pulse avalanche energy	(Note 2)	E _{AS}	540	mJ
Avalanche current		I _{AR}	20	Α
Repetitive avalanche energy	(Note 3)	E _{AR}	32	mJ
Channel temperature		T _{ch}	150	°C
Storage temperature		T _{stg}	-50 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R _{th(ch-c)}	0.39	°C/W
Channel-to-ambient thermal resistance	R _{th(ch-a)}	50	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 2.36 mH, R_G = 25 Ω , I_{AR} = 20 A

Note 3: Repetitive rating; pulse width limited by maximum channel temperature

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



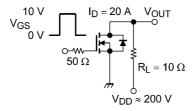
6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	_		±1	μΑ
Drain cut-off current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	_	_	100	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	600	_		V
Gate threshold voltage	V_{th}	V _{DS} = 10 V, I _D = 1 mA	3.0	_	5.0	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 20 A	_	0.065	0.08	Ω
Forward transfer admittance	Y _{fs}	V _{DS} = 10 V, I _D = 20 A	7.5	30		S

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 0.1 MHz	_	3400	_	pF
Reverse transfer capacitance	C _{rss}		_	180	_	
Output capacitance	C _{oss}		_	7800	_	
Switching time (rise time)	t _r	See Figure 6.2.1.	_	60	_	ns
Switching time (turn-on time)	t _{on}		_	120	_	
Switching time (fall time)	t _f		_	13	_	
Switching time (turn-off time)	t _{off}		_	160		



 $Duty \leq 1\%, \ t_W = 10 \ \mu s$

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$	_	55	_	nC
Gate-source charge	Q_{gs}		_	37	_	
Gate-drain charge	Q_{gd}			18	_	

6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (DC)	(Note 1)	I _{DR}	_	_	_	40	Α
Reverse drain current (pulsed)	(Note 1)	I _{DRP}	_	_	_	80	
Diode forward voltage		V _{DSF}	I _{DR} = 40 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time		t _{rr}	I _{DR} = 40 A, V _{GS} = 0 V	_	520	_	ns
Reverse recovery charge		Q _{rr}	-dI _{DR} /dt = 100 A/μs	_	13	_	μС



7. Marking (Note)

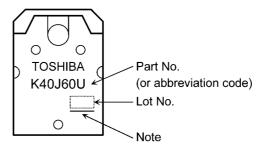


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS

compatibility of Product.

The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on

the restriction of the use of certain hazardous substances in electrical and electronic equipment.

8. Characteristics Curves (Note)

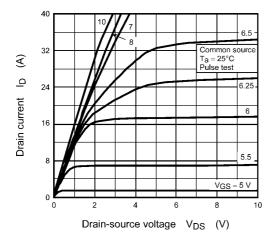


Fig. 8.1 $I_D - V_{DS}$

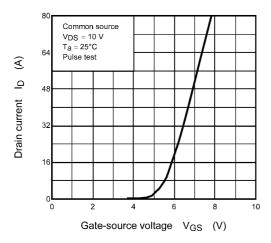


Fig. 8.3 I_D - V_{GS}

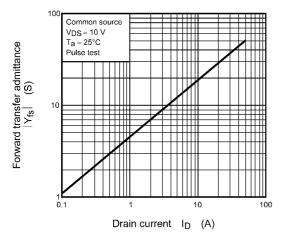


Fig. 8.5 |Y_{fs}| - I_D

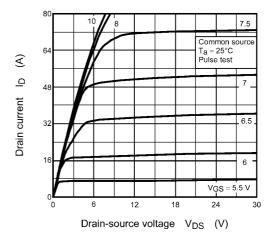


Fig. 8.2 I_D - V_{DS}

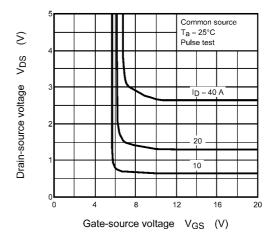


Fig. 8.4 V_{DS} - V_{GS}

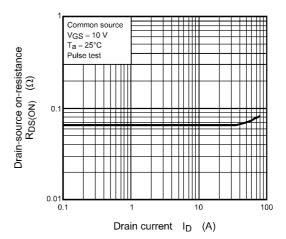


Fig. 8.6 R_{DS(ON)} - I_D

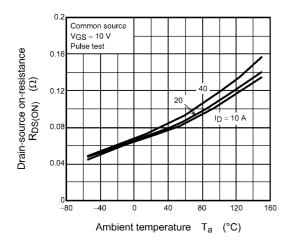


Fig. 8.7 R_{DS(ON)} - T_a

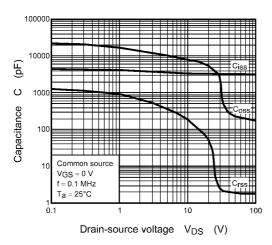


Fig. 8.9 C - V_{DS}

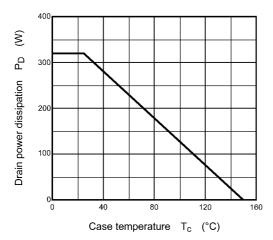


Fig. 8.11 P_D - T_c (Guaranteed Maximum)

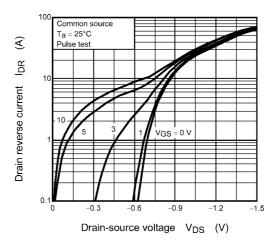


Fig. 8.8 I_{DR} - V_{DS}

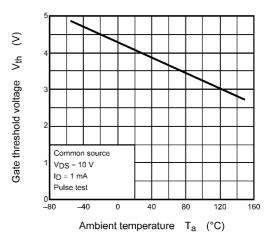


Fig. 8.10 V_{th} - T_a

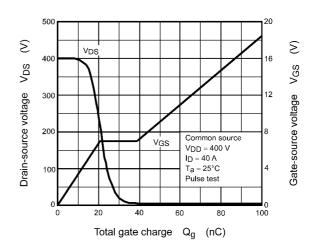


Fig. 8.12 Dynamic Input/Output Characteristics

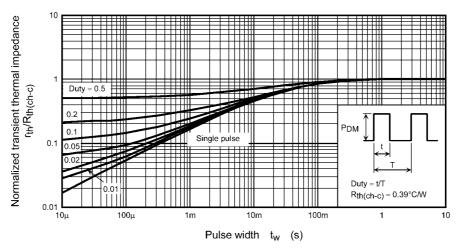


Fig. 8.13 $r_{th}/R_{th(ch-c)} - t_w$ (Guaranteed Maximum)

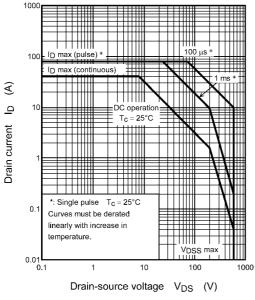


Fig. 8.14 Safe Operating Area (Guaranteed Maximum)

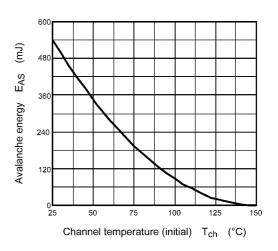


Fig. 8.15 E_{AS} - T_{ch} (Guaranteed Maximum)

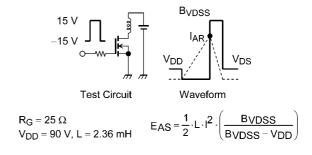


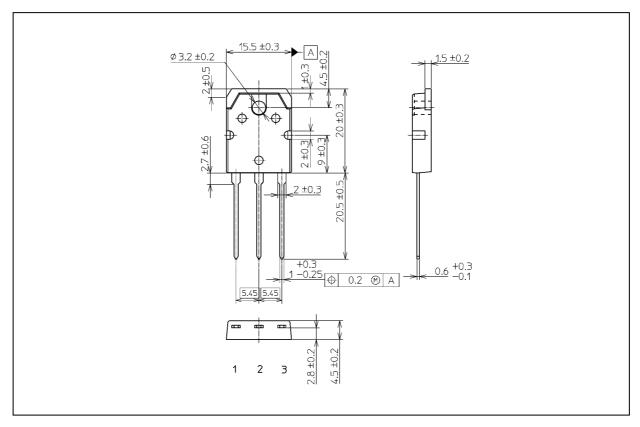
Fig. 8.16 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 4.6 g (typ.)

	Package Name(s)
JEITA: SC-65	
TOSHIBA: 2-16C1S	
Nickname: TO-3P(N)	



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