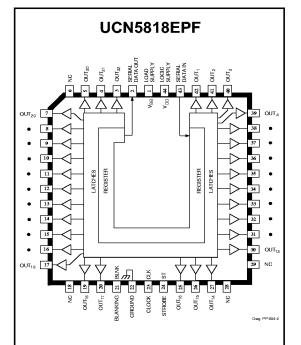
BiMOS II 32-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE-DMOS PULL-DOWNS



ABSOLUTE MAXIMUM RATINGS at $T_A = 25^{\circ}C$

| Logic Supply Voltage, V _{DD} | 15 | ٧ |
|--|----|---|
| Driver Supply Voltage, V _{BB} | 60 | ٧ |
| Continuous Output Current, | | |

I_{OUT}..... -40 mA to +15 mA Input Voltage Range,

 V_{IN} -0.3 V to V_{DD} + 0.3 V

Package Power Dissipation, Pn

(UCN5818AF) 3.5 W* (UCN5818EPF) 2.7 W+

Operating Temperature Range,

T_A -20°C to +85°C Storage Temperature Range,

T_S -55°C to +150°C

- * Derate at rate of 28 mW/°C above T_A = +25°C † Derate at rate of 22 mW/°C above TA = +25°C
- Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Designed primarily for use with vacuum-fluorescent displays, the UCN5818AF and UCN5818EPF smart power BiMOS II drivers combine CMOS shift registers, data latches, and control circuitry, with bipolar high-speed sourcing outputs and DMOS active pull-down circuitry. The high-speed shift register and data latches allow direct interfacing with microprocessor LSI-based systems. A CMOS serial data output enables cascade connections in applications requiring additional drive lines. Both devices feature 60 V and -40 mA output ratings, allowing them to be used in many other peripheral power driver applications.

These smart power drivers have been designed with BiMOS II logic for improved data entry rates. With a 5 V supply, they will typically operate above 5 MHz. At 12 V, significantly higher speeds are obtained. Use of these devices with TTL may require the use of appropriate pull-up resistors to ensure an input logic high. All devices can be operated over the ambient temperature range of -20°C to +85°C. The UCN5818AF is supplied in a 40-pin plastic dual in-line package with 0.600" (15.24 mm) row spacing. A copper lead frame, reduced supply current requirement, and low output saturation voltage permits operation with minimum junction temperature rise. The 'A' package allows all 32 outputs to be operated at -25 mA continuously over the operating temperature range.

For high-density packaging applications, the UCN5818EPF is furnished in a 44-lead plastic chip carrier (quad pack) for surface mounting on solder lands with 0.050" (1.27 mm) centers. The PLCC allows -25 mA continuous operation of all outputs simultaneously at ambient temperatures to 60°C. Similar devices are available as the UCN5810AF/LWF (10 bits), UCN5811A (12 bits), and UCN5812AF/ EPF (20 bits).

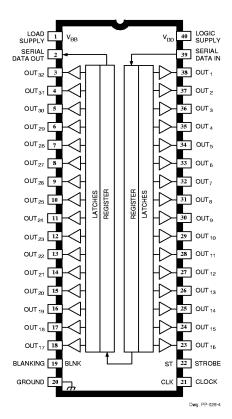
FEATURES

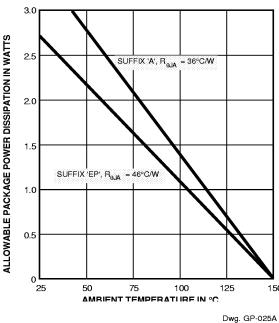
- 60 V Source Outputs
- High-Speed Source Drivers
- To 3.3 MHz Data Input Rate
- Low-Output Saturation Voltages
- Active DMOS Pull-Downs
- Low-Power CMOS Logic and Latches
- Reduced Supply Current Requirements
- Improved Replacements for SN75518N/FN

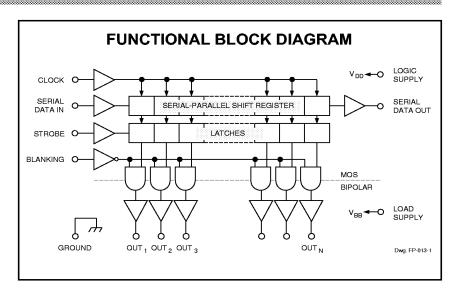
Always order by complete part number, e.g., UCN5818EPF.



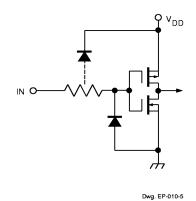
UCN5818AF



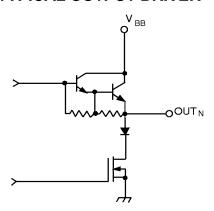




TYPICAL INPUT CIRCUIT



TYPICAL OUTPUT DRIVER



Dwg. No. A-14,219

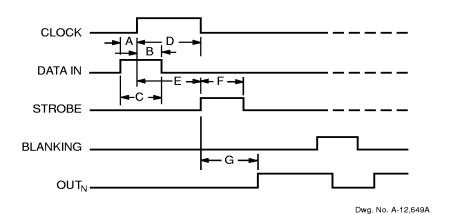


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ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{BB} = 60 V unless otherwise noted.

| | | | Limits | @ V _{DE} | , = 5 V | Limits | | | |
|----------------------------|---------------------|--|----------|-------------------|---------|--------|------|------|-------|
| Characteristic | Symbol | Test Conditions | MIn. | Тур. | Max. | Min. | Тур. | Max. | Units |
| Output Leakage Current | I _{CEX} | V _{OUT} = 0 V, T _A = +70°C | | -5.0 | -15 | _ | -5.0 | -15 | μΑ |
| Output Voltage | V _{OUT(1)} | I _{OUT} = -25 mA | 58 | 58.5 | _ | 58 | 58.5 | _ | ٧ |
| | V _{OUT(0)} | I _{OUT} = 1 mA | _ | 2.0 | 3.0 | _ | _ | _ | V |
| | | I _{OUT} = 2 mA | - | _ | _ | _ | 2.0 | 3.5 | V |
| Output Pull-Down Current | I _{OUT(0)} | V _{OUT} = 5 V to V _{BB} | 2.0 | 3.5 | _ | _ | _ | _ | mA |
| | | V _{OUT} = 20 V to V _{BB} | - | _ | _ | 8.0 | 13 | _ | mA |
| Input Voltage | V _{IN(1)} | | 3.5 | _ | 5.3 | 10.5 | _ | 12.3 | V |
| | V _{IN(0)} | | -0.3 | _ | +0.8 | -0.3 | _ | +0.8 | V |
| Input Current | I _{IN(1)} | $V_{IN} = V_{DD}$ | _ | 0.05 | 0.5 | _ | 0.1 | 1.0 | μΑ |
| | I _{IN(0)} | V _{IN} = 0.8 V | - | -0.05 | -0.5 | _ | -0.1 | -1.0 | μА |
| Serial Data Output Voltage | V _{OUT(1)} | I _{OUT} = -200 μA | 4.5 | 4.7 | _ | 11.7 | 11.8 | _ | V |
| | V _{OUT(0)} | I _{OUT} = 200 μA | _ | 200 | 250 | _ | 100 | 200 | mV |
| Maximum Clock Frequency | f _{clk} | | 3.3 | 5.0 | _ | _ | 7.5 | _ | MHz |
| Supply Current | I _{DD(1)} | All Outputs High | | 100 | 300 | _ | 200 | 500 | μА |
| | I _{DD(0)} | All Outputs Low | - | 100 | 300 | _ | 200 | 500 | μА |
| | I _{BB(1)} | Outputs High, No Load | - | 3.0 | 6.0 | _ | 3.0 | 6.0 | mA |
| | I _{BB(0)} | Outputs Low | - | 10 | 100 | _ | 10 | 100 | μΑ |
| Blanking to Output Delay | t _{PHL} | C _L = 30 pF, 50% to 50% | <u> </u> | 2000 | _ | _ | 1000 | _ | ns |
| | t _{PLH} | C _L = 30 pF, 50% to 50% | - | 1000 | _ | _ | 850 | _ | ns |
| Output Fall Time | t _f | C _L = 30 pF, 90% to 10% | - | 1450 | _ | _ | 650 | _ | ns |
| Output Rise Time | t _r | C _L = 30 pF, 10% to 90% | <u> </u> | 650 | _ | _ | 700 | _ | ns |

Negative current is defined as coming out of (sourcing) the specified device terminal.



TIMING CONDITIONS

 $(T_A = +25^{\circ}C, V_{DD} = 5.0 \text{ V}, \text{Logic Levels are } V_{DD} \text{ and Ground})$

 Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON, the information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

| Serial | l | | hift | Regi | ister | Cont | ents | Serial | | | Lat | ch C | Cont | ents | | | Output Contents | | | | |
|---------------|----------------|-------|----------------|----------------|-------|------------------|------------------|------------------|-----------------|----------------|----------------|----------------|------|------------------|----------------|----------|-----------------|----------------|------------------|------------------|-----------------------------|
| Data Input | Clock Input | | l ₂ | I ₃ | | I _{N-1} | I _N | Data Output | Strobe Input | I ₁ | l ₂ | l ₃ | | I _{N-1} | I _N | Blanking | I ₁ | l ₂ | l ₃ . | I _{N-1} | I _N |
| Н | 7 | Н | R ₁ | R ₂ | | R _{N-2} | R _{N-1} | R _{N-1} | | | | | | | | | | | | | |
| L | | L | R ₁ | R_2 | | R _{N-2} | R _{N-1} | R _{N-1} | | | | | | | | | | | | | |
| Х | l | R_1 | R_2 | R ₃ | | R _{N-1} | R_N | R _N | | | | | | | | | | | | | |
| | | Х | Х | Х | | Х | Х | Х | L | R ₁ | R_2 | Rз | | R _{N-1} | R_N | | | | | | |
| | | P_1 | P ₂ | P ₃ | | P _{N-1} | P_{N} | P _N | Н | P ₁ | P ₂ | Рз | | P _{N-1} | P_N | L | P ₁ | P_2 | Р3. | P _{N-} | ₁ P _N |
| | | | | | | | | | | Х | Х | Χ | | Х | Х | Н | L | L | L. | L | L |

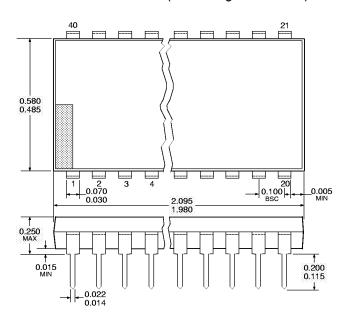
 $L = Low\ Logic\ Level \quad H = High\ Logic\ Level \quad X = Irrelevant \quad P = Present\ State \quad R = Previous\ State$

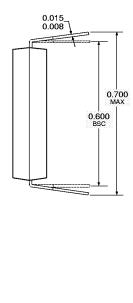


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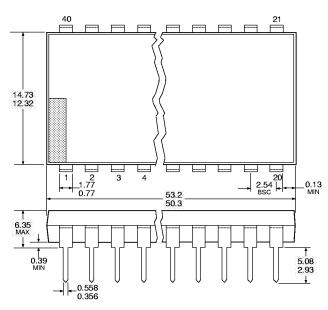
UCN5818AF

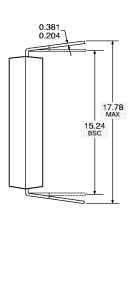
Dimensions in Inches (controlling dimensions)





Dimensions in Millimeters (for reference only)





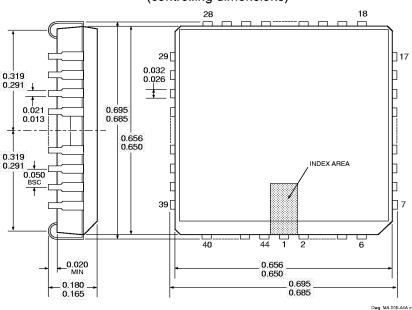
Dwg. MA-003-40 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

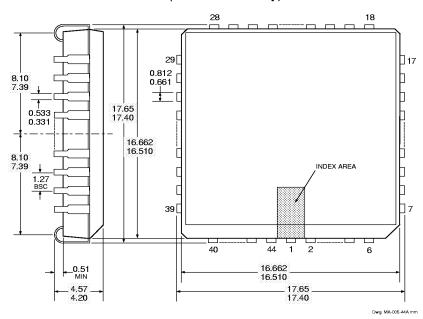
- Lead spacing tolerance is non-cumulative.
- 3. Lead thickness is measured at seating plane or below.

UCN5818EPF

Dimensions in Inches (controlling dimensions)



Dimensions in Millimeters (for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

2. Lead spacing tolerance is non-cumulative.

