PRELIMINARY

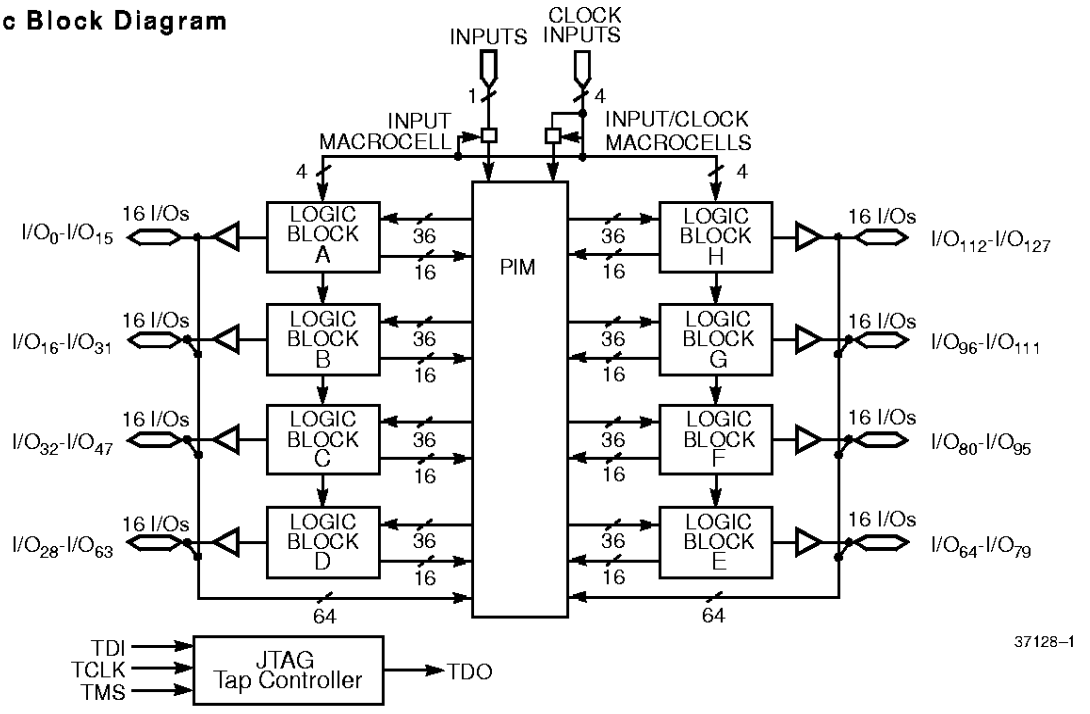
Ultra37128

UltraLogic™ 128-Macrocell ISR™ CPLD

Features

- 128 macrocells in eight logic blocks
- In-System Reprogrammable (ISR™)
  - JTAG compliant on board programming
  - Design changes don't cause pinout changes
  - Design changes don't cause timing changes
- I/O Intensive Version features an I/O for every Macocell
  - 128 I/O Macrocells
  - 128 I/O pins plus 5 dedicated inputs including 4 clock inputs
- Register Intensive Version
  - 64 buried Macrocells and 64 I/O Macrocells
  - 64 I/O pins and 5 or 6 dedicated inputs including 4 clock inputs
- IEEE 1149.1 JTAG boundary scan
- High speed
  - f_{MAX} = 167 MHz
  - t_{PD} = 6.5 ns
  - t_S = 3.5 ns
  - t_{CO} = 4.5 ns
- Product-term clocking
- Programmable slew rate control on individual I/Os
- Low power option on individual logic block basis
- 5V and 3.3V I/O capability
- Bus Hold capabilities on all I/Os
- Simple Timing Model
- Fully PCI compliant[1]
- Available in 84-pin PLCC, 100-pin TQFP and 160-pin PQFP packages
- Pinout compatible with and functional superset of FLASH374i/5i

Logic Block Diagram



Selection Guide

	Ultra37128–167	Ultra37128-154	Ultra37128-125	Ultra37128-83
Maximum Propagation Delay, t_{PD} (ns)	6.5	7.5	10	15
Minimum Set-Up, t_S (ns)	3.5	4.0	5.5	8
Maximum Clock to Output, t_{CO} (ns)	4.5	4.5	6.5	8
Typical Supply Current, I_{CC} (mA) in Low Power Mode	75	75	75	75

Note:
1. Due to the 5V tolerant nature of the I/Os, the I/Os are not clamped to V_{CC}.

Functional Description

The Ultra37128 is an In-System Reprogrammable (ISR) Complex Programmable Logic Device (CPLD) and is part of the Ultra37000™ family of high-density, high-speed CPLDs. Like all members of the Ultra37000 family, the Ultra37128 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 128 macrocell Ultra37128 is available in register intensive and I/O intensive versions. The Ultra37128P84 and Ultra37128P100 feature 64 Buried Macrocells and 64 I/O Macrocells for register intensive designs which require small footprint devices. The Ultra37128P160 I/O intensive device has an I/O pin for each macrocell.

For a more detailed description of the architecture and features of the Ultra37128 see the Ultra37000 family data sheet.

Fully Routable with 100% Logic Utilization

The Ultra37128 is designed with a robust routing architecture which allows utilization of the entire device, with a fixed pinout. This makes Ultra37000 optimal for implementing on board design changes using ISR without changing pinouts.

Simple Timing Model

The Ultra37128 features a very simple timing model with predictable delays. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. The timing model allows for design changes with ISR without causing changes to system performance.

Low Power Operation

Each Logic Block of the Ultra37128 can be configured as either High-Speed (default) or Low-Power. In the Low-Power mode, the logic block consumes 50% less power (9.3 mA max.) and slows down by 5 ns.

Output Slew Rate Control

Each output can be configured with either a fast edge rate (default) for high performance, or a slow edge rate for added noise reduction. In the fast edge rate mode, outputs switch at 3V/ns max. and in the slow edge rate mode, outputs switch at 1V/ns max. There is a 2ns delay for I/Os using the slow edge rate mode.

In System Reprogramming

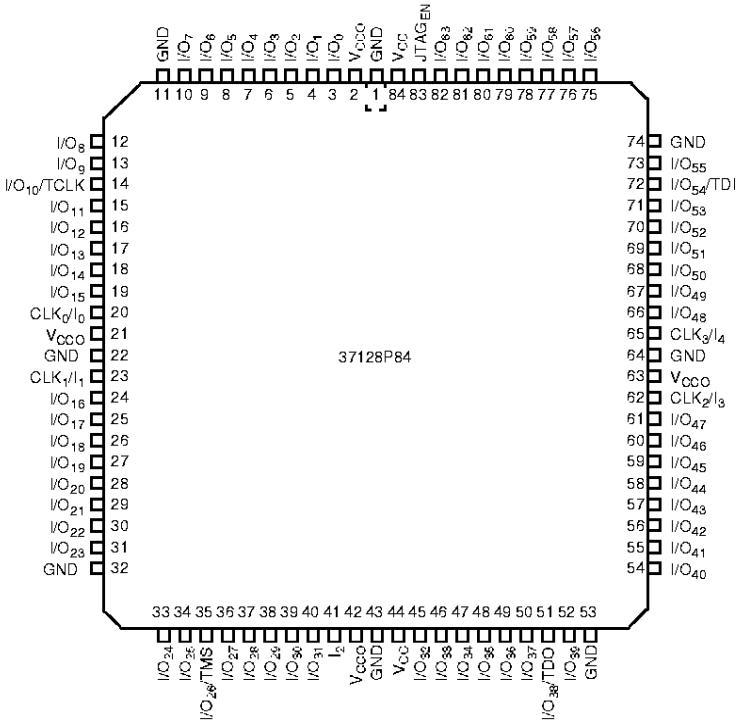
The Ultra37128 can be programmed in system using IEEE 1149.1 complaint JTAG programming protocol. The Ultra37128 can also be programmed on a number of traditional parallel programmers including Cypress's *Impulse3* programmer and industry standard third party programmers. For an overview of ISR programming, refer to the Ultra37000 Family data sheet and for ISR cable and software specifications, refer to the InSRkit: ISR programming data sheet (CY3600).

Design Tools

Development software for the Ultra37128 is available from Cypress's *Warp*™ or third party bolt-in software packages as well as a number of third party development packages. Please refer to the *Warp* or third party tool support data sheets for further information.

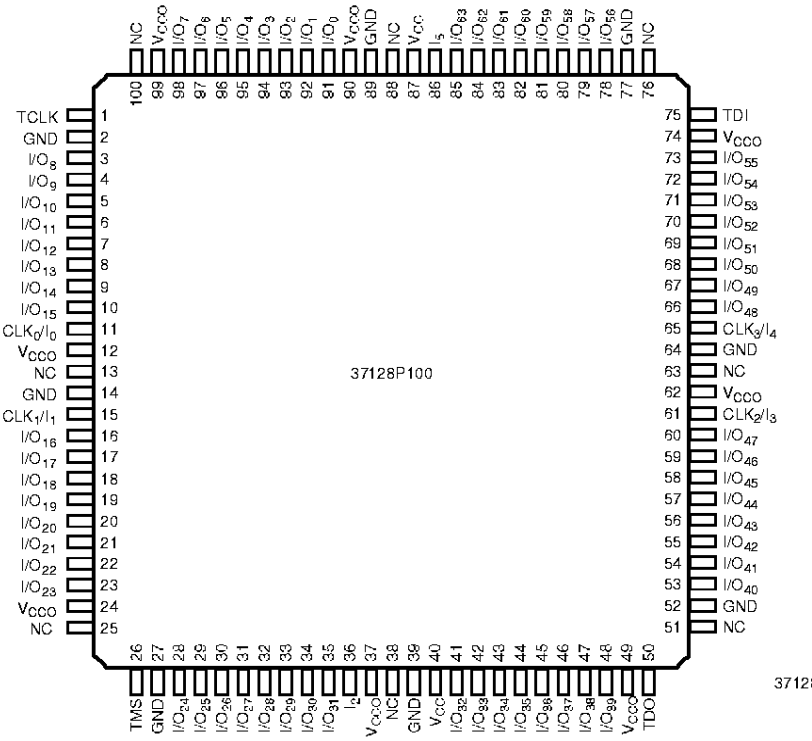
Pin Configurations

84-pin PLCC
Top View



37128-2

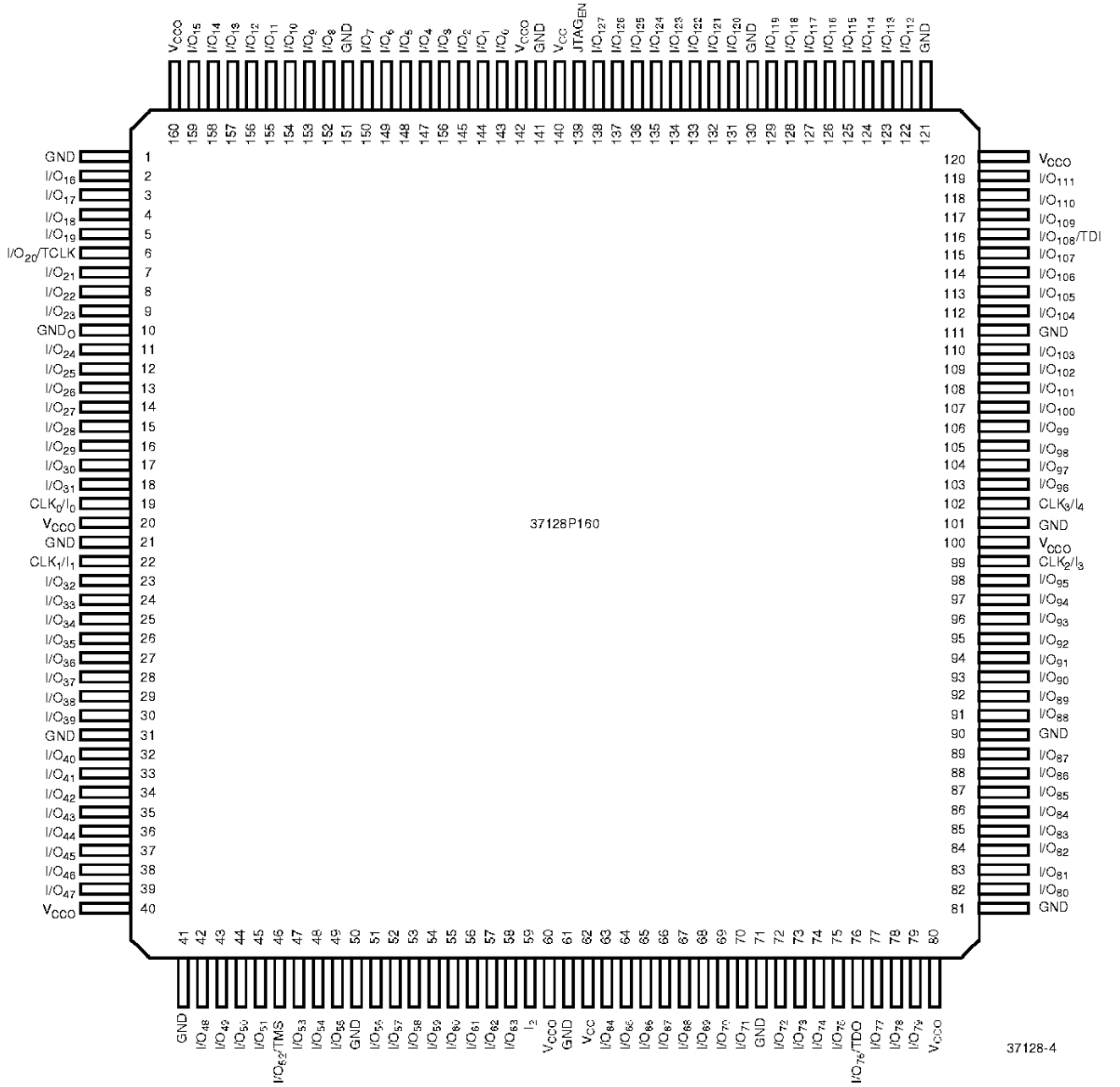
100-pin TQFP
Top View



37128-3

Pin Configurations (continued)

160-pin TQFP
Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State.....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

DC Program Voltage .....5V±5%

Output Current into Outputs ..... 16 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range[2]

Range	Ambient Temperature[2]	Output Condition	V_{CC}	V_{CCO}
Commercial	0°C to +70°C	5V	5V ± 5%	5V ± 5%
		3.3V	5V ± 5%	3.3V ± 0.3V
Industrial	-40°C to +85°C	5V	5V ± 10%	5V ± 10%
		3.3V	5V ± 10%	3.3V ± 0.3V
Military[3]	-55°C to +125°C	5V	5V ± 10%	5V ± 10%
		3.3V	5V ± 10%	3.3V ± 0.3V

Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3.2 mA[4]	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 16 mA[4]		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH voltage for all inputs[5]		2.0	5.25	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all inputs[5]		–0.5	0.8	V
I_{IX}	Input Load Current	V_I = Internal GND, V_I = V_{CC}		–10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–50	50	µA
I_{OS}	Output Short Circuit Current[6, 7]	V_{CC} = Max., V_{OUT} = 0.5V		–30	–160	mA
$I_{CC\text{-}HS}$	Power Supply Current[8] Per Logic Block - High Speed Mode	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 MHz, V_{IN} = GND or V_{CC}			18.7	mA
$I_{CC\text{-}LP}$	Power Supply Current[8] Per Logic Block - Low Power Mode	V_{CC} = Max., I_{OUT} = 0 mA, f = 1 MHz, V_{IN} = GND or V_{CC}			9.3	mA
I_{BHL}	Input Bus Hold LOW Sustaining Current	V_{CC} = Min., V_{IL} = 0.8V		+75		µA
I_{BHH}	Input Bus Hold HIGH Sustaining Current	V_{CC} = Min., V_{IH} = 2.0V		–75		µA
I_{BHLO}	Input Bus Hold LOW Overdrive Current	V_{CC} = Max.			+500	µA
I_{BHHO}	Input Bus Hold HIGH Overdrive Current	V_{CC} = Max.			–500	µA

Notes:

2. Normal Programming Conditions apply across Ambient Temperature Rnage for specified programming methods. For more information on programming the Ultra37000 family devices see the Ultra37000 family data sheet.
3. T_A is the "instant on" case temperature.
4. I_{OH} = –2 mA, I_{OL} = 2 mA for SDO.
5. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
6. Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Measured with 16-bit counter programmed into the logic block. Total device power calculated by summing the I_{CC} specifications for the mode of operation of each logic block.

Inductance[7]

Parameter	Description	Test Conditions	84-lead PLCC	100-lead TQFP	160-Lead TQFP	Unit
L	Maximum Pin Inductance	V_{IN} = 5.0V at f = 1 MHz	8	5	9	nH

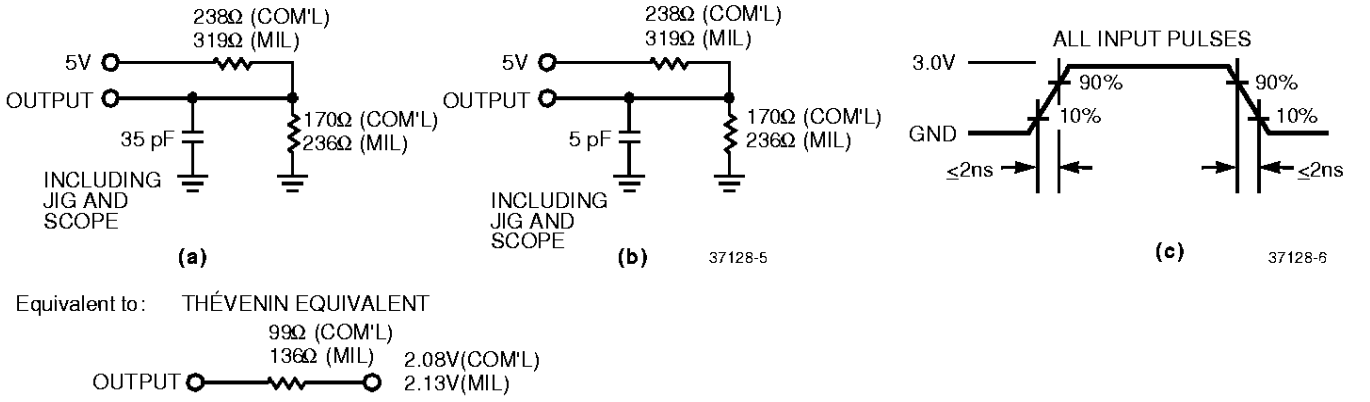
Capacitance[7]

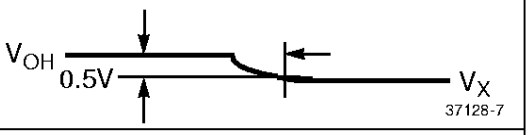
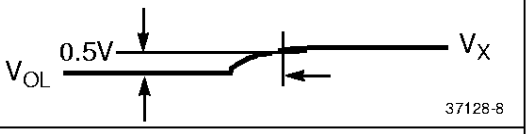
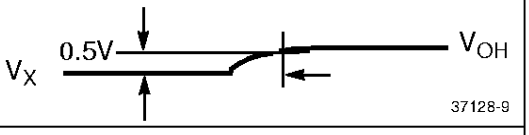
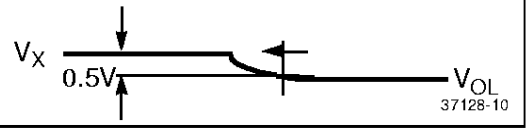
Parameter	Description	Test Conditions	Max.	Unit
$C_{I/O}$	Input/Output Capacitance	V_{IN} = 5.0V at f = 1 MHz	8	pF
C_{CLK}	Clock Signal Capacitance	V_{IN} = 5.0V at f = 1 MHz	12	pF

Endurance Characteristics[7]

Parameter	Description	Test Conditions	Min.	Typ.	Unit
N	Minimum Reprogramming Cycles	Normal Programming Conditions[2]	1,000	10,000	Cycles

AC Test Loads and Waveforms



Parameter[9]	V_X	Output Waveform--Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	1.5V	
$t_{EA(-)}$	V_{the}	

(d) Test Waveforms

Note:

9. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load.

Switching Characteristics Over the Operating Range[10]

Parameter	Description	37128-167		37128-154		37128-125		37128-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}[11]	Input to Combinatorial Output		6.5		7.5		10		15	ns
t_{PDL}[11]	Input to Output Through Transparent Input or Output Latch		9		10		13		18	ns
t_{PDLL}[11]	Input to Output Through Transparent Input and Output Latches		11		12		15		19	ns
t_{EA}[12]	Input to Output Enable		10		11		14		19	ns
t_{ER}	Input to Output Disable		10		11		14		19	ns
Input Register Parameters										
t_{WL}	Clock or Latch Enable Input LOW Time[7]	2.5		2.5		3		4		ns
t_{WH}	Clock or Latch Enable Input HIGH Time[7]	2.5		2.5		3		4		ns
t_{IS}	Input Register or Latch Set-Up Time	2		2		2		3		ns
t_{IH}	Input Register or Latch Hold Time	2		2		2		3		ns
t_{ICO}[11]	Input Register Clock or Latch Enable to Combinatorial Output		11		11		14		19	ns
t_{ICOL}[11]	Input Register Clock or Latch Enable to Output Through Transparent Output Latch		12		12		16		21	ns
Synchronous Clocking Parameters										
t_{CO}[12]	Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output		4.5		4.5		6.5		8	ns
t_S[11]	Set-Up Time from Input to Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	3.5		4.0		5.5		8		ns
t_H	Register or Latch Data Hold Time	0		0		0		0		ns
t_{CO2}[11, 12]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Combinatorial Output Delay (Through Logic Array)		10		11		14		19	ns
t_{SCS}[11]	Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable to Output Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable (Through Logic Array)	6		6.5		8		12		ns
t_{SL}[11]	Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	7.5		8.0		10		15		ns
t_{HL}	Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) or Latch Enable	0		0		0		0		ns
Product Term Clocking Parameters										
t_{COPT}[11, 12]	Product Term Clock or Latch Enable (PTCLK) to Output		9		10		12		17	ns

Switching Characteristics Over the Operating Range[10] (continued)

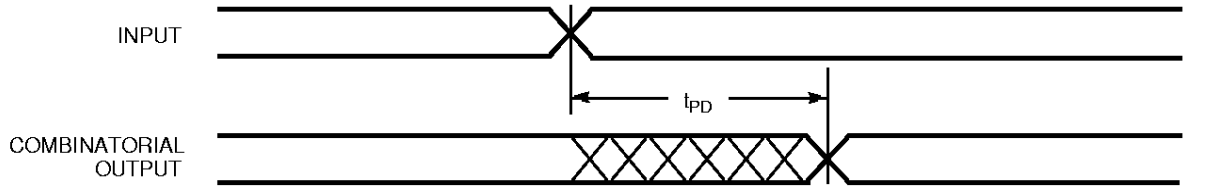
Parameter	Description	37128-167		37128-154		37128-125		37128-83		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SPT}[11]	Set-Up Time from Input to register Product Term Clock or Latch Enable (PTCLK)	2.5		2.5		3		3		ns
t_{HPT}	Register or Latch Data Hold Time	2.5		2.5		3		3		ns
t_{ISPT}[11]	Set-Up Time from buried register used as an input register from Input to Product Term Clock or Latch Enable (PTCLK)		-2		-2		-2		-2	ns
t_{IHPT}	Buried Register used as an input register or Latch Data Hold Time		5.5		6.5		9		14	ns
t_{CO2PT}[11, 12]	Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)		13		14		16		21	ns
Pipelined Mode Parameters										
t_{ICS}[11, 12]	Input Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3) to Output Register Synchronous Clock (CLK_0, CLK_1, CLK_2, or CLK_3)	5.5		6		8		12		ns
Operating Frequency Parameters										
f_{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$)[7]	167		154		125		83		MHz
f_{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_S + t_H)$, or $1/t_{CO}$)	200		200		153.8		125		MHz
f_{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$)	125		118		83.3		62.5		MHz
f_{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	154		154		125		66.6		MHz
Reset/Preset Parameters										
t_{RW}	Asynchronous Reset Width[7]	8		8		10		15		ns
t_{RR}	Asynchronous Reset Recovery Time[7]	10		10		12		17		ns
t_{RO}[11, 12]	Asynchronous Reset to Output		14		14		16		21	ns
t_{PW}	Asynchronous Preset Width[7]	8		8		10		15		ns
t_{PR}	Asynchronous Preset Recovery Time[7]	10		10		12		17		ns
t_{PO}[11, 12]	Asynchronous Preset to Output		14		14		16		21	ns
User Option Parameters										
t_{LP}	Low Power Adder	5		5		6		6		ns
t_{SLEW}	Slow Output Slew Rate Adder	2		2		2		2		ns
Tap Controller Parameter										
f_{TAP}	Tap Controller Frequency	20			20		20		20	MHz

Notes:

10. All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
11. Logic Blocks operating in low power mode, add t_{LP} to this spec.
12. Outputs using Slow Output Slew Rate, add t_{SLEW} to this spec.

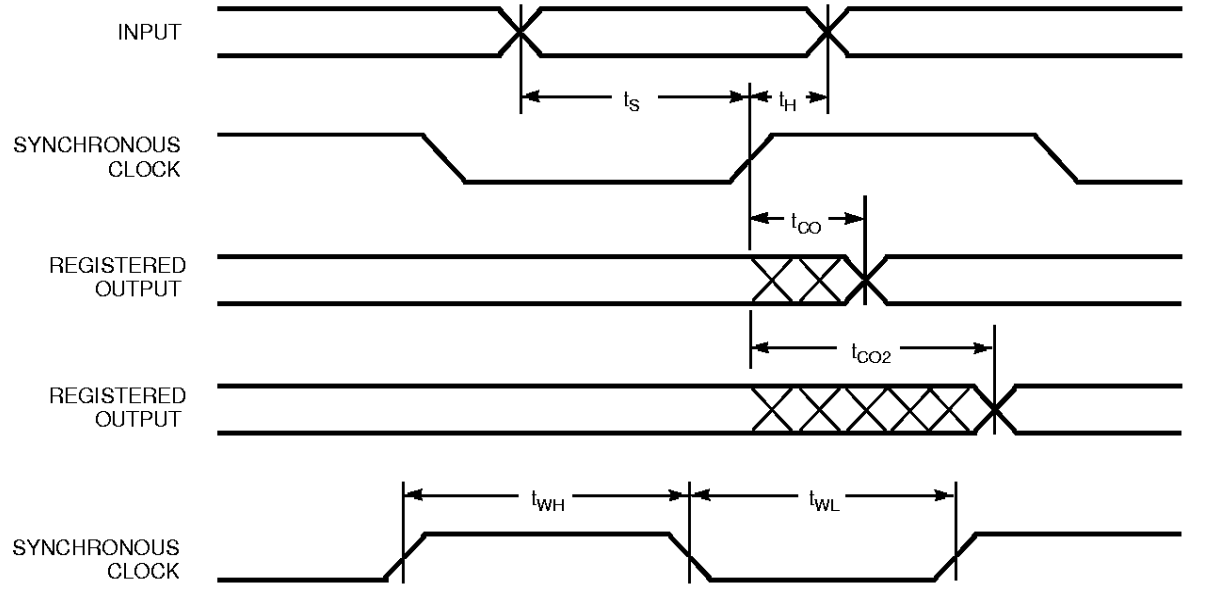
Switching Waveforms

Combinatorial Output



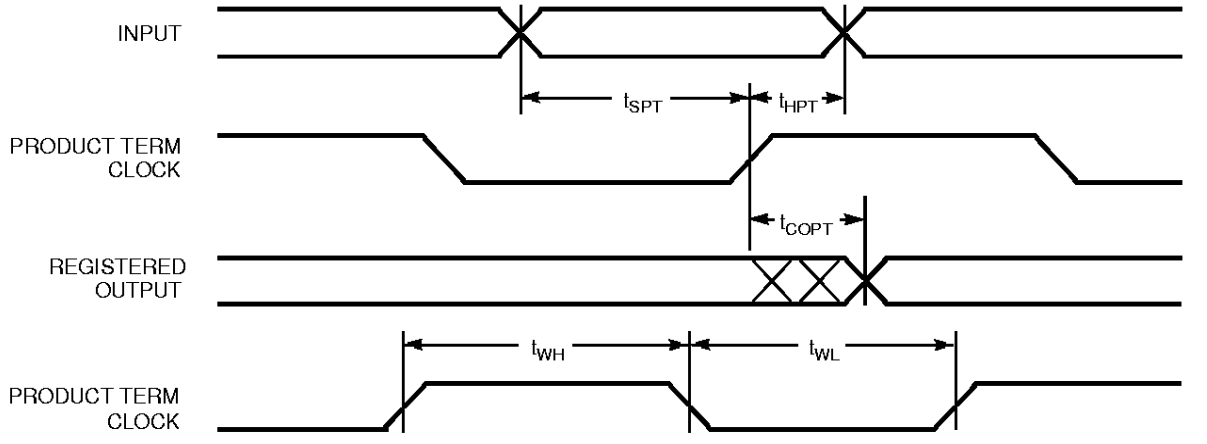
37128-11

Registered Output with Synchronous Clocking



37128-12

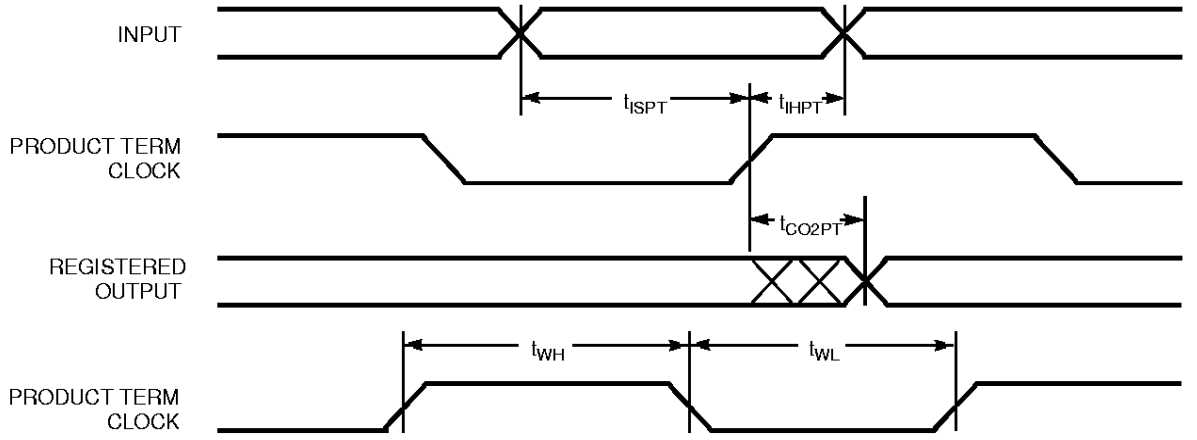
Registered Output with Product Term Clocking Input going through the Array



37128-13

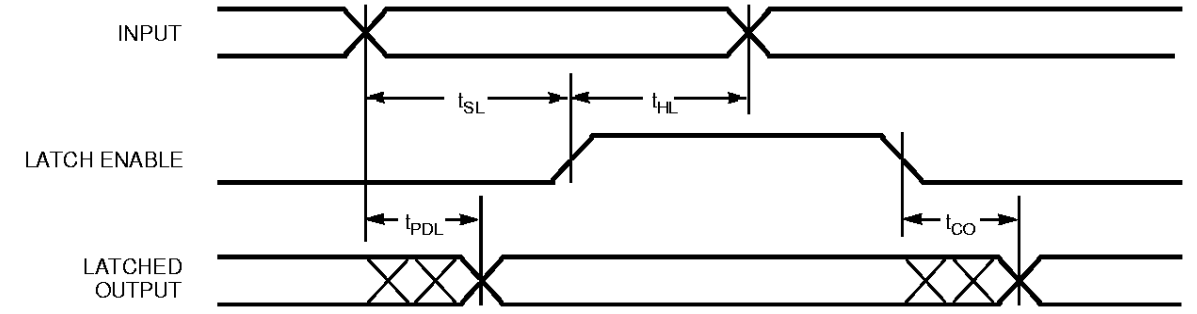
Switching Waveforms (continued)

Registered Output with Product Term Clocking Input coming from Adjacent Buried Register



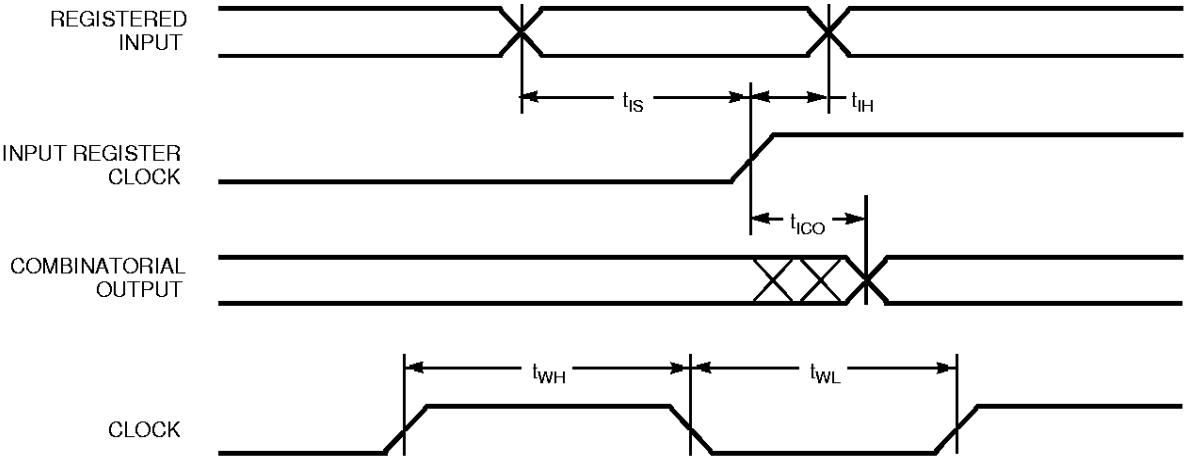
37128-14

Latched Output



37128-15

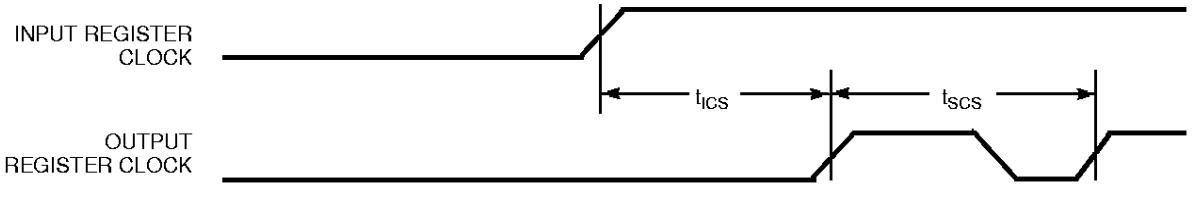
Registered Input



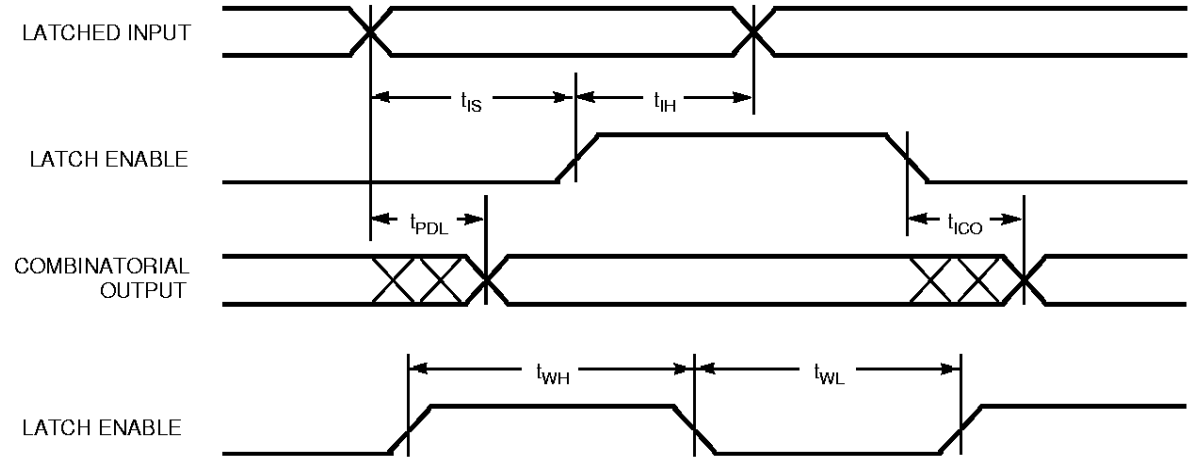
37128-16

Switching Waveforms (continued)

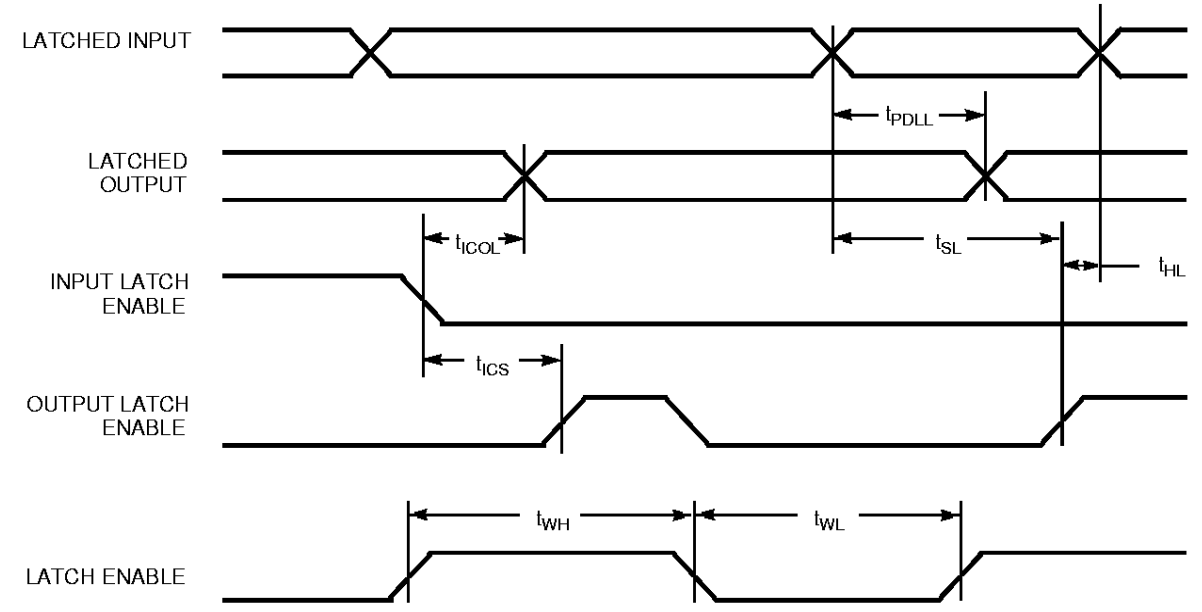
Clock to Clock



Latched Input

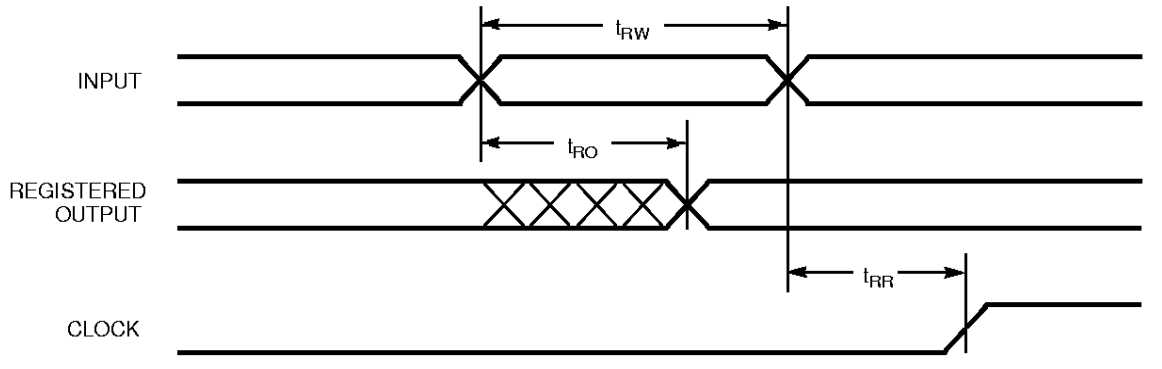


Latched Input and Output

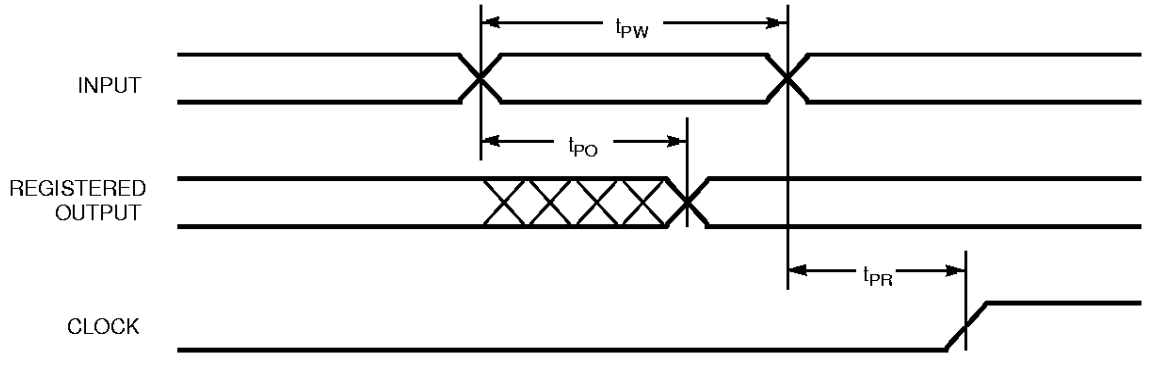


Switching Waveforms (continued)

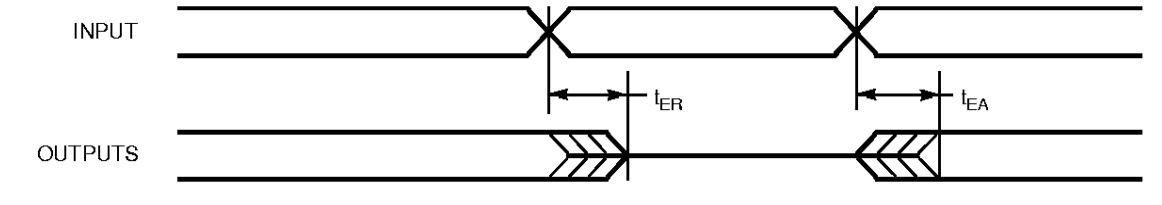
Asynchronous Reset



Asynchronous Preset



Output Enable/Disable



Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CY37128P84–167JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–167AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–167AC	A160	160-Pin Thin Quad Flatpack	
154	CY37128P84–154JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–154AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–154AC	A160	160-Pin Thin Quad Flatpack	
	CY37128P84–154JI	J83	84-Lead Plastic Leaded Chip Carrier	Industrial
	CY37128P100–154AI	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–154AI	A160	160-Pin Thin Quad Flatpack	
125	CY37128P84–125JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–125AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–125AC	A160	160-Pin Thin Quad Flatpack	
	CY37128P84–125JI	J83	84-Lead Plastic Leaded Chip Carrier	Indusrtial
	CY37128P100–125AI	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–125AI	A160	160-Pin Thin Quad Flatpack	
	CY37128P160–125GMB	G160	160-Pin Grid Array	Military
	CY37128P160–125UMB	U160	160-Pin Ceramic Quad Flatpack	
83	CY37128P84–83JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY37128P100–83AC	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–83AC	A160	160-Pin Thin Quad Flatpack	
	CY37128P84–83JI	J83	84-Lead Plastic Leaded Chip Carrier	Indusrtial
	CY37128P100–83AI	A100	100-Pin Thin Quad Flatpack	
	CY37128P160–83AI	A160	160-Pin Thin Quad Flatpack	
	CY37128P160-83GMB	G160	160-Pin Grid Array	Military
	CY37128P160-83UMB	U160	160-Pin Ceramic Quad Flatpack	

Shaded areas contain advance information.

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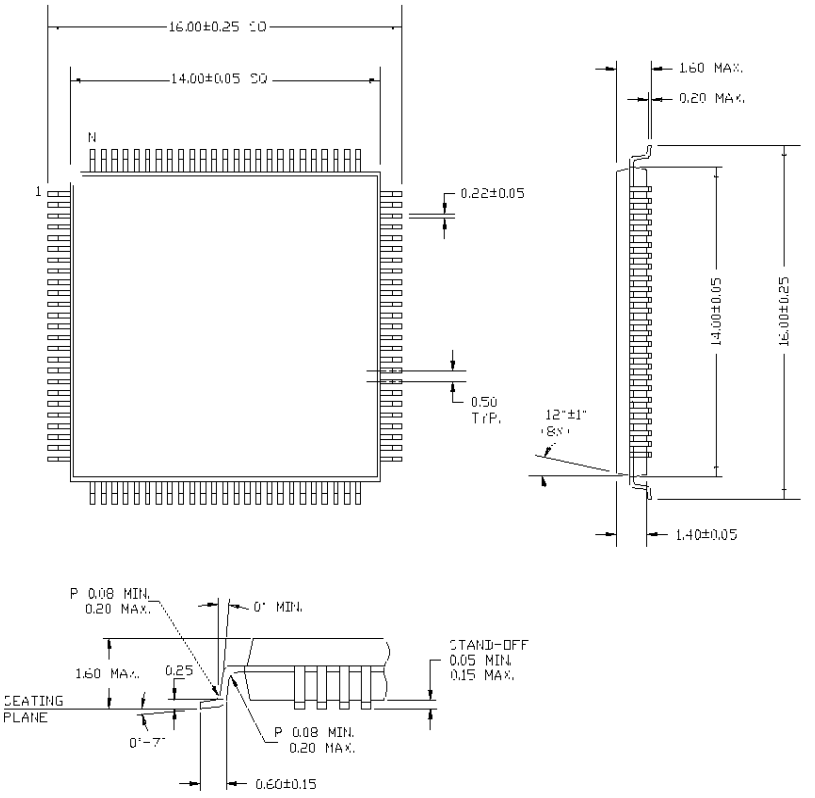
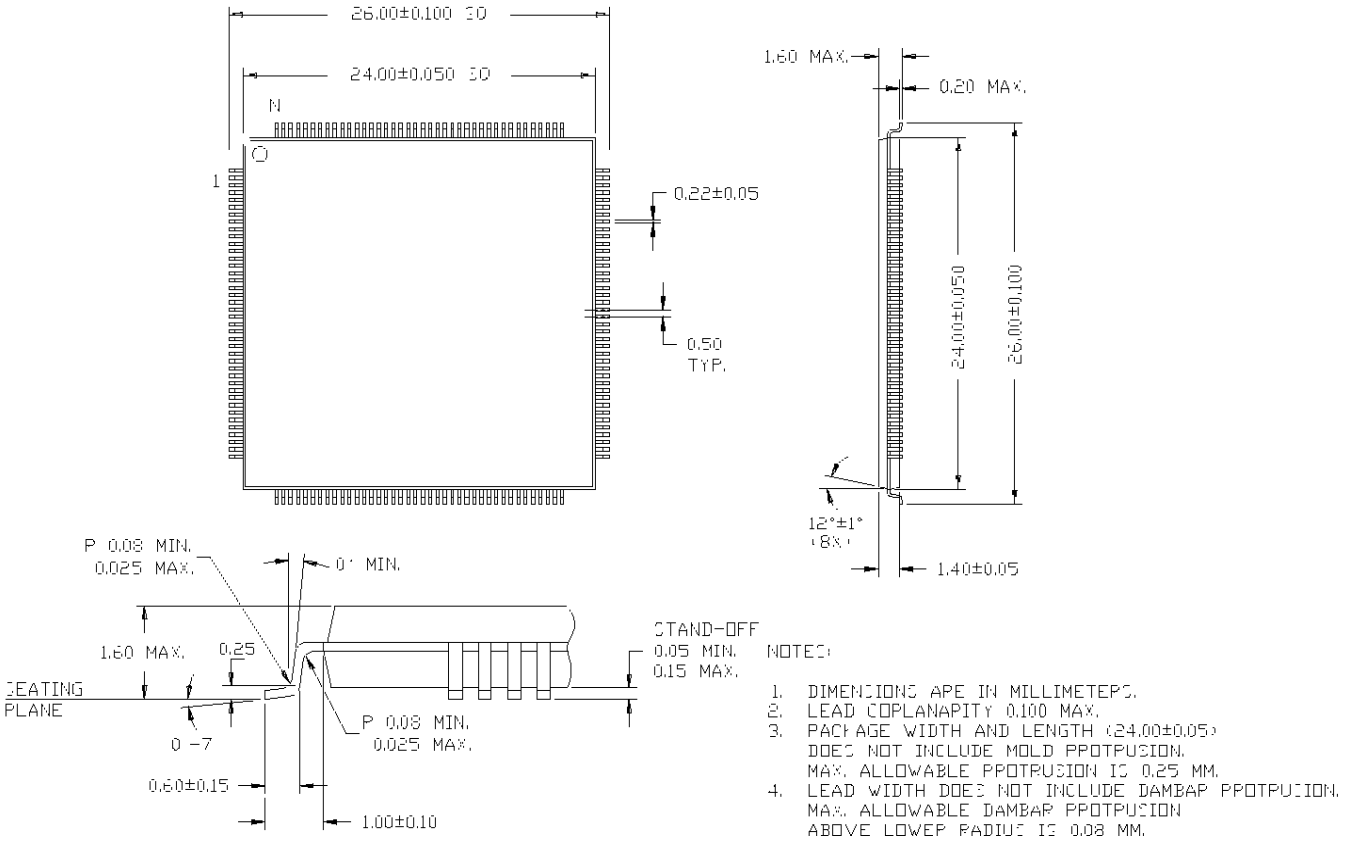
Package Diagrams

100-Pin Thin Quad Flat Pack A100



Package Diagrams (continued)

160-Lead Thin Quad Flat Pack (TQFP) A160



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH AND LENGTH (24.00±0.05) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM.

84-Lead Plastic Leaded Chip Carrier J83