

DESCRIPTION:

The DPS128M8nY & DPS128X8A3 SRAM devices are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages, or mounted on a 50-pin PGA co-fired ceramic substrate. These devices pack 1-Megabits of low-power CMOS static RAM in an area as small as 0.463 in², while maintaining a total height as low as 0.082 inches.

The SLCC devices contain an individual 128K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

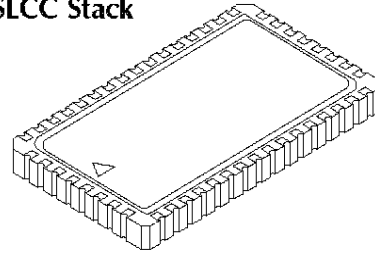
By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

FEATURES:

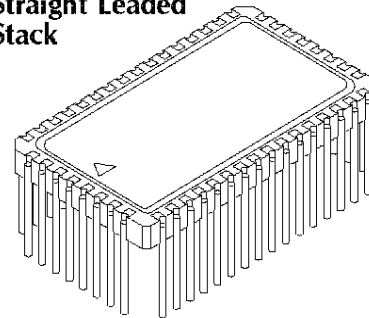
- Organizations Available: 128K x 8
- Access Times: 70*, 85, 100, 120, 150ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
 - 48 - Pin SLCC Stack
 - 48 - Pin Straight Leaded Stack
 - 48 - Pin Gullwing Leaded Stack
 - 48 - Pin "J" Leaded Stack
 - 50 - Pin PGA Dense-Stack

* Commercial only.

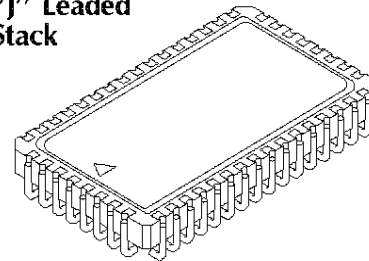
SLCC Stack



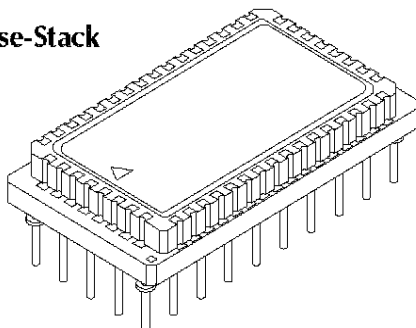
Straight Leaded Stack



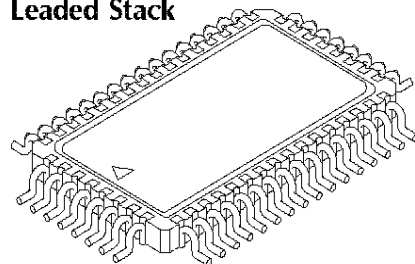
"J" Leaded Stack

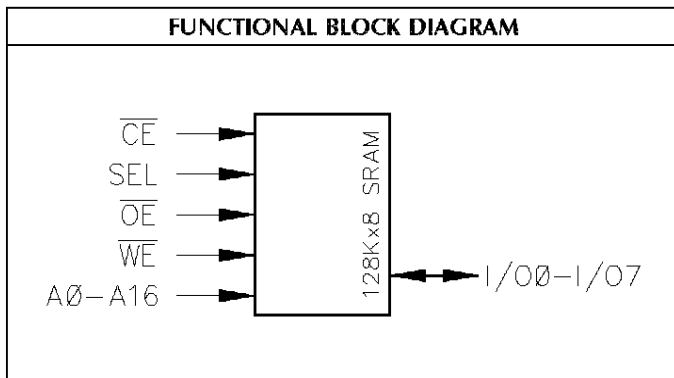


Dense-Stack

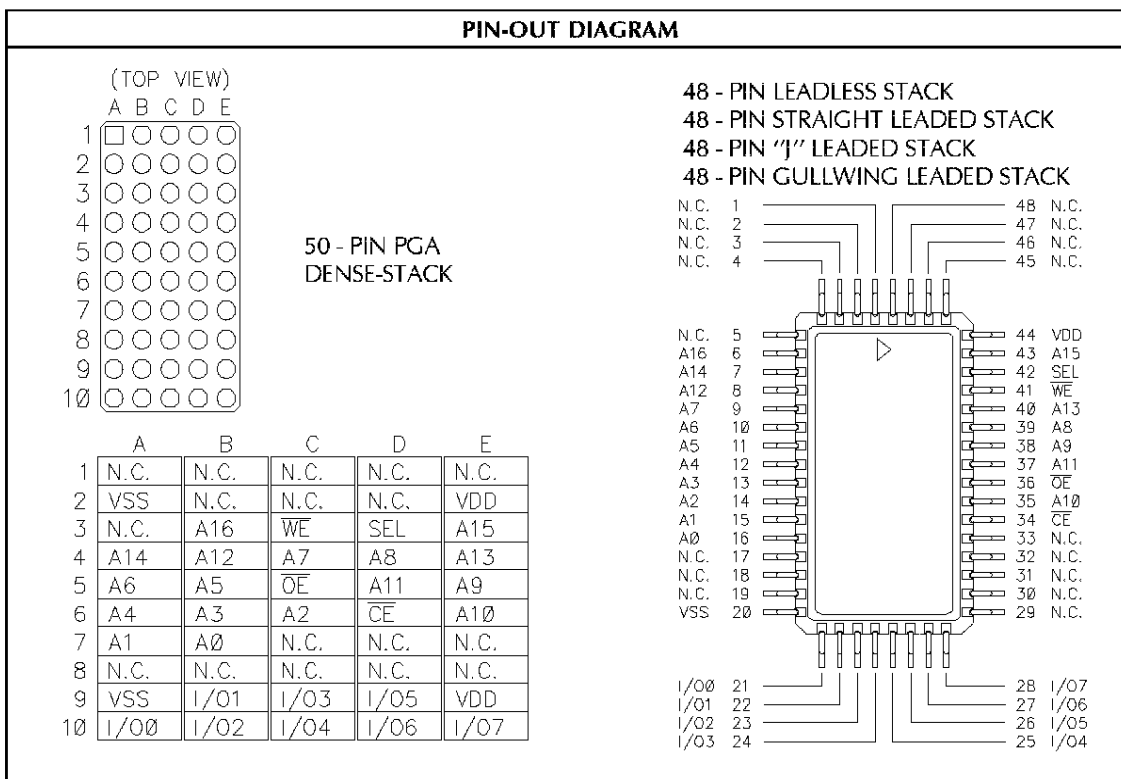


Gullwing Leaded Stack





PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O7	Data Input/Output
\overline{CE}	Low Chip Enable
SEL	High Chip Enable
\overline{WE}	Write Enable
\overline{OE}	Output Enable
V _{DD}	Power (+ 5V)
V _{SS}	Ground
N.C.	No Connect



RECOMMENDED OPERATING RANGE ³						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V _{DD}	Supply Voltage	4.5	5.0	5.5	V	
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V	
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V	
T _A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE						
Mode	SEL	CE	WE	OE	I/O Pin	Supply Current
Not Selected	L	X	X	X	HIGH-Z	Standby
Not Selected	X	H	X	X	HIGH-Z	Standby
D _{OUT} Disable	H	L	H	H	HIGH-Z	Active
Read	H	L	H	L	D _{OUT}	Active
Write	H	L	L	X	D _{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -1.0mA	2.4		V
V _{OL}	LOW Voltage	I _{OL} = 2.1mA		0.4	V

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	°C
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	12	pF	V _{IN} ² = 0V
C _{CE}	Chip Enable	12		
C _{SEL}	Active High Chip Select	12		
C _{WE}	Write Enable	12		
C _{OE}	Output Enable	12		
C _{I/O}	Data Input/Output	14		

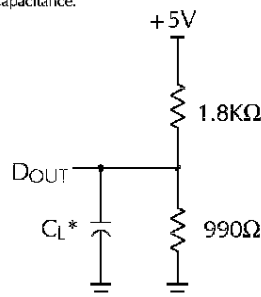
DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-	-2	+2	-2	+2	-2	+2	µA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE or OE = V _{IH} , or WE = V _{IL}	-	-2	+2	-2	+2	-2	+2	µA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	15		35		45		50	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA	45		70		75		80	mA
I _{SB1}	Full Standby Supply Current (CMOS)	V _{IN} ≥ V _{DD} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V CE ≥ V _{DD} - 0.2V, SEL ≥ V _{DD} - 0.2V or SEL ≤ V _{SS} + 0.2V	2		100		200		500	µA
I _{SB2}	Standby Current (TTL)	CE = V _{IH} , V _{IN} = V _{IH} or V _{IL}	1		3		3		2	mA
I _{DR3}	Data Retention Supply Current (3.0V)	V _{DR} = 3.0V, CE ≥ V _{DR} - 0.2V, SEL ≥ V _{DR} - 0.2V or SEL ≤ 0.2V	1		50		100		400	µA
I _{DR2}	Data Retention Supply Current (2.0V)	V _{DR} = 2.0V, CE ≥ V _{DR} - 0.2V, SEL ≥ V _{DR} - 0.2V or SEL ≤ 0.2V	1		45		85		350	µA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA	-		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

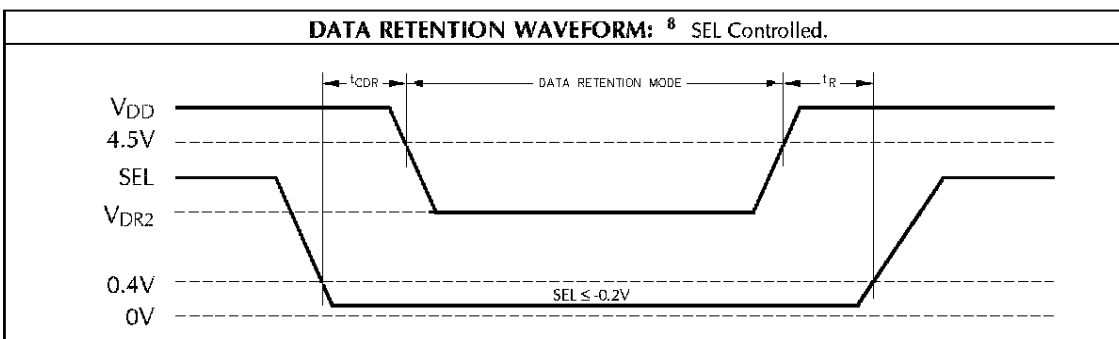
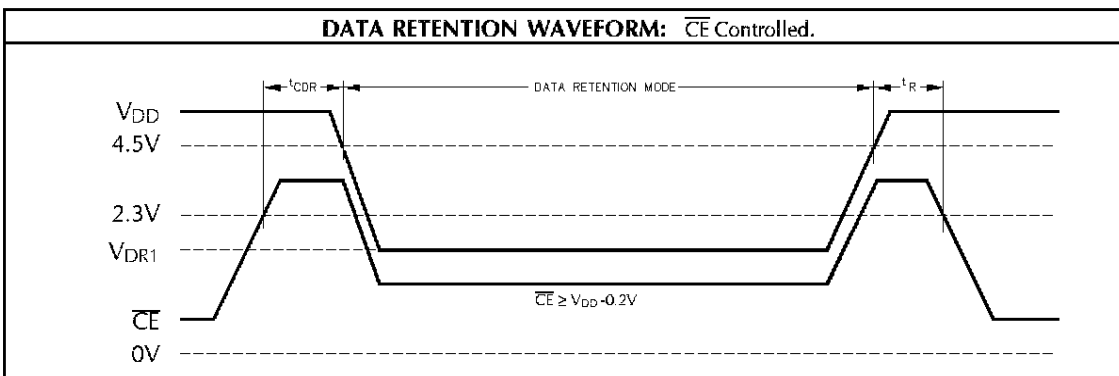
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	C _L	Parameters Measured
1	100pF	except t _{LZ1} , t _{LZ2} , t _{HZ1} , t _{HZ2} , t _{OHZ} , t _{OLZ} , and t _{WHZ}
2	5pF	t _{LZ1} , t _{LZ2} , t _{HZ1} , t _{HZ2} , t _{OHZ} , t _{OLZ} , and t _{WHZ}

Figure 1. Output Load
* Including Probe and Jig Capacitance.

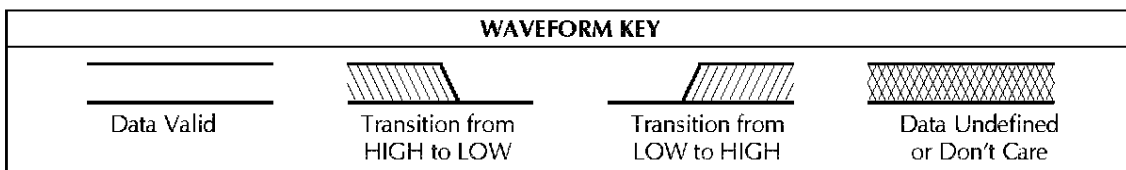
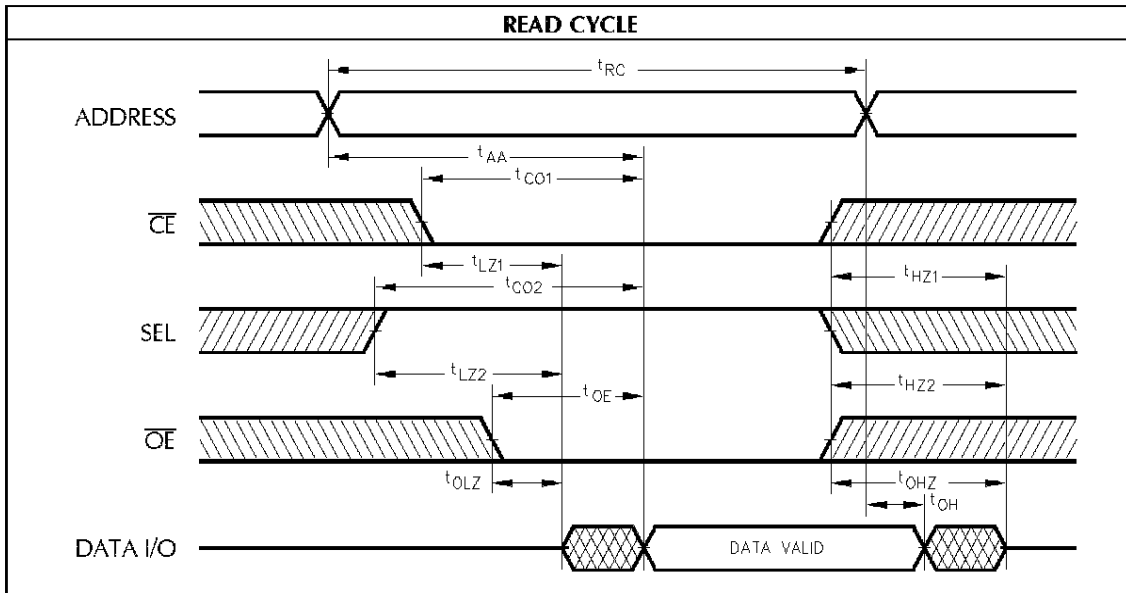


Data Retention AC Characteristics ⁸						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DR}	V _{DD} for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$, SEL $\geq V_{DR} - 0.2V$ or SEL $\leq V_{DR} + 0.2V$	2.0	-	-	V
V _{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t _R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	70ns*		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{RC}	Read Cycle Time	70		85		100		120		150		ns
2	t _{AA}	Address Access Time		70		85		100		120		150	ns
3	t _{CO1}	\overline{CE} to Output Valid		70		85		100		120		150	ns
4	t _{CO2}	SEL to Output Valid		70		85		100		120		150	ns
5	t _{OE}	Output Enable to Output Valid		40		45		50		60		70	ns
6	t _{LZ1}	\overline{CE} to Output in LOW-Z ^{4,5}	5		5		10		10		10		ns
7	t _{LZ2}	SEL to Output in LOW-Z ^{4,5}	5		5		10		10		10		ns
8	t _{OLZ}	Output Enable to Output in LOW-Z ^{4,5}	0		0		0		0		0		ns
9	t _{HZ1}	\overline{CE} to Output in HIGH-Z ^{4,5}		30		30		35		45		50	ns
10	t _{HZ2}	SEL to Output in HIGH-Z ^{4,5}		30		30		35		45		50	ns
11	t _{OHZ}	Output Enable to Output in HIGH-Z ^{4,5}		30		30		35		45		50	ns
12	t _{OH}	Output Hold from Address Change	10		10		10		10		10		ns

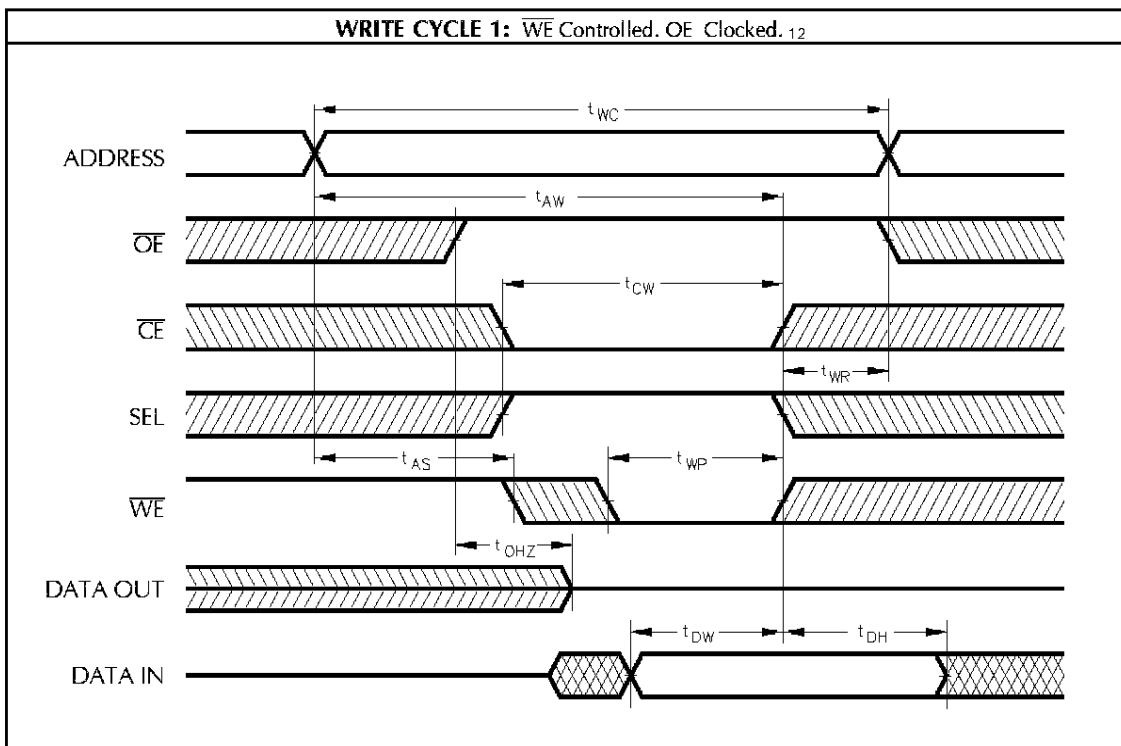
* Available in Commercial Only.

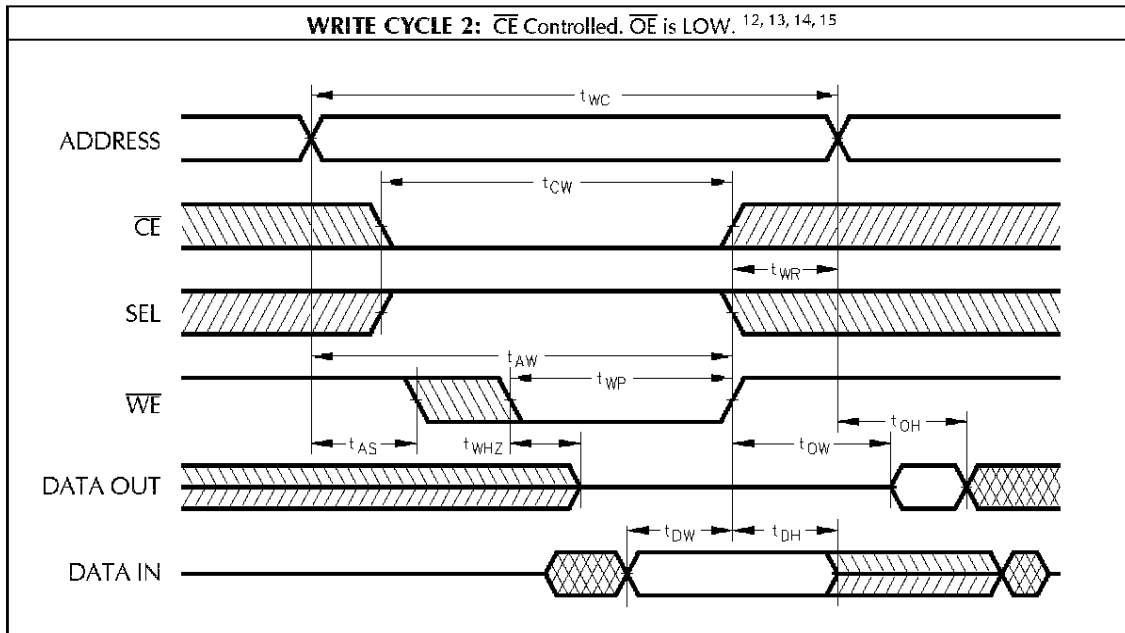


AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6,7} : Over operating ranges													
No.	Symbol	Parameter	70ns*		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	70		85		100		120		150		ns
14	t_{AW}	Address Valid to End of Write	65		75		90		100		120		ns
15	t_{CW}	Chip Enable to End of Write	65		75		90		100		120		ns
16	t_{AS}	Address Set-Up Time ^{9**}	0		0		0		0		0		ns
17	t_{WP}	Write Pulse Width ¹⁰	55		65		75		85		90		ns
18	t_{WR}	Write Recovery Time ¹¹	10		10		10		15		15		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z ^{4,5}		30		30		35		40		45	ns
20	t_{DW}	Data to Write Time Overlap	35		35		40		50		60		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	5		5		5		5		5		ns

* Available in Commercial Only.

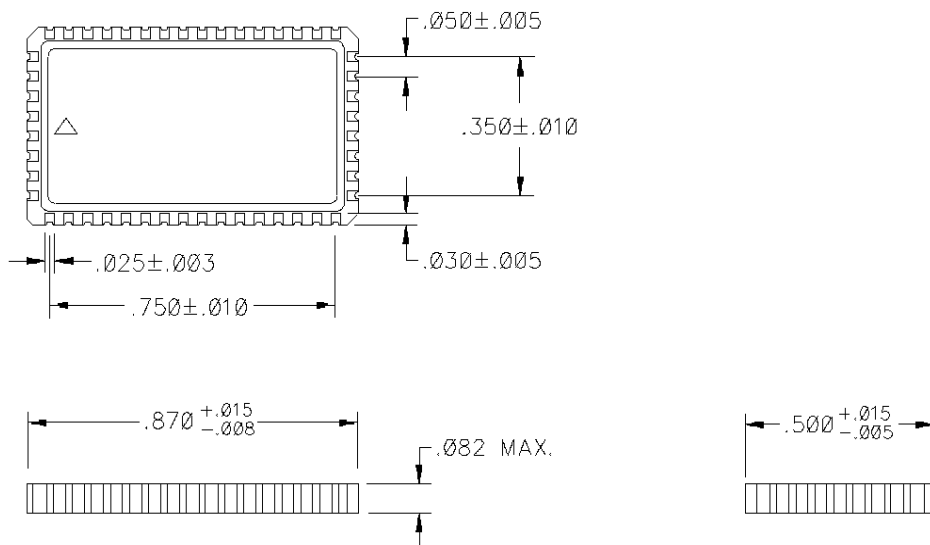
** Valid for both Read and Write Cycles.



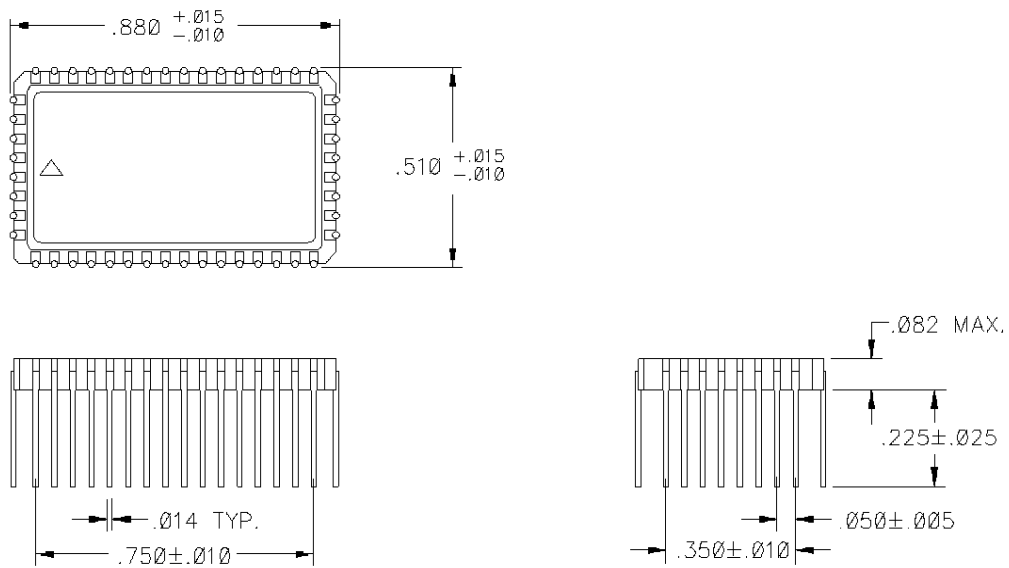
**NOTES:**

- All voltages are with respect to V_{SS} .
- 2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
- Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This parameter is guaranteed and not 100% tested.
- Transition is measured at the point of ± 500 mV from steady state voltage.
- When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
- The outputs are in a high impedance state when \overline{WE} is LOW.
- SEL controls address buffer, \overline{WE} buffer, \overline{CE} buffer and \overline{OE} buffer and D_{IN} buffer. If SEL controls Data Retention Mode, V_{IN} levels (Address, \overline{WE} , \overline{OE} , \overline{CE} , I/O) can be in the high impedance state.
- If \overline{CE} controls Data Retention Mode, SEL must be $SEL \geq V_{DD} - 0.2V$ or $SEL \leq 0.2V$. The other input levels (Address, \overline{WE} , \overline{OE} , I/O) can be in the High Impedance State.
- t_{AS} is measured from the Address Valid to the beginning of Write.
- A Write occurs during the overlap of a LOW \overline{CE} and a LOW \overline{WE} . A Write begins at the latest transition among \overline{CE} going LOW and \overline{WE} going LOW. A Write ends at the earliest transition among \overline{CE} going HIGH and \overline{WE} going HIGH. t_{WP} is measured from the beginning of Write to the end of Write.
- t_{WR} is measured from the earliest of \overline{CE} or \overline{WE} going HIGH to the end of Write Cycle.
- If \overline{CE} goes LOW simultaneously with \overline{WE} going LOW or after \overline{WE} going LOW, the outputs remain in high impedance state.
- D_{OUT} is the same phase of the last written data in this Write Cycle.
- D_{OUT} is the Read data of next Address.
- If \overline{CE} is LOW during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied.

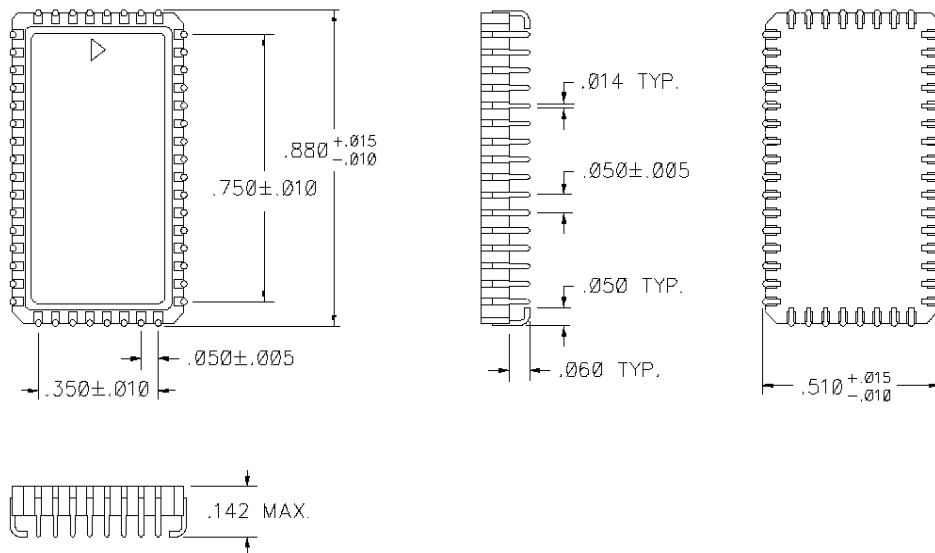
(48 - PIN LEADLESS STACK) MECHANICAL DRAWING



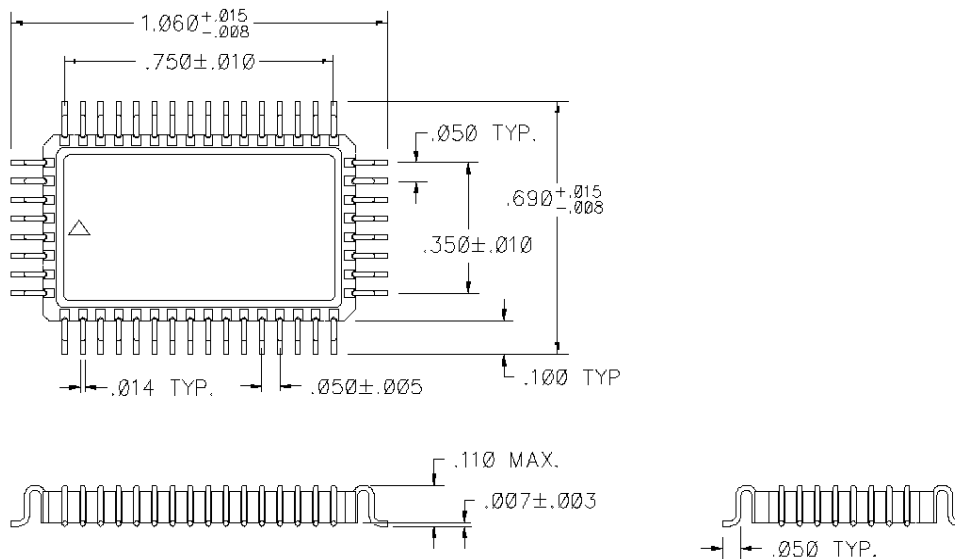
(48 - PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING

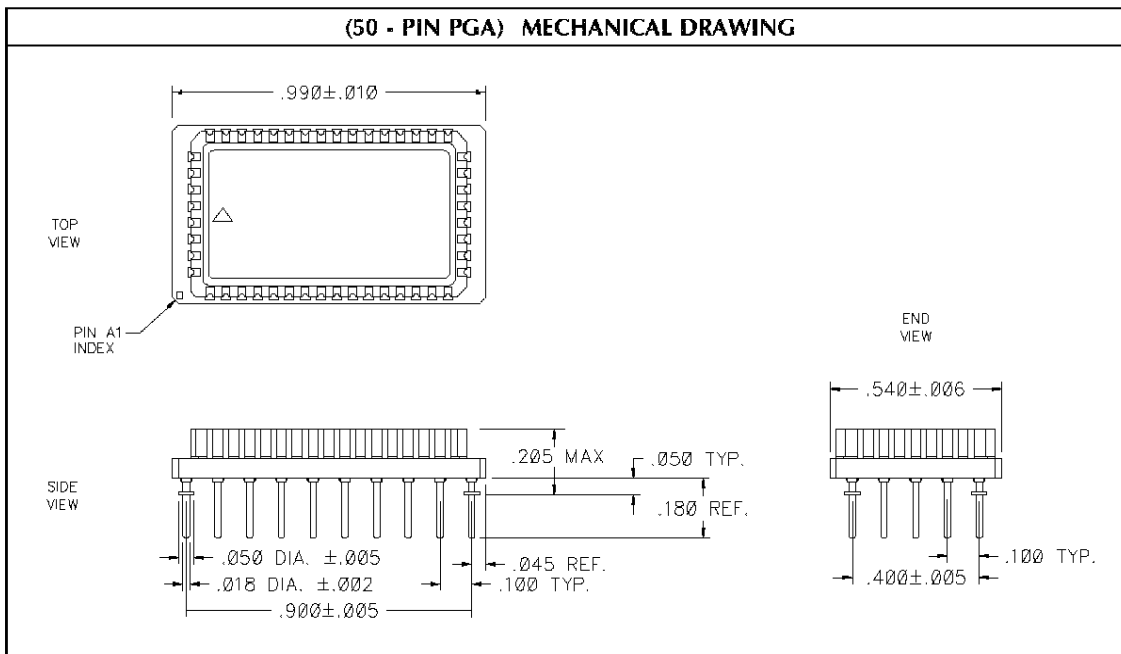


(48 - PIN "J" LEADED STACK) MECHANICAL DRAWING



(48 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING





ORDERING INFORMATION

DP	S	128	X	8	X3	-XX	X	
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	PACKAGE	SPEED	GRADE	
								C COMMERCIAL 0°C to $+70^{\circ}\text{C}$
								I INDUSTRIAL -40°C to $+85^{\circ}\text{C}$
								M MILITARY -55°C to $+125^{\circ}\text{C}$
								B MIL-PROCESSED -55°C to $+125^{\circ}\text{C}$
								70 70ns (COMMERCIAL ONLY)
								85 85ns
								10 100ns
								12 120ns
								15 150ns
								A3 DENSE-STACK PGA (PIN GRID ARRAY)
								H3 GULLWING LEADED SLCC STACK
								I3 THRU-HOLE LEADED SLCC STACK
								J3 "J" LEADED SLCC STACK
								Y3 LEADLESS SLCC STACK
								M MONOLITHIC DEVICE
								X MODULE WITHOUT SUPPORT LOGIC
								CMOS SRAM DEVICES

Dense-Pac Microsystems, Inc.

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