

DESCRIPTION:

The JEDEC compatible DPSD8MX64RW is a high speed 64 Megabyte CMOS Synchronous DRAM DIMM, consists of eight 4Mx4x4 SDRAM devices.

These modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, interleave between internal banks in order to hide precharge time, and the capability to randomly change column address on each clock cycle during a burst.

The DPSD8MX64RW is designed to operate in 3.3V, low power memory systems. An Auto Refresh Mode is provided along with a power saving Power-Down Mode. All inputs, outputs and clocks are LVTTTL-compatible.

FEATURES:

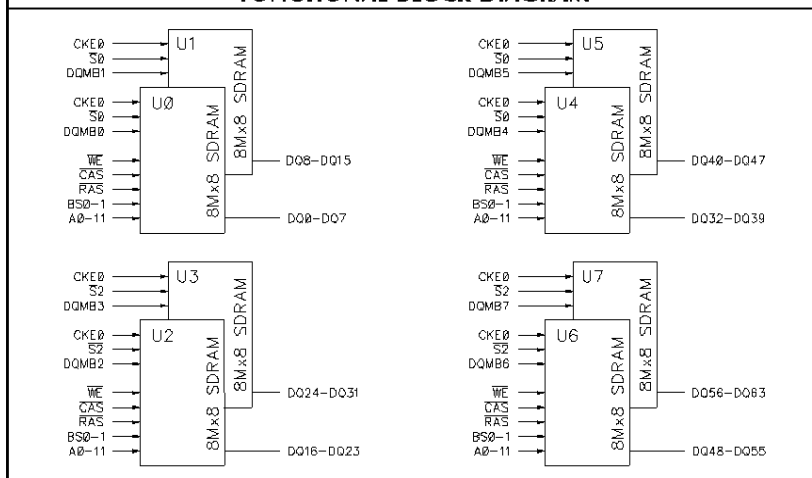
- Configuration: 8 Meg x 64
- 10ns(100MHz)/12ns(83MHz) Devices
- 3.3 ± 0.3 Volt Power Requirement
- Fully Synchronous;
 - All signals registered on positive edge of system clock
- LVTTTL Compatible I/O and Clock
- Internal Pipeline Operation;
 - Column address can be changed every clock cycle
- Un-buffered
- Program Burst Lengths:
 - 1, 2, 4, 8 or Full Page
- Programmable Burst Type, Burst Length, and CAS Latency
- 4096 Cycles / 64 ms Refresh
- Auto Precharge and Auto Refresh Modes
- Serial Presence-Detect (SPD)
- JEDEC Standard 168-Pin DIMM

PIN NAMES	
A0 - A13	Row Address: A0 - A11 Column Address: A0 - A8 Auto Precharge: A10 Bank Select: A12, A13
DQ0 - DQ63	Data In / Data Out
CAS	Column Address Strobe
RAS	Row Address Enable
WE	Data Write Enable
DQMB0-DQMB7	Data Input/Output Mask
CKE0, CKE1	Clock Enables
CK0 - CK3	System Clocks
S0 - S3	Chip Selects
SDA	Serial Presence-Detect Data
SCL	Serial Clock for Presence-Detect
VDD	Power Supply
VSS	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

VSS	1	85	VSS
DQ0	2	86	DQ32
DQ1	3	87	DQ33
DQ2	4	88	DQ34
DQ3	5	89	DQ35
VDD	6	90	VDD
DQ4	7	91	DQ36
DQ5	8	92	DQ37
DQ6	9	93	DQ38
DQ7	10	94	DQ39
DQ8	11	95	DQ40
VSS	12	96	VSS
DQ9	13	97	DQ41
DQ10	14	98	DQ42
DQ11	15	99	DQ43
DQ12	16	100	DQ44
DQ13	17	101	DQ45
VDD	18	102	VDD
DQ14	19	103	DQ46
DQ15	20	104	DQ47
N.C.	21	105	N.C.
N.C.	22	106	N.C.
VSS	23	107	VSS
N.C.	24	108	N.C.
N.C.	25	109	N.C.
VDD	26	110	VDD
WE	27	111	CAS
DQMB0	28	112	DQMB4
DQMB1	29	113	DQMB5
S0	30	114	S1
N.U.	31	115	RAS
VSS	32	116	VSS
A0	33	117	A1
A2	34	118	A3
A4	35	119	A5
A6	36	120	A7
A8	37	121	A9
A10/AP	38	122	BA0
BA1	39	123	A11
VDD	40	124	VDD
VDD	41	125	CK1
CLK0	42	126	A12
VSS	43	127	VSS
N.U.	44	128	CKE0
S2	45	129	S3
DQMB2	46	130	DQMB6
DQMB3	47	131	DQMB7
N.U.	48	132	A13
VDD	49	133	VDD
N.C.	50	134	N.C.
N.C.	51	135	N.C.
N.C.	52	136	N.C.
N.C.	53	137	N.C.
VSS	54	138	VSS
DQ16	55	139	DQ48
DQ17	56	140	DQ49
DQ18	57	141	DQ50
DQ19	58	142	DQ51
VDD	59	143	VDD
DQ20	60	144	DQ52
N.C.	61	145	N.C.
VREF/N.C.	62	146	VREF/N.C.
CKE1	63	147	N.C.
VSS	64	148	VSS
DQ21	65	149	DQ53
DQ22	66	150	DQ54
DQ23	67	151	DQ55
VSS	68	152	VSS
DQ24	69	153	DQ56
DQ25	70	154	DQ57
DQ26	71	155	DQ58
DQ27	72	156	DQ59
VDD	73	157	VDD
DQ28	74	158	DQ60
DQ29	75	159	DQ61
DQ30	76	160	DQ62
DQ31	77	161	DQ63
VSS	78	162	VSS
CK2	79	163	CK3
N.C.	80	164	N.C.
N.C.	81	165	SA0
SDA	82	166	SA1
SCL	83	167	SA2
VDD	84	168	VDD

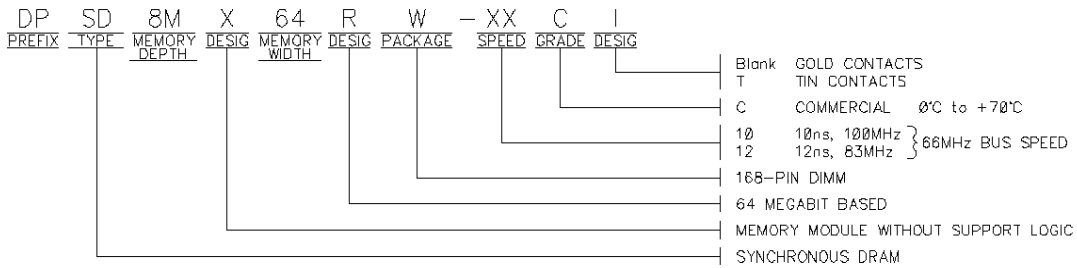
FUNCTIONAL BLOCK DIAGRAM



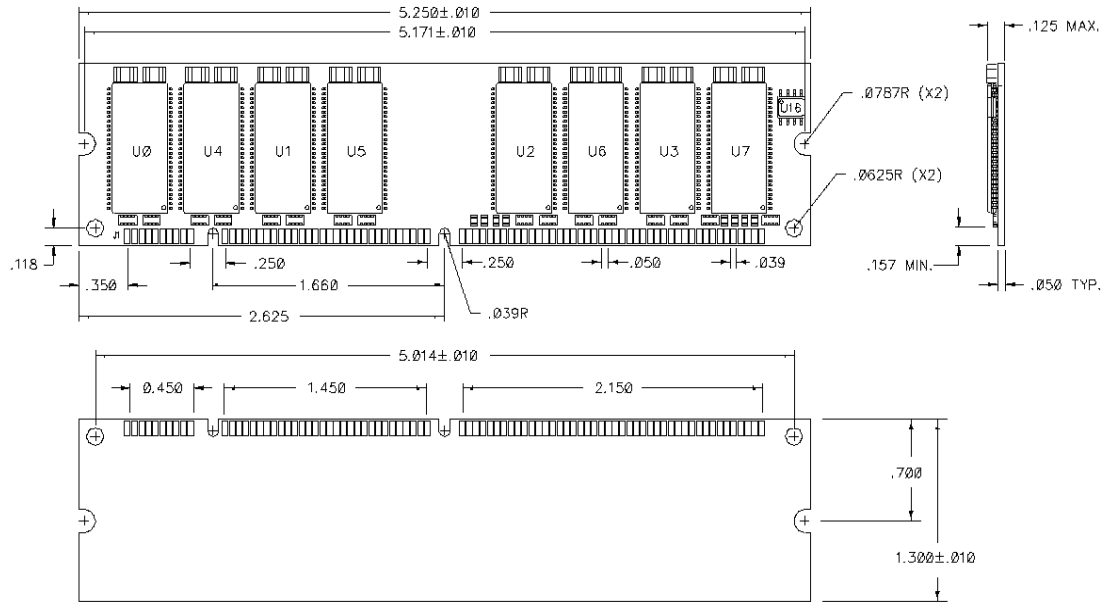
DPSD8MX64RW

Dense-Pac Microsystems, Inc.

ORDERING INFORMATION



MECHANICAL DRAWING



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