




Description

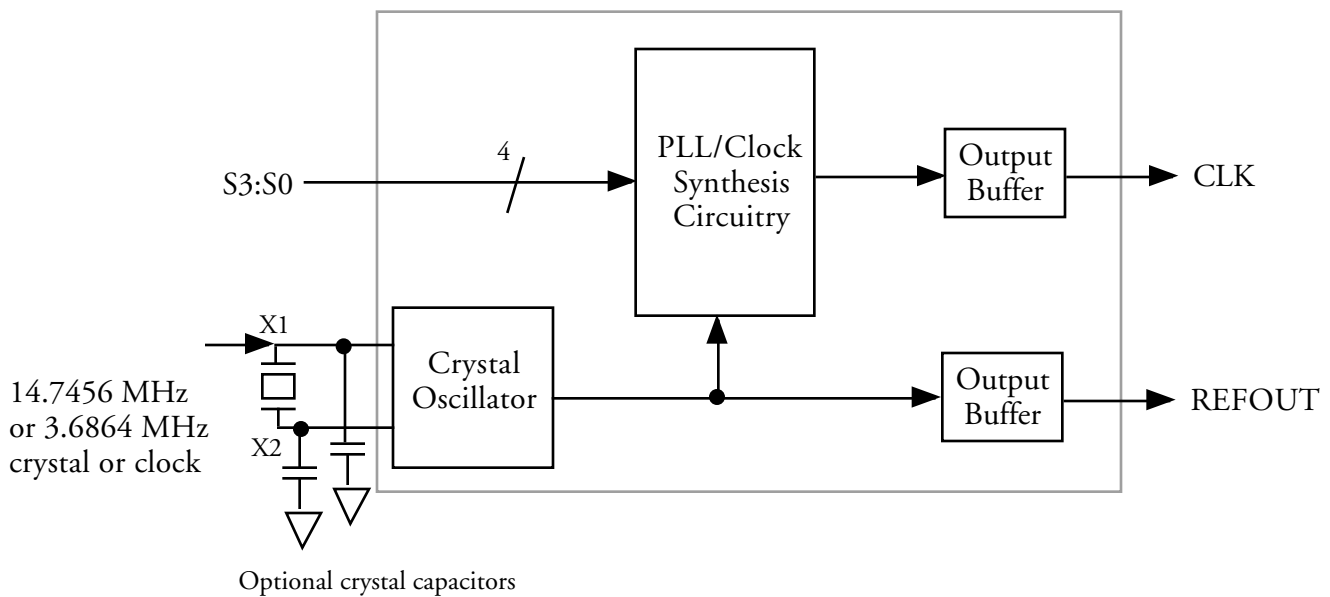
The ICS548-02 is a low cost, low jitter, high performance clock synthesizer designed to produce audio sampling rates for MP3 systems. Using ICS' patented analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 14.7456 MHz or 3.6864 MHz crystal input to produce all of the popular audio sampling frequencies. With the 3.6864 MHz input, the chip provides a clock output, allowing it to drive the Cirrus ARM controller.

ICS manufactures the largest variety of multimedia clock synthesizers for all applications. Consult ICS to eliminate VCXOs, crystals and oscillators from your board.

Features

- Packaged in 16 pin narrow SOIC 
- Ideal for Cirrus Logic's MP3 chips
- Replaces multiple oscillators
- 3.3V or 5V operation
- Uses an inexpensive 3.6864 MHz or 14.7456 MHz crystal, or clock input
- Supports 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz audio sampling rates
- Provides 128fs and 256fs clocks
- Zero ppm synthesis error
- Advanced, low power, sub-micron CMOS process

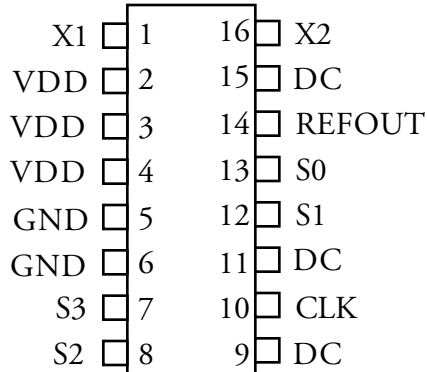
Block Diagram





Pin Assignment

ICS548-02



16 pin narrow (150 mil) SOIC

Output Clock Select Table

S3	S2	S1	S0	Input (MHz)	CLK (MHz)	REFOUT
Pin 7	Pin 8	Pin 12	Pin 13	Pins 1, (16)	Pin 10	Pin 14
0	0	0	0	14.7456	4.096	Off (low)
0	0	0	1	14.7456	5.6448	Off (low)
0	0	1	0	14.7456	6.144	Off (low)
0	0	1	1	14.7456	16.9344	Off (low)
0	1	0	0	14.7456	8.192	Off (low)
0	1	0	1	14.7456	11.2896	Off (low)
0	1	1	0	14.7456	12.288	Off (low)
0	1	1	1	14.7456	24.576	Off (low)
1	0	0	0	3.6864	4.096	3.6864
1	0	0	1	3.6864	5.6448	3.6864
1	0	1	0	3.6864	6.144	3.6864
1	0	1	1	TEST	TEST	TEST
1	1	0	0	3.6864	8.192	3.6864
1	1	0	1	3.6864	11.2896	3.6864
1	1	1	0	3.6864	12.288	3.6864
1	1	1	1	3.6864	2.048	3.6864

Key: 0 = connect directly to GND
1 = connect directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	X1	XI	Crystal connection. Connect to a parallel mode 14.7456 MHz or 3.6864 MHz crystal.
2, 3, 4	VDD	P	Connect to +3.3V or +5V. Must be same at all VDDs.
5, 6	GND	P	Connect to ground.
7	S3	I	Frequency select pin 3. Determines clock outputs per table above.
8	S2	I	Frequency select pin 2. Determines clock outputs per table above.
9, 11, 15	DC	-	Don't Connect. Do not connect anything to these pins.
10	CLK	O	Audio clock output set by status of S0-S3. See table above.
12	S1	I	Frequency select pin 1. Determines clock outputs per table above.
13	S0	I	Frequency select pin 0. Determines clock outputs per table above.
14	REFOUT	O	Buffered reference crystal output clock for 3.6864 MHz crystal (or clock) per table.
16	X2	XO	Crystal connection. Connect to a parallel mode 14.7456 MHz or 3.6864 MHz crystal.

Key: I = Input; O = output; P = power supply connection; XI, XO = crystal connections
The input pins S3:S0 lack pull-ups, so they cannot be left floating. Tie directly to VDD or GND. For a clock input, connect the input to X1, and leave X2 unconnected (floating).

**Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless noted)					
Core Operating Voltage, VDD		3.0		5.5	V
Input High Voltage, VIH, X1 pin only	Clock input only	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, X1 pin only	Clock input only		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Operating Supply Current, IDD	No Load, 14,7456 input		7		mA
Short Circuit Current	CLK output		±50		mA
Input Capacitance	S0, S1, S2, S3		7		pF
Frequency synthesis error	All selections			0	ppm
AC CHARACTERISTICS (VDD = 3.3V unless noted)					
Input Crystal or Clock Frequency			14.7456 or 3.6864		MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40	50	60	%
Maximum Absolute Jitter, short term			±100		ps
One sigma jitter			35		ps

Note: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

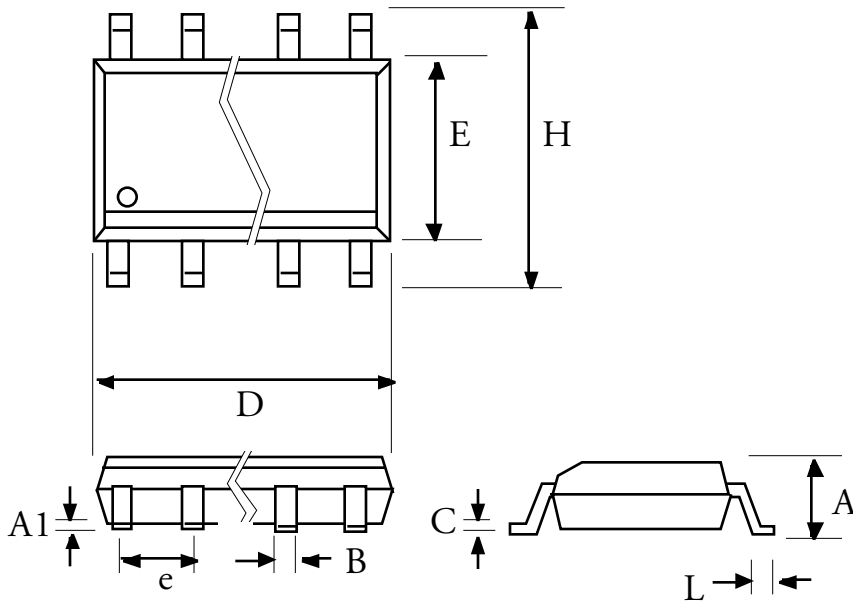
The ICS548-02 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 3 and 5, as close to the ICS548-02 as possible. Other VDDs can be connected to pin 3. A series termination resistor of 33Ω may be used for each clock output. Any unused clock outputs should be left unconnected. The input crystal must be connected as close to the chip as possible. The input crystal should be fundamental mode, parallel resonant, with a load capacitance of 18 pF. For other values of load (or correlation) capacitance, the crystal can be tuned with two identical capacitors to ground, as shown on the block diagram. The value of these two crystal caps should be equal to $(C_L-18)*2$, where C_L is the crystal load capacitance.



Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC publication no. 95.)

16 pin SOIC narrow



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.075	0.098	1.91	2.40
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS548M-02	ICS548M-02	tubes	16 pin SOIC	0-70 °C
ICS548M-02T	ICS548M-02	tape and reel	16 pin SOIC	0-70 °C

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