240pin Unbuffered DDR2 SDRAM MODULE

Based on 64Mx8 DDR2 SDRAM

Features

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 64Mx64 and 128Mx64 DDR2 Unbuffered DIMM based on 64Mx8 DDR2 SDRAM
- Performance:

		PC2-3200	PC2-4200	PC2-5300	Unit
Speed Sort		5A	37B	3C	
DIMM $\overline{CAS}$ Latency		3	4	5	
f_{CK}	Clock Frequency	200	266	333	MHz
t_{CK}	Clock Cycle	5	3.7	3	ns
f_{DQ}	DQ Burst Frequency	400	533	667	MHz

- Intended for 200 MHz, 266MHz, and 333MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8Volt \pm 0.1$
- SDRAM have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/rank) –
  M2Y51264TU88A2B, M2Y51264TU88A0B
  M2U51264TU88A2B, M2U51264TU88A0B
  M2U51264TU88A2F, M2U51264TU88A0F
- 14/10/2 Addressing (row/column/rank) –
  M2Y1G64TU8HA2B, M2Y1G64TU8HA0B
  M2U1G64TU8HA2B, M2U1G64TU8HA0B
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 60-ball FBGA Package
- RoHs compliance –
  M2Y1G64TU8HA2B, M2Y1G64TU8HA0B
  M2Y51264TU88A2B, M2Y51264TU88A0B

Description

M2Y51264TU88A2B, M2Y51264TU88A0B, M2Y1G64TU8HA2B, M2Y1G64TU8HA0B, M2U51264TU88A2B, M2U51264TU88A0B, M2U51264TU88A0F, M2U51264TU88A2F, M2U1G64TU8HA0B and M2U1G64TU8HA2B are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one-rank 64Mx64 and two ranks 128Mx64 high-speed memory array. Modules use eight 64Mx8 (M2Y51264TU88A2B, M2Y51264TU88A0B, M2U51264TU88A2B, M2U51264TU88A0F, M2U51264TU88A2F and M2U51264TU88A0B) and sixteen 64Mx8 (M2Y1G64TU8HA2B, M2Y1G64TU8HA0B, M2U1G64TU88A2B and M2U1G64TU88A0B) DDR2 SDRAMs in FBGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 200MHz (266MHz and 333MHz) clock speeds and achieves high-speed data transfer rates of up to 400MHz (533MHz and 667MHz). Prior to any access operation, the device $\overline{CAS}$ latency and burst / length / operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y1G64TU8HA2B-5A	200MHz (5ns @ CL = 3)	DDR2-400	PC2-3200	128Mx64	Gold	1.8V	Green
M2Y1G64TU8HA0B-5A							
M2U1G64TU8HA2B-5A							
M2U1G64TU8HA0B-5A							
M2Y51264TU88A2B-5A				64Mx64			Green
M2Y51264TU88A0B-5A							
M2U51264TU88A2B-5A							
M2U51264TU88A0B-5A							
M2U51264TU88A0F-5A							
M2U51264TU88A2F-5A							
M2Y1G64TU8HA2B-37B	266MHz (3.7ns @ CL = 4)	DDR2-533	PC2-4200	128Mx64			Green
M2Y1G64TU8HA0B-37B							
M2U1G64TU8HA2B-37B							
M2U1G64TU8HA0B-37B							
M2Y51264TU88A2B-37B				64Mx64			Green
M2Y51264TU88A0B-37B							
M2U51264TU88A2B-37B							
M2U51264TU88A0B-37B							
M2U51264TU88A0F-37B							
M2U51264TU88A2F-37B							
M2Y1G64TU8HA2B-3C	333MHz (3ns @ CL = 5)	DDR2-667	PC2-5300	128Mx64			Green
M2Y1G64TU8HA0B-3C							
M2U1G64TU8HA2B-3C							
M2U1G64TU8HA0B-3C							
M2Y51264TU88A2B-3C				64Mx64			Green
M2Y51264TU88A0B-3C							
M2U51264TU88A2B-3C							
M2U51264TU88A0B-3C							
M2U51264TU88A0F-3C							
M2U51264TU88A2F-3C							

Pin Description

CK0, $\overline{CK0}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM8/DQS9-17	Input Data Mask/High Data Strobes
$\overline{CAS}$	Column Address Strobe	$\overline{DQS0}$-$\overline{DQS17}$	Differential data strobes
$\overline{WE}$	Write Enable	V_{DD}	Power (1.8V)
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	V_{REF}	Ref. Voltage for SSTL_18 inputs
A0-A9, A11-A13	Address Inputs	V_{DDSPD}	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	V_{SS}	Ground
BA0, BA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
$\overline{RESET}$	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	Active termination control lines	SA0-2	Serial Presence Detect Address Inputs
NC	No Connect		

Pinout

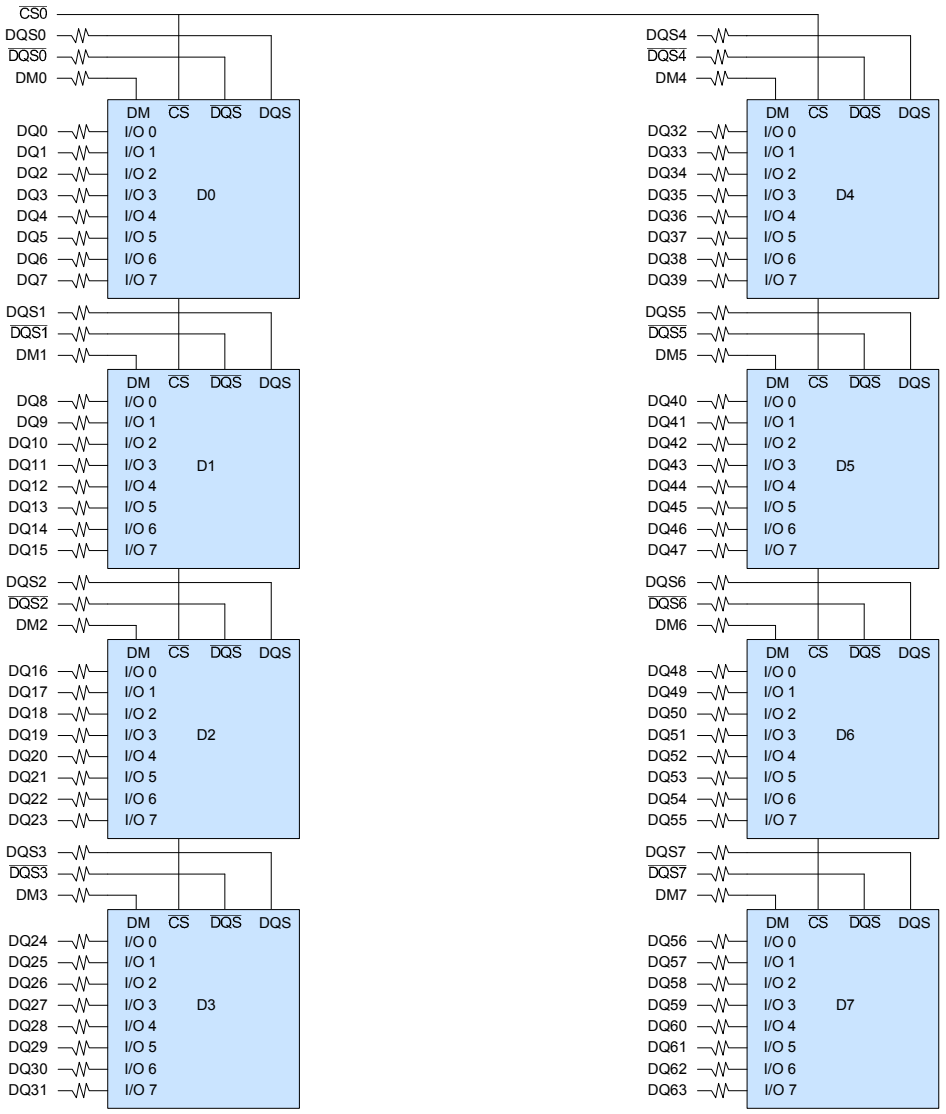
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	42	NC	82	V_{SS}	121	V_{SS}	162	NC	202	DM4
2	V_{SS}	43	NC	83	$\overline{DQS4}$	122	DQ4	163	V_{SS}	203	NC
3	DQ0	44	V_{SS}	84	DQS4	123	DQ5	164	NC	204	V_{SS}
4	DQ1	45	NC	85	V_{SS}	124	V_{SS}	165	NC	205	DQ38
5	V_{SS}	46	NC	86	DQ34	125	DM0, DQS9	166	V_{SS}	206	DQ39
6	$\overline{DQS0}$	47	V_{SS}	87	DQ35	126	$\overline{DQS9}$	167	NC	207	V_{SS}
7	DQS0	48	NC	88	V_{SS}	127	V_{SS}	168	NC	208	DQ44
8	V_{SS}	49	NC	89	DQ40	128	DQ6	169	V_{SS}	209	DQ45
9	DQ2	50	V_{SS}	90	DQ41	129	DQ7	170	V_{DDQ}	210	V_{SS}
10	DQ3	51	V_{DDQ}	91	V_{SS}	130	V_{SS}	171	CKE1	211	DM5
11	V_{SS}	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	V_{DD}	212	NC
12	DQ8	53	V_{DD}	93	DQS5	132	DQ13	173	NC	213	V_{SS}
13	DQ9	54	NC	94	V_{SS}	133	V_{SS}	174	NC	214	DQ46
14	V_{SS}	55	NC	95	DQ42	134	DM1, DQS10	175	V_{DDQ}	215	DQ47
15	$\overline{DQS1}$	56	V_{DDQ}	96	DQ43	135	$\overline{DQS10}$	176	A12	216	V_{SS}
16	DQS1	57	A11	97	V_{SS}	136	V_{SS}	177	A9	217	DQ52
17	V_{SS}	58	A7	98	DQ48	137	CK1	178	V_{DD}	218	DQ53
18	NC	59	V_{DD}	99	DQ49	138	$\overline{CK1}$	179	A8	219	V_{SS}
19	NC	60	A5	100	V_{SS}	139	V_{SS}	180	A6	220	CK2
20	V_{SS}	61	A4	101	SA2	140	DQ14	181	V_{DDQ}	221	$\overline{CK2}$
21	DQ10	62	V_{DDQ}	102	NC	141	DQ15	182	A3	222	V_{SS}
22	DQ11	63	A2	103	V_{SS}	142	V_{SS}	183	A1	223	DM6
23	V_{SS}	64	V_{DD}	104	$\overline{DQS6}$	143	DQ20	184	V_{DD}	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V_{SS}
25	DQ17	65	V_{SS}	106	V_{SS}	145	V_{SS}	185	CK0	226	DQ54
26	V_{SS}	66	V_{SS}	107	DQ50	146	DM2	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	VDD	108	DQ51	147	NC	187	VDD	228	V_{SS}
28	DQS2	68	NC	109	V_{SS}	148	V_{SS}	188	A0	229	DQ60
29	V_{SS}	69	VDD	110	DQ56	149	DQ22	189	V_{DD}	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V_{SS}
31	DQ19	71	BA0	112	V_{SS}	151	V_{SS}	191	V_{DDQ}	232	DM7
32	V_{SS}	72	VDDQ	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	NC
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{CS0}$	234	V_{SS}
34	DQ25	74	$\overline{CAS}$	115	V_{SS}	154	V_{SS}	194	V_{DDQ}	235	DQ62
35	V_{SS}	75	V_{DDQ}	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	$\overline{CS1}$	117	DQ59	156	NC	196	A13	237	V_{SS}
37	DQS3	77	ODT1	118	V_{SS}	157	V_{SS}	197	V_{DD}	238	V_{DDSPD}
38	V_{SS}	78	V_{DDQ}	119	SDA	158	DQ30	198	V_{SS}	239	SA0
39	DQ26	79	V_{SS}	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V_{SS}	200	DQ37		
41	V_{SS}	81	DQ33			161	NC	201	V_{SS}		

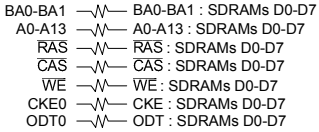
Input/Output Functional Description

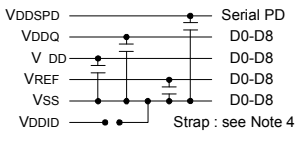
Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive differential clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative edge of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the command to be executed.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

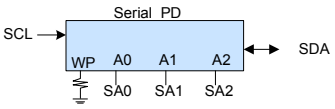
(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)





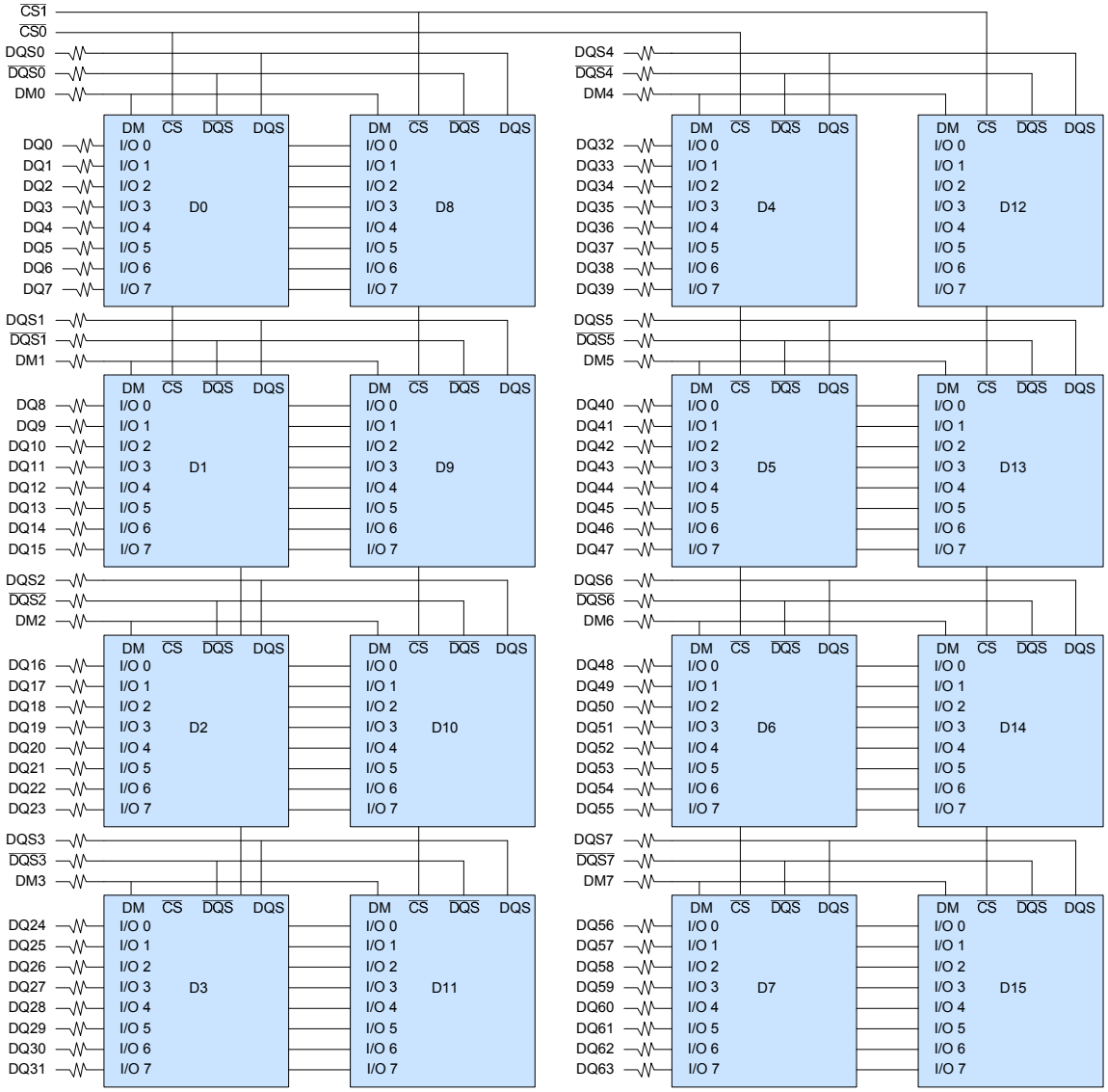


Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%

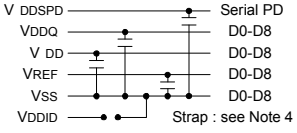


Functional Block Diagram

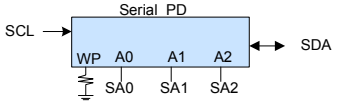
(1GB, 2 Rank, 64Mx8 DDR2 SDRAMs)



BA0-BA1 — BA0-BA1 : SDRAMs D0-D15
A0-A13 — A0-A13 : SDRAMs D0-D15
$\overline{RAS}$ — $\overline{RAS}$: SDRAMs D0-D15
$\overline{CAS}$ — $\overline{CAS}$: SDRAMs D0-D15
$\overline{WE}$ — $\overline{WE}$: SDRAMs D0-D15
CKE0 — CKE : SDRAMs D0-D7
CKE1 — CKE : SDRAMs D8-D15
ODT0 — ODT : SDRAMs D0-D7
ODT1 — ODT : SDRAMs D8-D15



Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/$\overline{DQS}$ resistors are 22 Ohms +/- 5%
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%



Serial Presence Detect – Part 1 of 2 (512MB)

64Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-5A	-37B	-3C	-5A	-37B	-3C	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	14			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank, Package, and Height	1 rank, Height=30mm			60			
6	Data Width of this Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at Maximum Support $\overline{CAS}$ Latency CL=5	5ns	3.75ns	3ns	50	3D	30	
10	DDR2 SDRAM Device Access Time (t_{ac}) from Clock at CL=5	±0.6ns	±0.5ns	±0.45ns	60	50	45	
11	DIMM Configuration Type	Non – ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDRII SDRAM Width	X8			08			
14	Error Checking DDRII SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	3/4/5			38			
19	DIMM Mechanical Characteristics	X <= 4.1mm			01			
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.35mm)			02			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver			01		03	
23	Minimum Clock Cycle at CL=4	5ns	3.75ns	3.75ns	50	3D		
24	Maximum Data Access Time (t_{ac}) from Clock at CL=4	0.6ns	0.5ns	0.5ns	60	50		
25	Minimum Clock Cycle Time at CL=3	5ns			50			
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3	0.6ns			60			
27	Minimum Row Precharge Time (t_{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns			1E			
29	Minimum RAS to CAS delay (t_{RCD})	15ns			3C			
30	Minimum Active to Precharge Time (t_{RAS})	45ns			2D			
31	Module Bank Density	512MB			80			
32	Address and Command Input Setup Time Before Clock (t_{IS})	0.35ns	0.25ns	0.2ns	35	25	20	
33	Address and Command Input Hold Time After Clock (t_{IH})	0.475ns	0.375ns	0.275ns	47	37	27	
34	Data Input Setup Time Before Clock (t_{DS})	0.15ns	0.1ns	0.1ns	15	10	10	
35	Data Input Hold Time After Clock (t_{DH})	0.275ns	0.225ns	0.175ns	27	22	17	
36	Write Recovery Time (t_{WR})	15ns			3C			
37	Internal Write to Read Command delay (t_{WTR})	10ns	7.5ns	7.5ns	28	1E	1E	
38	Internal Read to Precharge Command delay (t_{RTP})	7.5ns			1E			
39	Memory Analysis Probe Characteristics	Undefined			00			

Serial Presence Detect – Part 2 of 2 (512MB)

64Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-5A	-37B	-3C	-5A	-37B	-3C	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns			00			
41	Minimum Core Cycle Time (t_{RC})	60ns			3C			
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns			69			
43	Maximum Clock Cycle Time (t_{CK} max)	8ns			80			
44	Max. DQS-DQ Skew Factor (t_{QHS})	0.35ns	0.3ns	0.24ns	23	1E	18	
45	Read Data Hold Skew Factor (t_{QHS})	0.45ns	0.4ns	0.34ns	2D	28	22	
46	PLL Relock Time	N/A			00			
47	Tcasemax	1˚C	1˚C	3˚C	51	51	52	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	122˚C/W			7A			
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	16˚C	18˚C	20˚C	43	4B	53	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	37˚C	47˚C	58˚C	25	2E	3A	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	39˚C	39˚C	39˚C	27	27	27	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	27˚C	33˚C	39˚C	1B	21	27	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	30˚C	37˚C	44˚C	1E	25	2C	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	23˚C	23˚C	28˚C	17	17	1C	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	23˚C	26˚C	38˚C	2E	34	4C	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	30˚C	35˚C	37˚C	1E	23	25	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	35˚C	37˚C	40˚C	23	25	28	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00			
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00			
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00			
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00			00			
62	SPD Revision	1.2			12			
63	Checksum Data	Checksum Data			50	F7	F9	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72-255	Reserved	Undefined			--			

Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 2 BANKS UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-5A	-37B	-3C	-5A	-37B	-3C	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	14			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank, Package, and Height	2 rank, Height=30mm			61			
6	Data Width of this Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at Maximum Support $\overline{CAS}$ Latency CL=5	5ns	3.75ns	3ns	50	3D	30	
10	DDR2 SDRAM Device Access Time (t_{ac}) from Clock at CL=5	±0.6ns	±0.5ns	±0.45ns	60	50	45	
11	DIMM Configuration Type	Non – ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDRII SDRAM Width	X8			08			
14	Error Checking DDRII SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	3/4/5			38			
19	DIMM Mechanical Characteristics	X <= 4.1mm			01			
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.35mm)			02			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver			01		03	
23	Minimum Clock Cycle at CL=4	5ns	3.75ns	3.75ns	50	3D		
24	Maximum Data Access Time (t_{ac}) from Clock at CL=4	0.6ns	0.5ns	0.5ns	60	50		
25	Minimum Clock Cycle Time at CL=3	5ns			50			
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3	0.6ns			60			
27	Minimum Row Precharge Time (t_{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns			1E			
29	Minimum RAS to CAS delay (t_{RCD})	15ns			3C			
30	Minimum Active to Precharge Time (t_{RAS})	45ns			2D			
31	Module Bank Density	512MB			80			
32	Address and Command Input Setup Time Before Clock (t_{IS})	0.35ns	0.25ns	0.2ns	35	25	20	
33	Address and Command Input Hold Time After Clock (t_{IH})	0.475ns	0.375ns	0.275ns	47	37	27	
34	Data Input Setup Time Before Clock (t_{DS})	0.15ns	0.1ns	0.1ns	15	10	10	
35	Data Input Hold Time After Clock (t_{DH})	0.275ns	0.225ns	0.175ns	27	22	17	
36	Write Recovery Time (t_{WR})	15ns			3C			
37	Internal Write to Read Command delay (t_{WTR})	10ns	7.5ns	7.5ns	28	1E	1E	
38	Internal Read to Precharge Command delay (t_{RTP})	7.5ns			1E			
39	Memory Analysis Probe Characteristics	Undefined			00			

Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx64 2 BANKS UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		-5A	-37B	-3C	-5A	-37B	-3C	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of t_{RC} and t_{RFC} are 0, t_{RFC} is less than 256ns			00			
41	Minimum Core Cycle Time (t_{RC})	60ns			3C			
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns			69			
43	Maximum Clock Cycle Time (t_{CK} max)	8ns			80			
44	Max. DQS-DQ Skew Factor (t_{QHS})	0.35ns	0.3ns	0.24ns	23	1E	18	
45	Read Data Hold Skew Factor (t_{QHS})	0.45ns	0.4ns	0.34ns	2D	28	22	
46	PLL Relock Time	N/A			00			
47	Tcasemax	1˚C	1˚C	3˚C	51	51	52	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	122˚C/W			7A			
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	16˚C	18˚C	20˚C	43	4B	53	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	37˚C	47˚C	58˚C	25	2E	3A	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	39˚C	39˚C	39˚C	27	27	27	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	27˚C	33˚C	39˚C	1B	21	27	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	30˚C	37˚C	44˚C	1E	25	2C	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	23˚C	23˚C	28˚C	17	17	1C	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	23˚C	26˚C	38˚C	2E	34	4C	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	30˚C	35˚C	37˚C	1E	23	25	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	35˚C	37˚C	40˚C	23	25	28	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00			
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00			
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00			
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00			00			
62	SPD Revision	1.2			12			
63	Checksum Data	Checksum Data			51	F8	FA	
64-255	Reserved	Undefined			--			

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to +2.3	V
V_{DD}	Voltage on VDD pins relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.5 to +2.3	V
V_{DDL}	Voltage on VDDL pins relative to Vss	-0.5 to +2.3	V
T_{STG}	Storage Temperature (Plastic)	-55 to +100	℃

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	℃	1

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85℃ ➔ t_{REFI} = 3.9 µs

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDL}	DLL Supply Voltage	1.7	1.9	V	1
V_{DDQ}	Output Supply Voltage	1.7	1.9	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	Input Reference Voltage	0.49V_{DDQ}	0.51V_{DDQ}	V	1, 2
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF} + 0.04	V	3

Note:
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.

Input AC/DC logic level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH\ (AC)}$	Input High (Logic1) Voltage	V_{REF} + 0.250	-	V	1
$V_{IL\ (AC)}$	Input Low (Logic0) Voltage	-	V_{REF} - 0.250	V	1
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	V_{REF} - 0.125	V	1

On Die Termination (ODT) Current

Symbol	Parameter	Min	Max	Units	EMRS(1) State
IODTO	Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	5	7.5	mA/DQ	A6=0, A2=1
		2.5	3.75	mA/DQ	A6=1, A2=0
IODTT	Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING	10	15	mA/DQ	A6=0, A2=1
		5	7.5	mA/DQ	A6=1, A2=0

Operating, Standby, and Refresh Currents

T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-3200 (-5A)	PC2-4200 (-37B)	PC2-5300 (-3C)	Unit	Notes
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	520	560	600	mA	
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	560	640	720	mA	
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	40	40	40	mA	
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	256	320	400	mA	
I_{DD2Q}	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	-	-	320		
I_{DD3PF}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	104	128	152	mA	
I_{DD3PS}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	40	40	48	mA	
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	280	336	400	mA	
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	640	720	1040	mA	
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	600	760	1120	mA	
I_{DD5}	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	1040	1200	1280	mA	
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	40	40	40	mA	
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	1200	1280	1360	mA	

Note:
Module IDD was calculated from component IDD. It may different from the actual measurement.

Operating, Standby, and Refresh Currents

T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-3200 (-5A)	PC2-4200 (-37B)	PC2-5300 (-3C)	Unit	Notes
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	776	880	1000	mA	
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	816	960	1120	mA	
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	80	80	80	mA	
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	512	640	800	mA	
I_{DD2Q}	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	-	-	640		
I_{DD3PF}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	208	256	304	mA	
I_{DD3PS}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	80	80	96	mA	
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	536	656	800	mA	
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	896	1040	1440	mA	
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = t_{CK} (MIN)	856	1080	1520	mA	
I_{DD5}	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	1296	1520	1680	mA	
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	80	80	80	mA	
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	1456	1600	1760	mA	

Note:
Module IDD was calculated from component IDD. It may different from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-5A (DDR2-400)		-37B (DDR2-533)		-3C (DDR2-667)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	DQ output access time from CK/$\overline{CK}$	-0.6	0.6	-0.5	0.5	-0.45	0.45	ns
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$	-0.5	0.5	-0.45	0.45	-0.4	0.4	ns
t_{CH}	CK high-level width	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	CK low-level width	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	Min(t_{CL}, t_{CH})	-	Min(t_{CL}, t_{CH})	-	Min(t_{CL}, t_{CH})	-	t_{CK}
t_{CK}	Clock cycle time	5	8	3.75	8	3	8	ns
t_{DH}	DQ and DM input hold time(differential data strobe)	0.275	-	0.225	-	0.175	-	ns
t_{DS}	DQ and DM input setup time(differential data strobe)	0.15	-	0.1	-	0.1	-	ns
t_{IPW}	Input pulse width	0.6	-	0.6	-	0.6	-	t_{CK}
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	t_{CK}
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$	-	t_{AC} max	-	t_{AC} max	-	t_{AC} max	ns
$t_{LZ(DQ)}$	Data-out low-impedance time from CK/$\overline{CK}$	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	ns
$t_{LZ(DQS)}$	DQS low-impedance time from CK/$\overline{CK}$	t_{AC} min	t_{AC} max	t_{AC} min	t_{AC} max	t_{AC} min	t_{AC} max	ns
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.35	-	0.3	0.24		ns
t_{QHS}	Data hold Skew Factor	-	0.45	-	0.4	0.34		ns
t_{QH}	Data output hold time from DQS	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	ns
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	0.25	-0.25	0.25	t_{CK}
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	t_{CK}
t_{MRD}	Mode register set command cycle time	2	-	2	-	2	-	t_{CK}
t_{WPST}	Write postamble	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{WPRE}	Write preamble	0.35	-	0.35	-	0.35	-	t_{CK}
t_{IH}	Address and control input hold time	0.475	-	0.375	-	0.275	-	ns
t_{IS}	Address and control input setup time	0.35	-	0.35	-	0.2	-	ns
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	0.35		t_{CK}
t_{RPST}	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
t_{RRD}	Active bank A to Active bank B command	7.5	-	7.5	-	10	-	ns
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	t_{IS}+t_{CK}+ t_{IH}	-	t_{IS}+t_{CK}+ t_{IH}	-	t_{IS}+t_{CK}+ t_{IH}	-	ns
t_{REFI}	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	7.8						us
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	3.9						us
t_{OIT}	OCD drive mode output delay	0	12	0	12	0	12	ns
t_{RFC}	Auto-Refresh to Active/Auto-Refresh command period	105						ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$	2	-	2	-	2	0	t_{CK}

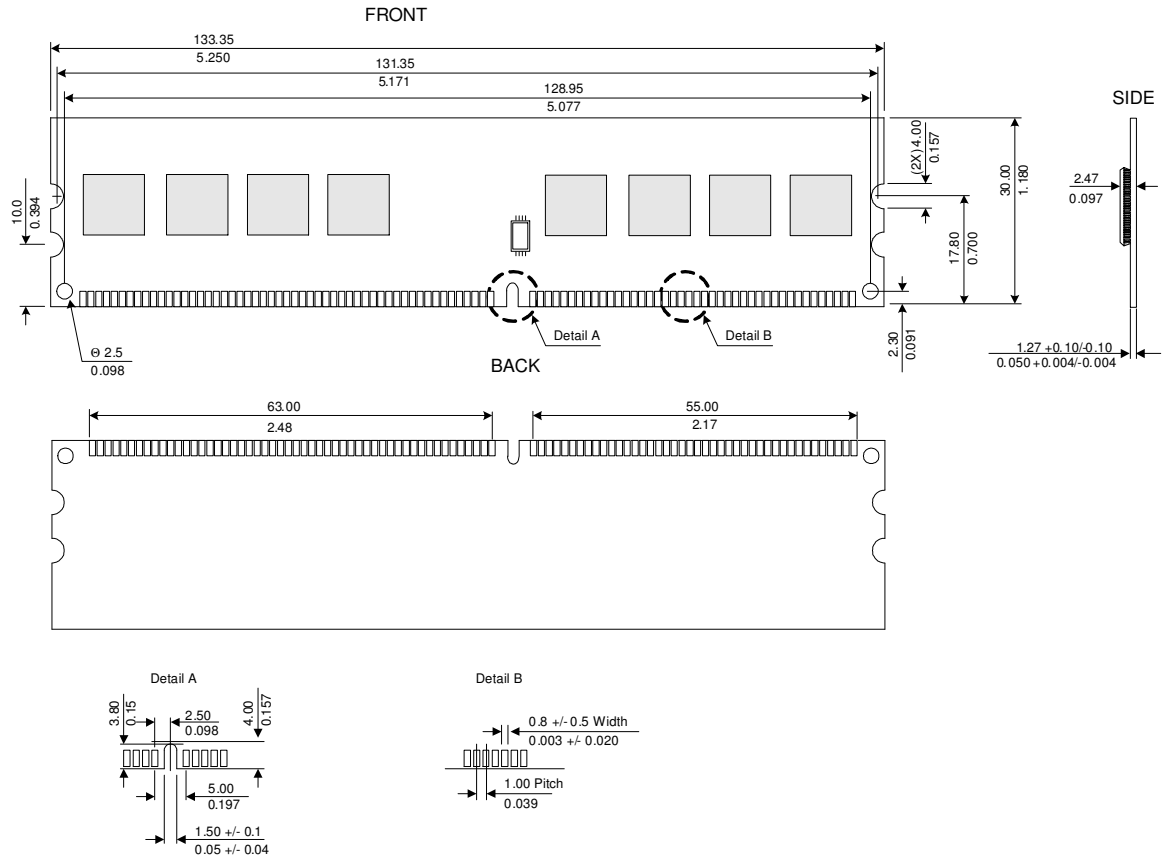
AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE}= 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-5A (DDR2-400)		-37B (DDR2-533)		-3C (DDR2-667)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tWR	Write recovery time without Auto-Precharge	15	-	15	-	15		ns
WR	Write recovery time with Auto-Precharge	t_{WR}/t_{CK}		t_{WR}/t_{CK}		t_{WR}/t_{CK}		
tDAL	Auto precharge write recovery + precharge time	WR + t_{RP}	-	WR + t_{RP}	-	WR + t_{RP}		tCK
tWTR	Internal write to read command delay	10	-	7.5	-	10		ns
tRTP	Internal read to precharge command delay	7.5		7.5		7.5		ns
tXSNR	Exit self refresh to a Non-read command	t_{RFC} + 10		t_{RFC} + 10		t_{RFC} + 10		ns
tXSRD	Exit self refresh to a Read command	200		200		200		tCK
tXP	Exit precharge power down to any Non- read command	2	-	2	-	2		tCK
tXARD	Exit active power down to read command	2	-	2	-	2		tCK
tXARDS	Exit active power down to read command	6 - AL		6 - AL		6 - AL		tCK
tCKE	CKE minimum pulse width	3		3		3		tCK
	ODT							
tAOND	ODT turn-on delay	2						tCK
tAON	ODT turn-on	t_{AC}(min)	t_{AC}(max) +1	t_{AC}(min)	t_{AC}(max) +1	t_{AC}(min)	t_{AC}(max) +1	ns
tAONPD	ODT turn-on (Power down mode)	t_{AC}(min) +2	$2t_{CK}$ + t_{AC}(max) +1	t_{AC}(min) +2	$2t_{CK}$ + t_{AC}(max) +1	t_{AC}(min) +2	$2t_{CK}$ + t_{AC}(max) +1	ns
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	tCK
tAOF	ODT turn-off	t_{AC}(min)	t_{AC}(max) +0.6	t_{AC}(min)	t_{AC}(max) +0.6	t_{AC}(min)	t_{AC}(max) +0.6	ns
tAOFPD	ODT turn-off (Power down mode)	t_{AC}(min) + 2	$2.5t_{CK}$ + t_{AC}(max) +1	t_{AC}(min) + 2	$2.5t_{CK}$ + t_{AC}(max) +1	t_{AC}(min) + 2	$2.5t_{CK}$ + t_{AC}(max) +1	ns
tANPD	ODT to power down entry latency	3	-	3	-	3	-	tCK
tAXPD	ODT power down exit latency	8	-	8	-	8	-	tCK
	Speed Grade Definition							
tRAS	Row Active Time	40	70000	45	70000	45	70000	ns
tRC	Row Cycle Time	55	-	60	-	60	-	ns
tRCD	RAS to CAS delay	15	-	15	-	15	-	ns
tRP	Row Precharge Time	15	-	15	-	15	-	ns

Package Dimensions

(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)



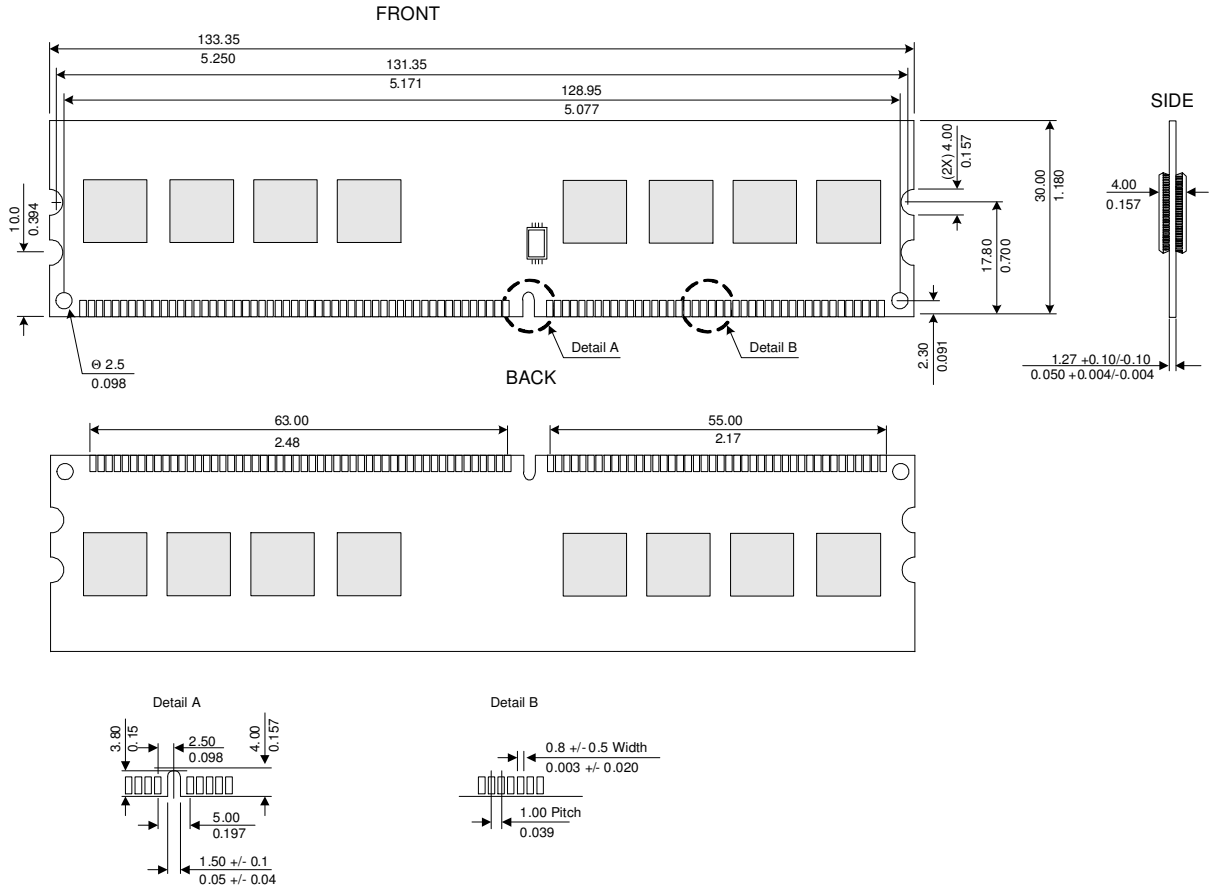
Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated

Units: Millimeters (Inches)

* Device position is only for reference.

Package Dimensions

(1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

* Device position is only for reference.

Revision Log

Rev	Date	Modification
1.0	08/2006	Official Release