240pin Unbuffered DDR2 SDRAM MODULE

Based on 64Mx8 DDR2 SDRAM

Features

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 64Mx64 and 128Mx64 DDR2 Unbuffered DIMM based on 64Mx8 DDR2 SDRAM
- Performance:

		PC2-4200	PC2-5300	Unit
Speed Sort		37B	3C	
DIMM $\overline{CAS}$ Latency*		4	5	
f_{CK}	Clock Frequency	266	333	MHz
t_{CK}	Clock Cycle	3.75	3	ns
f_{DQ}	DQ Burst Frequency	533	667	MHz

- Intended for 266MHz and 333MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ}$ = 1.8Volt ± 0.1
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Write Latency = Read Latency - 1
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/1 Addressing (row/column/bank) – 512MB
- 14/10/2 Addressing (row/column/bank) – 1GB
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- On Die Termination (ODT)
- Gold contacts
- SDRAMs in TSOP Package
- RoHS Compliance

Description

M2Y51264TU88A2G and M2Y1G64TU8HA2G are 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one-rank 64Mx64 and two ranks 128Mx64 high-speed memory array. Modules use eight 64Mx8 (M2Y51264TU88A2G) and sixteen 64Mx8 (M2Y1G64TU8HA2G) DDR2 SDRAMs in TSOP packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 266MHZ (333MHz) clock speeds and achieves high-speed data transfer rates of up to 533MHz (667MHz). Prior to any access operation, the device $\overline{CAS}$ latency and burst / length / operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y51264TU88A2G-37B	266MHz (3.75ns @ CL = 4)	DDR2-533	PC2-4200	64Mx64	Gold	1.8V	
M2Y1G64TU8HA2G-37B				128Mx64			
M2Y51264TU88A2G-3C	333MHz (3ns @ CL = 5)	DDR2-667	PC2-5300	64Mx64			
M2Y1G64TU8HA2G-3C				128Mx64			

Pin Description

CK0, $\overline{CK0}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM7	Input Data Mask/High Data Strobes
$\overline{CAS}$	Column Address Strobe	$\overline{DQS0}$-$\overline{DQS17}$	Differential data strobes
$\overline{WE}$	Write Enable	V_{DD}	Power (1.8V)
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	V_{REF}	Ref. Voltage for SSTL_18 inputs
A0-A9, A11-A13	Address Inputs	V_{DDSPD}	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	V_{SS}	Ground
BA0, BA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
$\overline{RESET}$	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	Active termination control lines	SA0-2	Serial Presence Detect Address Inputs
NC	No Connect		

Pinout

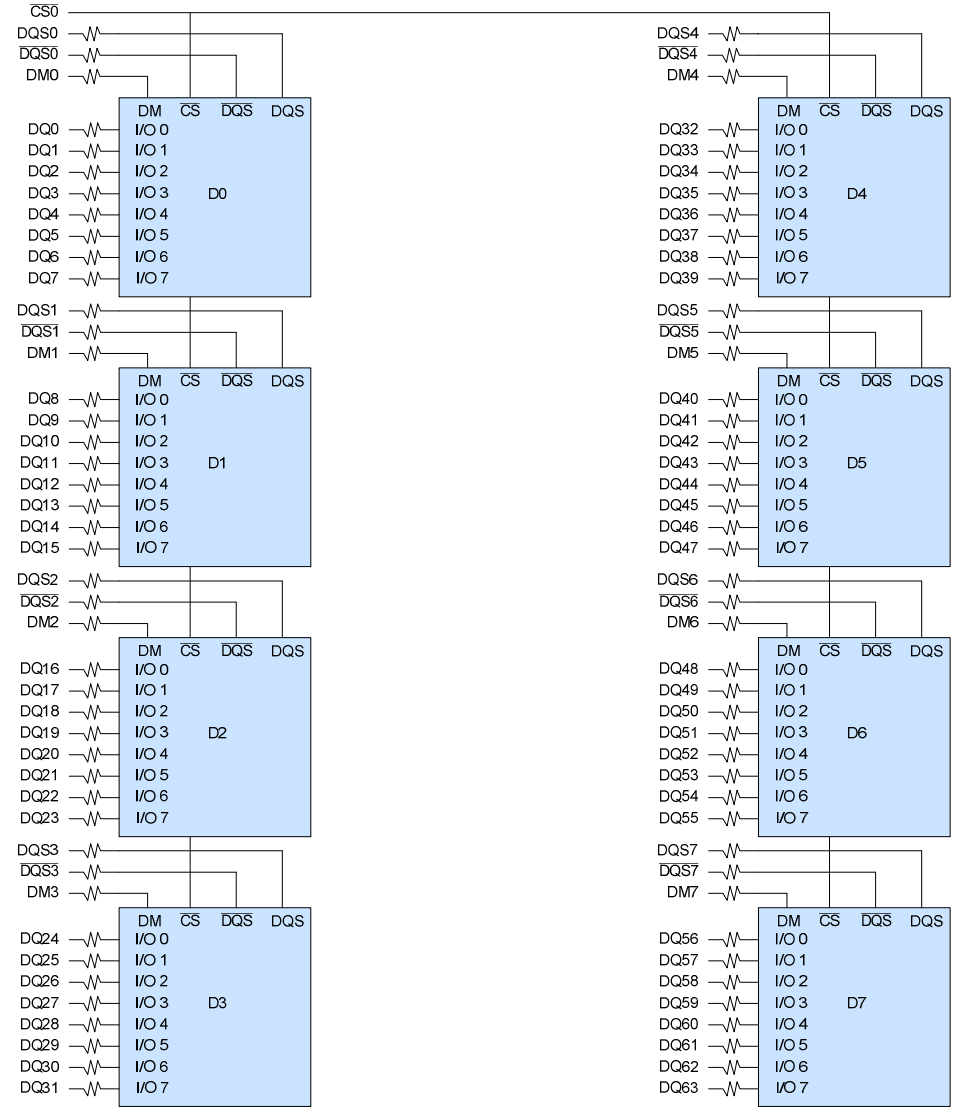
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	42	NC	82	V_{SS}	121	V_{SS}	162	NC	202	DM4
2	V_{SS}	43	NC	83	$\overline{DQS4}$	122	DQ4	163	V_{SS}	203	NC
3	DQ0	44	V_{SS}	84	DQS4	123	DQ5	164	NC	204	V_{SS}
4	DQ1	45	NC	85	V_{SS}	124	V_{SS}	165	NC	205	DQ38
5	V_{SS}	46	NC	86	DQ34	125	DM0	166	V_{SS}	206	DQ39
6	$\overline{DQS0}$	47	V_{SS}	87	DQ35	126	NC	167	NC	207	V_{SS}
7	DQS0	48	NC	88	V_{SS}	127	V_{SS}	168	NC	208	DQ44
8	V_{SS}	49	NC	89	DQ40	128	DQ6	169	V_{SS}	209	DQ45
9	DQ2	50	V_{SS}	90	DQ41	129	DQ7	170	V_{DDQ}	210	V_{SS}
10	DQ3	51	V_{DDQ}	91	V_{SS}	130	V_{SS}	171	CKE1	211	DM5
11	V_{SS}	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	V_{DD}	212	NC
12	DQ8	53	V_{DD}	93	DQS5	132	DQ13	173	NC	213	V_{SS}
13	DQ9	54	NC	94	V_{SS}	133	V_{SS}	174	NC	214	DQ46
14	V_{SS}	55	NC	95	DQ42	134	DM1	175	V_{DDQ}	215	DQ47
15	$\overline{DQS1}$	56	V_{DDQ}	96	DQ43	135	NC	176	A12	216	V_{SS}
16	DQS1	57	A11	97	V_{SS}	136	V_{SS}	177	A9	217	DQ52
17	V_{SS}	58	A7	98	DQ48	137	CK1	178	V_{DD}	218	DQ53
18	NC	59	V_{DD}	99	DQ49	138	$\overline{CK1}$	179	A8	219	V_{SS}
19	NC	60	A5	100	V_{SS}	139	V_{SS}	180	A6	220	CK2
20	V_{SS}	61	A4	101	SA2	140	DQ14	181	V_{DDQ}	221	$\overline{CK2}$
21	DQ10	62	V_{DDQ}	102	NC	141	DQ15	182	A3	222	V_{SS}
22	DQ11	63	A2	103	V_{SS}	142	V_{SS}	183	A1	223	DM6
23	V_{SS}	64	V_{DD}	104	$\overline{DQS6}$	143	DQ20	184	V_{DD}	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V_{SS}
25	DQ17	65	V_{SS}	106	V_{SS}	145	V_{SS}	185	CK0	226	DQ54
26	V_{SS}	66	V_{SS}	107	DQ50	146	DM2	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	VDD	108	DQ51	147	NC	187	VDD	228	V_{SS}
28	DQS2	68	NC	109	V_{SS}	148	V_{SS}	188	A0	229	DQ60
29	V_{SS}	69	VDD	110	DQ56	149	DQ22	189	V_{DD}	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V_{SS}
31	DQ19	71	BA0	112	V_{SS}	151	V_{SS}	191	V_{DDQ}	232	DM7
32	V_{SS}	72	VDDQ	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	NC
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{CS0}$	234	V_{SS}
34	DQ25	74	$\overline{CAS}$	115	V_{SS}	154	V_{SS}	194	V_{DDQ}	235	DQ62
35	V_{SS}	75	V_{DDQ}	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	$\overline{CS1}$	117	DQ59	156	NC	196	A13	237	V_{SS}
37	DQS3	77	ODT1	118	V_{SS}	157	V_{SS}	197	V_{DD}	238	V_{DDSPD}
38	V_{SS}	78	V_{DDQ}	119	SDA	158	DQ30	198	V_{SS}	239	SA0
39	DQ26	79	V_{SS}	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V_{SS}	200	DQ37		
41	V_{SS}	81	DQ33			161	NC	201	V_{SS}		

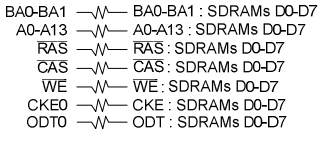
Input/Output Functional Description

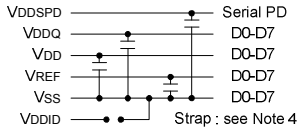
Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11 – A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0 – DQS7 $\overline{DQS0}$ – $\overline{DQS7}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

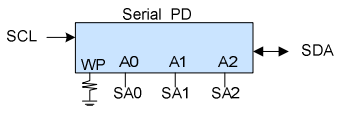
(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)





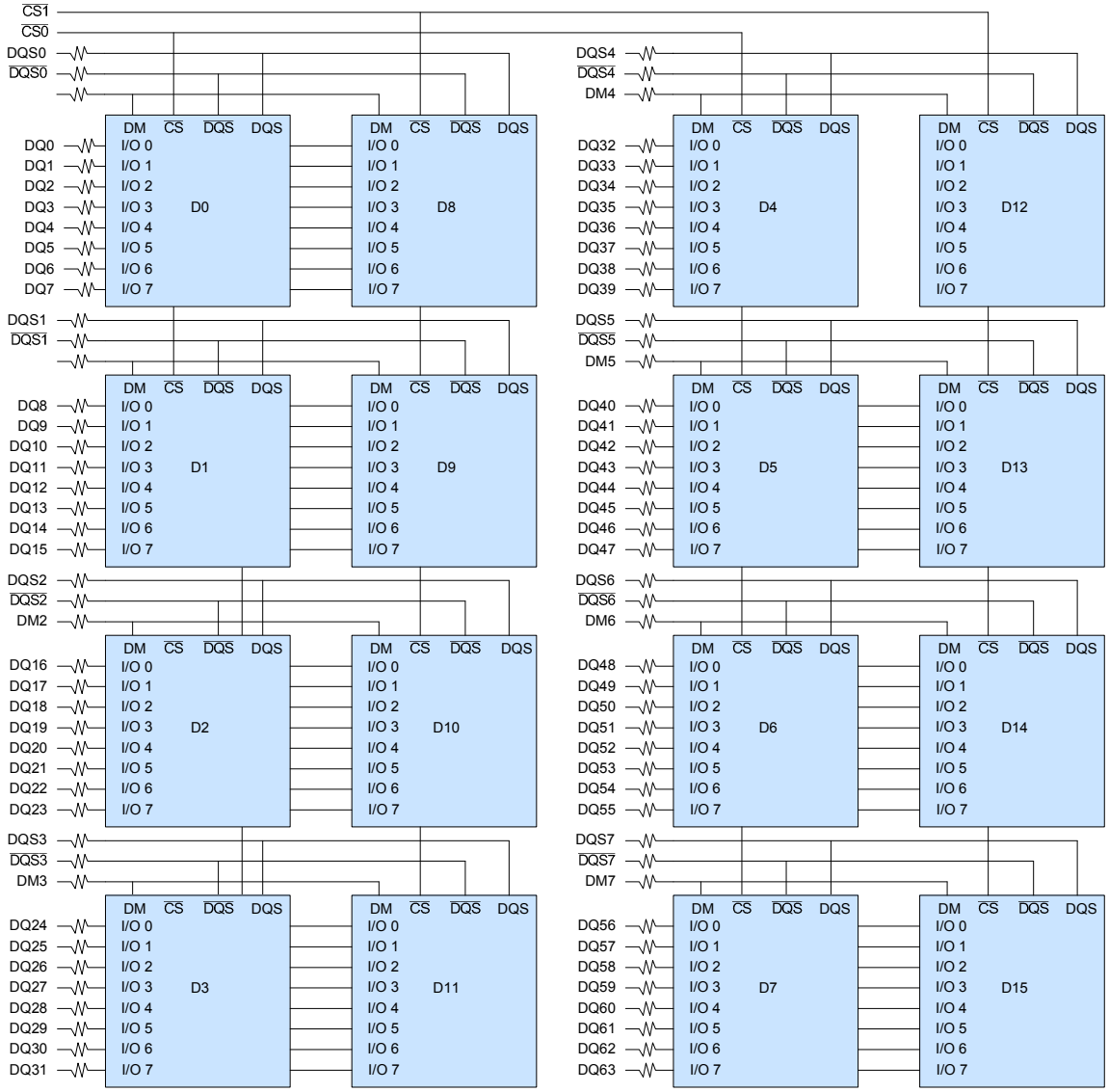


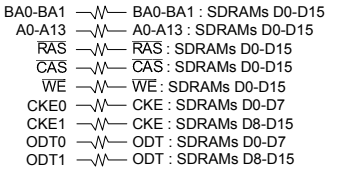
Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/$\overline{DQS}$ resistors are 22 Ohms +/- 5%
4. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%

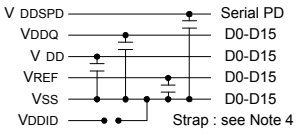


Functional Block Diagram

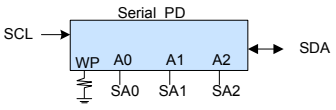
(1GB, 2 Rank, 64Mx8 DDR2 SDRAMs)







Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%



Serial Presence Detect – Part 1 of 2 (512MB)

64Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		667 -3C	533 -37B	667 -3C	533 -37B	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type (FPM, EDO.SRDAM, DDR, DDR2…)	DDR2		08		
3	Number of Row Addresses on Assembly	14		0E		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Bank, Package and Height	1 rank, Height >30.5mm		A0		
6	Data Width of This Assembly	64		40		
7	Reserved	Undefined		00		
8	Voltage Interface Level of this Assembly	SSTL_1.8V		05		
9	DDR2 SDRAM Device Cycle Time at Maximum Support /CAS Latency CL=5	3ns	3.75ns	30	3D	
10	DDR2 SDRAM Device Access Time (tac) from Clock at CL=5	0.45ns	0.5ns	45	50	
11	DIMM Configuration Type (non-parity, parity or ECC)	Non Parity/ECC		00		
12	Refresh Rate/Type	7.8µs/self		82		
13	Primary DDRII SDRAM Width	x8		08		
14	Error Checking DDRII SDRAM Device Width	N/A		00		
15	Reserved	Undefined		00		
16	DDR SDRAM Device Attributes: Burst Lengths Supported	4,8		0C		
17	DDR SDRAM Device Attributes: Number of Banks on DDRII SDRAM Device	4		04		
18	DDR SDRAM Device Attributes: /CAS Latencies Supported	5,4,3		38		
19	DIMM Mechanical Characteristics	<4.10mm		01		
20	DIMM type information	Regular UDIMM(133.35mm)		02		
21	DDRII SDRAM Modules Attributes	Normal DIMM		00		
22	DDRII SDRAM Device Attributes: General	Support weak driver		03	01	
23	Minimum Clock Cycle Time at CL=4	3.75ns	3.75ns	3D	3D	
24	Maximum Data Access Time (t_{AC}) from Clock at CL=4	0.5ns	0.5ns	50	50	
25	Minimum Clock Cycle Time at CL=3	5.0ns	5.0ns	50	50	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=3	0.6ns		60		
27	Minimum Row Precharge Time (t_{RP})	15ns		3C		
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns		1E		
29	Minimum RAS to CAS delay (t_{RCD})	15.0ns		3C		
30	Minimum Active to Precharge Time (t_{RAS})	45.0		2D		
31	Module Bank Density	512MB		80		
32	Address and Command Input Setup Time Before Clock (tIS)	0.2ns	0.25ns	20	25	
33	Address and Command Input Hold Time After Clock (tIH)	0.275ns	0.375ns	27	37	
34	Data Input Setup Time Before Clock (tDS)	0.10ns	0.10ns	10	10	
35	Data Input Hold Time After Clock (tDH)	0.175ns	0.225ns	17	22	
36	Write recovery time (tWR)	15.0ns		3C		
37	Internal write to read command delay (tWTR)	7.5ns	7.5ns	1E	1E	
38	Internal Read to Precharge command delay(tRTP)	7.5ns		1E		
39	Memory Analysis Probe Characteristics	Undefined		00		
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns		00		
41	SDRAM Device Minimum Active to Active/Auto-Refresh Time (tRC)	60.0ns		3C		
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	105ns		69		
43	SDRAM Device Maximum Cycle Time (tCK max)	8.0ns		80		
44	SDRAM Device Maximum skew between DQS and DQ signals (tDQS)	0.24ns	0.30ns	18	1E	
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.34ns	0.40ns	22	28	
46	PLL Relock Time	N/A		00		
47	Tcasemax DT4R4W Delta	95℃ 0.8℃	95℃ 0.4℃	52	51	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	61℃/W		7A		
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	8.8℃	8.2℃	53	4B	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby(DT2N/DT2Q)	5.8℃	4.6℃	3A	2E	

Serial Presence Detect – Part 2 of 2 (512MB)

64Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		667 -3C	533 -37B	667 -3C	533 -37B	
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down(DT2P)	0.585℃		27		
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	5.85℃	4.95℃	27	21	
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	2.2℃	1.85℃	2C	25	
54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	0.7℃	0.575℃	1C	17	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	15.2℃	10.4℃	4C	34	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	18.5℃	17.5℃	25	23	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	20℃	18.5℃	28	25	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	00	00	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	00	00	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	00	00	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	00	00	00	
62	SPD Reversion	1.2		12		
63	Checksum for bytes 0-62	Checksum data		39	37	
64-71	Manufacturer's JEDED ID Code	0B Hex bank 3		7F7F7F0B00000000		
72	Module Manufacturing Location	Manufacturing code		--		
73-91	Module Part Number	Module Part Number in ASCII		--		1
92-255	Reserved	Undefined		--		

Note1:
M2Y51264TU88A2G-37B ➔ 4D3259353132363454553838413247 2D333742
M2Y51264TU88A2G-3C ➔ 4D3259353132363454553838413247 2D334320

Serial Presence Detect -- Part 1 of 2 (1GB)

128Mx64 2 BANKS UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		667 -3C	533 -37B	667 -3C	533 -37B	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	DDR2		08		
3	Number of Row Addresses on Assembly	14		0E		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Bank, Package and Height	2 rank, Height >30.5mm		A1		
6	Data Width of This Assembly	64		40		
7	Reserved	Undefined		00		
8	Voltage Interface Level of this Assembly	SSTL_1.8V		05		
9	DDR2 SDRAM Device Cycle Time at Maximum Support /CAS Latency CL=5	3ns	3.75ns	30	3D	
10	DDR2 SDRAM Device Access Time (tac) from Clock at CL=5	0.45ns	0.5ns	45	50	
11	DIMM Configuration Type (non-parity, parity or ECC)	Non Parity/ECC		00		
12	Refresh Rate/Type	7.8µs/self		82		
13	Primary DDRII SDRAM Width	x8		08		
14	Error Checking DDRII SDRAM Device Width	N/A		00		
15	Reserved	Undefined		00		
16	DDR SDRAM Device Attributes: Burst Lengths Supported	4,8		0C		
17	DDR SDRAM Device Attributes: Number of Banks on DDRII SDRAM Device	4		04		
18	DDR SDRAM Device Attributes: /CAS Latencies Supported	5,4,3		38		
19	DIMM Mechanical Characteristics	<4.10mm		01		
20	DIMM type information	Regular UDIMM (133.35mm)		02		
21	DDRII SDRAM Modules Attributes	Normal DIMM		00		
22	DDRII SDRAM Device Attributes: General	Support weak driver		03	01	
23	Minimum Clock Cycle Time at CL=4	3.75ns	3.75ns	3D	3D	
24	Maximum Data Access Time (t_{AC}) from Clock at CL=4	0.5ns	0.5ns	50	50	
25	Minimum Clock Cycle Time at CL=3	5.0ns	5.0ns	50	50	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=3	0.6ns		60		
27	Minimum Row Precharge Time (t_{RP})	15ns		3C		
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns		1E		
29	Minimum RAS to CAS delay (t_{RCD})	15.0ns		3C		
30	Minimum Active to Precharge Time (t_{RAS})	45.0		2D		
31	Module Bank Density	512MB		80		
32	Address and Command Input Setup Time Before Clock (tIS)	0.2ns	0.25ns	20	25	
33	Address and Command Input Hold Time After Clock (tIH)	0.275ns	0.375ns	27	37	
34	Data Input Setup Time Before Clock (tDS)	0.10ns	0.10ns	10	10	
35	Data Input Hold Time After Clock (tDH)	0.175ns	0.225ns	17	22	
36	Write recovery time (tWR)	15.0ns		3C		
37	Internal write to read command delay (tWTR)	7.5ns	7.5ns	1E	1E	
38	Internal Read to Precharge command delay(tRTP)	7.5ns		1E		
39	Memory Analysis Probe Characteristics	Undefined		00		
40	Extension of Byte 41 tRC and Byte 42 tRFC	The number below a decimal point of tRC and tRFC are 0, tRFC is less than 256ns		00		
41	SDRAM Device Minimum Active to Active/Auto-Refresh Time (tRC)	60.0ns		3C		
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	105ns		69		
43	SDRAM Device Maximum Cycle Time (tCK max)	8.0ns		80		
44	SDRAM Device Maximum skew between DQS and DQ signals (tDQS)	0.24ns	0.30ns	18	1E	
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.34ns	0.40ns	22	28	
46	PLL Relock Time	N/A		00		
47	Tcasemax	3℃	1℃	52	51	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	61℃/W		7A		
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	8.8℃	8.2℃	53	4B	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby(DT2N/DT2Q)	5.8℃	4.6℃	3A	2E	
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down(DT2P)	0.585℃		27		

Serial Presence Detect -- Part 2 of 2 (1GB)

128Mx64 2 BANKS UNBUFFERED DDR2 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		667 -3C	533 -37B	667 -3C	533 -37B	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	5.85℃	4.95℃	27	21	
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	2.2℃	1.85℃	2C	25	
54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	0.7℃	0.575℃	1C	17	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	15.2℃	10.4℃	4C	34	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	18.5℃	17.5℃	25	23	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	20℃	18.5℃	28	25	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	00	00	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	00	00	00	
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	00	00	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	00	00	00	
62	SPD Reversion	1.2		12		
63	Checksum for bytes 0-62	Checksum data		3A	38	
64-71	Manufacturer's JEDED ID Code	0B Hex bank 3		7F7F7F0B00000000		
72	Module Manufacturing Location	Manufacturing code		--		1
73-91	Module Part Number	Module Part Number in ASCII		--		
92-255	Reserved	Undefined		--		

Note1:
M2Y1G64TU8HA2G-37B ➔ 4D3259314736345455384841324 62D33374220
M2Y1G64TU8HA2G-3C ➔ 4D3259314736345455384841324 72D33432020

Environmental Requirements

Symbol	Parameter	Rating	Units
T_{OPR}	Operating Temperature (ambient)	0 to 55	℃
H_{OPR}	Operating Humidity (relative)	10 to 90	%
T_{STG}	Storage Temperature	-50 to 100	℃
H_{STG}	Storage Humidity (without condensation)	5 to 95	%
	Barometric pressure (operating & storage) up to 9850ft.	105 to 69	kPa

Note: Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Voltage on VDD pins relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.5 to +2.3	V
V_{DDL}	Voltage on VDDL pins relative to Vss	-0.5 to +2.3	V
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to +2.3	V
T_{STG}	Storage Temperature (Plastic)	-55 to +100	℃

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Storage temperature is the case surface temperature on the center/top side of the DRAM.

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	℃	1

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85℃ ➔ t_{REFI} = 3.9 µs

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	1.7	1.9	V	1
V_{DDL}	DLL Supply Voltage	1.7	1.9	V	1
V_{DDQ}	Output Supply Voltage	1.7	1.9	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	Input Reference Voltage	0.49V_{DDQ}	0.51V_{DDQ}	V	1, 2
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF} + 0.04	V	3

Note:
1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However, VDDQ must be less than or equal to VDD under all conditions.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.

ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min.	Nom.	Max.	Units	Note
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50ohm	Rtt3(eff)	40	50	60	ohm	1
Deviation of V_M with respect to VDDQ/2	Delta VM	-6		+6	%	1
Note1: Test condition for Rtt measurements.						

Input AC/DC logic level

Symbol	Parameter	DDR2-533		DDR2-667		Units
		Min.	Max.	Min.	Max.	
$V_{IH\ (AC)}$	Input High (Logic1) Voltage	V_{REF} + 0.250	-	V_{REF} + 0.200	-	V
$V_{IL\ (AC)}$	Input Low (Logic0) Voltage	-	V_{REF} - 0.250	-	V_{REF} - 0.200	V
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.125	V_{DDQ} + 0.3	V_{REF} + 0.125	V_{DDQ} + 0.3	V
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	V_{REF} - 0.125	-0.3	V_{REF} - 0.125	V

Operating, Standby, and Refresh Currents

T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	560	600
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); IOUT = 0mA; address and control inputs changing once per clock cycle	640	720
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	40	40
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	320	400
I_{DD2Q}	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	240	320
I_{DD3PF}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	128	152
I_{DD3PS}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	40	48
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	336	400
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	720	1040
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	760	1120
I_{DD5B}	Burst Auto-Refresh Current: t_{RFC} = t_{RFC} (MIN)	1200	1280
I_{DD5D}	Distributes Auto-Refresh Current: t_{RFC} = t_{REFI}	48	48
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	40	40
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	1280	1360

Note: Module IDD was calculated from component IDD. It may different from the actual measurement.

Operating, Standby, and Refresh Currents

T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (1GB, 2 Ranks, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	880	1000
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	960	1120
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	80	80
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	640	800
I_{DD2Q}	Precharge quiet standby current; All banks idle; t_{CK}=t_{CK}(IDD); CKE is HIGH; $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	480	640
I_{DD3PF}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Fast PDN Exit MRS(12) = 0mA	256	304
I_{DD3PS}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN); Slow PDN Exit MRS(12) = 1mA	80	96
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	656	800
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	1040	1440
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; tCK = t_{CK} (MIN)	1080	1520
I_{DD5B}	Burst Auto-Refresh Current: t_{RFC} = t_{RFC} (MIN)	1520	1680
I_{DD5D}	Distributes Auto-Refresh Current: t_{RFC} = t_{REFI}	288	368
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	80	80
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	1600	1760
Note: Module IDD was calculated from component IDD. It may different from the actual measurement.			

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-37B		-3C		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{AC}	DQ output access time from CK/$\overline{CK}$	-0.5	+0.5	-0.45	+0.45	ns	
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$	-0.45	+0.45	-0.4	+0.4	ns	
t_{CH}	CK high-level width	0.45	0.55	0.45	0.55	t_{CK}	
t_{CL}	CK low-level width	0.45	0.55	0.45	0.55	t_{CK}	
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	t_{CH} or t_{CL}	-	t_{CH} or t_{CL}	-	t_{CK}	
t_{CK}	Clock Cycle Time	3.75	8	3	8	ns	
t_{DH}	DQ and DM input hold time	225	-	175	-	ps	
t_{DS}	DQ and DM input setup time	100	-	100	-	ps	
t_{IPW}	Input pulse width	0.6	-	0.6	-	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$	-	$t_{AC\ max}$	-	$t_{AC\ max}$	ns	
$t_{LZ(DQ)}$	Data-out low-impedance time from CK/$\overline{CK}$	$2t_{AC\ min}$	$t_{AC\ max}$	$2t_{AC\ min}$	$t_{AC\ max}$	ns	
$t_{LZ(DQS)}$	DQS low-impedance time from CK/$\overline{CK}$	$t_{AC\ min}$	$t_{AC\ max}$	$t_{AC\ min}$	$t_{AC\ max}$	ns	
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.30	-	0.24	ns	
t_{QHS}	Data hold Skew Factor	-	0.4	-	0.34	ns	
t_{QH}	Data output hold time from DQS	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	ns	
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	0.25	t_{CK}	
t_{DQSH}	DQS input high pulse width	0.35	-	0.35	-	t_{CK}	
t_{DQSL}	DQS input low pulse width	0.35	-	0.35	-	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	t_{CK}	
t_{MRD}	Mode register set command cycle time	2	-	2	-	t_{CK}	
t_{WPST}	Write postamble	0.40	0.60	0.40	0.60	t_{CK}	
t_{WPRE}	Write preamble	0.35	-	0.35	-	t_{CK}	
t_{IH}	Address and control input hold time	0.375	-	0.275	-	ns	
t_{IS}	Address and control input setup time	0.25	-	0.2	-	ns	
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	t_{CK}	
t_{RPST}	Read postamble	0.4	0.6	0.4	0.6	t_{CK}	
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS} + t_{CK} + t_{IH}$	-	$t_{IS} + t_{CK} + t_{IH}$	-	ns	
t_{RFC}	Refresh to active/Refresh command time	105		105		ns	

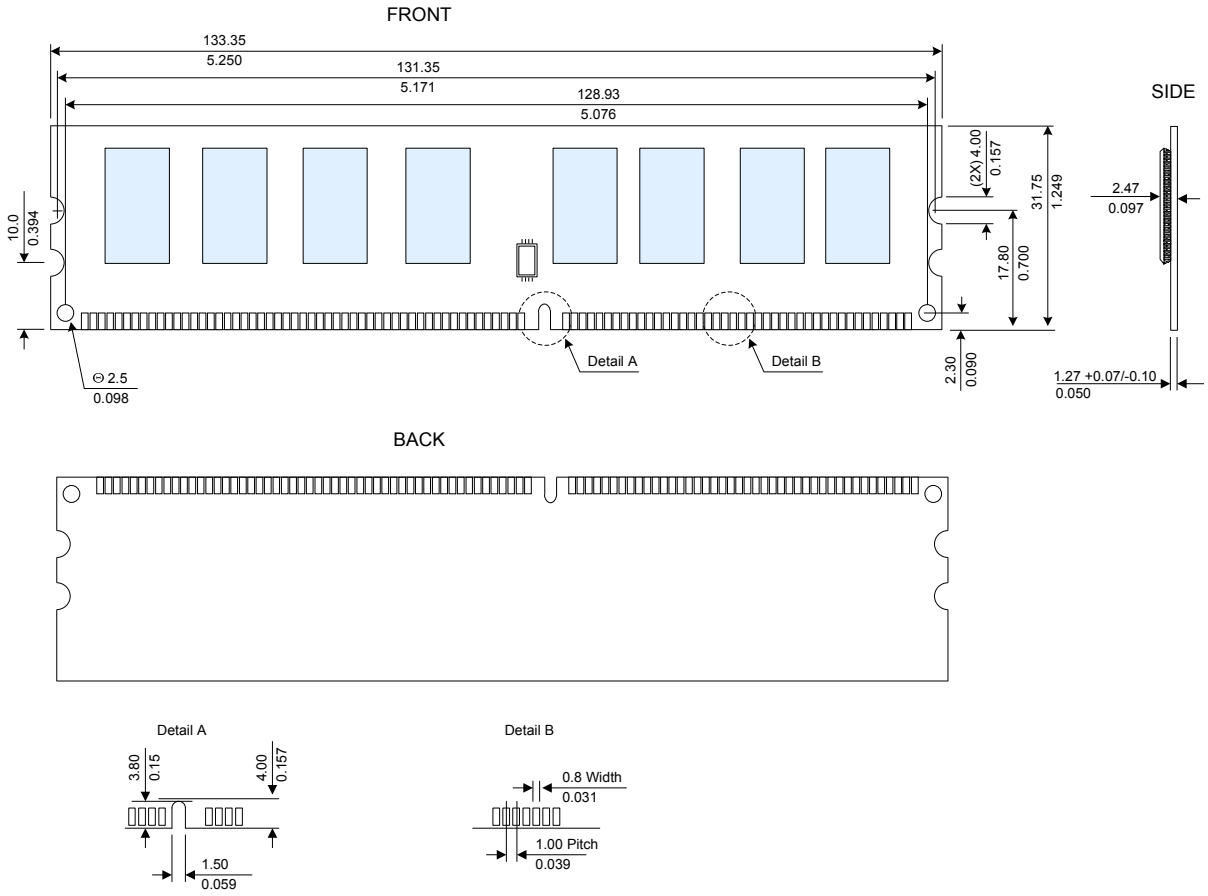
AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ºC ~ 85 ºC; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-37B		-3C		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{REFI}	Average Periodic Refresh Interval ($85ºC < T_{CASE} \leq 95ºC$)	3.9		3.9		µs	
	Average Periodic Refresh Interval ($0ºC \leq T_{CASE} \leq 85ºC$)	7.8		7.8		µs	
t_{RRD}	Active bank A to Active bank B command	7.5	-	7.5	-	ns	
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$	2	-	2	-	t_{CK}	
t_{WR}	Write recovery time	15	-	15	-	ns	
WR	Write recovery time with Auto-Precharge	t_{WR}/t_{CK}		t_{WR}/t_{CK}		ns	
t_{DAL}	Auto precharge write recovery + precharge time	WR +t_{RP}	-	WR +t_{RP}	-	t_{CK}	
t_{WTR}	Internal write to read command delay	7.5	-	7.5	-	ns	
t_{RTP}	Internal read to precharge command delay	7.5	-	7.5	-	ns	
t_{XSNR}	Exit self refresh to a Non-read command	t_{RFC} +10	-	t_{RFC} +10	-	ns	
t_{XSRD}	Exit self refresh to a Read command	200	-	200	-	t_{CK}	
t_{XP}	Exit precharge power down to any Non- read command	2	-	2	-	t_{CK}	
t_{XARD}	Exit active power down to read command	2	-	2	-	t_{CK}	
t_{XARDS}	Exit active power down to read command	6-AL	-	7-AL	-	t_{CK}	
t_{CKE}	CKE minimum pulse width	3	-	3	-	t_{CK}	
t_{OIT}	OCD drive mode output delay	0	12	0	12	ns	
ODT							
t_{AOND}	ODT turn-on delay	2	2	2	2	t_{CK}	
t_{AON}	ODT turn-on	t_{AC} (min)	t_{AC} (max) +1	$t_{AC(min)}$	$t_{AC(max)}$ +0.7	ns	
t_{AONPD}	ODT turn-on (Power down mode)	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	ns	
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$ +1	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{ANPD}	ODT to power down entry latency	3	-	3	-	t_{CK}	
t_{AXPD}	ODT power down exit latency	8	-	8	-	t_{CK}	
Speed Grade Definition							
t_{RAS}	Row Active Time	45	70000	45	70000	ns	
t_{RCD}	RAS to CAS delay	15	-	15	-	ns	
t_{RC}	Row Cycle Time	60	-	60	-	ns	
t_{RP}	Row Precharge Time	15	-	15	-	ns	

Package Dimensions

(512MB, 1 Rank, 64Mx8 DDR2 SDRAMs)



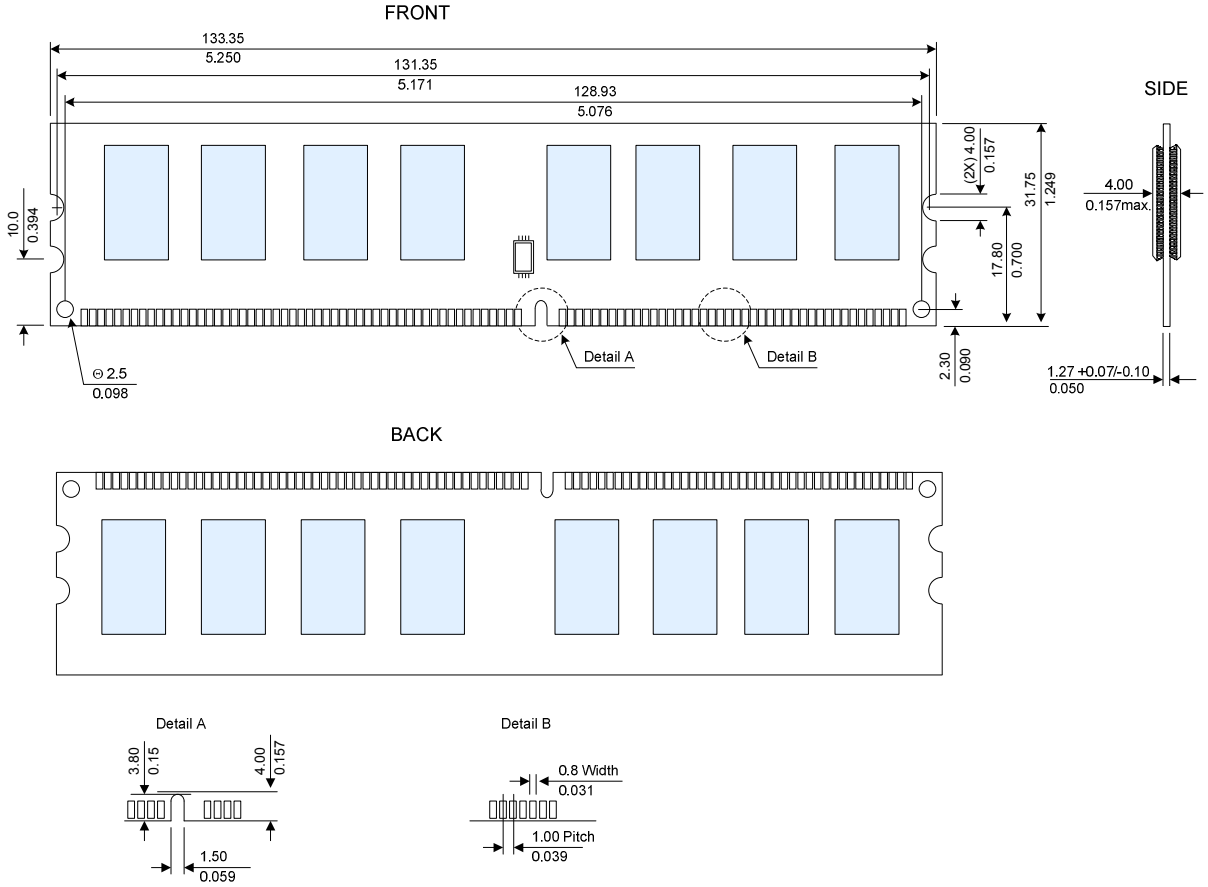
Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: Device position is only for reference.

Package Dimensions

(1GB, 2 Rank, 64Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Note: Device position is only for reference.

Revision Log

Rev	Date	Modification
0.1	05/2006	Preliminary Release.
1.0	06/2006	Official Release.