PRELIMINARY

MH8M36DJ/DNJ-5,-6,-7

FAST PAGE MODE 301989888-BIT (8388608 - WORD BY 36-BIT) DYNAMIC RAM MODULE

DESCRIPTION

The MH8M36DJ/DNJ is 8388608 - word by 36 - bit dynamic RAM module . That module consists of sixteen industry 4M x 4 dynamic RAMs and two industry quad $\overline{\text{cas}}$ 4M x 4 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required.

FEATURES

Performance renges

Type name	Access time (max. ns)	Cycle time (max. ns)	Power dissipation (max.mW)
MH8M36DJ/DNJ - 5	50	90	5895
MH8M36DJ/DNJ - 6	60	110	4860
MH8M36DJ/DNJ - 7	70	130	4275

- Single 5V±10% supply operation
- 72pin Single In-Line Package
- Low stand-by power dissipation
  - - - - 55mW(Max) CMOS input level
- Low operation power dissipation
  - MH8M36DJ/DNJ - 5 - - - 7.23W(Max)
  - MH8M36DJ/DNJ - 6 - - - 5.97W(Max)
  - MH8M36DJ/DNJ - 7 - - - 5.25W(Max)
- Includes decoupling capacitors (0.22μF x 18)
- 2048 refresh cycles every 32.0ms (A0~A10)
- **MH8M36DJ is gold plating contact .**
  MH8M3DNJ is solder with Nickel under plating contact .

APPLICATION

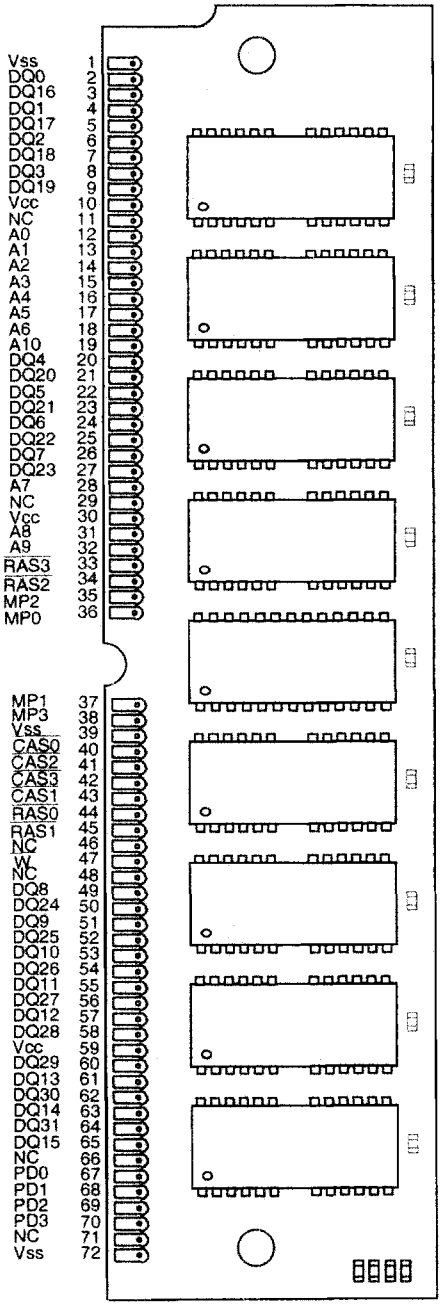
Main memory unit for computers, Microcomputer memory, Refresh memory for CRT.

FUNCTION

The MH8M36DJ/DNJ provide, in addition to normal read, write a number of other functions, e. g., fast page mode, RAS-only refresh. The input conditions for each are shown in Table1.

PIN CONFIGURATION (TOP VIEW)

[Double side]



Outline 72N9R-C

	- 5	- 6	- 7
PD0	NC	NC	NC
PD1	Vss	Vss	Vss
PD2	Vss	NC	Vss
PD3	Vss	NC	NC

NC: NO CONNECTION

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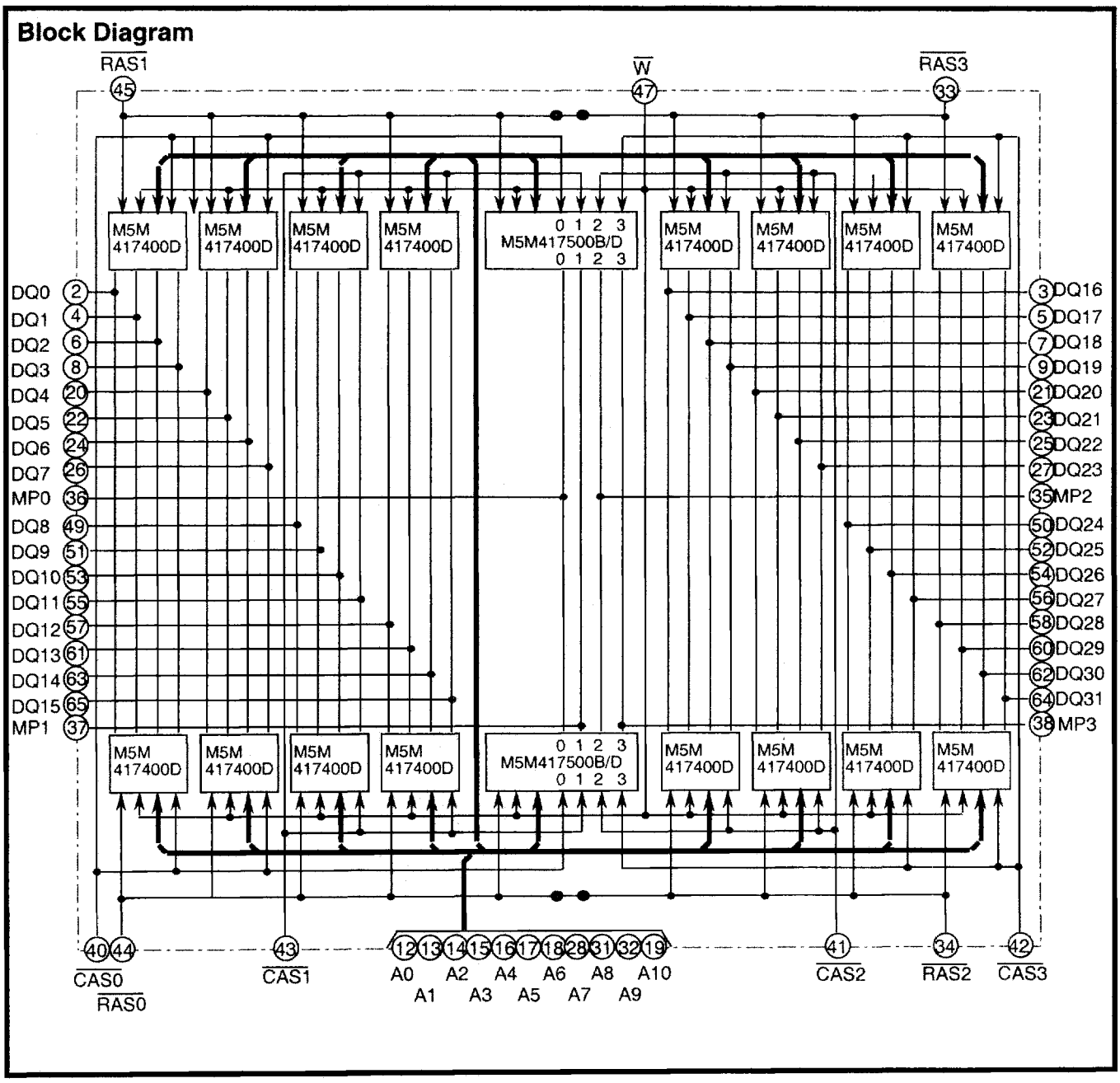
Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1 ~ 7	V
VI	Input voltage		-1 ~ 7	V
V0	Output voltage		-1 ~ 7	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25 °C	18	W
Topr	Operating temperature		0 ~70	°C
Tstg	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 ~ 70 °C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-1.0**		0.8	V

Note 1 : All voltage values are with respect to Vss
**:VIL(min.) is -2.0V when pulse width is less than 25ns. (Pulse width is with respect to VSS.)

ELECTRICAL CHARACTERISTICS

(Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V ≤ V_{OUT} ≤ 5.5V	-20		20	μA
I_I	Input current		0V ≤ V_{IN} ≤ 6.0V,Other inputs pins=0V	-180		180	μA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4)	MH8M36D -5	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			1323	mA
		MH8M36D -6				1098	
		MH8M36D -7				963	
I_{CC2}	Supply current from Vcc , stand-by		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			36	mA
			$\overline{RAS}$= $\overline{CAS}$ ≥ Vcc -0.2			10	
$I_{CC3\ (AV)}$	Average supply current from Vcc refreshing (Note 3)	MH8M36D -5	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			2610	mA
		MH8M36D -6				2160	
		MH8M36D -7				1890	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	MH8M36D -5	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			758	mA
		MH8M36D -6				648	
		MH8M36D -7				558	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH8M36D -5	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			2610	mA
		MH8M36D -6				2160	
		MH8M36D -7				1890	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) , Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE

(Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\ (A)}$	Input capacitance, address inputs	Vi=Vss f=1MHz Vi=25mVrms			145	pF
$C_{I\ (\overline{W})}$	Input capacitance, write control input				189	pF
$C_{I\ (\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				50	pF
$C_{I\ (\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				50	pF
$C_{I/O}$	Input/Output capacitance, data ports				22	pF

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SWITCHING CHARACTERISTICS

(Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			MH8M36D -5		MH8M36D -6		MH8M36D -7		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		50		60		70	ns
t_{AA}	Column address access time	(Note 6,9)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		30		35		40	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	13	0	15	0	15	ns

Note 5: An initial pause of 500É s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of RAS inactivity before proper device operation is achieved.
6: Measured with a load circuit equivalent to 2TTL loads and 100pF.
7: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
8: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.
9: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.
10: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
11: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 10\ \mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70 °C, Vcc=5V ± 10%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits						Unit
			MH8M36D -5		MH8M36D -6		MH8M36D -7		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			32		32		32	ms
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low		0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data		13		15		15		ns
t_T	Transition time	(Note17)	1	50	1	50	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.
13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.
15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.
16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.
17: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH8M36D -5		MH8M36D -6		MH8M36D -7		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ low (Note 18)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ low (Note 18)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		ns

Note 18: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write)

Symbol	Parameter	Limits						Unit
		MH8M36D -5		MH8M36D -6		MH8M36D -7		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns

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Fast-Page Mode Cycle (Read, Early Write) (Note 19)

Symbol	Parameter		Limits						Unit
			MH8M36D -5		MH8M36D -6		MH8M36D -7		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		35		40		45		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note20)	85	125000	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note21)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns

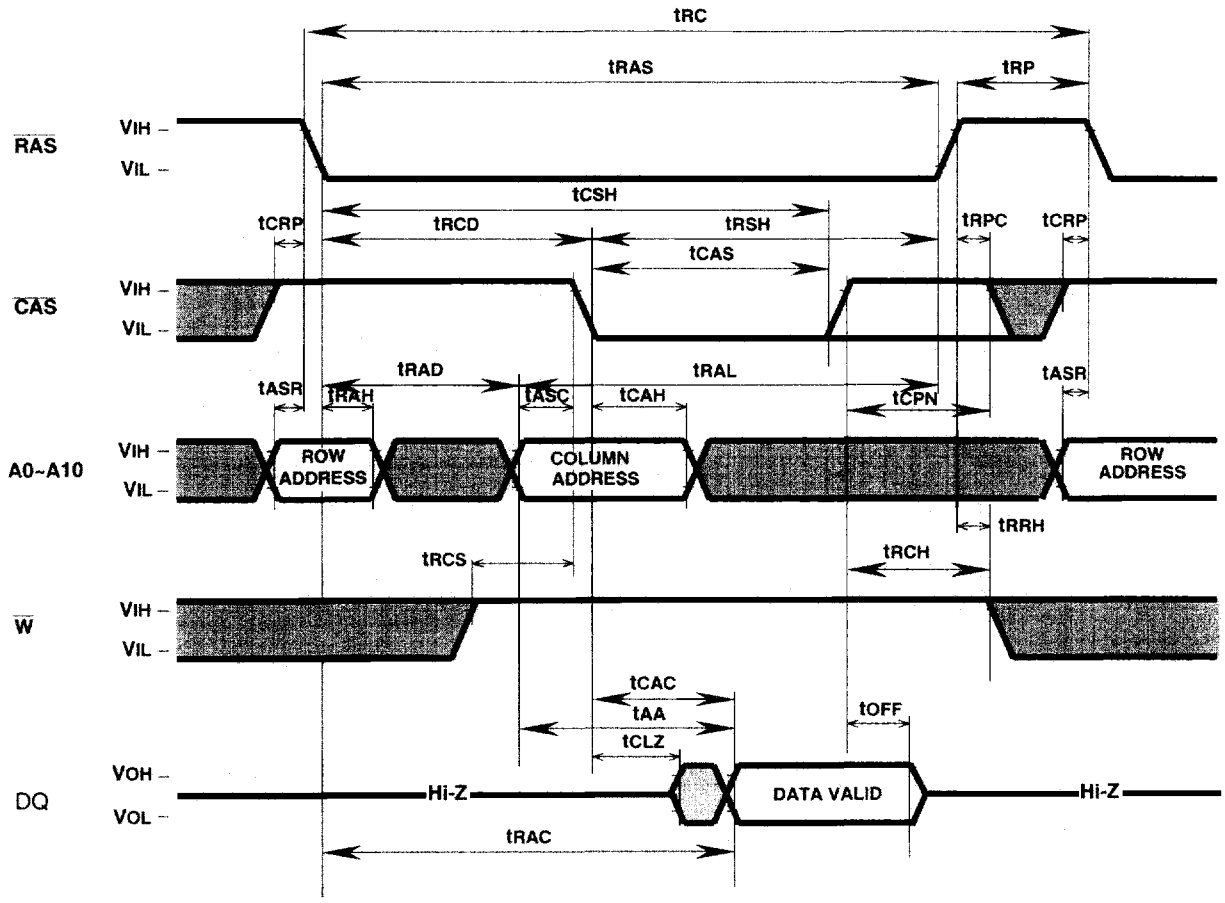
Note 19: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
20: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
21: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		MH8M36D -5		MH8M36D -6		MH8M36D -7		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 22: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 23)
Read Cycle

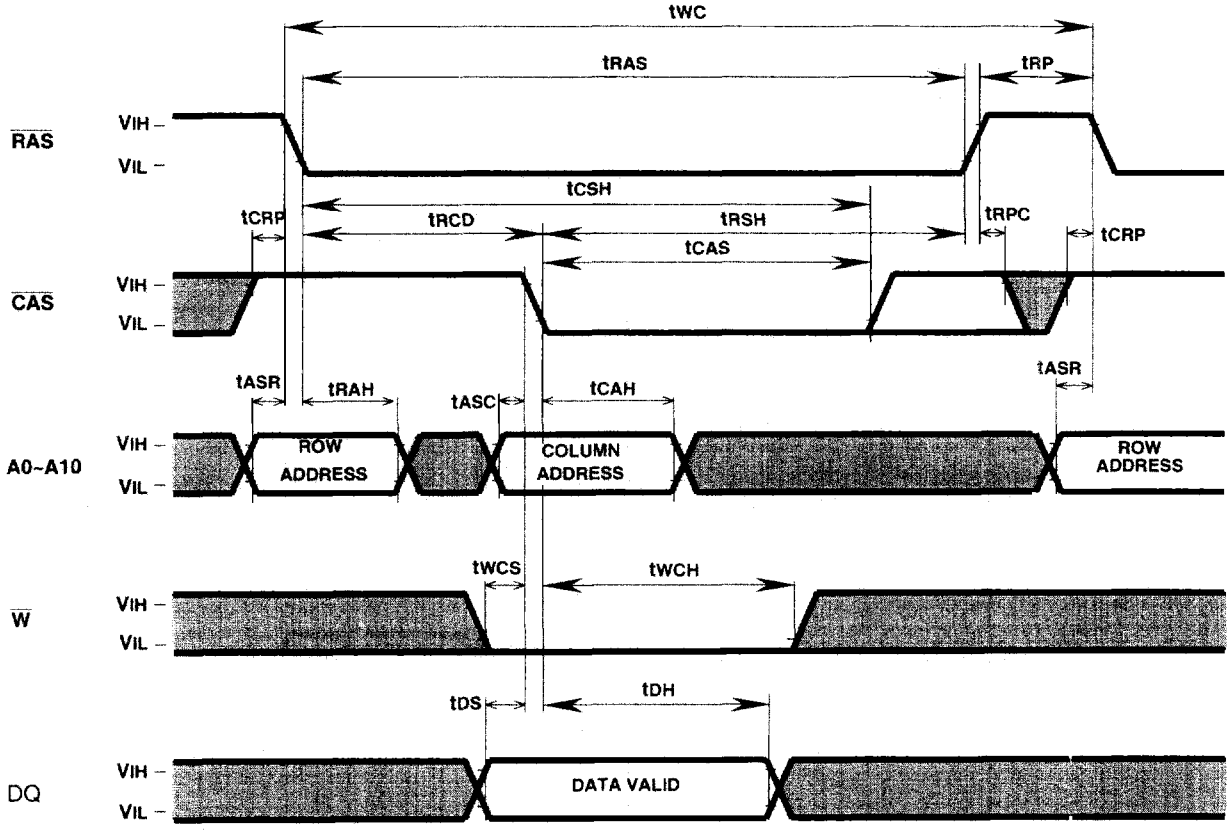


Note 23

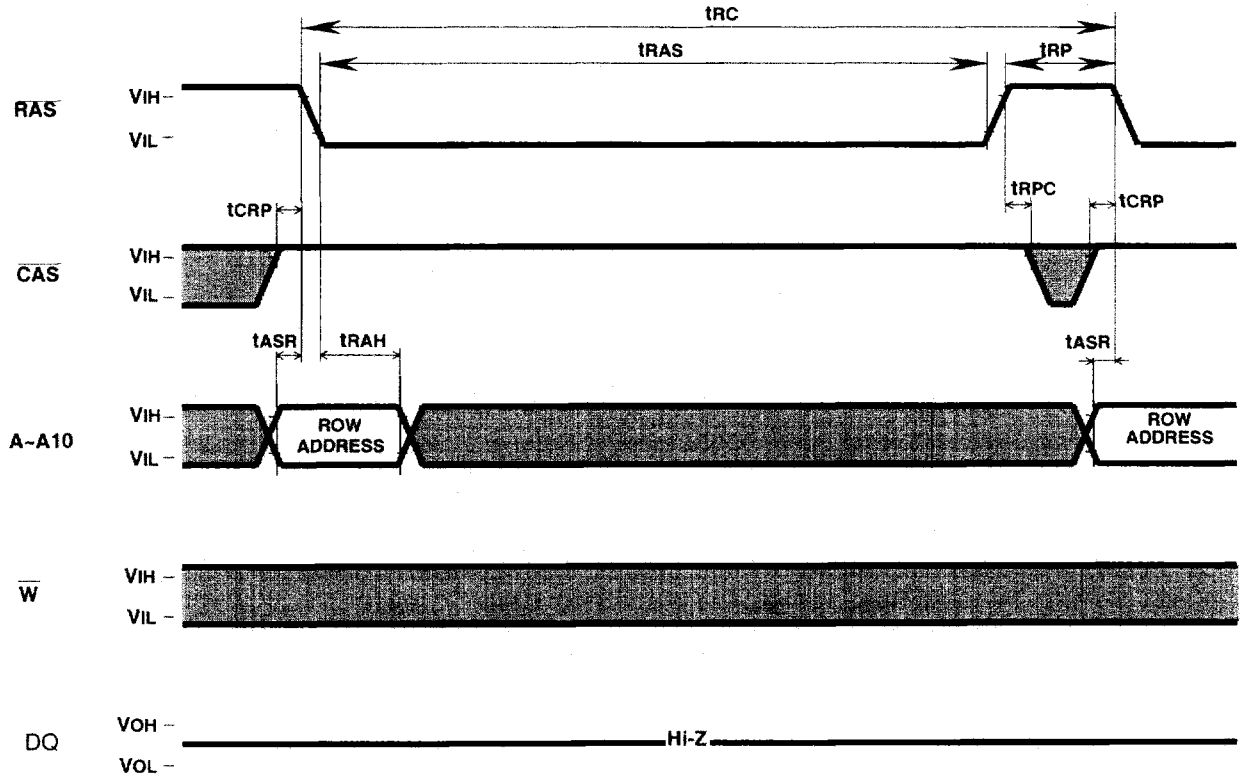
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

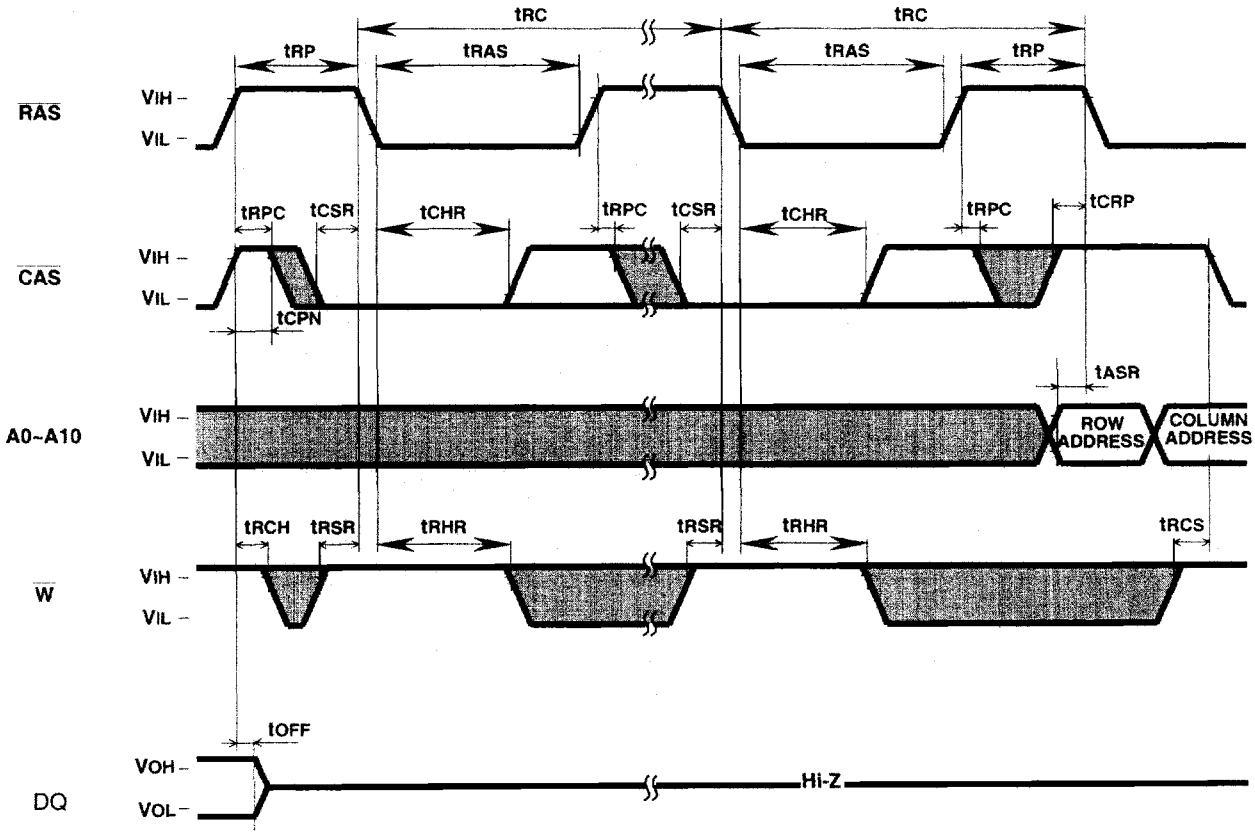
Write Cycle (Early write)



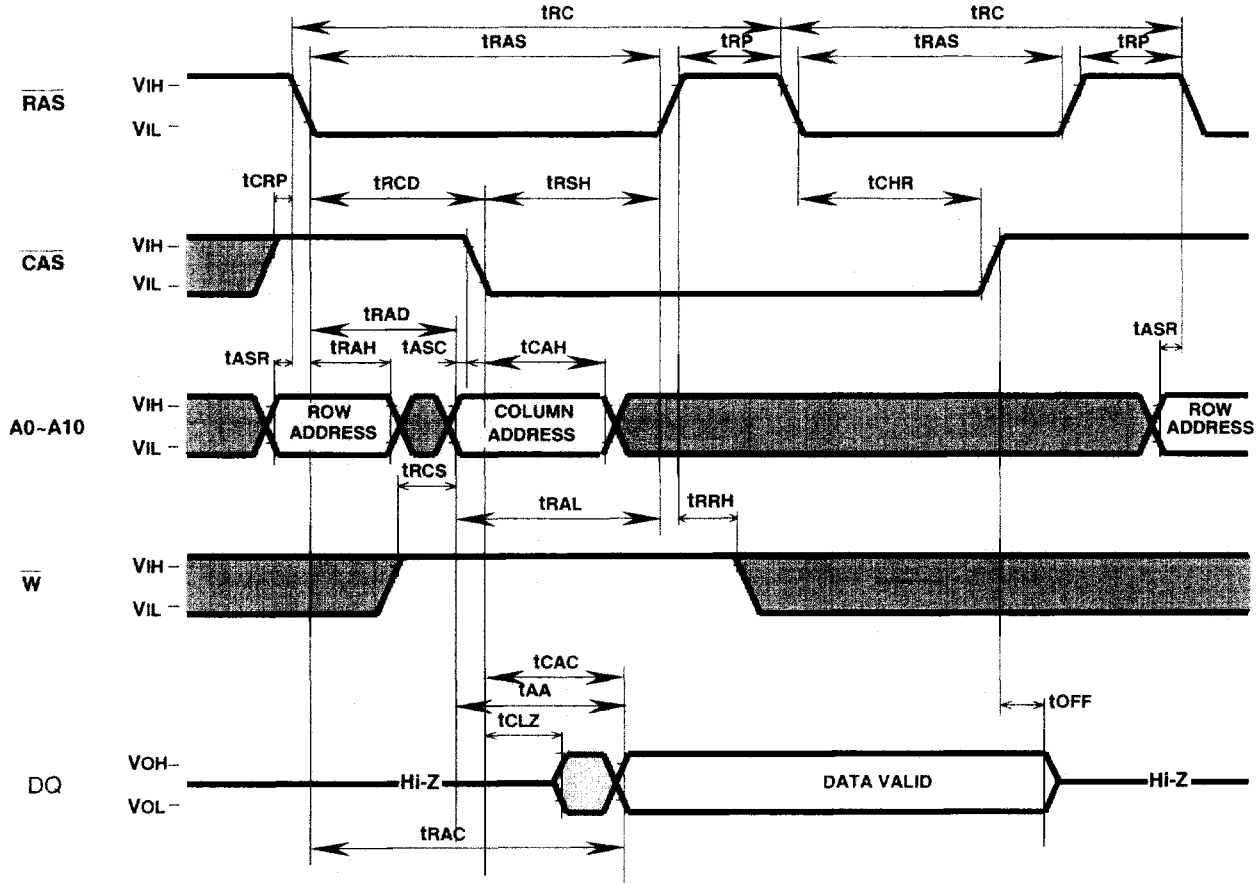
RAS-only Refresh Cycle



CAS before RAS Refresh Cycle

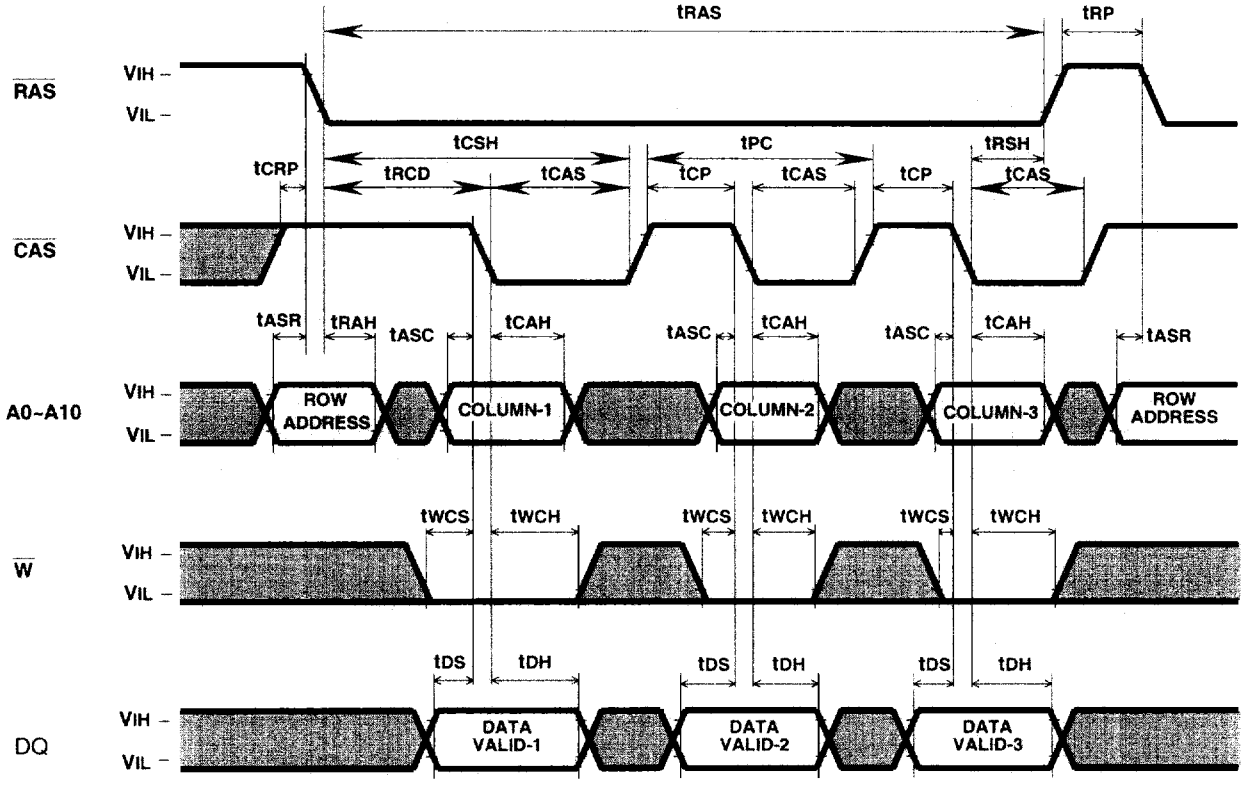


Hidden Refresh Cycle (Read) (Note 28)

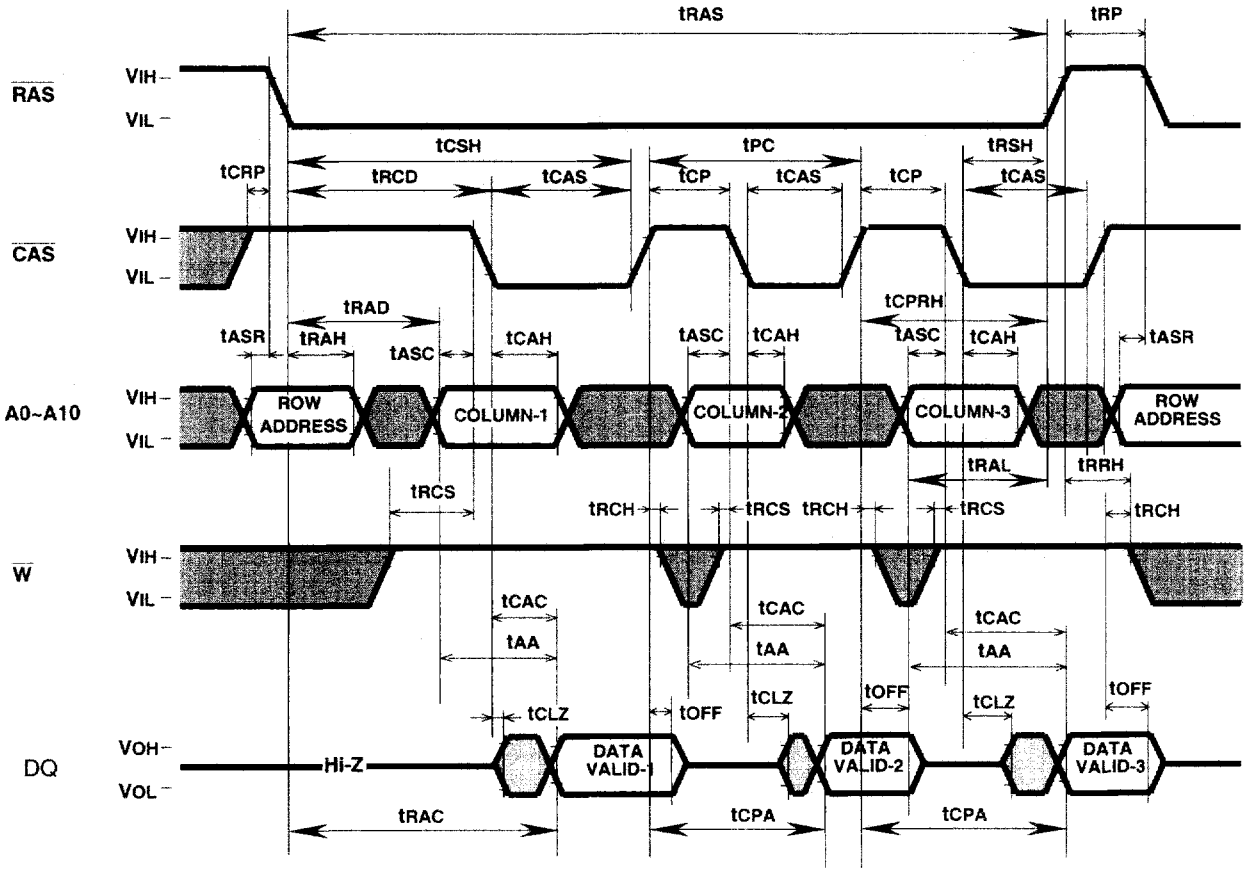


Note 28: Early write is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Read Cycle



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72Pin SIMM outline