NEW

SYNCHRONOUS DRAM

SYNCHRONOUS DRAM

2 MEG x 8 SDRAM

Level $\overline{RAS}$, Single Bank,
BURST Mode, 3.3V, SELF REFRESH

FEATURES

- Fully synchronous; all signals registered to positive edge of system clock
- JEDEC-standard 3.3V power supply
- Single bank: 2 Meg x 8 architecture
- Programmable burst-lengths: 2, 4, 8 cycles or full-page burst
- Programmable burst-sequence: sequential or interleave
- Hidden precharge capability
- Programmable READ latency: 1, 2 or 3 clocks
- Standard x8 pinouts, timing, functions and packages
- Refresh modes: AUTO and SELF REFRESH
- High-performance CMOS silicon-gate process
- Lead-over-chip assembly architecture
- Single +3.3V ±0.3V power supply
- Low power, 2mW standby; 200mW active, typical
- LVTTL-compatible
- CKE-controlled power-down and suspend operations
- Mode register programming with power-up default
- Second source to Samsung's level-$\overline{RAS}$ synchronous DRAM (SDRAM)

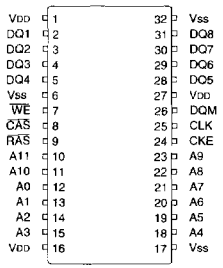
OPTIONS

	MARKING
• Timing	
10ns access (≤100 MHz)	-10
12ns access (≤83 MHz)	-12
13ns access (≤77 MHz)	-13
• Auto Refresh	
2,048-cycle in 32ms (15.6µs/row)	none
• Plastic Packages	
32-pin SOJ (400 mil)	DJ
44-pin TSOP (400 mil)	TG

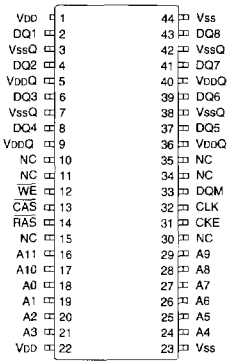
- Part Number Example: MT48LC2M8K3TG-10 S

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(DC-5)



44-Pin TSOP
(DD-7)



GENERAL DESCRIPTION

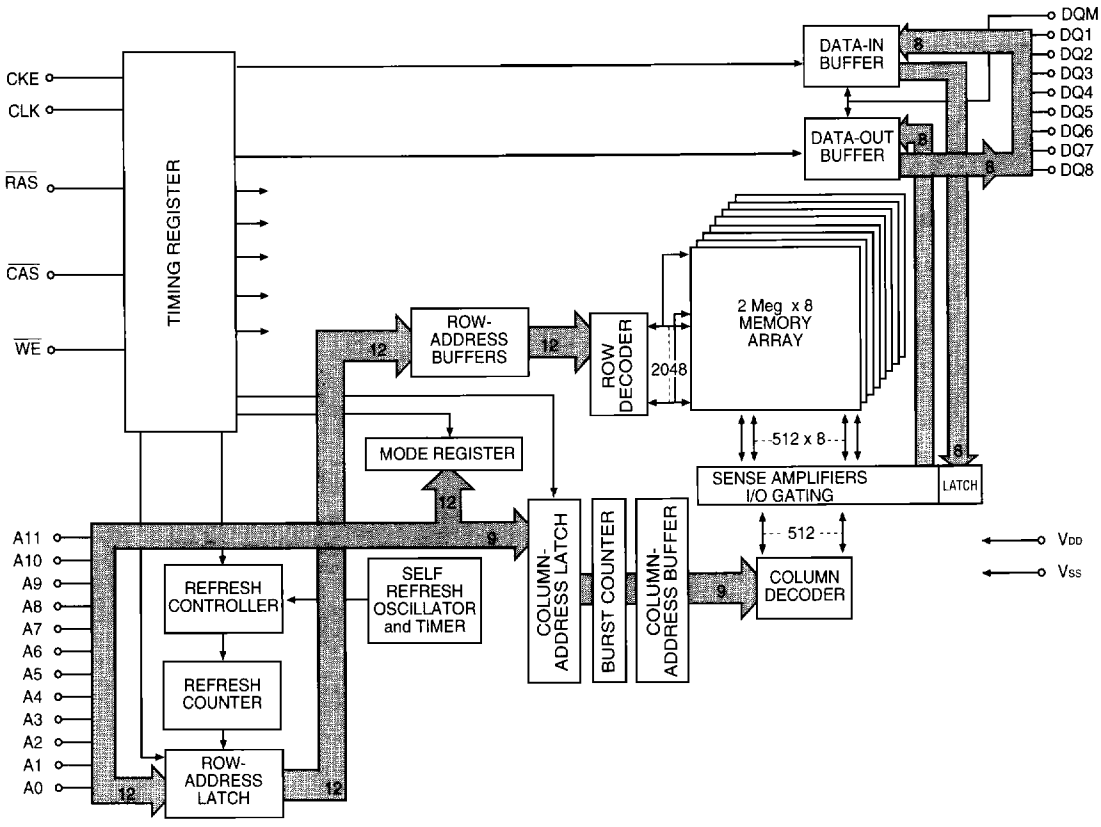
The MT48LC2M8K3 S is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x8 configuration. It is structured as a 2 Meg x 8 DRAM with a synchronous interface. Each byte is uniquely addressed through a bank-select bit and 20 address bits. The addresses are entered first by $\overline{RAS}$ registering 12 bits (A0-A11) and then $\overline{CAS}$ registering 9 bits (A0-A8).

The MT48LC2M8K3 S is designed to operate in a synchronous, 3.3V memory system. All input and output signals are synchronized to the positive going edge of the system clock (CLK).

The synchronous DRAM has several programmable features to allow maximum performance in each user's system. Additionally, the programmable BURST mode provides very high-speed performance.

The synchronous DRAM allows both AUTO REFRESH (during normal operation) and SELF REFRESH (for low-power, data-retention operation).

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MT48LC2M8K3 S is a 16 Meg synchronous DRAM organized in a x8 configuration. It is structured as a 2 Meg x 8 DRAM with synchronous interfacing and control logic. The key advancement of the synchronous DRAM is its ability to synchronously burst data (BURST mode) at a high-speed data rate via automatic column-address generation. Additionally, all input and output signals are synchronized to the system's clock. The positive-going edge of the system clock (CLK) provides the registering trigger which synchronizes the synchronous DRAM.

The synchronous DRAM must first be initialized and have its mode register set or it will be in the default state. Once the mode register is set, the synchronous DRAM may be accessed. Each byte is uniquely accessed by registering the 12 row-address bits (A0-A11) via the active command ($\overline{RAS}$ latched LOW), followed by registering the nine column-address bits (A0-8) via a READ or WRITE command.