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SSI 32F8144
Programmable Electronic Filter

January 1996

DESCRIPTION

This custom integrated circuit incorporates a pulse equalizer of variable equalization and variable bandwidth with a transfer function of a 2 zero/7 pole linear phase filter, as well as variable gain stages controlled by DACs. Equalization, gain and bandwidth changes are user-programmable via three serial lines to a microprocessor. The equalizer is totally contained and calibrating. It is realized in a high speed fully differential mode. A seven pole linear phase equiripple ± 0.05 degree filter forms the low-pass function. The cutoff frequency of the low-pass section is programmed via a 7-bit serial shift register and can be programmed from 7 to 27 MHz. Pulse slimming equalization uses two programmable magnitude, opposite sign zeroes on the real axis. Pulse slimming boost is from 0 to 9.5 dB at the filter cutoff frequency using a 7 bit serial shift register. Gain can be programmed from 10 V/V to 100 V/V for normal outputs and from 10 V/V to 50 V/V for differentiated outputs.

FEATURES

- **Programmable filter cutoff frequency (7 MHz ≤ fc ≤ 27 MHz) with no external components**
- **± 10% cutoff frequency accuracy**
- **Programmable pulse slimming equalization (0 to 9.5 dB boost at the filter cutoff frequency)**
- **Matched delay normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device idle mode (45 mW nom.)**
- **+5V only operation**
- **Supports constant density recording**
- **Input stage gain control with DAC**
- **Relative gain between normal and differentiated outputs controlled with serial port**

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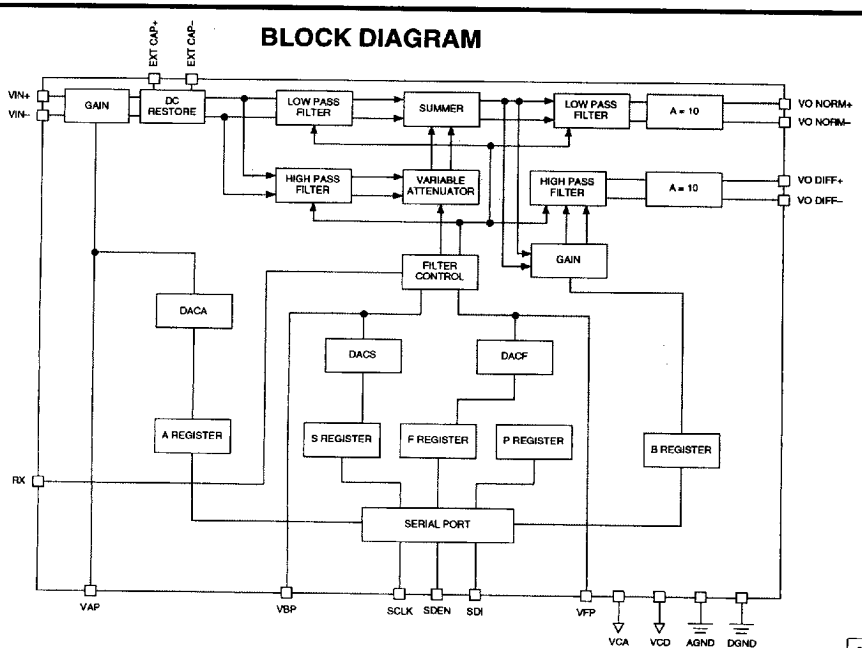
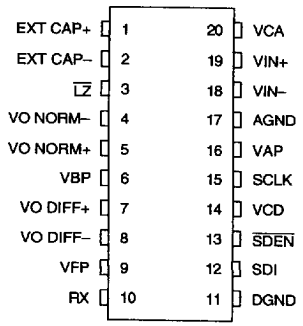
BLOCK DIAGRAM



PIN DIAGRAM



20-lead SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8144
Programmable
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FUNCTIONAL DESCRIPTION

The SSI 32F8144, a high performance programmable electronic filter, provides a low pass equiripple type seven pole filter with matched normal and differentiated outputs with variable gain using DACs.

The SSI 32F8144 has seven control registers: A, B, S1, S2, F1, F2 and P registers. Register A contains four bits, B is three bits, and P is one bit. S1, S2, F1, and F2 contain seven bits. Register A controls the gain of the input stage and register B controls the gain between the normal and differentiated outputs. Since the F, S registers contain 7 bits, they require two data packets which must be loaded sequentially. S1-2 registers are for high frequency boost. F1-2 registers are for cutoff frequency control. The P register is for power down command. The structure and command of each register are described as follows.

Data is loaded serially with MSB first. Each data packet contains 8 bits. The first four bits (D7 - D4) are designated as address bits with D7 always a "don't care." The last four bits (D3 - D0) are the data bits (see Table 1).

The registers are loaded by using the serial port through the SDI, $\overline{\text{SDEN}}$ and SCLK pins. The SDI pin is the serial bit input. The $\overline{\text{SDEN}}$ pin is the control register enable. The SCLK is the control register clock. The packet is transmitted MSB (D7) first.

GAIN PROGRAMMING

The input gain stage is programmed with register A (Register 4, R4). The A_Code programs this gain as follows:

$$Av(V/V) = 10 \bullet \frac{A\_Code}{15}$$

$$1 \le A\_Code \le 15$$

This input gain stage is DC coupled to the filter core through DC restore circuitry. A large capacitor (1 µF) is placed between pins EXT_CAP+ and EXT_CAP- to null the input offset to the filter. Register B (Register 5, R5) controls the relative gain between the normal and differentiated outputs. There are three discrete options which are listed as follows:

AN/AD = 1.0 B_Code = 3 (B2 = 0, B1 = 1, B0 = 1)

1 ≤ A_Code ≤ 7

AN/AD = 1.5 B_Code = 5 (B2 = 1, B1 = 0, B0 = 1)

1 ≤ A_Code ≤ 11

AN/AD = 2.0 B_Code = 6 (B2 = 1, B1 = 1, B0 = 0)

1 ≤ A_Code ≤ 15 (B3 is a "don't care")

CUTOFF FREQUENCY PROGRAMMING

The filter cutoff frequency can be set from 7 to 27 MHz. The 7-bit F_Code programs the cutoff frequency as follows:

$$fc(MHz) = 27 \bullet \frac{F\_Code}{127} \qquad 33 \le F\_Code \le 127$$

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the DACS output, the boost can be determined. The amount of boost at the cutoff frequency is related to the DACS output by the following formula:

BOOST (dB) = 20 • log [0.01563(S_Code) +1].

The 7-bit S_Code is loaded into S1 and S2 registers (registers 0 and 1 - R0, R1).

POWER-DOWN CONTROL

The D0 bit of the P register (register 7, R7) determies the power up/down state of the SSI 32F8144. Upon initial power up, the D0 bit of the P register should be initialized to "1" for normal operation. D3 - D1 are "don't care."

By programming D0 to "0," the SSI 32F8144 is switched into a power-down state, dissipating minimum idle power. The filter is switched off. The serial port remains active awaiting the next command.

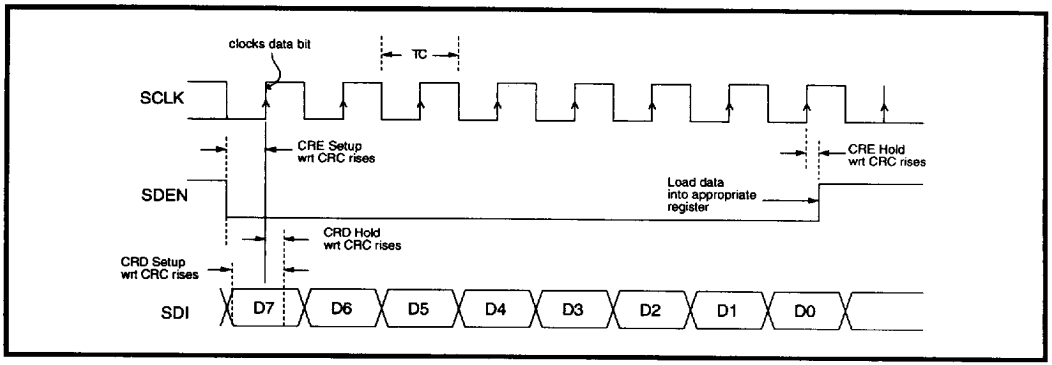

FIGURE 1: Serial Port Timing Relationship

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TABLE 1: Control Register Assignment

ADDRESS BITS					USAGE	DATA BITS			
	D7	D6	D5	D4		D3	D2	D1	D0
R0	X	0	0	0	S1 REGISTER	X	S6	S5	S4
R1	X	0	0	1	S2 REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F1 REGISTER	X	F6	F5	F4
R3	X	0	1	1	F2 REGISTER	F3	F2	F1	F0
R4	X	1	0	0	A REGISTER	A3	A2	A1	A0
R5	X	1	0	1	B REGISTER	X	B2	B1	B0
R7	X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = Boost (Slimming) Control
F = Frequency (Bandwidth) Control
A = Gain Setting (0-10)
B = Gain of VO_DIFF relative to the gain of VO_NORM
P = Sleep Mode Control (P0 = 1, On Mode; P0 = 0, Sleep Mode)

SDI is the serial data input for an 8-bit control shift register. The data packet is transmitted Most Significant Bit (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS
$\overline{SDEN}$	CONTROL REGISTER ENABLE. A logic LOW level allows CONTROL REGISTER CLOCK to clock data into the control register via the CONTROL REGISTER DATA input. A logic HIGH level latches the register data and issues the information to the appropriate circuitry. This is a TTL input.
SCLK	CONTROL REGISTER CLOCK. Positive edge triggered clock input for serial register. This is a TTL input.
SDI	CONTROL REGISTER DATA. This is a TTL input (see Figure 1).
RX	CURRENT SET RESISTOR. This external resistor to ground provides a reference current. (RX = 5 kΩ ±1%) A 1000 pF capacitor must be connected in parallel with Rx.
VCA	ANALOG +5V SUPPLY.
VCD	DIGITAL +5V SUPPLY.
AGND	ANALOG GROUND.
DGND	DIGITAL GROUND.
VAP	ANALOG TO DIGITAL TEST VOLTAGE. This is an analog voltage that is proportional to the setting on the digital output on the A/D convertor. This is a test pin related to the variable gain.
VBP	BOOST PROGRAMMING VOLTAGE. A voltage that is related to the boost. A test pin.
VFP	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. A voltage that is related to the cutoff frequency. A test pin.
EXT CAP+ EXT CAP-	EXTERNAL CAPACITOR. These pins are available for an external capacitor which is used in a feedback network to null the input offset. $C_{EXT} \geq 0.47\ \mu F$, 1.0 µF nominal.
$\overline{LZ}$	LOW IMPEDANCE. This is a control signal which causes the input impedance of the filter to be low when this pin is low. The impedance is high if the pin is open or in the high state. This is a TTL input.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCCV
Maximum Power Dissipation, fc = 27 MHz, Vcc = 5.5V	.55W
T1 Lead Temperature (1/16" from case for 10 seconds)	260°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

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RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.50 < VCC < 5.50 V
Ambient Temperature	0 < Ta < 70°C
Tj Junction Temperature	0 < Tj < 130°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Idle Mode Current	P0 = "0"		11	15	mA
Supply Current	Vcc = 5.5V		85	100	mA
PD Power Dissipation	P0 = "0"		45	71.5	mW
	P0 = "1"		400	550	mW
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs
DC Characteristics					
VIH High Level Input Voltage	TTL input	2.0			V
VIL Low Level Input Voltage				0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			–1.5	mA
Filter Characteristics					
fc Filter Cutoff Frequency	33 ≤ F_Code ≤ 127	7		27	MHz

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
FCA	Filter *fc* Accuracy	Over full *fc* range, 33 ≤ F_Code ≤ 127	-10		10	%
AO	VO_NORM Diff Gain (Note)	F = 0.67 *fc*	10		100	V/V
AD	VO_DIFF Diff Gain (Note)	F = 0.67 *fc*, set with serial port	10		50	V/V
VO_NORM Gain Tolerance		AO = 100	-15		15	%
VO_DIFF Gain Tolerance		AD = 50	-15		15	%
FB	Frequency Boost at *fc*	FB(dB) = 20 log [.01563 (S_Code) +1]	0		9.5	dB
FBA	Frequency Boost Accuracy	0 to 9.5 dB	−1.25		+1.25	dB
TGD0	Group Delay Variation Without Boost gdm = group delay magnitude	0.2 *fc* - *fc*	−2% gdm		+2% gdm	ns
		fc - 1.75 *fc*	−3% gdm		+3% gdm	ns
TGDB	Group Delay Variation With Boost	0.2 *fc* - *fc*	−2% gdm		+2% gdm	ns
		fc - 1.75 *fc*	−3% gdm		+3% gdm	ns
VOF	Filter Output Dynamic Range	Vo_NORM, THD = 1.5%	1			Vp-p
		Vo_DIFF, THD = 2.0%	1			Vp-p
		Vo_NORM, THD = 2.0%	1.5			Vp-p
		Vo_DIFF, THD = 3.0%	1.5			Vp-p
RIN	Filter Diff Input Resistance		3.0	3.5	4.0	kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input, 0 dB Boost		2.5	4.0	mV rms
		fc = 27 MHz, 9.5 dB Boost		3.7	10	mV rms
EOUT	Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input, 0 dB Boost		4.4	6	mV rms
		fc = 27 MHz, 9.5 dB Boost		7.8	14	mV rms
IO−	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		3.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1 mA		30	50	Ω
$\overline{SCLK}$ Period, TC			100			ns
$\overline{SDEN}$ Set-up WRT $\overline{SCLK}$ Rising Edge			10		25	ns
$\overline{SDEN}$ Hold WRT $\overline{SCLK}$ Rising Edge			5		TC/2-10	ns

Note: The overall gain of VO_DIFF with respect to VIN is 10 to 50 V/V. Additionally, the gain of VO_NORM with respect to VO_DIFF will be adjustable and have gain values of 1.0, 1.5 and 2.0.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
$\overline{SDEN}$ Rises Prior to $\overline{SCLK}$ Falls		15			ns
SDI Set-up WRT $\overline{SCLK}$ Rising Edge		15			ns
SDI Hold WRT $\overline{SCLK}$ Rising Edge		15			ns
Power Supply Rejection Ratio	100 mVp-p in VCA, VCD from 100 kHz to 10 MHz	45	70		dB
Common Mode Rejection Ratio	VIN = 0 VDC + 100 mVp-p from 100 kHz to 10 MHz	40	65		dB
DC Bias: VO_NORM+, VO_NORM-, VO_DIFF+, VO_DIFF-	VCC = 5V, single ended	2.05	2.55	3.05	V
Vin+, Vin-		2.5	3.0	3.5	V
Delay mismatch normal and differentiated outputs				1	ns

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TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

e.g., fc = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

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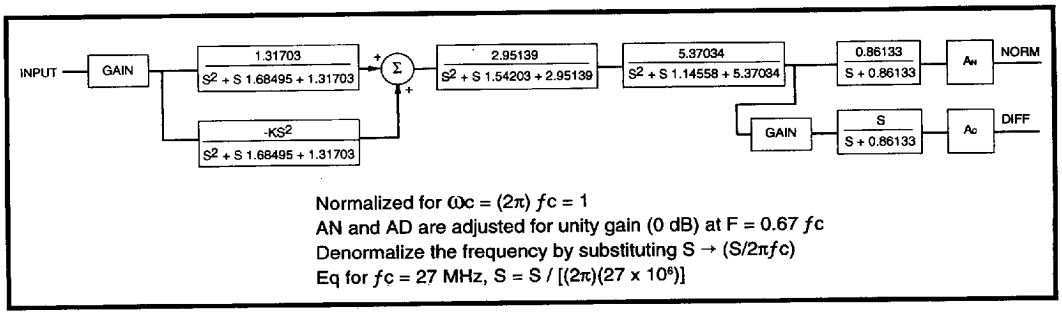
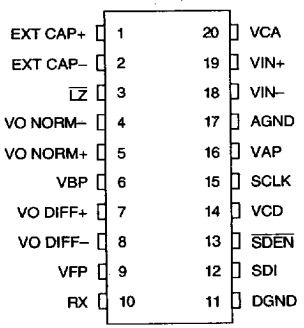


FIGURE 2: 32F8144 Normalized Block Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



20-lead SOL, SOV

THERMAL CHARACTERISTICS: θja

20-lead SOL	95°C/W
20-Lead SOV	125°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDERING NUMBER	PACKAGE MARK
SSI 32F8144	20-Lead SOL (300 mil)	32F8144 - CL	32F8144 - CL
SSI 32F8144	20-Lead SOV (220mil)	32F8144 - CV	32F8144 - CV

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