

STRH100N10FSY1 STRH100N10FSY3

N-channel 100V - 0.024Ω - TO-254AA rad-hard low gate charge STripFET™ Power MOSFET

Features

Туре	V _{DSS}
STRH100N10FSY1	100 V
STRH100N10FSY3	100 V

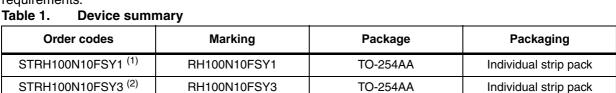
- Low R_{DS(on)}
- Fast switching
- Single event effect (SEE) hardned
- Low total gate charge
- Light weight
- 100% avalanche tested
- Application oriented characterization
- Hermetically sealed
- Heavy ion SOA
- 100 kRad TID
- SEL & SEGR with 34Mev/cm²/mg LET ions

Applications

- Satellite
- High reliability

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to sustain high TID and provide immunity to heavy ion effects. It is therefore suitable as power switch in mainly high-efficiency DC-DC converters. It is also intended for any application with low gate charge drive requirements.



^{1.} Mil temp range

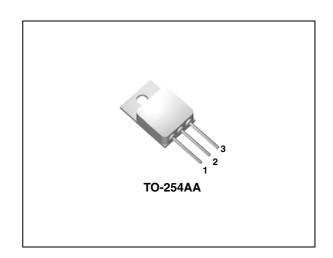
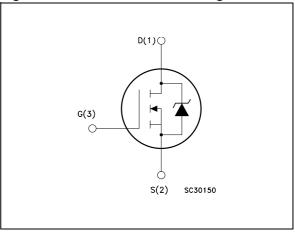


Figure 1. Internal schematic diagram



^{2.} Space flights parts (full ESCC flow screening)

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1 Electrical ratings

Table 2. Absolute maximum ratings (pre-irradiation)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	100	٧
V _{GS}	Gate-source voltage	±14	٧
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	72	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	52	Α
I _{DM} ⁽²⁾	Drain current (pulsed)	288	Α
P _{TOT} ⁽¹⁾	Total dissipation at T _C = 25 °C	170	W
dv/dt (3)	Peak diode recovery voltage slope	3.7	V/ns
T _{stg}	Storage temperature	-55 to 150	°C
T _j	Max. operating junction temperature	150	°C

^{1.} Rated according to the Rthj-case + Rthc-s

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.52	°C/W
Rthc-s	Case-to-sink typ	0.21	°C/W
Rthj-amb	Thermal resistance junction -amb max	48	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	40	Α
E _{AS}	Single pulse avalanche energy (starting Tj=25 °C, I _D = I _{AR} , V _{DD} =50 V)	824	mJ
E _{AR}	Repetitive avalanche ⁽¹⁾	53	mJ

^{1.} Pulse number = 10; f= 10 KHz; D.C. = 50%

^{2.} Pulse width limited by safe operating area

^{3.} $I_{SD} \le 80 \text{ A}$, di/dt $\le 1100 \text{A/}\mu\text{s}$, $V_{DD} = 80\% \ V_{(BR)DSS}$

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

2.1 Pre-irradiation

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	80% BV _{Dss}			10	μΑ
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±14 V			±100	nA
BV _{DSS}	Drain-to-source breakdown voltage	V _{GS} = 0V, I _D = 1m A	100			٧
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 1m A$	2		4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 12V; I _D = 36 A		0.024	0.028	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{GS} = 0, V_{DS} = 25 V, f=1MHz V_{DD} = 50 V, I_{D} = 36 A, V_{GS} =12 V $f=1MHz \text{ Gate DC Bias=0}$ Test signal level=20mV open drain	5280 568 168	6600 710 210	7980 852 252	pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-to-source charge Gate-to-drain ("Miller") charge		128 25.6 40	160 32 50	192 38.4 60	nC nC nC
R _G	Gate input resistance		1.6	2	2.4	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
t _{d(on)}	Turn-on delay time		29.6	37	44.4	ns
t _r	Rise time	$V_{DD} = 50 \text{ V}, I_{D} = 40 \text{ A},$	48	60	72	ns
t _{d(off)}	Turn-off-delay time	$R_G = 4.7 \Omega$, $V_{GS} = 12 V$	92	115	138	ns
ì, ′	Fall time		46.4	58	69.6	ns

Symbol	Parameter Test conditions I		Min.	Тур.	Max	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)				72 288	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 72 A, V _{GS} = 0			1.1	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 72 A, di/dt = 100 A/μs V _{DD} = 50 V, Tj = 25 °C	265	332 4.48 27	398	ns µC A
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 72 A, di/dt = 100 A/μs V _{DD} = 50 V, Tj = 150 °C	304	380 5.62 29.6	456	ns μC A

Table 8. Source drain diode

2.2 Post-irradiation

The ST rad-hard Power MOSFETs are tested to verify the radiation capability. The technology is extremely resistant to assurance well functioning of the device inside the radiation environments. Every manufacturing lot is tested for total ionizing dose.

(@Tj=25 °C up to 100 Krad (a))

Table 9. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	80% BV _{Dss}			10	μΑ
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±14 V			±100	nA
BV _{DSS}	Drain-to-source breakdown voltage	$V_{GS} = 0V$, $I_D = 1$ mA	100			٧
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	2		4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 12 V; I _D = 36 A		0.024	0.028	Ω

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration = 300µs, duty cycle 1.5%

a. According to ESCC 22900 specification, Co60 gamma rays, dose rags:0.1rad/sec.

Table 10. Single event effect, SOA⁽¹⁾

lon	Let (Mev/(mg/cm ²)	Energy (MeV)	Range (µm)	V _{DS} (V) @V _{GS} 0V
Kr	34	316	43	100
Xe	55.9	459	43	100

Rad-Hard Power MOSFETs have been characterized in heavy ion environment for single event effect (SEE). Single event effect characterization is illustrated

Figure 2. Bias condition during radiation

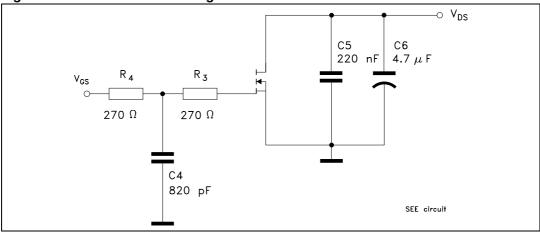


Table 11. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)				72 288	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 72 A, V _{GS} = 0			1.1	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 72 A, di/dt = 100 A/μs V _{DD} = 50 V, Tj = 25 °C	265	332 4.48 27	398	ns μC A
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- 1. Pulse width limited by safe operating area
- 2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.3 Electrical characteristics (curves)

Figure 3. Safe operating area

Figure 4. Thermal impedance

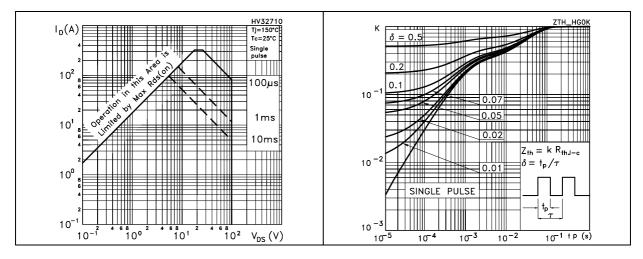


Figure 5. Output characteristics

Figure 6. Transfer characteristics

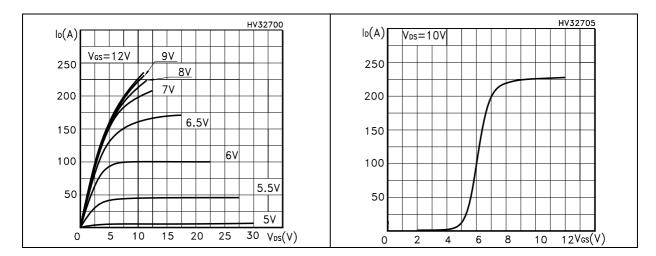


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

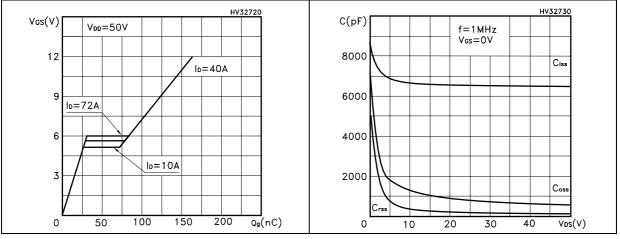


Figure 9. Normalized BV_{DSS} vs temperature Figure 10. Static drain-source on resistance

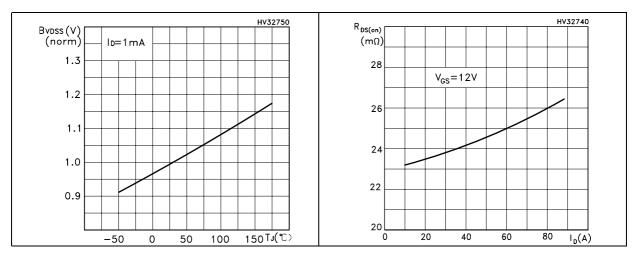


Figure 11. Normalized gate threshold voltage Figure 12. Normalized on resistance vs vs temperature temperature

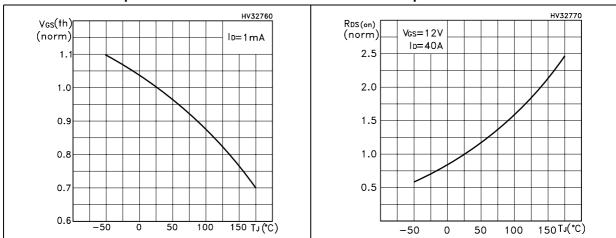
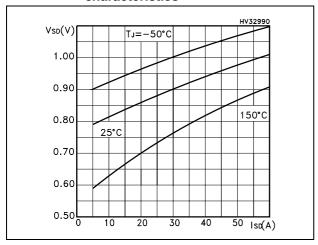


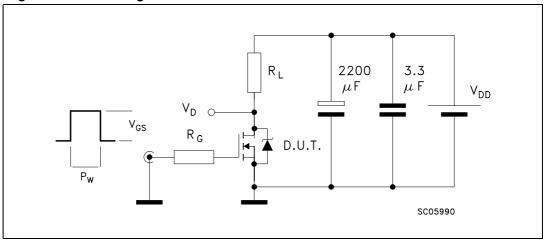
Figure 13. Source drain-diode forward characteristics



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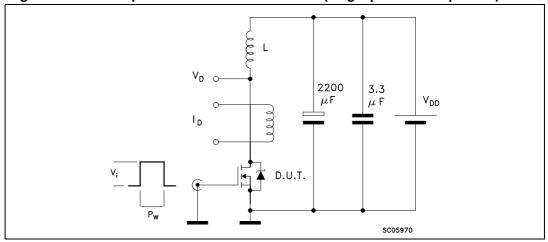
3 Test circuit

Figure 14. Switching times test circuit for resistive load ⁽¹⁾



1. Max driver V_{GS} slope = 1V/ns (no DUT)

Figure 15. Unclamped inductive load test circuit (single pulse and repetitive)



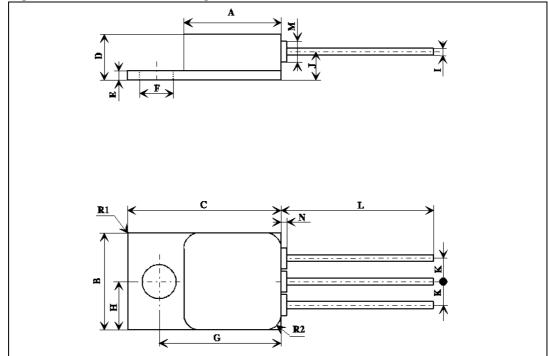
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 12. TO-254AA mechanical data

DIM.	mm.			inch		
	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
Α	13.59		13.84	0.535		0.545
В	13.59		13.84	0.535		0.545
С	20.07		20.32	0.790		0.80
D	6.32		6.60	0.249		0.260
E	1.02		1.27	0.040		0.050
F	3.53		3.78	0.139		0.149
G	16.89		17.40	0.665		0.685
Н		6.86			0.270	
I	0.89		1.14	0.035		0.045
J		3.81			0.150	
К		3.81			0.150	
L	12.95		14.50	0.510		0.570
М		3.05			0.120	
N			0.71			0.025
R1			1.0			0.040
R2		1.65			0.065	

Figure 16. Mechanical drawing



5 Revision history

Table 13. Document revision history

Date	Revision	Changes	
03-Jul-2006	1	First release	
18-Dec-2006	2	Figure 3. has been updated	
15-Mar-2007	3	Complete version	
22-Oct-2007	4 Note 2 on device summary has been updated		
14-Nov-2007 5		Added figures: 2 and 15. Updated values on tables: 6, 7, 8 and 11 Minor text changes to improve readability	

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