NEC

MOS INTEGRATED CIRCUIT

μPD750104,750106,750108,750104(A),750106(A),750108(A)

4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD750108 is one of the 75XL series 4-bit single-chip microcontrollers, which provide data processing capability equal to that of an 8-bit microcontroller.

The μPD750108 is produced by replacing the main system clock oscillator of the μPD750008 with an RC oscillator, enabling operation at a relatively low voltage of 1.8 V. In addition, it is best suited to applications using batteries. The μPD750108(A) has a higher reliability than the μPD750108.

A built-in one-time PROM product, μPD75P0116, is also available. It is suitable for small-scale production and evaluation of application systems.

The following user's manual describes the details of the functions of the μPD750108. Be sure to read it before designing application systems.

μPD750108 User's Manual: U11330E

FEATURES

- Built-in RC oscillator
- Enables the immediate start of processing after the release of standby mode
- Capable of low-voltage operation: V_{DD} = 1.8 to 5.5 V
- Internal memory
  Program memory (ROM)
  : 4,096 × 8 bits (μPD750104 and μPD750104(A))
  : 6,144 × 8 bits (μPD750106 and μPD750106(A))
  : 8,192 × 8 bits (μPD750108 and μPD750108(A))
  Data memory (RAM)
  : 512 × 4 bits
- Function for specifying the instruction execution time (useful for saving power)
  4 μs, 8 μs, 16 μs, 64 μs (when operating at 1.0 MHz)
  2 μs, 4 μs, 8 μs, 32 μs (when operating at 2.0 MHz)
  122 μs (when operating at 32.768 kHz)
- Enhanced timer function (4 channels)
- Can be easily substituted for the μPD750008 because this product succeeds to the functions and instructions of the μPD750008.

APPLICATIONS

- μPD750104, μPD750106, and μPD750108
  Cameras, meters, and pagers
- μPD750104(A), μPD750106(A), and μPD750108(A)
  Electrical equipment for automobiles

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The mark ★ shows major revised points.

The μPD750104, μPD750106, μPD750108, μPD750104(A), μPD750106(A), and μPD750108(A) differ only in quality grade. In this manual, the μPD750108 is described unless otherwise specified. Users of other than the μPD750108 should read μPD750108 as referring to the pertinent product.

When the description differs among μPD750104, μPD750106, and μPD750108, they also refer to the pertinent (A) products.

μPD750104 → μPD750104(A), μPD750106 → μPD750106(A), μPD750108 → μPD750108(A)

ORDERING INFORMATION

Part number	Package	Quality grade
μPD750104CU-×××	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Standard
★ μPD750104CU-×××-A	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Standard
μPD750104GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Standard
★ μPD750104GB-×××-3BS-MTX-A	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Standard
μPD750106CU-×××	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Standard
★ μPD750106CU-×××-A	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Standard
μPD750106GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Standard
★ μPD750106GB-×××-3BS-MTX-A	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Standard
μPD750108CU-×××	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Standard
★ μPD750108CU-×××-A	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Standard
μPD750108GB-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Standard
★ μPD750108GB-×××-3BS-MTX-A	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Standard
μPD750104CU(A)-×××	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Special
μPD750104GB(A)-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm-pitch)	Special
μPD750106CU(A)-×××	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Special
μPD750106GB(A)-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Special
μPD750108CU(A)-×××	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)	Special
μPD750108GB(A)-×××-3BS-MTX	44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	Special

Remarks 1. Products with "-A" at the end of the part number are lead-free products.

2. ××× is a mask ROM code number.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of quality grade on the devices and its recommended applications.

DIFFERENCES BETWEEN μPD75010× AND μPD75010×(A)

Product number / Item	μPD750104 μPD750106 μPD750108	μPD750104(A) μPD750106(A) μPD750108(A)
Quality grade	Standard	Special

FUNCTIONS

Item		Function	
Command execution time		• 4, 8, 16, or 64 μs (when the main system clock operates at 1.0 MHz) • 2, 4, 8, or 32 μs (when the main system clock operates at 2.0 MHz) • 122 μs (when the subsystem clock operates at 32.768 kHz)	
Internal memory	ROM	4,096 × 8 bits (μPD750104)	
		6,144 × 8 bits (μPD750106)	
		8,192 × 8 bits (μPD750108)	
	RAM	512 × 4 bits	
General-purpose register		• When operating in 4 bits: 8 × 4 banks • When operating in 8 bits: 4 × 4 banks	
I/O port	CMOS input	8	Can incorporate 7 pull-up resistors that are specified with the software.
	CMOS I/O	18	Can directly drive the LED. Can incorporate 18 pull-up resistors that are specified with the software.
	N-ch open drain I/O	8	Can directly drive the LED. Can withstand 13 V. Can incorporate pull-up resistors that are specified with the mask option.
	Total	34	
Timer		4 channels • 8-bit timer/event counter: 1 channel • 8-bit timer counter: 1 channel • Basic interval timer/watchdog timer: 1 channel • lock timer: 1 channel	
Serial interface		• Three-wire serial I/O mode ... switchable between the start LSB and the start MSB • Two-wire serial I/O mode • SBI mode	
Bit sequential buffer (BSB)		16 bits	
Clock output (PCL)		• Φ, 125, 62.5, or 15.6 kHz (when the main system clock operates at 1.0 MHz) • Φ, 250, 125, or 31.3 kHz (when the main system clock operates at 2.0 MHz)	
Buzzer output (BUZ)		• 2, 4, or 32 kHz (when the subsystem clock operates at 32.768 kHz) • 0.488, 0.977, or 7.813 kHz (when the main system clock operates at 1.0 MHz) • 0.977, 1.953, or 15.625 kHz (when the main system clock operates at 2.0 MHz)	
Vectored interrupt		External : 3 Internal : 4	
Test input		External : 1 Internal : 1	
System clock oscillator		• RC oscillator for main system clock (with external resistor and capacitor) • Crystal oscillator for subsystem clock	
Standby		STOP/HALT mode	
Operating ambient temperature range		T_A = -40 to +85 °C	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)	

CONTENTS

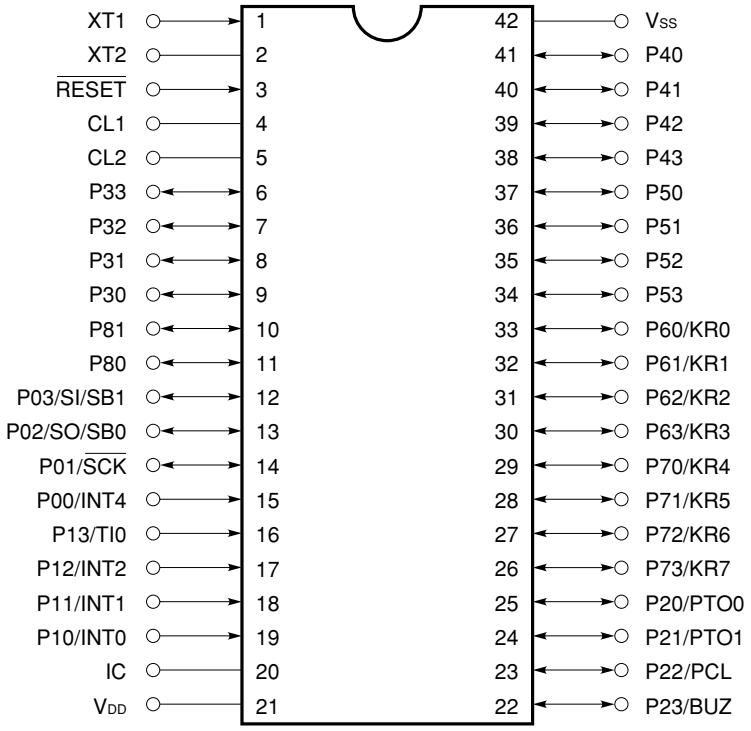
1. PIN CONFIGURATION (TOP VIEW)

- **42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)**

★ μPD750104CU-×××, μPD750104CU-×××-A, μPD750104CU(A)-×××

★ μPD750106CU-×××, μPD750106CU-×××-A, μPD750106CU(A)-×××

★ μPD750108CU-×××, μPD750108CU-×××-A, μPD750108CU(A)-×××



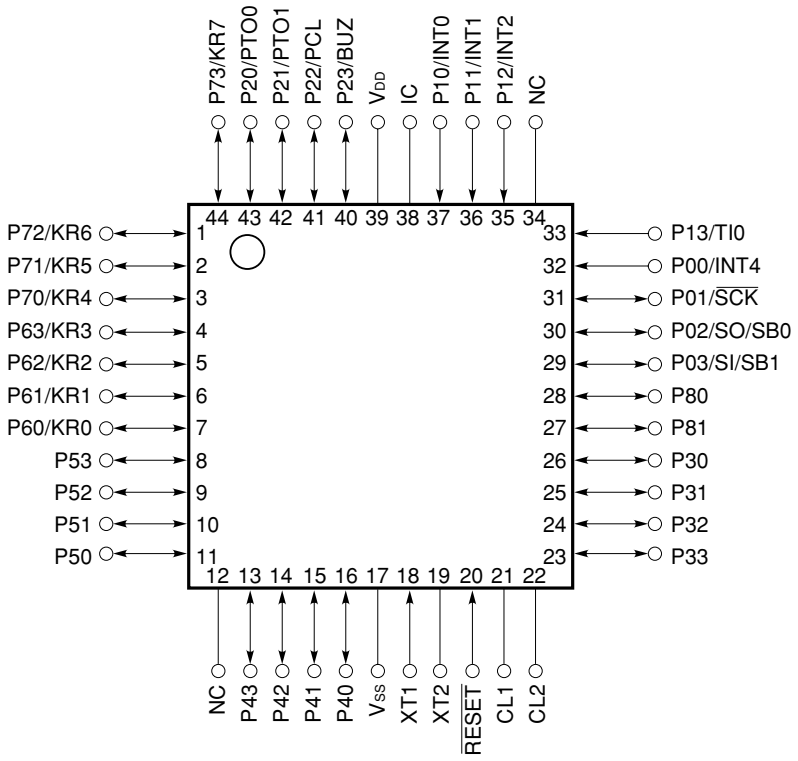
IC : Internally connected (Connect directly to V_{DD}.)

- **44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)**

★ μPD750104GB-×××-3BS-MTX, μPD750104GB-×××-3BS-MTX-A, μPD750104GB(A)-×××-3BS-MTX

★ μPD750106GB-×××-3BS-MTX, μPD750106GB-×××-3BS-MTX-A, μPD750106GB(A)-×××-3BS-MTX

★ μPD750108GB-×××-3BS-MTX, μPD750108GB-×××-3BS-MTX-A, μPD750108GB(A)-×××-3BS-MTX

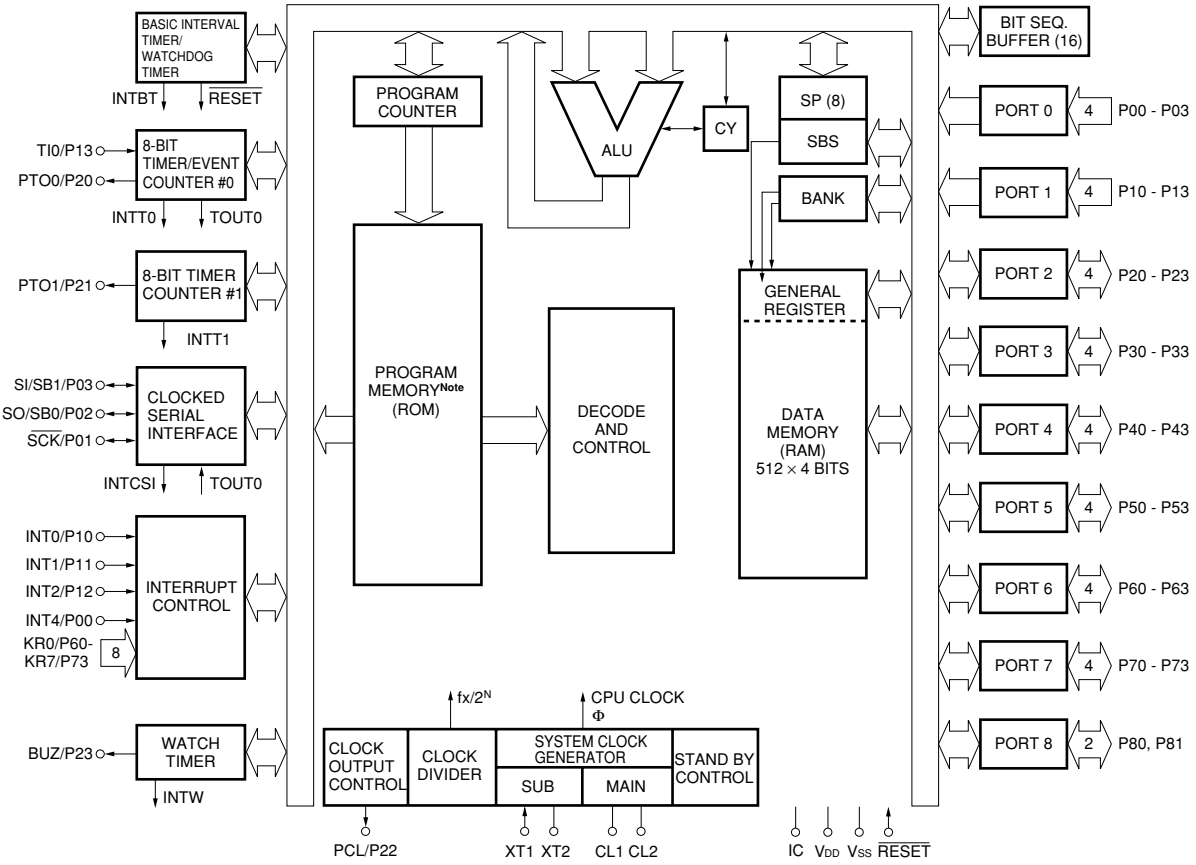


IC : Internally connected (Connect directly to V_{DD}.)

PIN NAMES

BUZ	:	Buzzer Clock	P70-P73	:	Port 7
CL1, CL2	:	Main System Clock (RC)	P80, P81	:	Port 8
IC	:	Internally Connected	PCL	:	Programmable Clock
INT0, 1, 4	:	External Vectored Interrupt 0, 1, 4	PTO0, PTO1	:	Programmable Timer Output 0, 1
INT2	:	External Test Input 2	$\overline{\text{RESET}}$	:	Reset
KR0-KR7	:	Key Return 0-7	SB0, SB1	:	Serial Bus 0, 1
NC	:	No connection	$\overline{\text{SCK}}$	:	Serial Clock
P00-P03	:	Port 0	SI	:	Serial Input
P10-P13	:	Port 1	SO	:	Serial Output
P20-P23	:	Port 2	TI0	:	Timer Input 0
P30-P33	:	Port 3	V_{DD}	:	Positive Power Supply
P40-P43	:	Port 4	V_{SS}	:	Ground
P50-P53	:	Port 5	XT1, XT2	:	Subsystem Clock (Crystal)
P60-P63	:	Port 6			

2. BLOCK DIAGRAM



Note The ROM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin name	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0). For P01 - P03, built-in pull-up resistors can be connected by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	4-bit input port (PORT1). Built-in pull-up resistors can be connected by software in units of 4 bits. A noise eliminator can be selected only when the P10/INT0 pin is used.	×	Input	Ⓑ-C
P11		INT1				
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Built-in pull-up resistors can be connected by software in units of 4 bits.	×	Input	E-B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30 - P33	I/O	-	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Built-in pull-up resistors can be connected by software in units of 4 bits.	×	Input	E-B
P40 - P43[Note 2]	I/O	-	N-ch open-drain 4-bit I/O port (PORT4). A pull-up resistor can be provided bit by bit (mask option). Withstand voltage is 13 V in open-drain mode.	○	High level (when pull-up resistors are provided) or high impedance	M-D
P50 - P53[Note 2]	I/O	-	N-ch open-drain 4-bit I/O port (PORT5). A pull-up resistor can be provided bit by bit (mask option). Withstand voltage is 13 V in open-drain mode.		High level (when pull-up resistors are provided) or high impedance	M-D
P60	I/O	KR0	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Built-in pull-up resistors can be connected by software in units of 4 bits.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	4-bit I/O port (PORT7). Built-in pull-up resistors can be connected by software in units of 4 bits.		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	I/O	-	2-bit I/O port (PORT8). Built-in pull-up resistors can be connected by software in units of 2 bits.	×	Input	E-B
P81		-				

Notes 1. The circle (○) indicates the Schmitt trigger input.

2. When pull-up resistors that can be specified with the mask option are not incorporated (when pins are used as N-ch open-drain input ports), the input leak low current increases when an input instruction or bit operation instruction is executed.

3.2 Non-Port Pins

Pin name	Input/ output	Shared pin	Function	When reset	I/O circuit type Note 1
TI0	Input	P13	Inputs external event pulse to the timer/event counter	Input	Ⓑ-C
PTO0	Output	P20	Timer/event counter output	Input	E-B
PTO1		P21	Timer counter output		
PCL		P22	Clock output		
BUZ		P23	Arbitrary frequency output (for buzzer output or system clock trimming)		
$\overline{SCK}$	I/O	P01	Serial clock I/O	Input	Ⓕ-A
SO/SB0		P02	Serial data output Serial data bus I/O		Ⓕ-B
SI/SB1		P03	Serial data input Serial data bus I/O		Ⓜ-C
INT4	Input	P00	Edge detection vectored interrupt input (both rising and falling edges are detected)		Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input (detection edge selectable). A noise eliminator can be selected when INT0/P10 is used. Note 2	Input	Ⓑ-C
INT1		P11	Note 3		
INT2	Input	P12	Rising edge detection testable input Note 3		
KR0 - KR3	Input	P60 - P63	Falling edge detection testable input	Input	Ⓕ-A
KR4 - KR7	Input	P70 - P73	Falling edge detection testable input	Input	Ⓕ-A
CL1	-	-	Pin for connecting a resistor (R) or capacitor (C) for main system clock oscillation. An external clock cannot be input.	-	-
CL2	-				
XT1	Input	-	Crystal connection pin for subsystem clock generation. When external clock signal is used, it is applied to XT1, and it reverse phase signal is applied to XT2. XT1 can be used as a 1-bit input (test).	-	-
XT2	-				
$\overline{RESET}$	Input	-	System reset input (active low)	-	Ⓑ
IC	-	-	Internally connected. (To be connected directly to V_{DD})	-	-
V_{DD}	-	-	Positive power supply	-	-
V_{SS}	-	-	Ground potential	-	-

Notes 1. The circle (◯) indicates the Schmitt trigger input.

2. With a noise eliminator/asynchronously selectable

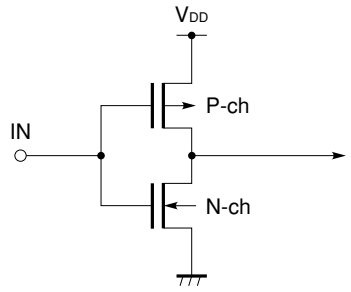
3. Asynchronous

3.3 Pin Input/Output Circuits

The input/output circuit of each μPD750108 pin is shown below in a simplified manner.

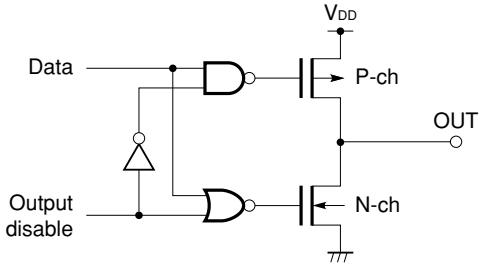
(1/2)

Type A



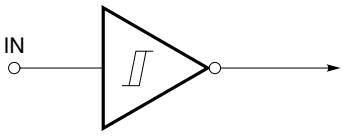
CMOS input buffer

Type D



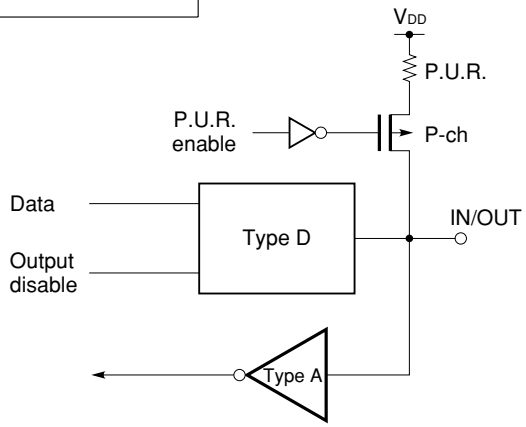
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



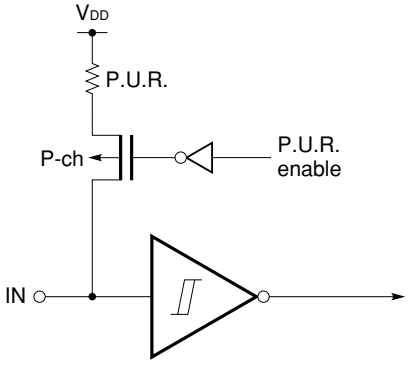
Schmitt trigger input with hysteresis

Type E-B



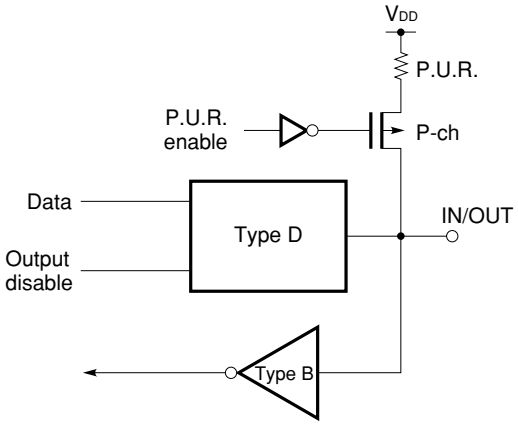
P.U.R.: Pull-Up Resistor

Type B-C



P.U.R.: Pull-Up Resistor

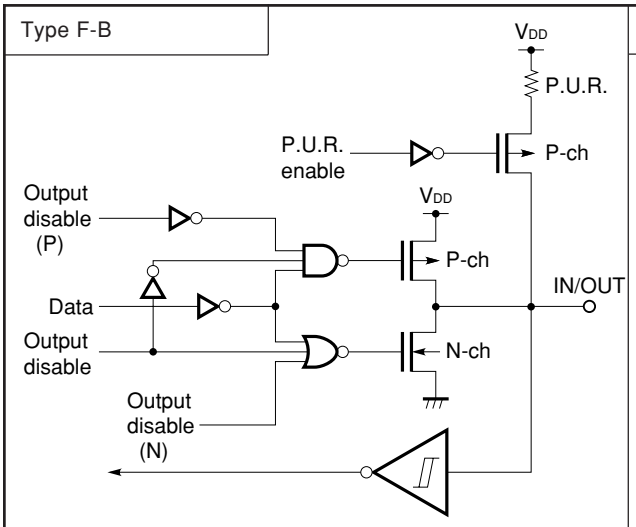
Type F-A



P.U.R.: Pull-Up Resistor

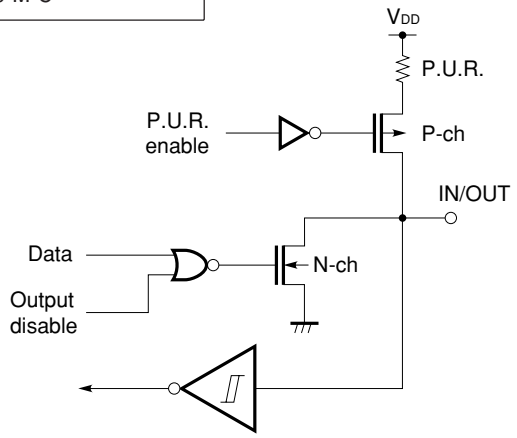
(2/2)

Type F-B



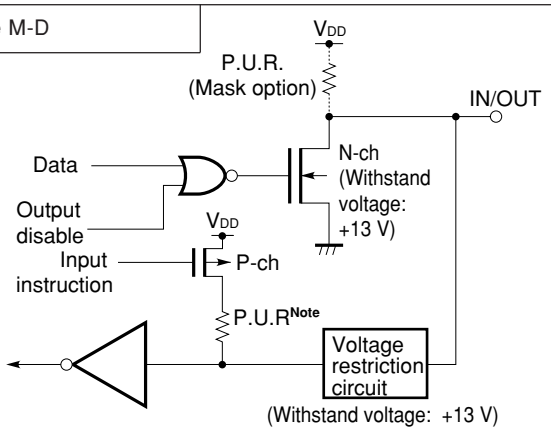
P.U.R.: Pull-Up Resistor

Type M-C



P.U.R.: Pull-Up Resistor

Type M-D



P.U.R.: Pull-Up Resistor

Note Pull-up resistor that operates only when pull-up resistors that can be specified with the mask option are not incorporated and an input instruction is executed. (When the pin is low, the current flows from V_{DD} to the pin.)

3.4 Connection of Unused Pins

Table 3-1. Connection of Unused Pins

Pin name	Recommended connection
P00/INT4	To be connected to V_{SS} or V_{DD}
P01/$\overline{SCK}$	To be connected to V_{SS} or V_{DD} through a separate resistor
P02/SO/SB0	
P03/SI/SB1	To be connected to V_{SS}
P10/INT0 - P12/INT2	To be connected to V_{SS} or V_{DD}
P13/TI0	
P20/PTO0	Input state : To be connected to V_{SS} or V_{DD} through a separate resistor Output state : To be left open
P21/PTO1	
P22/PCL	
P23/BUZ	
P30 - P33	
P40 - P43	Input state : To be connected to V_{SS} Output state : To be connected to V_{SS} (Do not connect to a pull-up resistor specified with a mask option.)
P50 - P53	
P60/KR0 - P63/KR3	Input state : To be connected to V_{SS} or V_{DD} through a separate resistor Output state : To be left open
P70/KR4 - P73/KR7	
P80, P81	
XT1**Note**	To be connected to V_{SS} or V_{DD}
XT2**Note**	To be left open
IC	To be connected directly to V_{DD}

Note When the subsystem clock is not used, set SOS.0 to 1 (not to use the built-in feedback resistor).

4. Mk I MODE/Mk II MODE SWITCH FUNCTION

4.1 Differences between Mk I Mode and Mk II Mode

The CPU of the μPD750108 has two modes (Mk I mode and Mk II mode) and which mode is used is selectable. Bit 3 of the stack bank selection register (SBS) determines the mode.

- Mk I mode: This mode has the upward compatibility with the 75X series.
  It can be used in the 75XL CPUs having a ROM of up to 16 KB.
- Mk II mode: This mode is not compatible with the 75X series.
  It can be used in all 75XL CPUs, including those having a ROM of 16 KB or more.

Table 4-1 shows the differences between Mk I mode and Mk II mode.

Table 4-1. Differences between Mk I Mode and Mk II Mode

	Mk I mode	Mk II mode
Number of stack bytes in a subroutine instruction	2 bytes	3 bytes
BRA !addr1 instruction CALLA !addr1 instruction	None	Available
CALL !addr instruction	3 machine cycles	4 machine cycles
CALLF !faddr instruction	2 machine cycles	3 machine cycles

Caution Mk II mode can be used to support a program area larger than 16K bytes in the 75X series or 75XL series. This mode enhances a software compatibility with products whose program area is larger than 16K bytes. If Mk II mode is selected, when the subroutine call instruction is executed, the number of stack bytes (use area) will be increased by one byte for each stack, compared to Mk I mode. When a CALL !addr or CALLF !faddr instruction is executed, it takes one more machine cycle. Therefore, Mk I mode should be used for applications for which RAM efficiency or processing capabilities is more critical than a software compatibility.

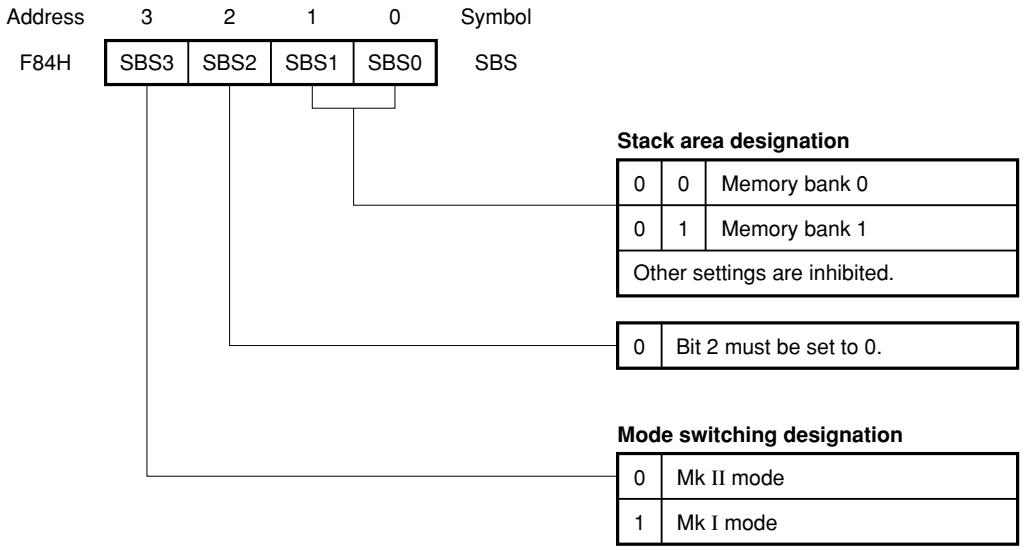
4.2 Setting of the Stack Bank Selection Register (SBS)

The Mk I mode and Mk II mode are switched by stack bank selection register. Figure 4-1 shows the register configuration.

The stack bank selection register is set with a 4-bit memory operation instruction. To use the CPU in Mk I mode, initialize the register to 100×B**Note** at the beginning of the program. To use the CPU in Mk II mode, initialize it to 000×B**Note**.

Note Specify the desired value in ×.

Figure 4-1. Stack Bank Selection Register Format



Caution The CPU operates in Mk I mode after the $\overline{\text{RESET}}$ signal is issued, because bit 3 of SBS is set to 1. Set bit 3 of SBS to 0 (Mk II mode) to use the CPU in Mk II mode.

5. MEMORY CONFIGURATION

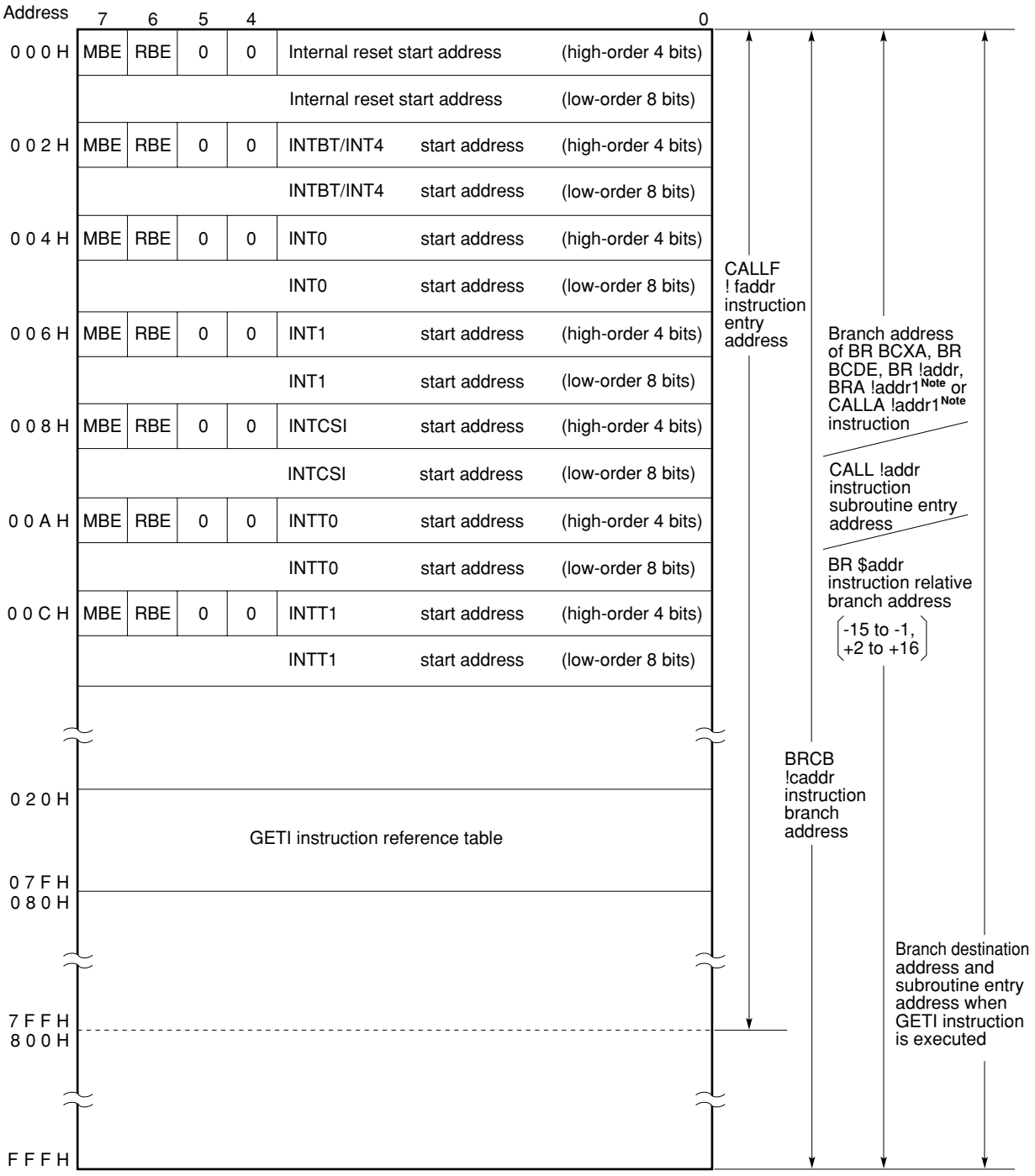
- **Program memory (ROM) : 4,096 × 8 bits (0000H-0FFFH): μPD750104**
  6,144 × 8 bits (0000H-17FFH): μPD750106
  8,192 × 8 bits (0000H-1FFFH): μPD750108

  - 0000H to 0001H
    Vector address table for holding the RBE and MBE values and program start address when a $\overline{\text{RESET}}$ signal is issued (allowing a reset start at an arbitrary address)
  - 0002H to 000DH
    Vector address table for holding the RBE and MBE values and program start address for each vectored interrupt (allowing interrupt processing to be started at an arbitrary address)
  - 0020H to 007FH
    Table area referenced by the GETI instruction**Note**

  Note The GETI instruction requires only one byte to represent an arbitrary two-byte or three-byte instruction or two one-byte instructions, reducing the number of program bytes.

- **Data memory (RAM)**
  - Data area : 512 × 4 bits (000H to 1FFH)
  - Peripheral hardware area: 128 × 4 bits (F80H to FFFH)

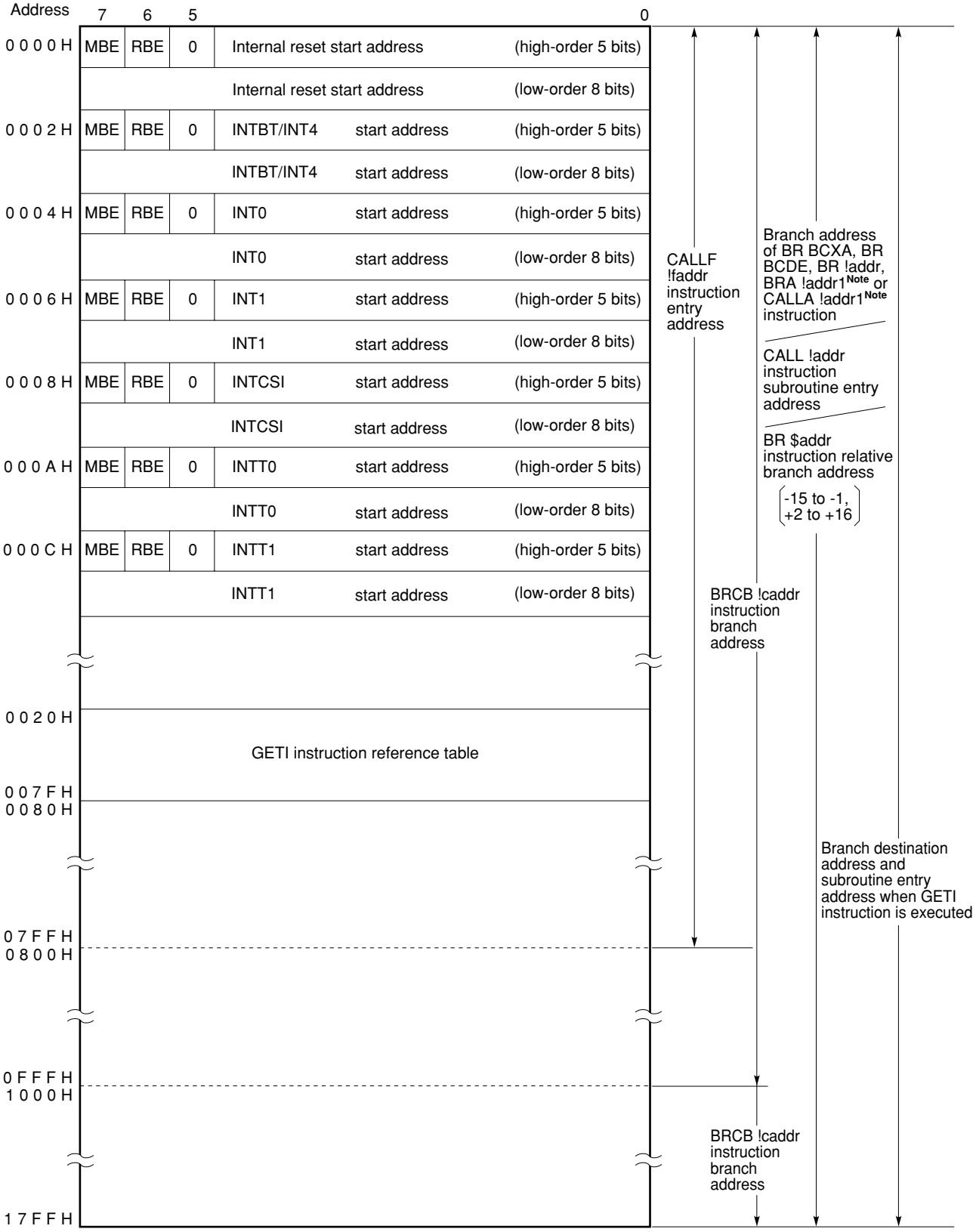
Figure 5-1. Program Memory Map (in μPD750104)



Note Can be used only in the Mk II mode.

Remark In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the 8 low-order bits of the PC changed.

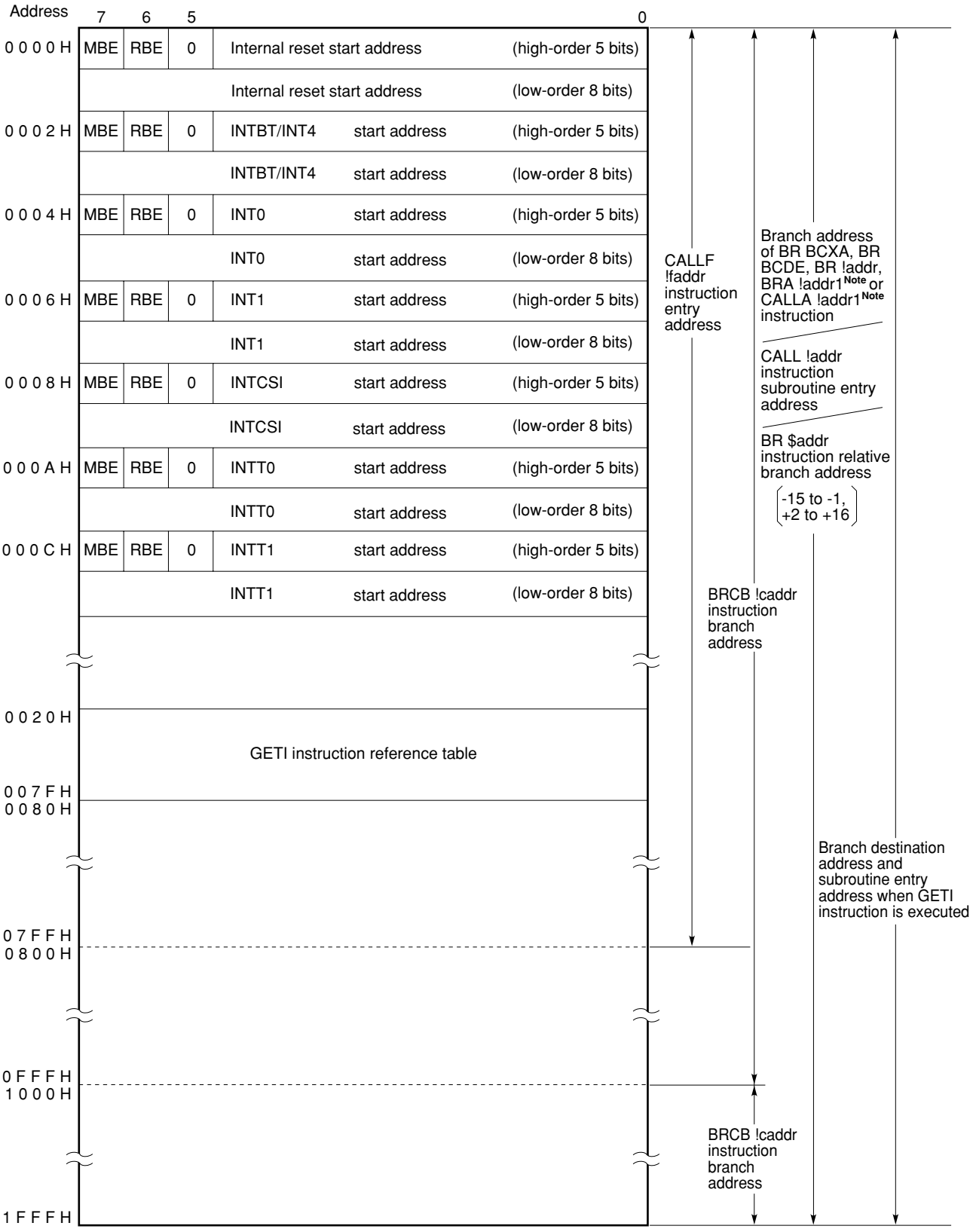
Figure 5-2. Program Memory Map (in μPD750106)



Note Can be used only in the Mk II mode.

Remark In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the 8 low-order bits of the PC changed.

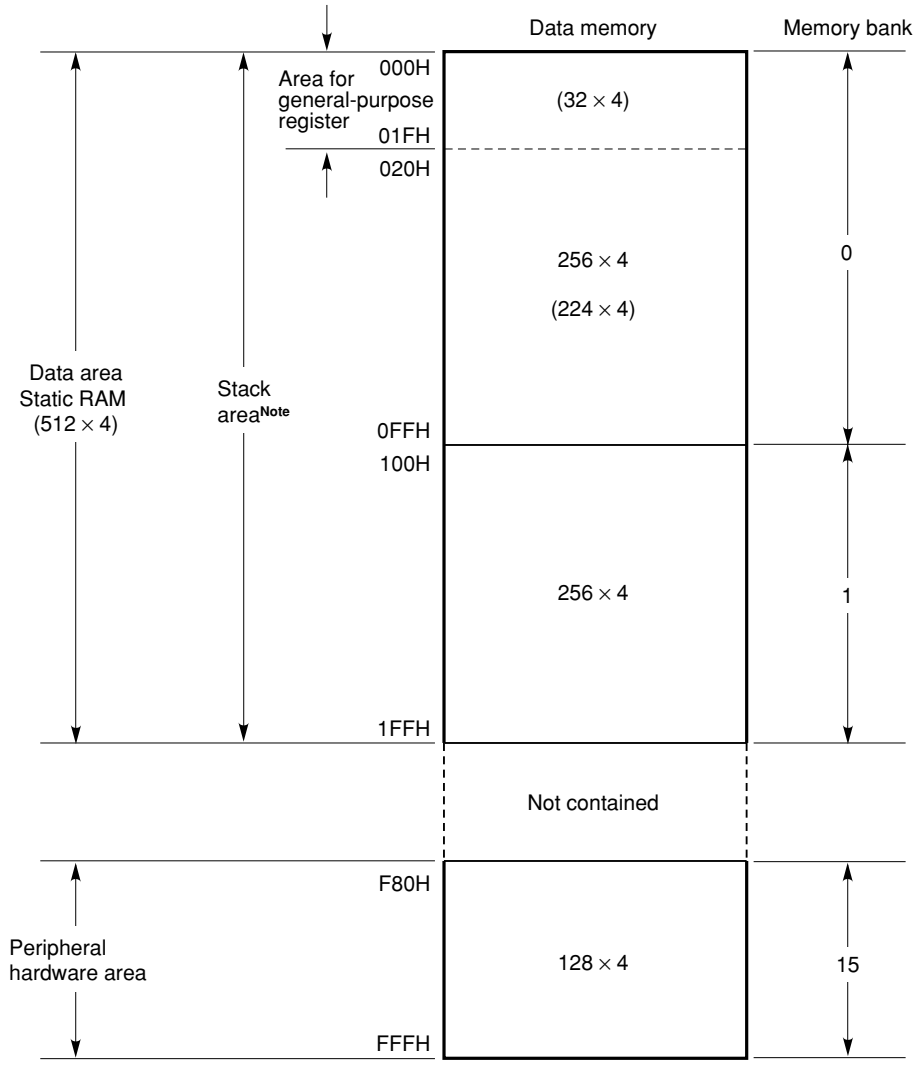
Figure 5-3. Program Memory Map (in μPD750108)



Note Can be used only in the Mk II mode.

Remark In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the 8 low-order bits of the PC changed.

Figure 5-4. Data Memory Map



Note Memory bank 0 or 1 can be selected as the stack area.

6. PERIPHERAL HARDWARE FUNCTIONS

6.1 Digital I/O Ports

The μPD750108 has the following three types of I/O port:

- 8 CMOS input pins (PORT0 and PORT1)
- 18 CMOS I/O pins (PORT2, PORT3, and PORT6 to PORT8)
- 8 N-ch open-drain I/O pins (PORT4 and PORT5)

Total: 34 pins

Table 6-1. Digital Ports and Their Features

Port name	Function	Operation and feature		Remarks
PORT0	4-bit input	When the serial interface function is used, dual-function pins function as output pins in some operation modes.		Also used as INT4, $\overline{SCK}$, SO/SB0, or SI/SB1.
PORT1		4-bit input port		Also used as INT0, INTI, INT2 or TI0.
PORT2	4-bit I/O	Allows input or output mode setting in units of 4 bits.		Also used as PTO0, PTO1, PCL, or BUZ.
PORT3		Allows input or output mode setting in units of 1 bit.		-
PORT4	4-bit I/O (N-ch open-drain can withstand 13 V)	Allows input or output mode setting in units of 4 bits. Whether to use pull-up resistors can be specified bit by bit with the mask option.	Ports 4 and 5 can be paired, allowing data I/O in units of 8 bits.	
PORT5				
PORT6	4-bit I/O	Allows input or output mode setting in units of 1 bit.	Ports 6 and 7 can be paired, allowing data I/O in units of 8 bits.	Also used as one of KR0 to KR3.
PORT7		Allows input or output mode setting in units of 4 bits.		Also used as one of KR4 to KR7.
PORT8	2-bit I/O	Allows input or output mode setting in units of 2 bits.		-

6.2 Clock Generator

The clock generator generates clocks which are supplied to the peripheral hardware in the CPU. Figure 6-1 shows the configuration of the clock generator.

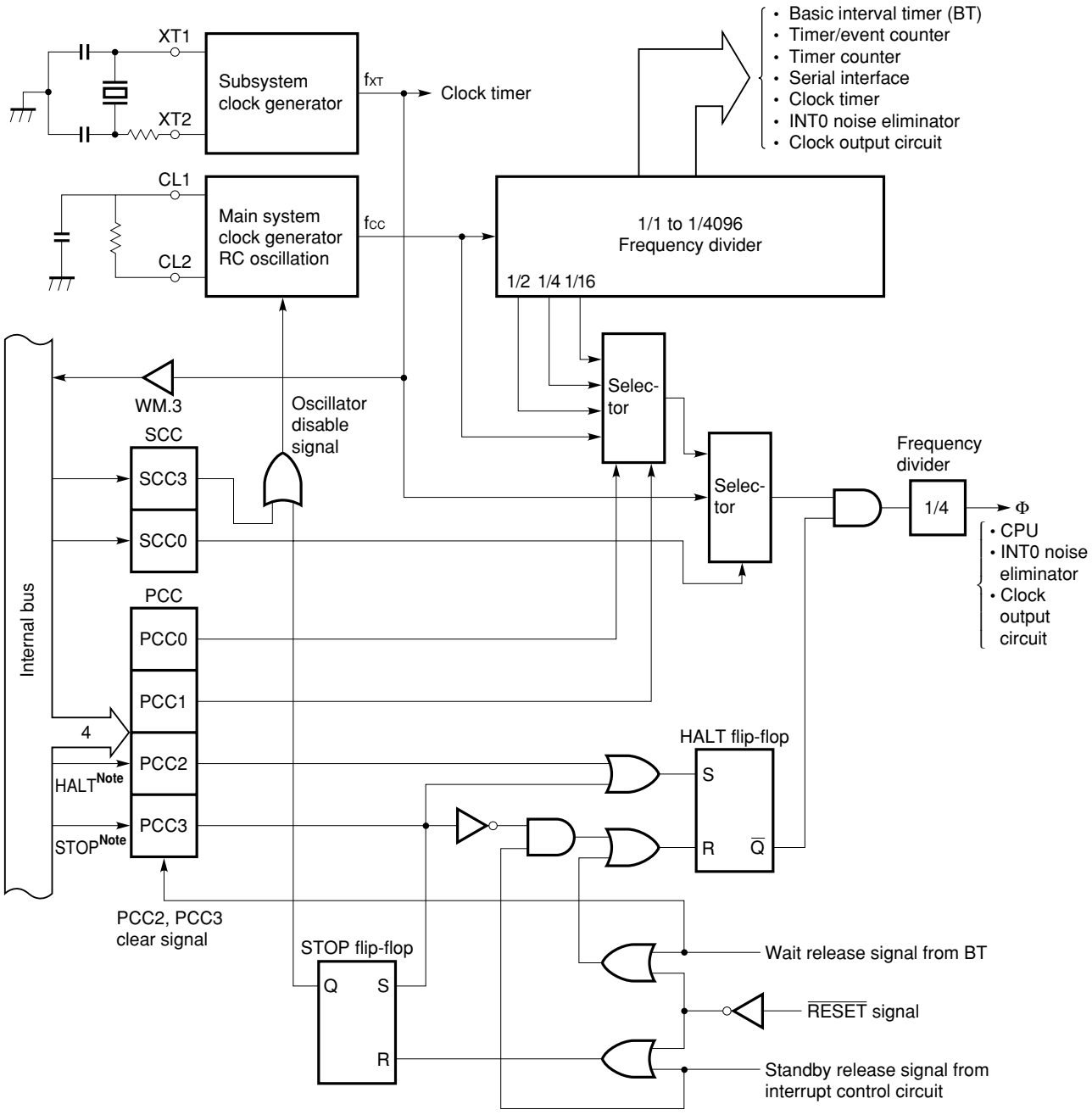
Operation of the clock generator is specified by the processor clock control register (PCC) and system clock control register (SCC).

The main system clock and subsystem clock are used.

The instruction execution time can be made variable.

- 4, 8, 16, or 64 μs (when the main system clock is at 1.0 MHz)
- 2, 4, 8, or 32 μs (when the main system clock is at 2.0 MHz)
- 122 μs (when the subsystem clock is at 32.768 kHz)

Figure 6-1. Clock Generator Block Diagram



Note Instruction execution

Remarks 1. f_{CC} = Main system clock frequency

2. f_{XT} = Subsystem clock frequency

3. Φ = CPU clock

4. PCC: Processor clock control register

5. SCC: System clock control register

6. One clock cycle (t_{CY}) of the CPU clock (Φ) is equal to one machine cycle of an instruction.

6.3 Control Functions of Subsystem Clock Oscillator

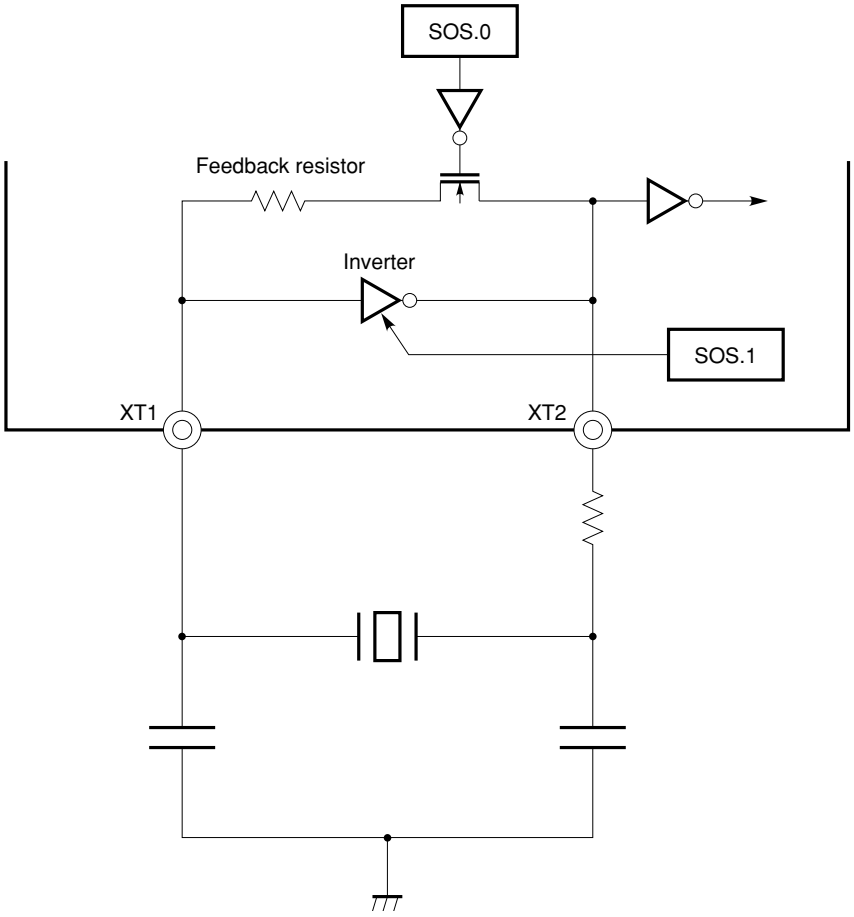
The subsystem clock oscillator of the μPD750108 has two control functions to decrease the supply current.

- The function to select with the software whether to use the built-in feedback resistor**Note**
- The function to suppress the supply current by reducing the drive current of the built-in inverter when the supply voltage is high ($V_{DD} \geq 2.7$ V)

Note When the subsystem clock is not used, set SOS.0 to 1 (not to use the built-in feedback resistor), connect XT1 to V_{SS} or V_{DD}, and open XT2. This makes it possible to reduce the supply current required by the subsystem clock oscillator.

Each function can be used by switching bits 0 and 1 in the sub-oscillator control register (SOS). (See **Figure 6-2.**)

Figure 6-2. Subsystem Clock Oscillator

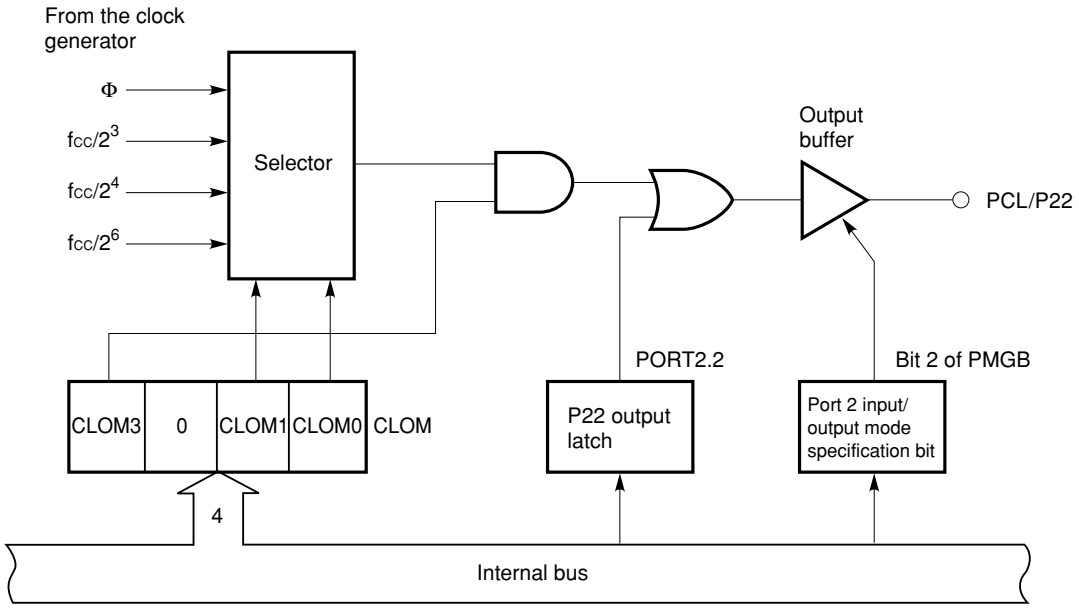


6.4 Clock Output Circuit

The clock output circuit outputs a clock pulse from the P22/PCL pin. This clock pulse is used for remote control waveform output, peripheral LSIs, etc.

- Clock output (PCL): Φ, 125, 62.5, or 15.6 kHz (at 1.0 MHz)
  Φ, 250, 125, or 31.3 kHz (at 2.0 MHz)

Figure 6-3. Clock Output Circuit Configuration



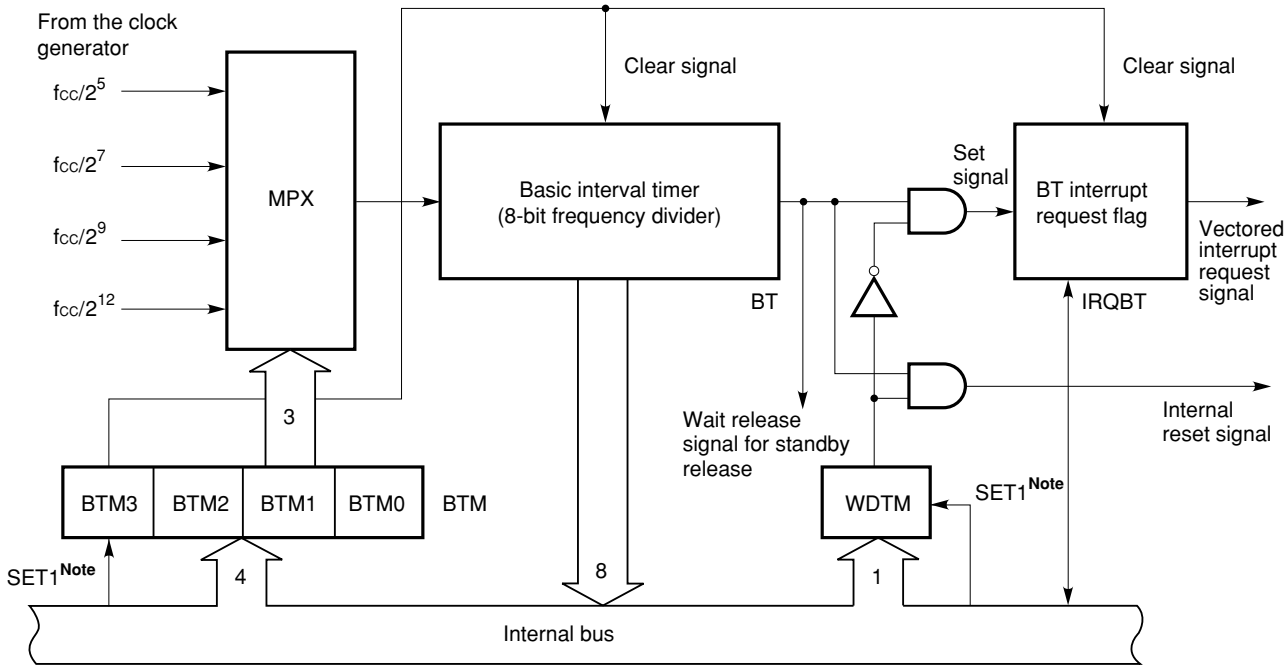
Remark Measures are taken to prevent outputting a narrow pulse when selecting clock output enable/disable.

6.5 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has these functions:

- Interval timer operation which generates a reference timer interrupt
- Operation as a watchdog timer for detecting program crashes and resetting the CPU
- Selection of wait time for releasing the standby mode and counting the wait time
- Reading out the count value

Figure 6-4. Block Diagram of the Basic Interval Timer/Watchdog Timer



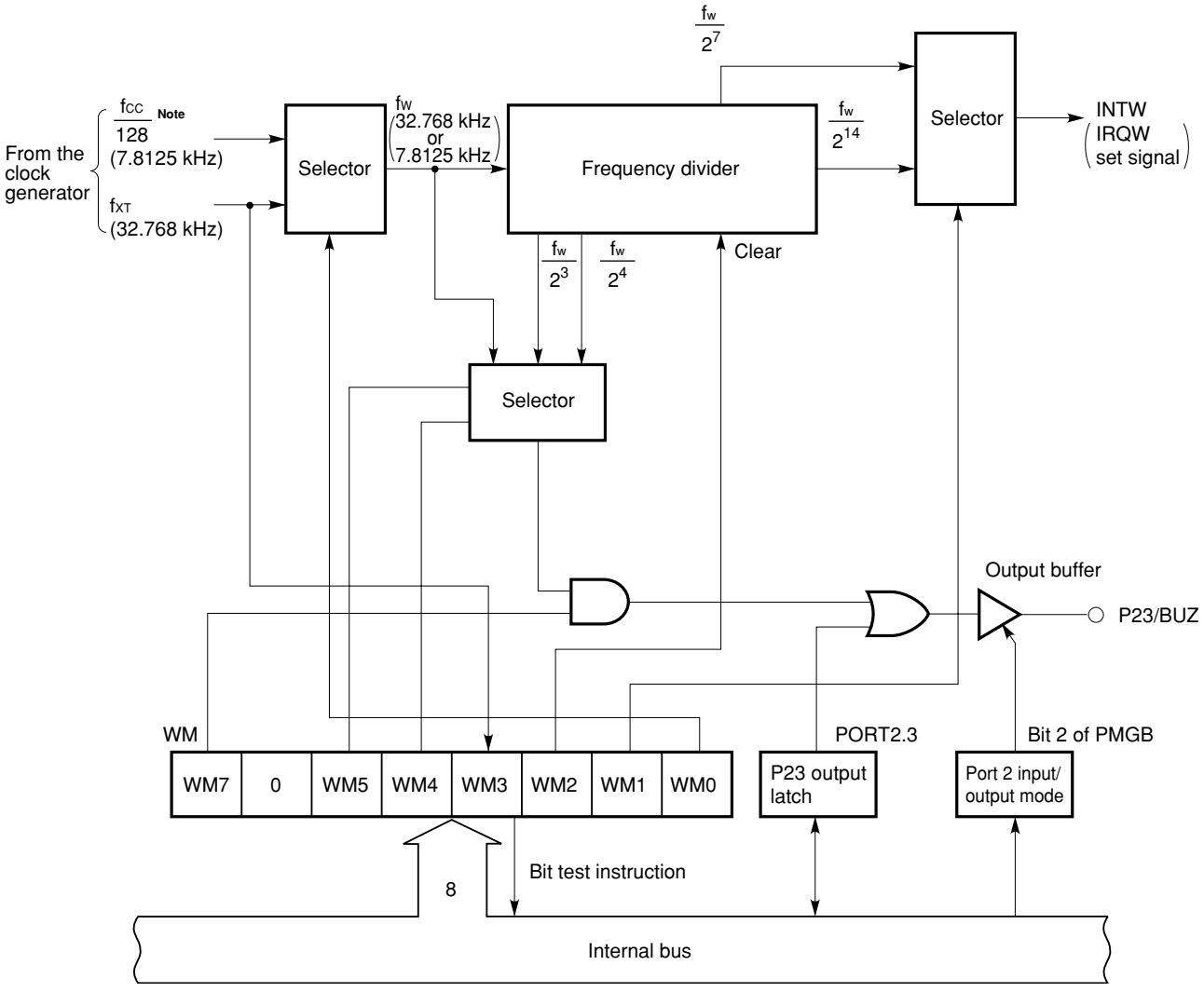
Note Instruction execution

6.6 Clock Timer

The μPD750108 contains one channel for a clock timer. The clock timer provides the following functions:

- Sets the test flag (IRQW) with a 0.5 sec interval (when WM0 = 1).
- The standby mode can be released by IRQW.
- The 0.5 second interval can be generated from the subsystem clock (32.768 kHz).
- The time interval can be made 128 times faster by selecting the fast mode. This is convenient for program debugging, testing, etc.
- Any of the frequencies ($f_W/2^4$, $f_W/2^3$, or f_W can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The clock can be started from zero seconds by clearing the frequency divider.

Figure 6-5. Clock Timer Block Diagram



Note When a frequency-divided main system clock is used, 32.768 kHz cannot be selected as the source clock frequency.

Remark The values in parentheses in the figure above are for f_{CC} = 1.0 MHz, f_{XT} = 32.768 kHz.

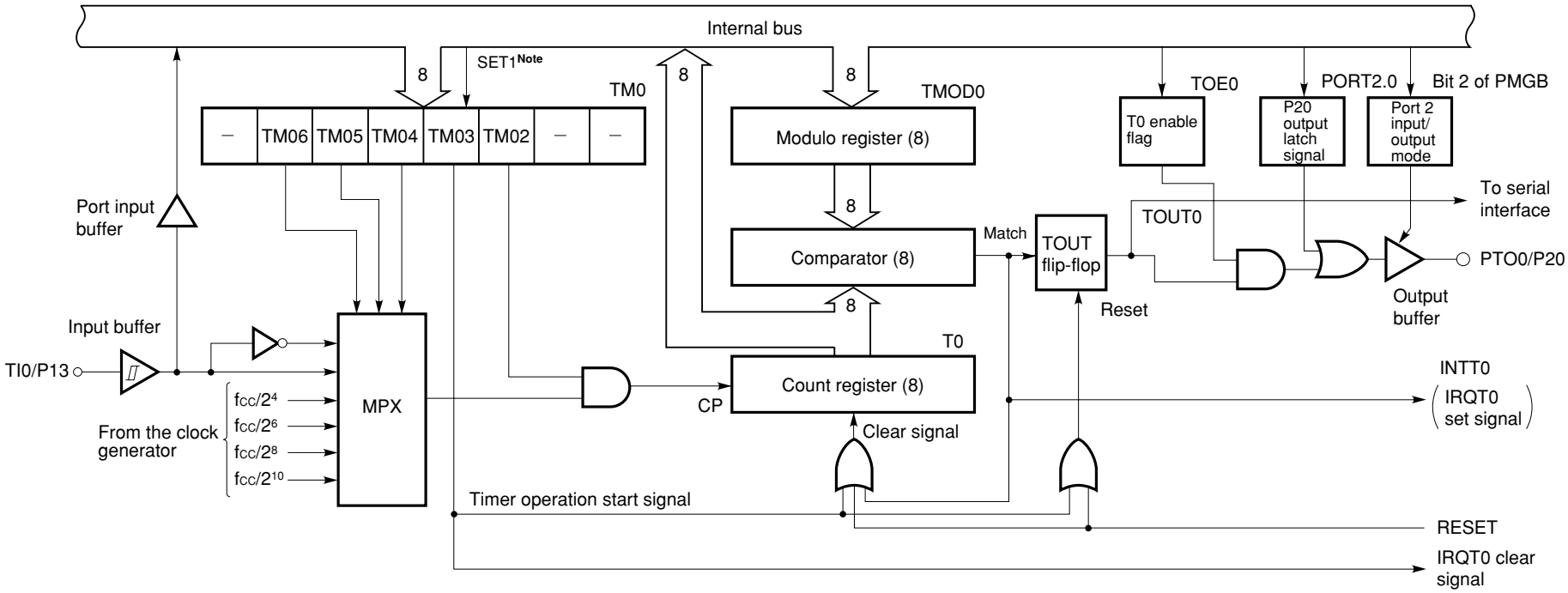
6.7 Timer/Event Counter

The μPD750108 contains one channel for a timer/event counter and one channel for a timer counter. Figures 6-6 and 6-7 show their configurations.

The timer/event counter provides the following functions:

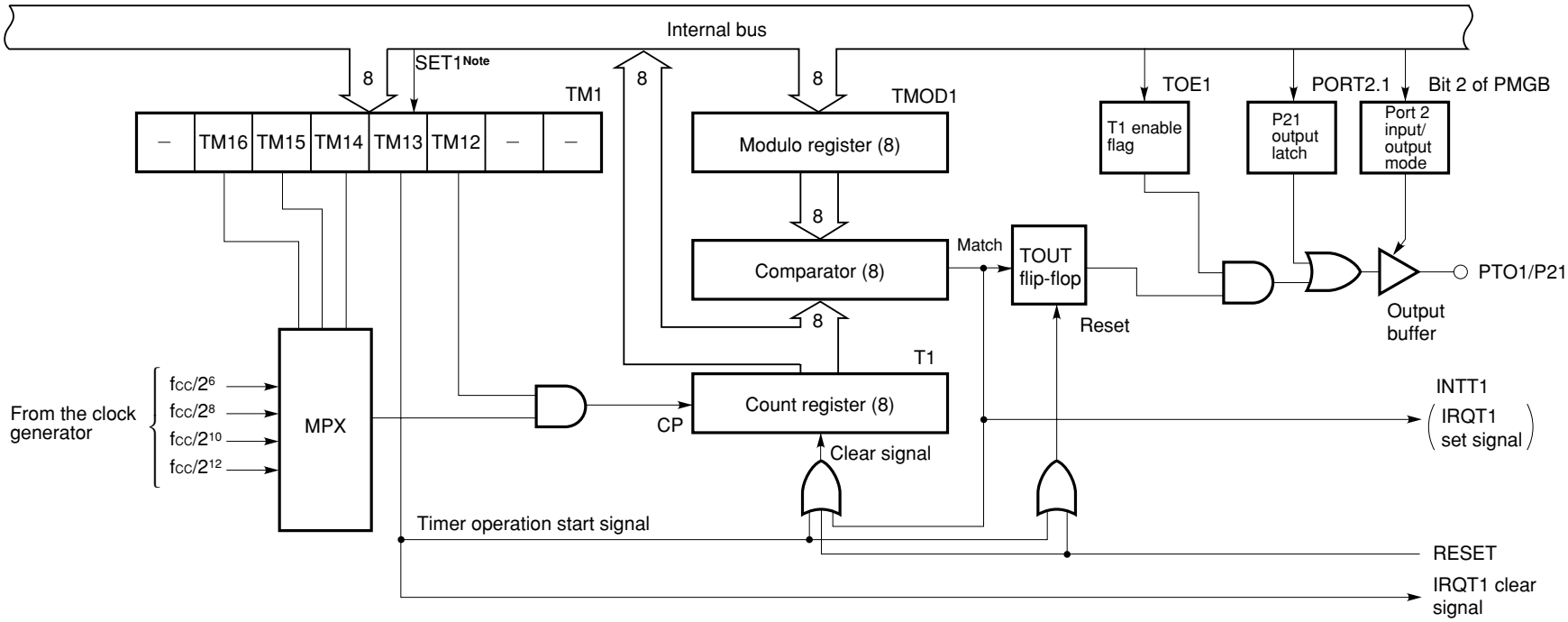
- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTOn pin (n = 0, 1)
- Event counter operation (channel 0 only)
- Divides the TI0 pin input by N and outputs to the PTO0 pin (frequency divider operation) (channel 0 only)
- Supplies serial shift clock to the serial interface circuit (channel 0 only)
- Count read function

Figure 6-6. Timer/Event Counter Block Diagram



Note Instruction execution

Figure 6-7. Timer Counter Block Diagram



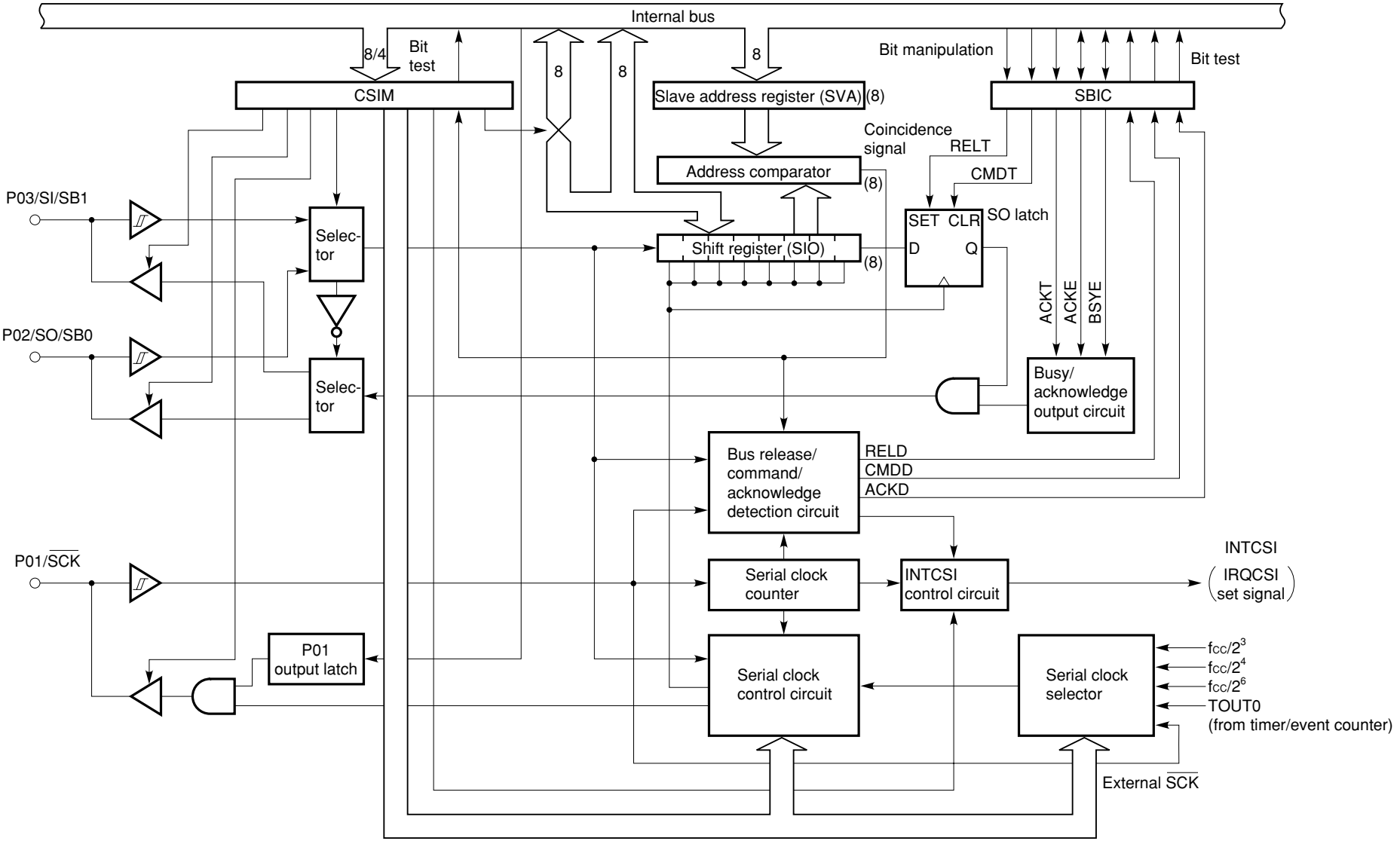
Note Instruction execution

6.8 Serial Interface

μPD750108 has an 8-bit synchronous serial interface. The serial interface has the following four types of mode.

- Operation stop mode
- Three-wire serial I/O mode
- Two-wire serial I/O mode
- SBI mode

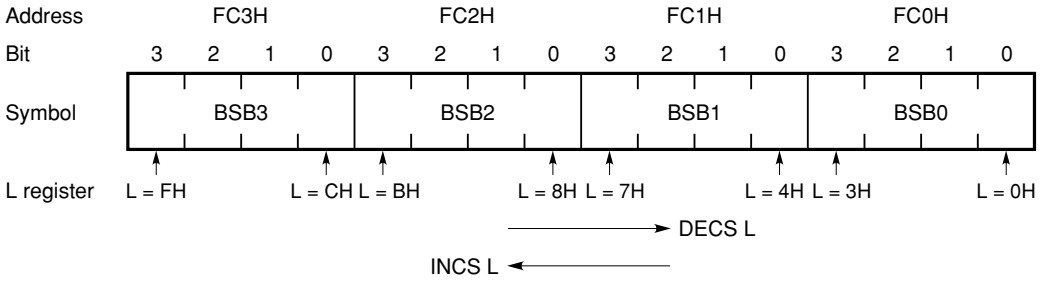
Figure 6-8. Serial Interface Block Diagram



6.9 Bit Sequential Buffer: 16 Bits

The bit sequential buffer (BSB) is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially updated by bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.

Figure 6-9. Bit Sequential Buffer Format



Remarks 1. In pmem.@L addressing, bit specification is shifted according to the L register.

2. In pmem.@L addressing, the bit sequential buffer can be manipulated at any time regardless of MBE/MBS specification.

7. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

The μPD750108 has seven interrupt sources and two test sources. One test source, INT2, has two types of edge detection testable input pins.

The interrupt control circuit of the μPD750108 has the following functions.

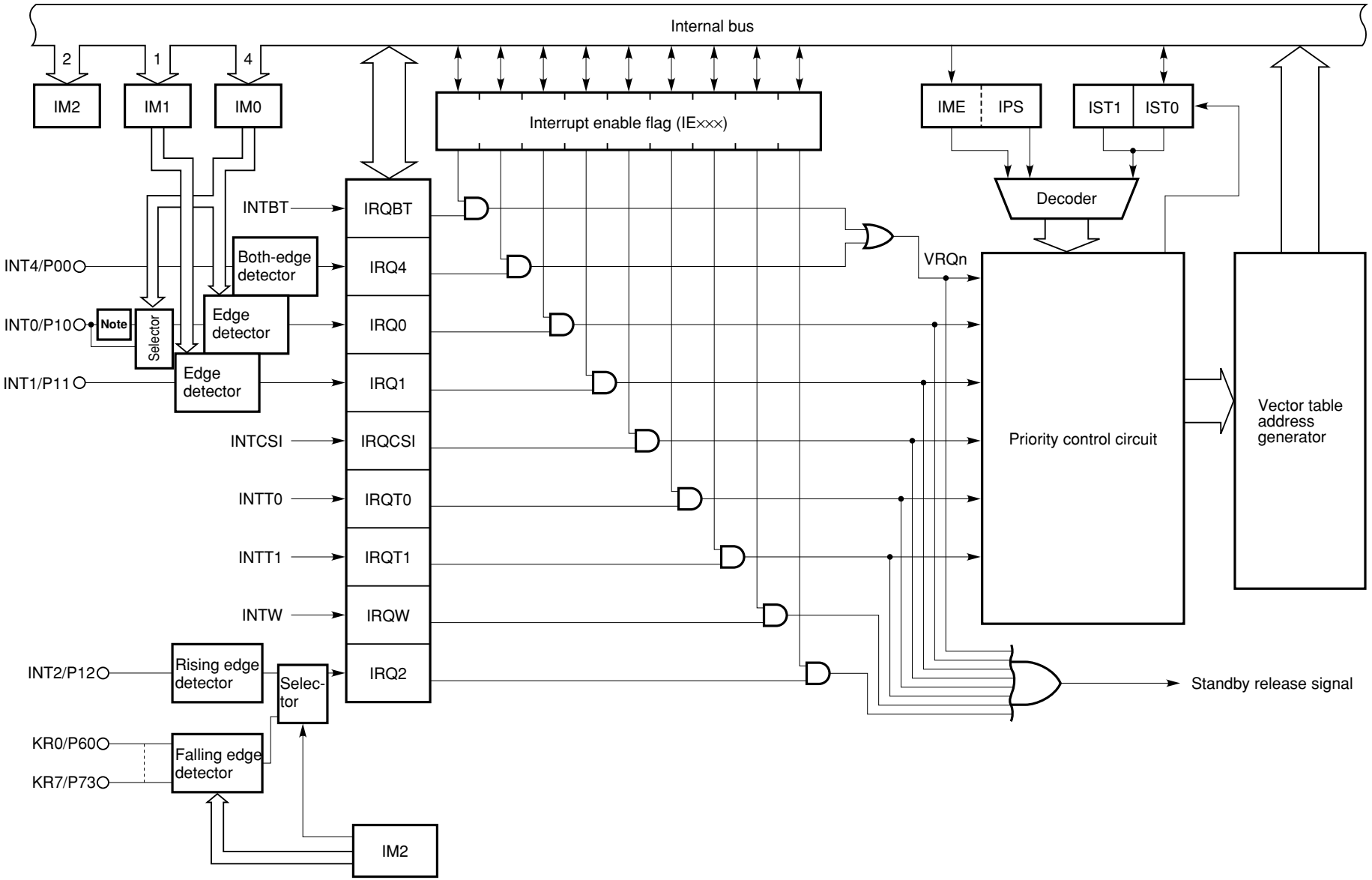
(1) Interrupt functions

- Hardware controlled vectored interrupt function which can control whether or not to accept an interrupt using the interrupt flag (IE×××) and interrupt master enable flag (IME).
- The interrupt start address can be set arbitrarily.
- Multiple interrupt function which can specify the priority by the interrupt priority specification register (IPS)
- Test function of an interrupt request flag (IRQ×××)
  (The software can confirm that an interrupt occurred.)
- Release of the standby mode (Interrupts released by an interrupt enable flag can be selected.)

(2) Test functions

- Whether test request flags (IRQ×××) are issued can be checked with software.
- Release of the standby mode (A test source to be released can be selected with test enable flags.)

Figure 7-1. Interrupt Control Circuit Block Diagram



Note Noise eliminator (Standby release is not possible when the noise eliminator is selected.)

8. STANDBY FUNCTION

The μPD750108 has two different standby modes (STOP mode and HALT mode) to reduce power dissipation while waiting for program execution.

Table 8-1. Standby Mode Statuses

Item \ Mode		STOP mode	HALT mode
Instruction for setting		STOP instruction	HALT instruction
System clock for setting		Can be set only when operating on the main system clock.	Can be set either with the main system clock or the subsystem clock.
Operation status	Clock oscillator	The main system clock stops its operation.	Only the CPU clock Φ stops its operation (oscillation continues).
	Basic interval timer/watchdog timer	Does not operate.	Can operate only at main system clock oscillation. BT mode : IRQBT is set at the reference interval. WT mode : A reset signal is generated when the BT overflows.
	Serial interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock.	Can operate only when external $\overline{SCK}$ input is selected as the serial clock or at main system clock oscillation.
	Timer/event counter	Can operate only when the TI0 pin input is selected for the count clock.	Can operate only when TI0 pin input is specified as the count clock or at main system clock oscillation.
	Timer counter	Does not operate.	Can operate.**Note 1**
	Clock timer	Can operate when f_{XT} is selected as the count clock.	Can operate.
	External interrupt	INT1, INT2, and INT4 can operate. Only INT0 cannot operate.**Note 2**	
	CPU	Does not operate.	
Release signal		An interrupt request signal from hardware whose operation is enabled by the interrupt enable flag or the generation of a $\overline{RESET}$ signal	

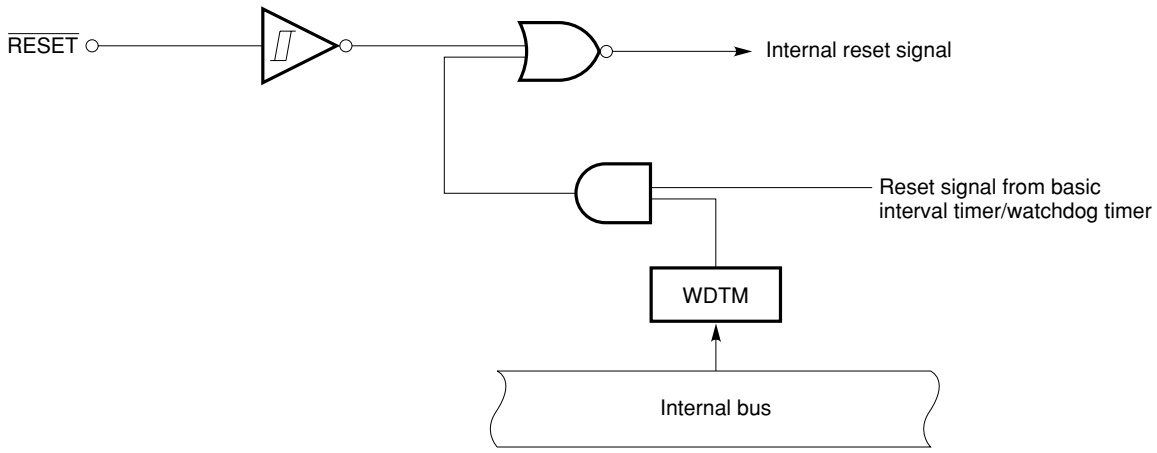
Notes 1. Operation is possible only when the main system clock operates.

2. Operation is possible only when the noise eliminator is not selected by bit 2 of the edge detection mode register (IM0) (when IM02 = 1).

9. RESET FUNCTION

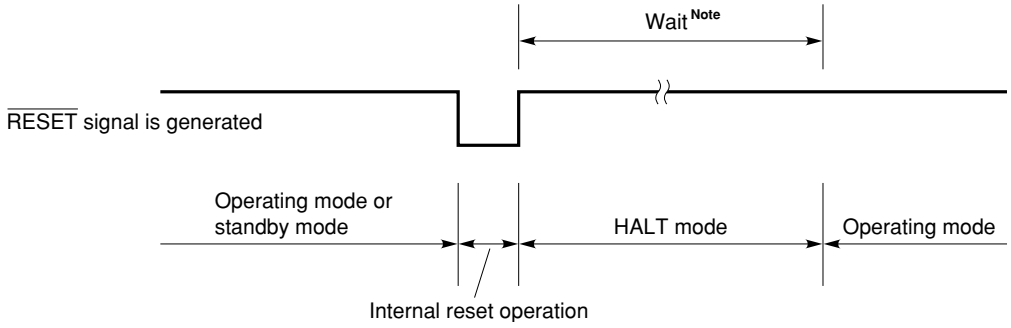
The μPD750108 is reset with the external reset signal ($\overline{\text{RESET}}$) or the reset signal received from the basic interval timer/watchdog timer. When either reset signal is input, the internal reset signal is generated. Figure 9-1 shows the configuration of the reset circuit.

Figure 9-1. Configuration of Reset Functions



When the $\overline{\text{RESET}}$ signal is generated, all hardware is initialized as indicated in Table 9-1. Figure 9-2 shows the reset operation timing.

Figure 9-2. Reset Operation by Generation of $\overline{\text{RESET}}$ Signal



Note 56/fcc (28 μs at 2.0 MHz, 56 μs at 1.0 MHz)

Table 9-1. Status of the Hardware after a Reset (1/2)

Hardware			Generation of a $\overline{\text{RESET}}$ signal in a standby mode	Generation of a $\overline{\text{RESET}}$ signal during operation
Program counter (PC)		μPD750104	4 low-order bits at address 0000H in program memory are set in PC bits 11 to 8, and the data at address 0001H are set in PC bits 7 to 0.	4 low-order bits at address 0000H in program memory are set in PC bits 11 to 8, and the data at address 0001H are set in PC bits 7 to 0.
		μPD750106, 750108	5 low-order bits at address 0000H in program memory are set in PC bits 12 to 8, and the data at address 0001H are set in PC bits 7 to 0.	5 low-order bits at address 0000H in program memory are set in PC bits 12 to 8, and the data at address 0001H are set in PC bits 7 to 0.
PSW	Carry flag (CY)		Held	Undefined
	Skip flags (SK0 to SK2)		0	0
	Interrupt status flags (IST0, IST1)		0	0
	Bank enable flags (MBE, RBE)		Bit 6 at address 0000H in program memory is set in RBE, and bit 7 is set in MBE.	Bit 6 at address 0000H in program memory is set in RBE, and bit 7 is set in MBE.
Stack pointer (SP)			Undefined	Undefined
Stack bank selection register (SBS)			1000B	1000B
Data memory (RAM)			Held	Undefined
General-purpose registers (X, A, H, L, D, E, B, C)			Held	Undefined
Bank selection register (MBS, RBS)			0, 0	0, 0
Basic interval timer/watchdog timer	Counter (BT)		Undefined	Undefined
	Mode register (BTM)		0	0
	Watchdog timer enable flag (WDTM)		0	0
Timer/event counter	Counter (T0)		0	0
	Modulo register (TMOD0)		FFH	FFH
	Mode register (TM0)		0	0
	TOE0, TOUT flip-flop		0, 0	0, 0
Timer counter	Counter (T1)		0	0
	Modulo register (TMOD1)		FFH	FFH
	Mode register (TM1)		0	0
	TOE1, TOUT flip-flop		0, 0	0, 0
Clock timer	Mode register (WM)		0	0
Serial interface	Shift register (SIO)		Held	Undefined
	Operation mode register (CSIM)		0	0
	SBI control register (SBIC)		0	0
	Slave address register (SVA)		Held	Undefined

Table 9-1. Status of the Hardware after a Reset (2/2)

Hardware		Generation of a $\overline{\text{RESET}}$ signal in a standby mode	Generation of a $\overline{\text{RESET}}$ signal during operation
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Sub-oscillator control register (SOS)		0	0
Interrupt	Interrupt request flag (IRQ×××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE×××)	0	0
	Priority selection register (IPS)	0	0
	INT0, INT1, and INT2 mode registers (IM0, IM1, IM2)	0, 0, 0	0, 0, 0
Digital ports	Output buffer	Off	Off
	Output latch	Clear (0)	Clear (0)
	I/O mode registers (PMGA, PMGB, PMGC)	0	0
	Pull-up resistor specification registers (POGA, POGB)	0	0
Bit sequential buffers (BSB0 to BSB3)		Held	Undefined

10. MASK OPTION

The μPD750108 has the following mask options:

- Mask option of P40 to P43 and P50 to P53
  Can specify whether to incorporate the pull-up resistor.
  ① The pull-up resistor is incorporated bit by bit.
  ② The pull-up resistor is not incorporated.

- Mask option of standby function
  Can specify the wait time when STOP mode was released by an interrupt.
  ① $2^9/f_{CC}$ (256 μs at 2.0 MHz, 512 μs at 1.0 MHz)
  ② No wait

- Mask option of subsystem clock
  Can specify whether to enable the built-in feedback resistor.
  ① The built-in feedback resistor is enabled (it is turned on or off by software).
  ② The built-in feedback resistor is disabled (it is cut by hardware).

11. INSTRUCTION SET

(1) Operand identifier and its descriptive method

The operands are described in the operand column of each instruction according to the descriptive method for the operand format of the appropriate instructions. (For details, refer to the **RA75X Assembler Package User's Manual: Language** (EEU-1363).) For descriptions in which alternatives exist, one element should be selected. Capital letters and plus and minus signs are keywords; therefore, they should be described as they are.

For immediate data, the appropriate numerical values or labels should be described.

The symbols of register flags can be used as a label instead of mem, fmem, pmem, and bit. (For details, refer to the **μPD750108 User's Manual** (U11330E).) However, there are some restrictions on usable labels for fmem and pmem.

Representation format	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL-, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label**Note** 2-bit immediate data or label
fmem pmem	FB0H - FBFH, FF0H - FFFH immediate data or label FC0H - FFFH immediate data or label
addr	0000H - 0FFFH immediate data or label (μPD750104) 0000H - 17FFH immediate data or label (μPD750106) 0000H - 1FFFH immediate data or label (μPD750108)
addr1(for Mk II mode only)	0000H - 0FFFH immediate data or label (μPD750104) 0000H - 17FFH immediate data or label (μPD750106) 0000H - 1FFFH immediate data or label (μPD750108)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H - 7FH immediate data (however, bit 0 = 0) or label
PORTn IE××× RBn MBn	PORT0 - PORT8 IEBT, IET0, IET1, IE0 - IE2, IE4, IECSI, IEW RB0 - RB3 MB0, MB1, MB15

Note Only even address can be specified for 8-bit data processing.

(2) Symbol definitions in operation description

A	:	A register; 4-bit accumulator
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
X	:	X register
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA'	:	Extended register pair (XA')
BC'	:	Extended register pair (BC')
DE'	:	Extended register pair (DE')
HL'	:	Extended register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; Bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 8)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority specification register
IE×××	:	Interrupt enable flag
RBS	:	Register bank selection register
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
.	:	Address bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Symbols used for the addressing area column

* 1	MB = MBE • MBS (MBS = 0, 1, 15)	Data memory addressing
* 2	MB = 0	
* 3	MBE = 0 : MB = 0 (000H - 07FH), MB = 15 (F80H - FFFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
* 4	MB = 15, fmem = FB0H - FBFH, FF0H - FFFH	
* 5	MB = 15, pmem = FC0H - FFFH	
* 6	addr = 0000H - 0FFFH (μPD750104), 0000H - 17FFH (μPD750106) 0000H - 1FFFH (μPD750108)	Program memory addressing
* 7	addr, addr1 = (Current PC) - 15 to (Current PC) - 1 (Current PC) + 2 to (Current PC) + 16	
* 8	caddr = 0000H - 0FFFH (μPD750104) 0000H - 0FFFH (PC_{12} = 0: μPD750106, 750108) 1000H - 17FFH (PC_{12} = 1: μPD750106) 1000H - 1FFFH (PC_{12} = 1: μPD750108)	
* 9	faddr = 0000H - 07FFH	
* 10	taddr = 0020H - 007FH	
* 11	Mk II mode only addr1 = 0000H - 0FFFH (μPD750104) 0000H - 17FFH (μPD750106) 0000H - 1FFFH (μPD750108)	

Remarks 1. MB indicates the memory bank that can be accessed.

2. For *2, MB = 0 regardless of MBE and MBS settings.

3. For *4 and *5, MB = 15 regardless of MBE and MBS settings.

4. For *6 to *11, each addressable area is indicated.

(4) Description of machine cycle column

S indicates the number of machine cycles necessary for skipping any skip instruction. The value of S changes as follows:

- When no skip is performed : S = 0
- When a 1-byte or 2-byte instruction is skipped : S = 1
- When a 3-byte instruction**Note** is skipped : S = 2

Note 3-byte instruction: BR !addr, BRA !addr1, CALL !addr, and CALLA !addr1 instructions.

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle (= t_{CY}) of the CPU clock (Φ), and four types of times are available for selection according to the PCC setting.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String A
		HL, #n8	2	2	HL ← n8		String B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL-	1	2 + S	A ← (HL), then L ← L - 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A, @HL-	1	2 + S	A ↔ (HL), then L ← L - 1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table reference	MOVT	XA, @PCDE	1	3	• **μPD750104** XA ← $(PC_{11-8} + DE)_{ROM}$		
					• **μPD750106, 750108** XA ← $(PC_{12-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	• **μPD750104** XA ← $(PC_{11-8} + XA)_{ROM}$		
					• **μPD750106, 750108** XA ← $(PC_{12-8} + XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ **Note**	*6	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ **Note**	*6	

Note Set register B to 0 in the μPD750104. Only the LSB is valid in register B in the μPD750106 and μPD750108.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← (H + mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit, CY	2	2	(H + mem_{3-0}.bit) ← CY	*1	
Arithmetic	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp'	2	2 + S	XA ← XA + rp'		carry
		rp'1, XA	2	2 + S	rp'1 ← rp'1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp'	2	2	XA, CY ← XA + rp' + CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A - (HL)	*1	borrow
		XA, rp'	2	2 + S	XA ← XA - rp'		borrow
		rp'1, XA	2	2 + S	rp'1 ← rp'1 - XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A - (HL) - CY	*1	
		XA, rp'	2	2	XA, CY ← XA - rp' - CY		
		rp'1, XA	2	2	rp'1, CY ← rp'1 - XA - CY		
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∧ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∨ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	
		XA, rp'	2	2	XA ← XA ∀ rp'		
		rp'1, XA	2	2	rp'1 ← rp'1 ∀ XA		
Accumulator manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg - 1		reg = FH
		rp'	2	2 + S	rp' ← rp' - 1		rp' = FFH

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H+mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 0	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H + mem$_{3-0}$.bit) = 1 and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∧ (H + mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∨ (H + mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ (pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∀ (H + mem$_{3-0}$.bit)	*1	

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Branch	BR**Note**	addr	-	-	• **μPD750104** PC_{11-0} ← addr [The assembler selects the most adequate instruction from BR !addr, BRCB !caddr, or BR $addr.]	*6	
					• **μPD750106, 750108** PC_{12-0} ← addr [The assembler selects the most adequate instruction from BR !addr, BRCB !caddr, or BR $addr.]		
		addr1	-	-	• **μPD750104** PC_{11-0} ← addr1 [The assembler selects the most adequate instruction from instructions below. • BR !addr • BRA !addr1 • BRCB !caddr • BR $addr1]	*11	
					• **μPD750106, 750108** PC_{12-0} ← addr1 [The assembler selects the most adequate instruction from instructions below. • BR !addr • BRA !addr1 • BRCB !caddr • BR $addr1]		
		!addr	3	3	• **μPD750104** PC_{11-0} ← addr	*6	
					• **μPD750106, 750108** PC_{12-0} ← addr		
		$addr	1	2	• **μPD750104** PC_{11-0} ← addr	*7	
					• **μPD750106, 750108** PC_{12-0} ← addr		
		$addr1	1	2	• **μPD750104** PC_{11-0} ← addr1		
					• **μPD750106, 750108** PC_{12-0} ← addr1		

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Branch	BR	PCDE	2	3	• **μPD750104** $PC_{11-0} \leftarrow PC_{11-8} + DE$ • **μPD750106, 750108** $PC_{12-0} \leftarrow PC_{12-8} + DE$		
		PCXA	2	3	• **μPD750104** $PC_{11-0} \leftarrow PC_{11-8} + XA$ • **μPD750106, 750108** $PC_{12-0} \leftarrow PC_{12-8} + XA$		
		BCDE	2	3	• **μPD750104** $PC_{11-0} \leftarrow$ BCDE**Note 1** • **μPD750106, 750108** $PC_{12-0} \leftarrow$ BCDE**Note 2**	*6	
		BCXA	2	3	• **μPD750104** $PC_{11-0} \leftarrow$ BCXA**Note 1** • **μPD750106, 750108** $PC_{12-0} \leftarrow$ BCXA**Note 2**	*6	
	BRA**Note 3**	!addr1	3	3	• **μPD750104** $PC_{11-0} \leftarrow$ addr1 • **μPD750106, 750108** $PC_{12-0} \leftarrow$ addr1	*11	
	BRCB	!caddr	2	2	• **μPD750104** $PC_{11-0} \leftarrow caddr_{11-0}$ • **μPD750106, 750108** $PC_{12-0} \leftarrow PC_{12} + caddr_{11-0}$	*8	
Subroutine stack control	CALLA**Note 3**	!addr1	3	3	• **μPD750104** (SP - 2) ← ×, ×, MBE, RBE (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, 0 $PC_{11-0} \leftarrow$ addr1, SP ← SP - 6 • **μPD750106, 750108** (SP - 2) ← ×, ×, MBE, RBE (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, PC_{12} $PC_{12-0} \leftarrow$ addr1, SP ← SP - 6	*11	

Notes 1. Set register B to 0.

2. Only the LSB is valid in register B.

3. The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALL[Note]	!addr	3	3	• **μPD750104** (SP - 3) ← MBE, RBE, 0, 0 (SP - 4) (SP - 1) (SP - 2) ← PC_{11-0} PC_{11-0} ← addr, SP ← SP - 4	*6	
					• **μPD750106, 750108** (SP - 3) ← MBE, RBE, 0, PC_{12} (SP - 4) (SP - 1) (SP - 2) ← PC_{11-0} PC_{12-0} ← addr, SP ← SP - 4		
				4	• **μPD750104** (SP - 2) ← ×, ×, MBE, RBE (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, 0 PC_{11-0} ← addr, SP ← SP - 6		
					• **μPD750106, 750108** (SP - 2) ← ×, ×, MBE, RBE (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, PC_{12} PC_{12-0} ← addr, SP ← SP - 6		
	CALLF[Note]	!faddr	2	2	• **μPD750104** (SP - 3) ← MBE, RBE, 0, 0 (SP - 4) (SP - 1) (SP - 2) ← PC_{11-0} PC_{11-0} ← 0 + faddr, SP ← SP - 4	*9	
					• **μPD750106, 750108** (SP - 3) ← MBE, RBE, 0, PC_{12} (SP - 4) (SP - 1) (SP - 2) ← PC_{11-0} PC_{12-0} ← 00 + faddr, SP ← SP - 4		
				3	• **μPD750104** (SP - 2) ← ×, ×, MBE, RBE (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, 0 PC_{11-0} ← 0 + faddr, SP ← SP - 6		
					• **μPD750106, 750108** (SP - 2) ← ×, ×, MBE, RBE (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, PC_{12} PC_{12-0} ← 00 + faddr, SP ← SP - 6		

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Subroutine stack control	RET[Note]		1	3	• **μPD750104** $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ MBE, RBE, 0, 0 ← (SP + 1), SP ← SP + 4		
					• **μPD750106, 750108** $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ MBE, RBE, 0, $PC_{12} \leftarrow (SP+1)$ SP ← SP + 4		
				3	• **μPD750104** ×, ×, MBE, RBE ← (SP + 4) 0, 0, 0, 0 ← (SP + 1) $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ SP ← SP + 6		
					• **μPD750106, 750108** ×, ×, MBE, RBE ← (SP + 4) MBE, 0, 0, $PC_{12} \leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ SP ← SP + 6		
	RETS[Note]		1	3 + S	• **μPD750104** MBE, RBE, 0, 0 ← (SP + 1) $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ SP ← SP + 4 then skip unconditionally		Uncondition
					• **μPD750106, 750108** MBE, RBE, 0 ← $PC_{12} \leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ SP ← SP + 4 then skip unconditionally		
				3 + S	• **μPD750104** 0, 0, 0, 0 ← (SP + 1) $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ ×, ×, MBE, RBE ← (SP + 4) SP ← SP + 6 then skip unconditionally		
					• **μPD750106, 750108** 0, 0, 0, $PC_{12} \leftarrow (SP+1)$ $PC_{11-0} \leftarrow (SP)\ (SP+3)\ (SP+2)$ ×, ×, MBE, RBE ← (SP + 4) SP ← SP + 4 then skip unconditionally		

Note The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Subroutine stack control	RETI Note 1		1	3	• **μPD750104** MBE, RBE, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
					• **μPD750106, 750108** MBE, RBE, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
					• **μPD750104** 0, 0, 0, 0 ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
					• **μPD750106, 750108** 0, 0, 0, PC_{12} ← (SP + 1) PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP - 1)(SP - 2) ← rp, SP ← SP - 2		
		BS	2	2	(SP - 1) ← MBS, (SP - 2) ← RBS, SP ← SP - 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME (IPS.3) ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IExxx	2	2	IExxx ← 0		
Input/output	IN Note 2	A, PORTn	2	2	A ← PORTn (n = 0 - 8)		
		XA, PORTn	2	2	XA ← PORTn+1,PORTn (n = 4, 6)		
	OUT Note 2	PORTn, A	2	2	PORTn ← A (n = 2 - 8)		
		PORTn, XA	2	2	PORTn+1,PORTn ← XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		

Notes 1. The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

2. When executing the IN/OUT instruction, MBE must be set to 0 or MBE and MBS must be set to 1 and 15, respectively.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Special	SEL	RBn	2	2	RBS ← n (n = 0 - 3)		
		MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI[Notes 1, 2]	taddr	1	3	• **μPD750104** When the TBR instruction is used $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr + 1)$	*10	
					When the TCALL instruction is used (SP - 4) (SP - 1) (SP - 2) ← PC_{11-0} (SP - 3) ← MBE, RBE, 0, 0 $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr + 1)$ SP ← SP - 4		
					When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.
					• **μPD750106, 750108** When the TBR instruction is used $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$		
					When the TCALL instruction is used (SP - 4) (SP - 1) (SP - 2) ← PC_{11-0} (SP - 3) ← MBE, RBE, 0, PC12 $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ SP ← SP - 4		
					When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.
				3	• **μPD750104** When the TBR instruction is used $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr + 1)$	*10	
				4	When the TCALL instruction is used (SP - 6) (SP - 3) (SP - 4) ← PC_{11-0} (SP - 5) ← 0, 0, 0, 0 (SP - 2) ← ×, ×, MBE, RBE $PC_{11-0} \leftarrow (taddr)_{3-0} + (taddr + 1)$ SP ← SP - 6		
				3	When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.

Notes 1. The shaded portion is supported in Mk II mode only. The other portions are supported in Mk I mode only.

2. TBR and TCALL instructions are assembler pseudo instructions to define tables used for GETI instructions.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Special	GETI[Notes 1, 2]	taddr	1	3	• **μPD750106, 750108** When the TBR instruction is used $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$	*10	
				4	When the TCALL instruction is used (SP - 6) (SP - 3) (SP - 4) $\leftarrow PC_{11-0}$ (SP - 5) $\leftarrow$ 0, 0, 0, PC_{12} (SP - 2) $\leftarrow \times, \times$, MBE, RBE $PC_{12-0} \leftarrow (taddr)_{4-0} + (taddr + 1)$ SP $\leftarrow$ SP - 6		
				3	When an instruction other than the TBR and TCALL instructions is used Execution of (taddr)(taddr + 1) instruction		Depends on the referenced instruction.

Notes 1. The shaded portion is supported in Mk II mode only.

2. TBR and TCALL instructions are assembler pseudo instructions to define tables used for GETI instructions.

12. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

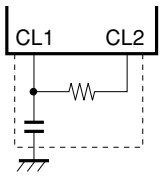
Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			-0.3 to +7.0	V
Input voltage	V_{I1}	Other than ports 4 and 5		-0.3 to V_{DD} + 0.3	V
	V_{I2}	Ports	With a built-in pull-up resistor	-0.3 to V_{DD} + 0.3	V
		4 and 5	With N-ch open drain	-0.3 to +14.0	V
Output voltage	V_O			-0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	Each pin		-10	mA
		Total of all pins		-30	mA
Low-level output current	I_{OL}	Each pin		30	mA
		Total of all pins		220	mA
Operating ambient temperature	T_A			-40 to +85	°C
Storage temperature	T_{stg}			-65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATOR (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

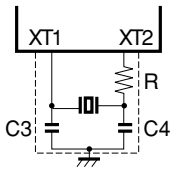
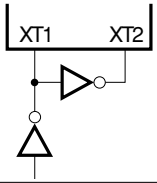
Resonator	Recommended constant	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillator		Oscillator frequency (f_{CC})[Note]		0.4		2.0	MHz

Note The oscillator frequency indicates only the oscillator characteristics. See AC characteristics for the instruction execution time and oscillator frequency characteristics.

Caution When the main system clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{SS}.**
- **It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

CHARACTERISTICS OF THE SUBSYSTEM CLOCK OSCILLATOR (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constant	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillator frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation settling time**Note 2**	V_{DD} = 4.5 to 5.5 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})**Note 1**		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} is applied.

Caution When the subsystem clock oscillator is used, conform to the following guidelines when wiring at the portions of surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of Vss**
- **It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

When the subsystem clock is used, pay special attention to its wiring; the subsystem clock oscillator has low amplification to minimize current consumption and is more likely to malfunction due to noise than the main system clock oscillator.

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Low-level output current	I_{OL}	Each pin					15	mA
		Total of all pins					150	mA
High-level input voltage	V_{IH1}	Ports 2, 3, and 8		2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, and 7 and $\overline{\text{RESET}}$		2.7 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	With a Built-in pull-up resistor	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
			With N-ch open drain	2.7 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		13	V
				1.8 V ≤ V_{DD} < 2.7 V	0.9V_{DD}		13	V
	V_{IH4}	XT1			V_{DD} - 0.1		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2 to 5, and 8		2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, and 7 and $\overline{\text{RESET}}$		2.7 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
				1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL3}	XT1			0		0.1	V
High-level output voltage	V_{OH}	$\overline{\text{SCK}}$, SO, and ports 2, 3, and 6 to 8 I_{OH} = -1.0 mA			V_{DD} - 0.5			V
Low-level output voltage	V_{OL1}	$\overline{\text{SCK}}$, SO, and ports 2 to 8	I_{OL} = 15 mA, V_{DD} = 5.0 V ± 10%			0.2	2.0	V
			I_{OL} = 1.6 mA				0.4	V
	V_{OL2}	SB0, SB1	N-ch open drain Pull-up resistor ≥ 1 kΩ				0.2V_{DD}	V
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Other than XT1				3	μA
	I_{LIH2}		XT1				20	μA
	I_{LIH3}	V_{IN} = 13 V	Ports 4 and 5 (With N-ch open drain)				20	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Other than XT1 and ports 4 and 5				-3	μA
	I_{LIL2}		XT1				-20	μA
	I_{LIL3}		Ports 4 and 5 (With N-ch open drain) At other than input instruction execution				-3	μA
			Ports 4 and 5 (With N-ch open drain) When the input instruction is executed				-30	μA
				V_{DD} = 5.0 V		-10	-27	μA
				V_{DD} = 3.0 V		-3	-8	μA
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{\text{SCK}}$, SO/SB0, SB1, and ports 2, 3, and 6 to 8 Ports 4 and 5 (With a built-in pull-up resistor)				3	μA
	I_{LOH2}	V_{OUT} = 13 V	Ports 4 and 5 (With N-ch open drain)				20	μA
Low-level output leakage current	I_{LOL}	V_{OUT} = 0 V					-3	μA
Built-in pull-up resistor	R_{L1}	V_{IN} = 0 V	Ports 0 to 3 and 6 to 8 (except P00 pin)		50	100	200	kΩ
	R_{L2}		Ports 4 and 5 (mask option)		15	30	60	kΩ

DC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	1.0 MHz[Note 2] RC oscillation R = 22 kΩ, C = 22 pF	V_{DD} = 5.0 V ± 10%[Note 3]			0.65	1.6	mA
			V_{DD} = 3.0 V ± 10%[Note 4]			180	360	μA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		370	920	μA
				V_{DD} = 3.0 V ± 10%		170	340	μA
	I_{DD3}	32.768 kHz[Note 5] crystal oscillation	Low-voltage mode[Note 6]	V_{DD} = 3.0 V ± 10%		11.0	40.0	μA
				V_{DD} = 2.0 V ± 10%		5.5	18.0	μA
				V_{DD} = 3.0 V, T_A = 25 °C		11.0	18.0	μA
			Low-current-drain mode[Note 7]	V_{DD} = 3.0 V ± 10%		8.0	24.0	μA
				V_{DD} = 3.0 V, T_A = 25 °C		8.0	14.0	μA
	I_{DD4}		HALT mode	Low-voltage mode[Note 6] V_{DD} = 3.0 V ± 10%		5.0	30.0	μA
				Low-voltage mode[Note 6] V_{DD} = 3.0 V, T_A = -40 to +50 °C		5.0	12.0	μA
				Low-voltage mode[Note 6] V_{DD} = 2.0 V ± 10%		2.5	10.0	μA
				Low-voltage mode[Note 6] V_{DD} = 3.0 V, T_A = 25 °C		5.0	10.0	μA
				Low-current-drain mode[Note 7] V_{DD} = 3.0 V ± 10%		4.0	15.0	μA
				Low-current-drain mode[Note 7] V_{DD} = 3.0 V, T_A = -40 to +50 °C		4.0	8.0	μA
				Low-current-drain mode[Note 7] V_{DD} = 3.0 V, T_A = 25 °C		4.0	7.0	μA
	I_{DD5}	XT1 = 0 V[Note 8] STOP mode	V_{DD} = 5.0 V ± 10%			0.05	5.0	μA
			V_{DD} = 3.0 V ± 10%			0.02	2.5	μA
				T_A = 25 °C		0.02	0.2	μA

Notes 1. This current excludes the current which flows through the built-in pull-up resistors.

2. This value applies also when the subsystem clock oscillates.

3. Value when the processor clock control register (PCC) is set to 0011 and the μPD750108 is operated in the high-speed mode.

4. Value when the PCC is set to 0000 and the μPD750108 is operated in the low-speed mode.

5. This value applies when the system clock control register (SCC) is set to 1001 to stop the main system clock pulse and to start the subsystem clock pulse.

6. Mode when the sub-oscillator control register (SOS) is set to 0000.

7. Mode when the SOS is set to 0010.

8. This value applies when the SOS is set to 00×1 and the sub-oscillator feedback resistor is not used (× = don't care).

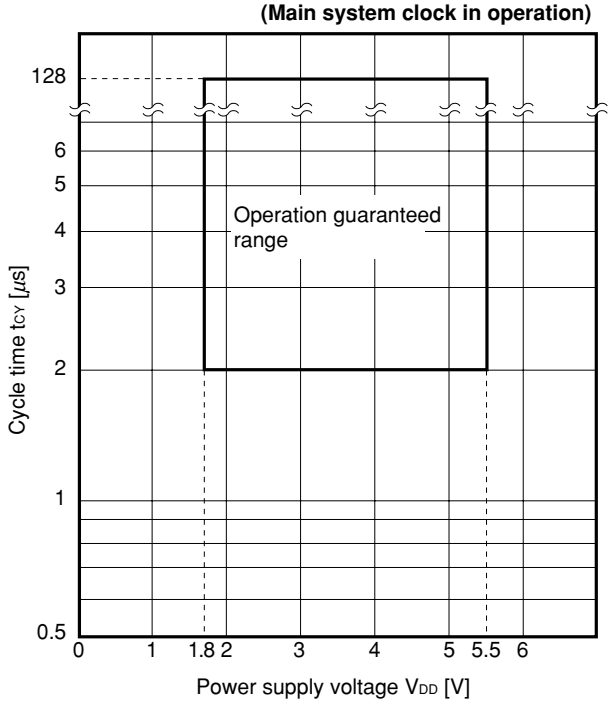
AC CHARACTERISTICS (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time[Note 1] (minimum instruction execution time = 1 machine cycle)	t_{CY}	Operated by main system clock pulse		2.0		128	μs
		Operated by subsystem clock pulse		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1	MHz
				0		275	kHz
TI0 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	Note 2			μs
			IM02 = 1	10			μs
		INT1, INT2, and INT4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs
RC oscillator frequency	f_{CC}	R = 22 kΩ,	V_{DD} = 2.7 to 5.5 V	0.90	1.00	1.30	MHz
		C = 22 pF	V_{DD} = 2.7 to 5.5 V	0.55	1.00	1.30	MHz

Notes 1. When the main system clock is used, the cycle time of the CPU clock (Φ) (minimum instruction execution time) depends on the time constants of connected resistors (R) and capacitors (C) and the processor clock control register (PCC).
When the subsystem clock is used, the cycle time of the CPU clock (Φ) (minimum instruction execution time) depends on the frequency of the connected resonator (and external clock), the system clock control register (SCC), and the processor clock control register (PCC).
The figure on the right side shows the cycle time t_{CY} characteristics for the supply voltage V_{DD} during main system clock operation.

2. This value becomes $2t_{CY}$ or $128/f_{CC}$ according to the setting of the interrupt mode register (IM0).

t_{CY} vs. V_{DD}
(Main system clock in operation)



SERIAL TRANSFER OPERATION

Two-wire and three-wire serial I/O modes ($\overline{SCK}$: Internal clock output): (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1,300			ns
				3,800			ns
$\overline{SCK}$ high/low level width	t_{KL1}, t_{KH1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2 - 50			ns
				t_{KCY1}/2 - 150			ns
SI[Note 1] setup time (referred to $\overline{SCK}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI[Note 1] hold time (referred to $\overline{SCK}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCK}$↓ to SO[Note 1] output	t_{KSO1}	R_L = 1 kΩ[Note 2], C_L = 100 pF	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1,000	ns

Notes 1. In two-wire serial I/O mode, SO should be read as SB0 or SB1.

2. R_L is the resistance of the SO output line load, while C_L is the capacitance.

Two-wire and three-wire serial I/O modes ($\overline{SCK}$: External clock input): (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3,200			ns
$\overline{SCK}$ high/low level width	t_{KL2}, t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1,600			ns
SI[Note 1] setup time (referred to $\overline{SCK}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI[Note 1] hold time (referred to $\overline{SCK}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
Delay time from $\overline{SCK}$↓ to SO[Note 1] output	t_{KSO2}	R_L = 1 kΩ[Note 2], C_L = 100 pF	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1,000	ns

Notes 1. In two-wire serial I/O mode, SO should be read as SB0 or SB1.

2. R_L is the resistance of the SO output line load, while C_L is the capacitance.

SBI mode ($\overline{SCK}$: Internal clock output (master)): (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1,300			ns
				3,800			ns
$\overline{SCK}$ high/low level width	t_{KL3}, t_{KH3}	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2 - 50			ns
				t_{KCY3}/2 - 150			ns
SB0/SB1 setup time (referred to $\overline{SCK}$↑)	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SB0/SB1 hold time (referred to $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
Delay time from $\overline{SCK}$↓ to SB0/SB1 output	t_{KSO3}	R_L = 1 kΩ[Note] C_L = 100 pF	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1,000	ns
From $\overline{SCK}$↑ to SB0/SB1↓	t_{KSB}			t_{KCY3}			ns
From SB0/SB1↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY3}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY3}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY3}			ns

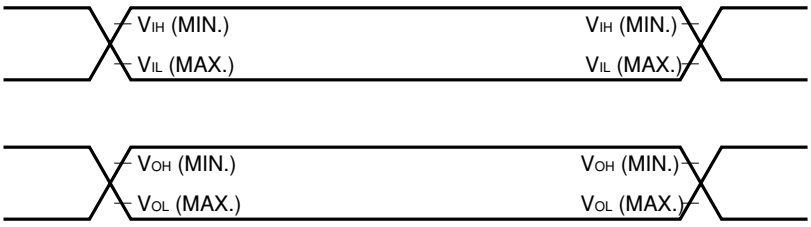
Note R_L is the resistance of the SB0/SB1 output line load, while C_L is the capacitance.

SBI mode ($\overline{SCK}$: External clock input (slave)): (T_A = -40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

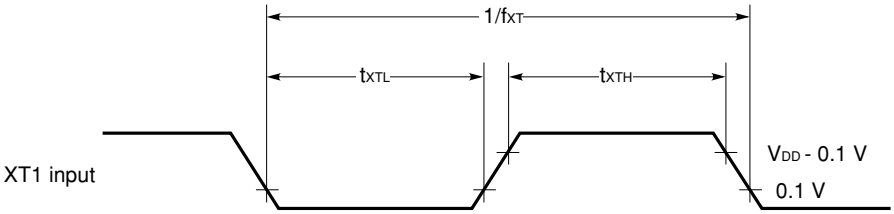
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3,200			ns
$\overline{SCK}$ high/low level width	t_{KL4}, t_{KH4}	V_{DD} = 2.7 to 5.5 V		400			ns
				1,600			ns
SB0/SB1 setup time (referred to $\overline{SCK}$↑)	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SB0/SB1 hold time (referred to $\overline{SCK}$↑)	t_{KSI4}			t_{KCY4}/2			ns
Delay time from $\overline{SCK}$↓ to SB0/SB1 output	t_{KSO4}	R_L = 1 kΩ[Note] C_L = 100 pF	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1,000	ns
From $\overline{SCK}$↑ to SB0/SB1↓	t_{KSB}			t_{KCY4}			ns
From SB0/SB1↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY4}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY4}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY4}			ns

Note R_L is the resistance of the SB0/SB1 output line load, while C_L is the capacitance.

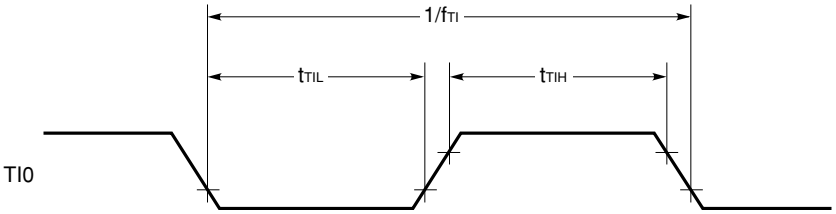
AC timing measurement points (excluding XT1 input)



Clock timing

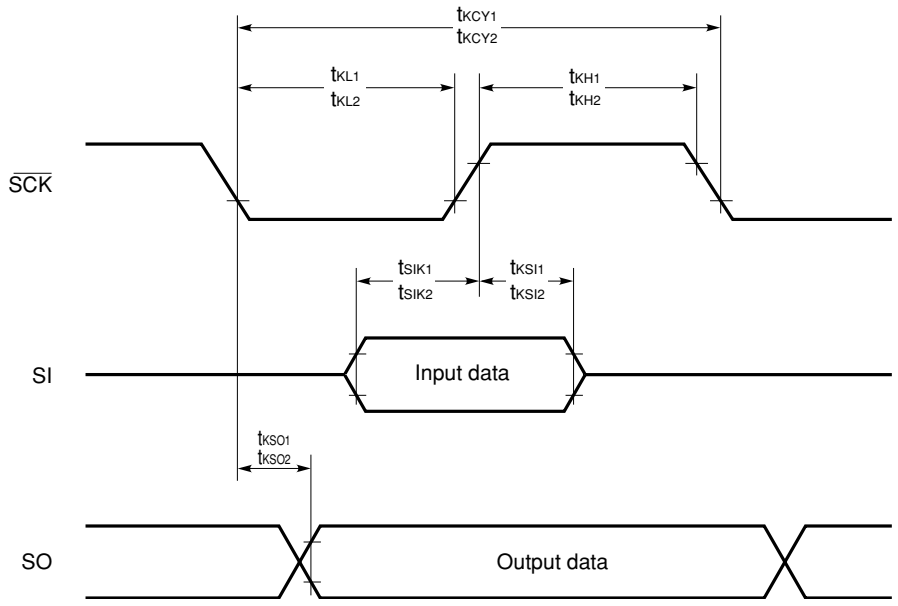


TI0 timing

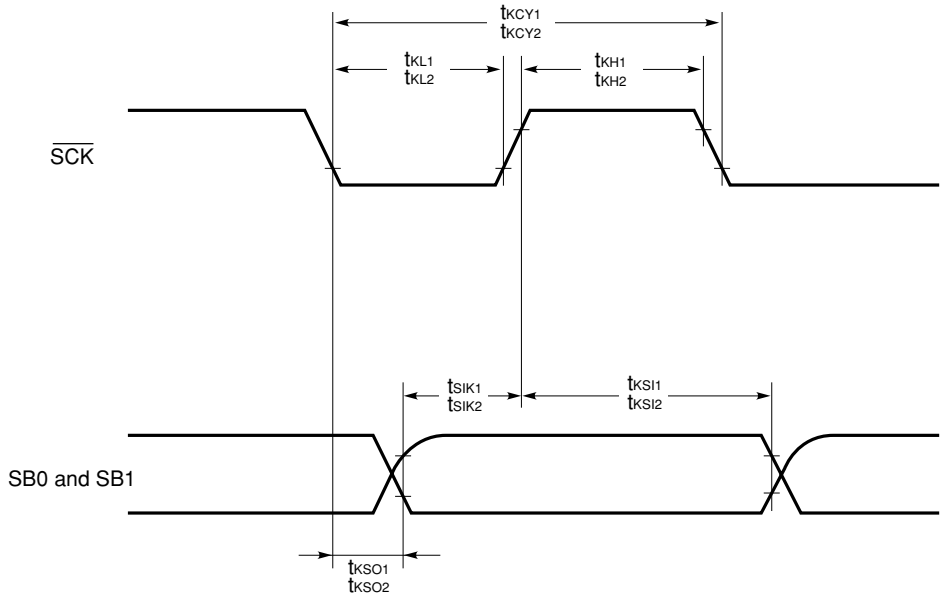


Serial transfer timing

Three-wire serial I/O mode:

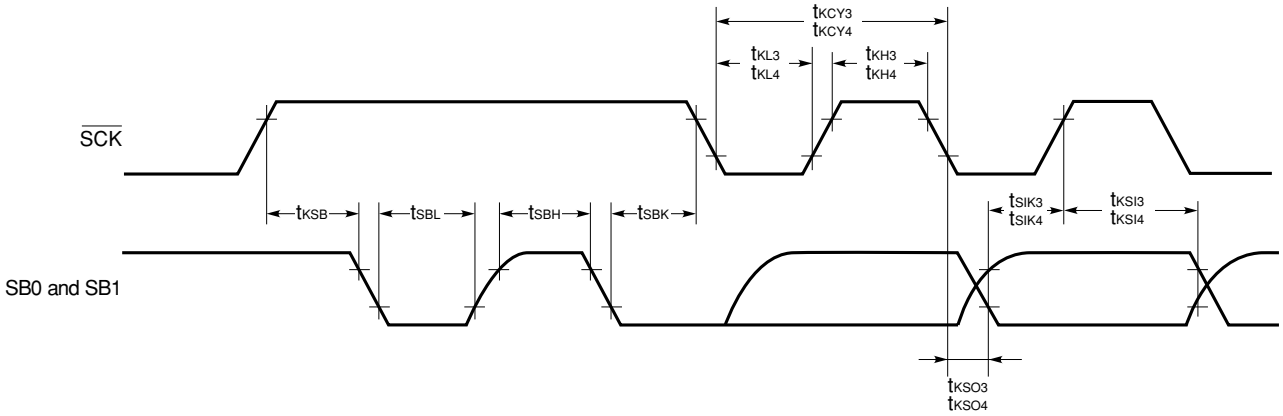


Two-wire serial I/O mode:

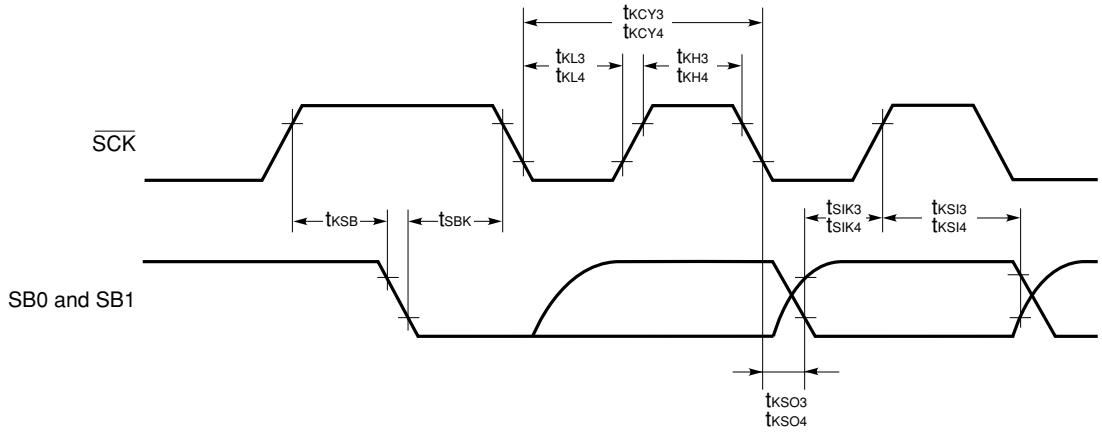


Serial transfer timing

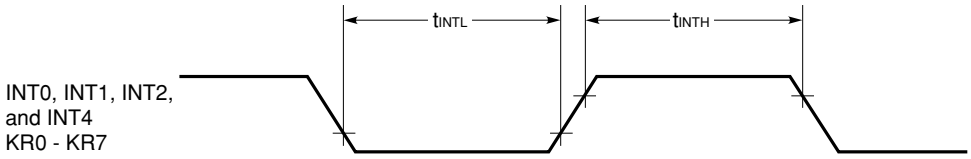
Bus release signal transfer:



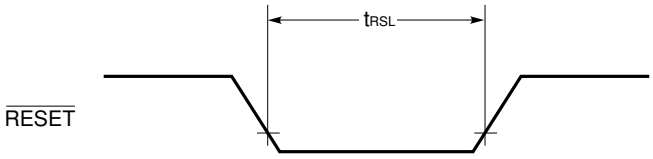
Command signal transfer:



Interrupt input timing



$\overline{\text{RESET}}$ input timing



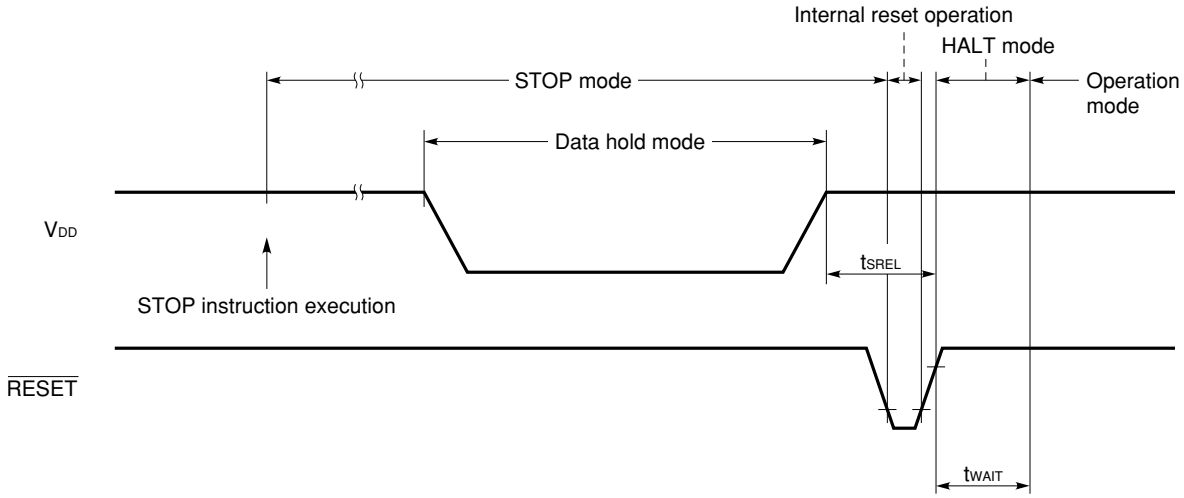
DATA HOLD CHARACTERISTICS BY LOW SUPPLY VOLTAGE IN DATA MEMORY STOP MODE (T_A = -40 to +85 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Release signal setting time	t_{SREL}		0			μs
Oscillation settling time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		56/f_{CC}		μs
		Release by interrupt request		Note 2		μs

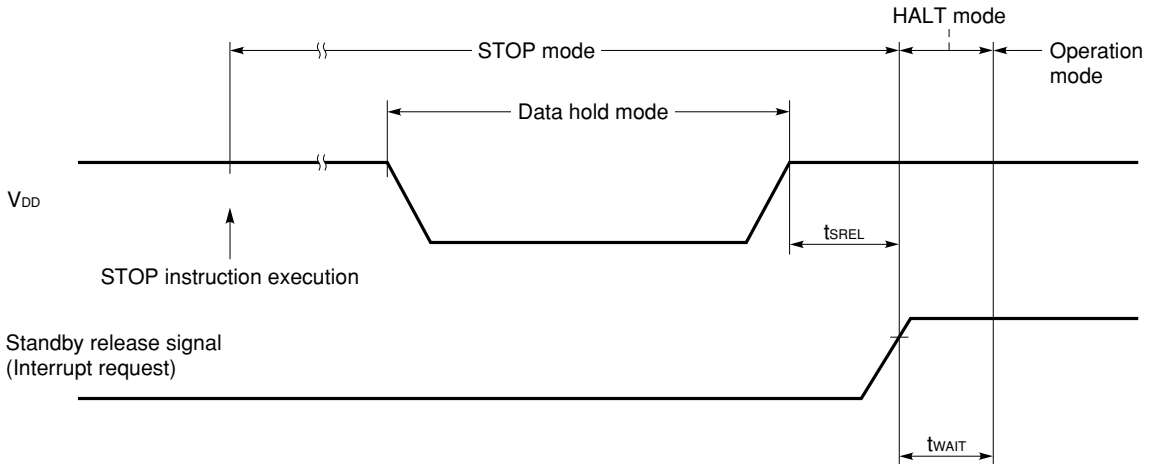
Notes 1. CPU operation stop time for preventing unstable operation at the beginning of oscillation.

2. Select either 512/f_{CC} or no wait with the mask option.

Data hold timing (STOP mode release by $\overline{RESET}$)

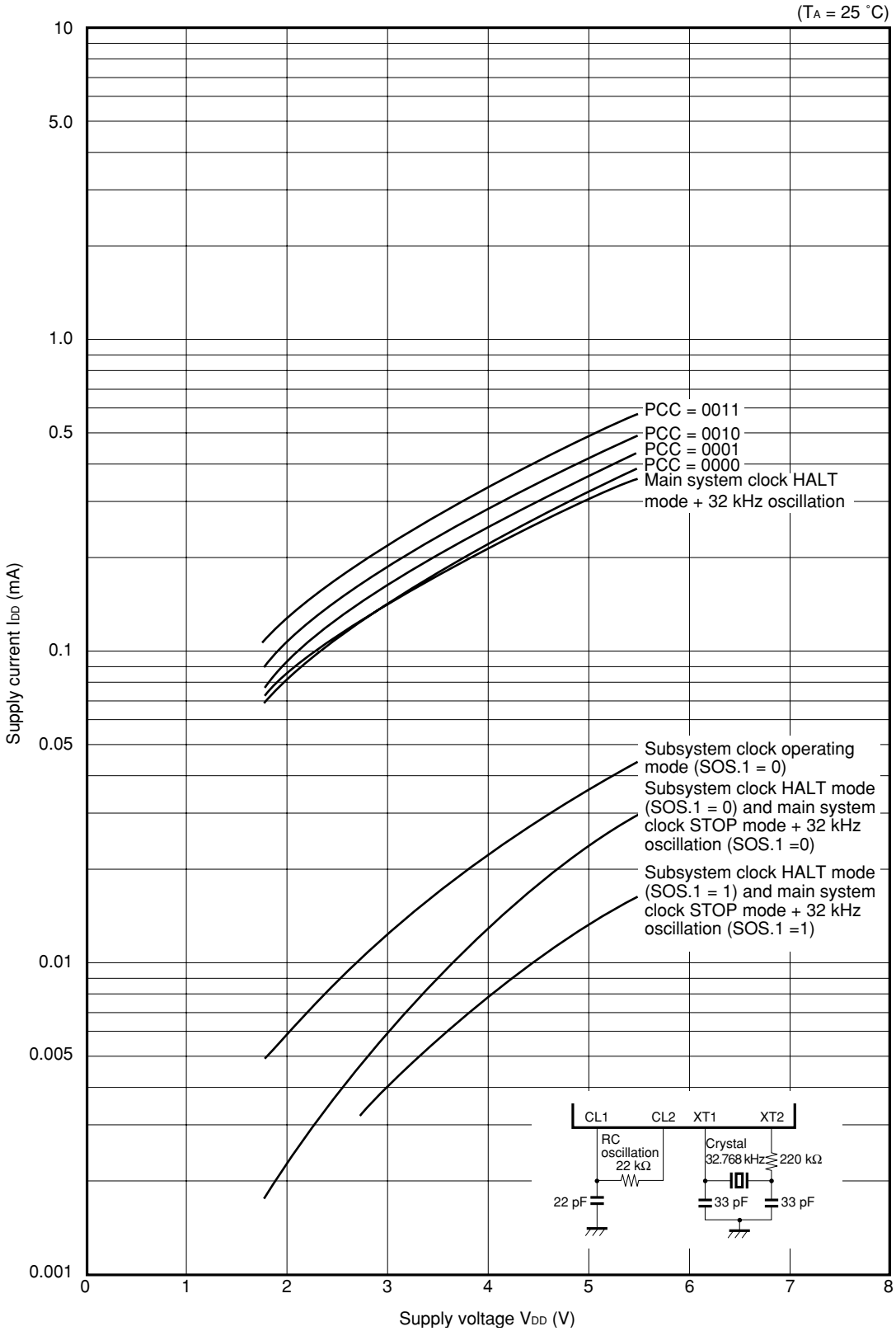


Data hold timing (standby release signal: STOP mode release by interrupt signal)



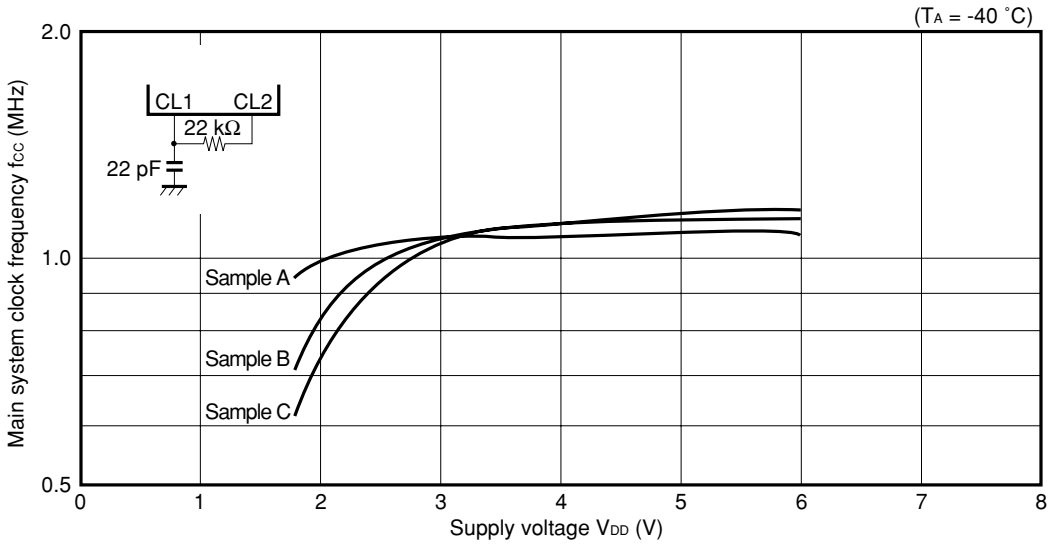
13. CHARACTERISTIC CURVE (REFERENCE VALUES)

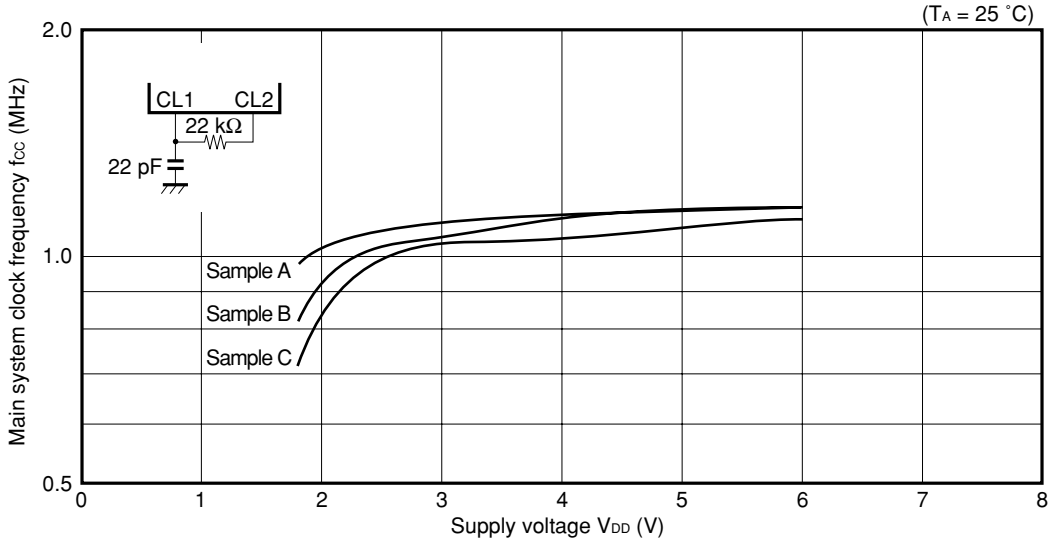
I_{DD} vs. V_{DD} (When the main system clock is operating at 1.0 MHz with an RC oscillation)

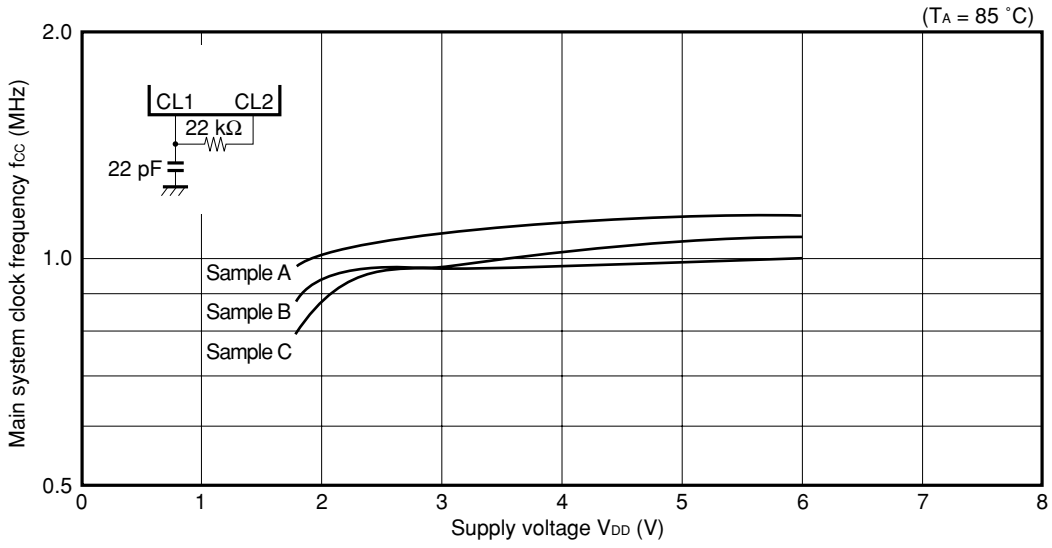


14. EXAMPLES OF RC OSCILLATOR FREQUENCY CHARACTERISTICS (REFERENCE VALUES)

f_{CC} vs. V_{DD} (RC oscillation , R = 22 kΩ, C = 22 pF)

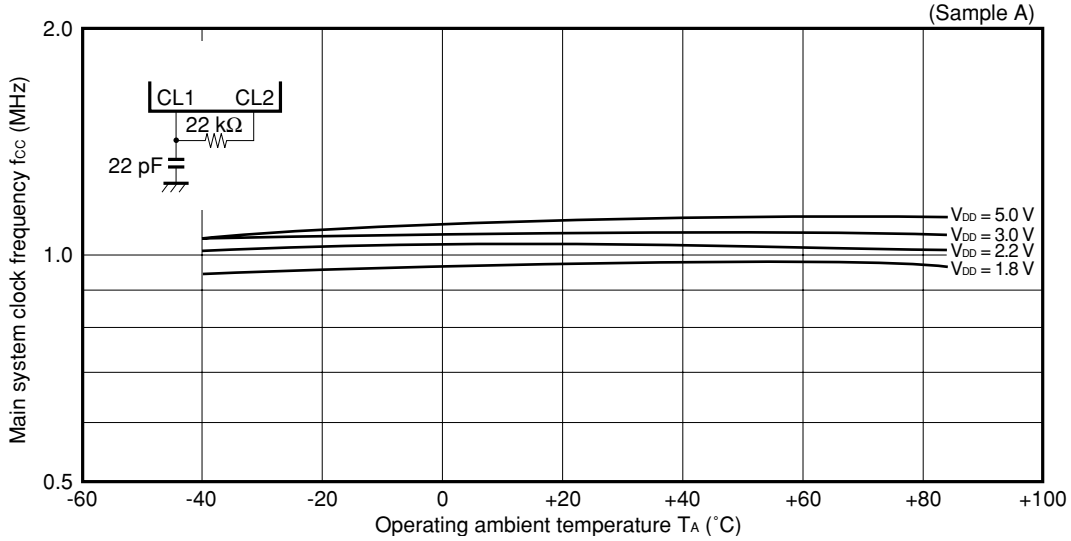




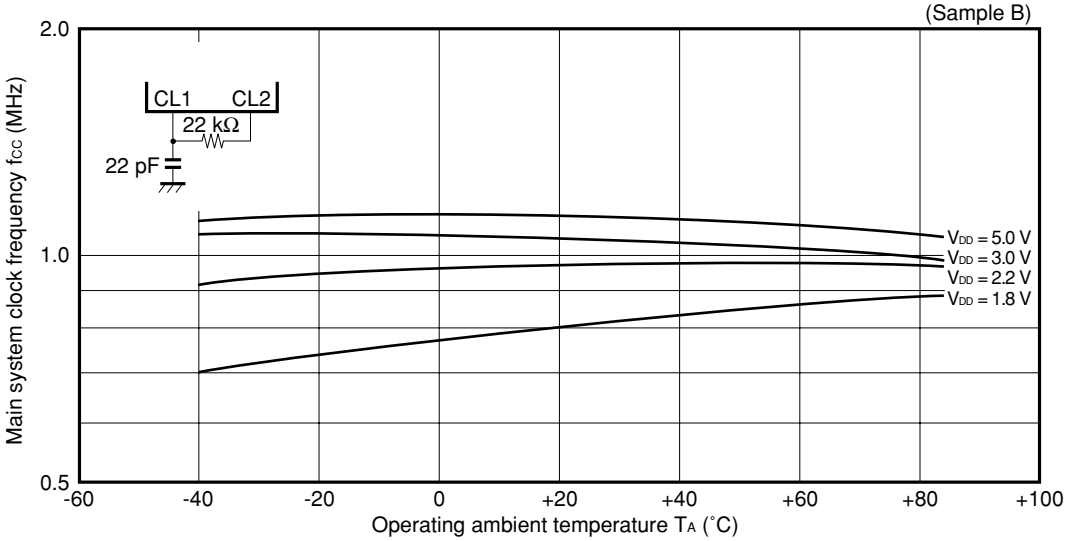


f_{CC} vs. T_A (RC oscillation, R = 22 kΩ, C = 22 pF)

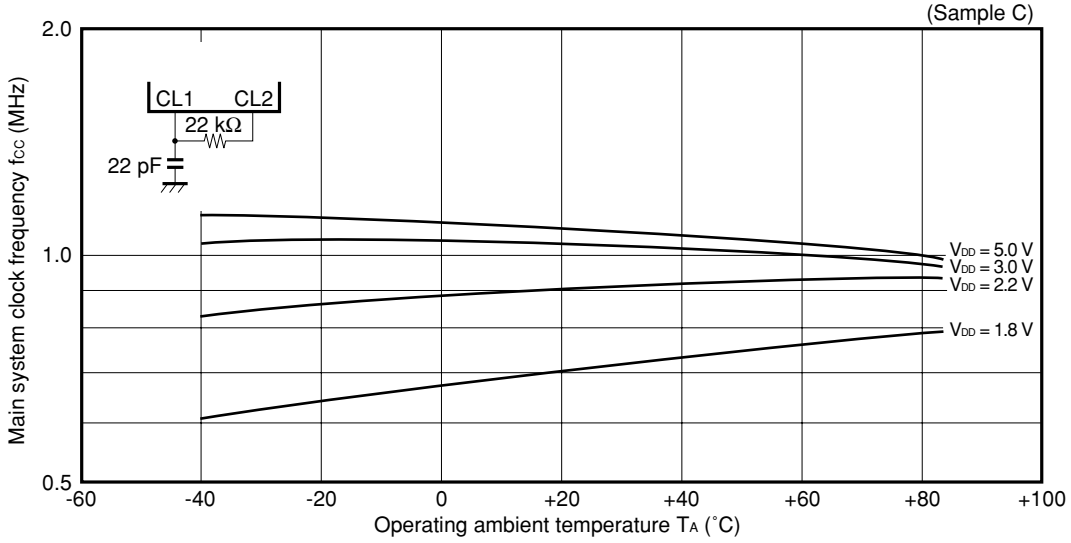
(Sample A)



(Sample B)

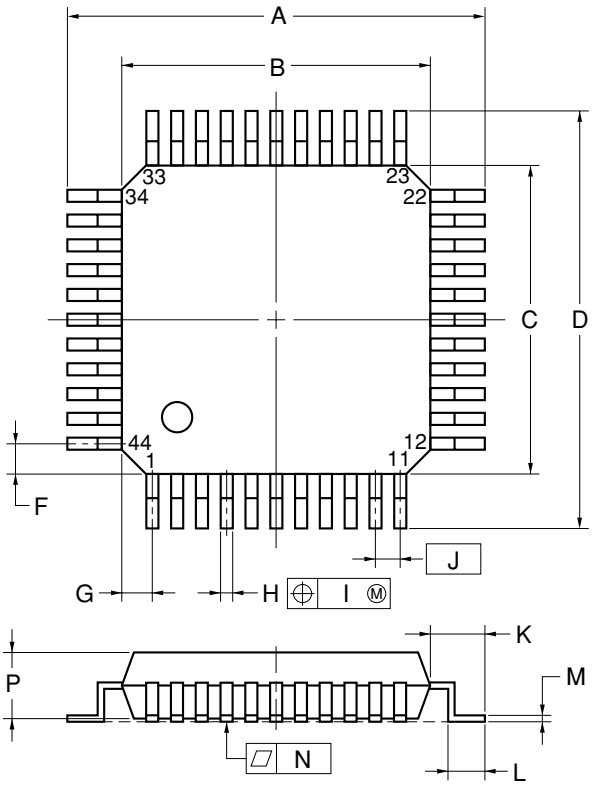


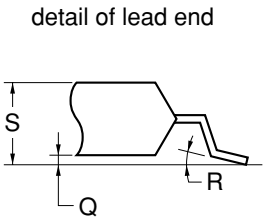
(Sample C)



15. PACKAGE DRAWINGS

44 PIN PLASTIC QFP (□10)





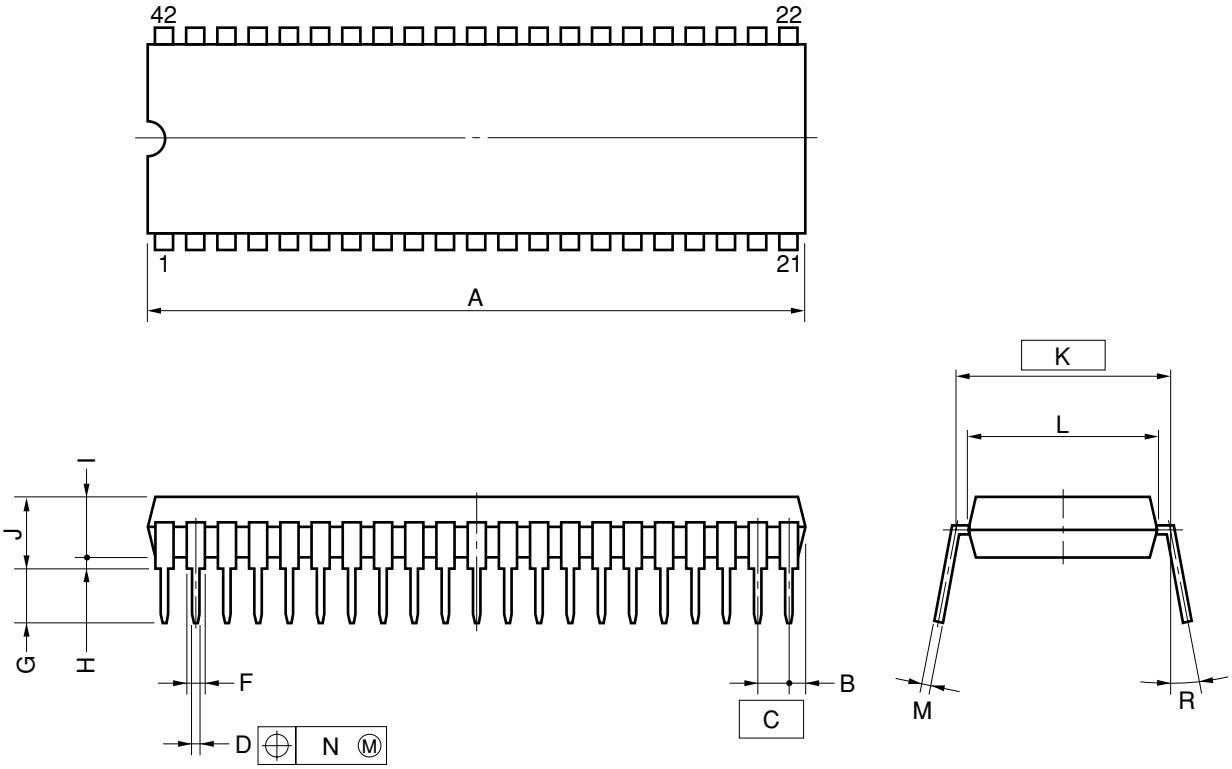
NOTE

Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

16. RECOMMENDED SOLDERING CONDITIONS

The μPD750104, μPD750106, and μPD750108 should be soldered and mounted under the following recommended conditions.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 16-1. Surface Mounting Type Soldering Conditions

(1) μPD750104GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)
μPD750106GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)
μPD750108GB-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)
μPD750104GB(A)-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)
μPD750106GB(A)-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)
μPD750108GB(A)-×××-3BS-MTX: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

★ **(2) μPD750104GB-×××-3BS-MTX-A: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)**
μPD750106GB-×××-3BS-MTX-A: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)
μPD750108GB-×××-3BS-MTX-A: 44-pin plastic QFP (10 × 10 mm, 0.8 mm pitch)

Undefined

Remark Products with “-A” at the end of the part number are lead-free products.

Table 16-2. Insertion Type Soldering Conditions

μPD750104CU-×××: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
μPD750106CU-×××: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
μPD750108CU-×××: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
★ **μPD750104CU-×××-A: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)**
★ **μPD750106CU-×××-A: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)**
★ **μPD750108CU-×××-A: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)**
μPD750104CU(A)-×××: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
μPD750106CU(A)-×××: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)
μPD750108CU(A)-×××: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)

Soldering method	Soldering conditions
Wave soldering (pin only)	Solder bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (for each pin)

Caution Apply wave soldering to pins only. See to it that the jet solder does not contact with the chip directly.

Remarks 1. Products with "-A" at the end of the part number are lead-free products.
2. For soldering methods and conditions other than those recommended above, contact an NEC Electronics sales representative.

APPENDIX A FUNCTIONS OF THE μPD750008, μPD750108, AND μPD75P0116

(1/2)

Item		μPD750008	μPD750108	μPD75P0116
Program memory		Masked ROM 0000H - 1FFFH (8,192 × 8 bits)		One-time PROM 0000H - 3FFFH (16,384 × 8 bits)
Data memory		000H - 1FFH (512 × 4 bits)		
CPU		75XL CPU		
General-purpose register		(4 bits × 8 or 8 bits × 4) × 4 banks		
Main system clock oscillator		Crystal/ceramic oscillator	RC oscillator (with external resistor and capacitor)	
Time required for start after reset		$2^{17}/f_X$, $2^{15}/f_X$ (selected using a mask option)	Fixed to $56/f_{CC}$	
Wait time applied when STOP mode is released by an interrupt		$2^{20}/f_X$, $2^{17}/f_X$, $2^{15}/f_X$, $2^{13}/f_X$ (selected according to BTM setting)	$2^9/f_{CC}$ or no wait (selected using a mask option)	Fixed to $2^9/f_{CC}$
Subsystem clock oscillator		Crystal oscillator		
Instruction execution time	When selecting the main system clock	• 0.95, 1.91, 3.81, or 15.3 μs (when operating at f_X = 4.19 MHz) • 0.67, 1.33, 2.67, or 10.7 μs (when operating at f_X = 6.0 MHz)	• 4, 8, 16, or 64 μs (when operating at f_{CC} = 1.0 MHz) • 2, 4, 8, or 32 μs (when operating at f_{CC} = 2.0 MHz)	
	When selecting the subsystem clock	122 μs (when operating at 32.768 kHz)		
I/O port	CMOS input	8 (Built-in pull-up resistors that can be connected by software: 7)		
	CMOS I/O	18 (Built-in pull-up resistors that can be connected by software)		
	N-ch open-drain I/O	8 (Pull-up resistors that can be incorporated by mask option) Withstand voltage of 13 V		8 (No mask option) Withstand voltage of 13 V
	Total	34		
Timer		4 channels • 8-bit timer counter: 1 • 8-bit timer/event counter: 1 • Basic interval timer/watchdog timer: 1 • Clock timer: 1	4 channels • 8-bit timer counter (clock timer output function provided): 1 • 8-bit timer/event counter: 1 • Basic interval timer/watchdog timer: 1 • Clock timer: 1	

(2/2)

Item	μPD750008	μPD750108	μPD75P0116
Serial interface	3 modes supported • Three-wire serial I/O mode: First transferred bit switchable between LSB and MSB • Two-wire serial I/O mode • SBI mode		
Clock output (PCL)	• Φ, 524, 262, or 65.5 kHz (when the main system clock operates at 4.19 MHz) • Φ, 750, 375, or 93.8 kHz (when the main system clock operates at 6.0 MHz)	• Φ, 125, 62.5, or 15.6 kHz (when the main system clock operates at 1.0 MHz) • Φ, 250, 125, or 31.3 kHz (when the main system clock operates at 2.0 MHz)	
Buzzer output (BUZ)	• 2, 4, or 32 kHz (when the main system clock operates at 4.19 MHz or the subsystem clock operates at 32.768 kHz) • 2.93, 5.86, or 46.9 kHz (when the main system clock operates at 6.0 MHz)	• 2, 4, or 32 kHz (when the subsystem clock operates at 32.768 kHz) • 0.488, 0.977, or 7.813 kHz (when the main system clock operates at 1.0 MHz) • 0.977, 1.953, or 15.625 kHz (when the main system clock operates at 2.0 MHz)	
Vectored interrupt	External: 3, internal: 4		
Test input	External: 1, internal: 1		
Supply voltage	V_{DD} = 2.2 to 5.5 V	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature	T_A = -40 to +85 °C		
Package	• 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) • 44-pin plastic QFP (10 × 10 mm, 0.8-mm pitch)		

APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for the development of a system which employs the μPD750108. In the 75XL series, use the common relocatable assembler together with a device file of each model.

Language processors

RA75X relocatable assembler	Host machine		Part number
	OS	Distribution media	
	PC-9800 series	MS-DOS™ Ver. 3.30 to Ver. 6.2Note	3.5-inch 2HD	μS5A13RA75X
			5.25-inch 2HD	μS5A10RA75X
	IBM PC/AT™ and compatibles	See "**OS for IBM PC**."	3.5-inch 2HC	μS7B13RA75X
			5.25-inch 2HC	μS7B10RA75X

Device file	Host machine		Part number
	OS	Distribution media	
	PC-9800 series	MS-DOS Ver. 3.30 to Ver. 6.2Note	3.5-inch 2HD	μS5A13DF750008
			5.25-inch 2HD	μS5A10DF750008
	IBM PC/AT and compatibles	See "**OS for IBM PC**."	3.5-inch 2HC	μS7B13DF750008
			5.25-inch 2HC	μS7B10DF750008

Note These software products cannot use the task swap function, which is available in MS-DOS Ver. 5.00 or later.

Remark The operations of the assembler and device file are guaranteed only on the above host machines and OSs.

PROM programming tools

<table>
<tr><td rowspan="2">Hardware</td><td>PG-1500</td><td colspan="4">The PG-1500 PROM programmer is used together with an accessory board and optional program adapter. It allows the user to program a single chip microcontroller containing PROM from a standalone terminal or a host machine. The PG-1500 can be used to program typical 256K-bit to 4M-bit PROMs.</td></tr>
<tr><td>PA-75P008CU</td><td colspan="4">The PA-75P008CU is a PROM programmer adapter provided for the μPD75P0116CU/GB. It is used in conjunction with the PG-1500.</td></tr>
<tr><td rowspan="6">Software</td><td rowspan="6">PG-1500 controller</td><td colspan="4">This program enables the host machine to control the PG-1500 through the serial and parallel interfaces.</td></tr>
<tr><td rowspan="2">Host machine</td><td rowspan="2">OS</td><td rowspan="2">Distribution media</td><td rowspan="2">Part number</td></tr>
<tr></tr>
<tr><td rowspan="2">PC-9800 series</td><td rowspan="2">MS-DOS
(Ver. 3.30 to Ver. 6.2^{Note})</td><td>3.5-inch 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>5.25-inch 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td rowspan="2">IBM PC/AT and compatibles</td><td rowspan="2">See "OS for IBM PC."</td><td>3.5-inch 2HD</td><td>μS7B13PG1500</td></tr>
<tr><td>5.25-inch 2HC</td><td>μS7B10PG1500</td></tr>
</table>

Note These software products cannot use the task swap function, which is available in MS-DOS Ver. 5.00 or later.

Remark Operation of the PG-1500 controller is guaranteed only on the above host machines and OSs.

Debugging tools

The in-circuit emulators (IE-75000-R and IE-75001-R) are provided to debug programs used for the μPD750108. The system configuration is shown below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator used to debug hardware and software when developing an application system using the 75X series and 75XL series. Use this emulator together with optional emulation board IE-75300-R-EM and emulation probe EP-75008CU-R or EP-75008GB-R to develop application systems of the μPD750108 subseries. For efficient debugging, connect the emulator to the host machine and a PROM programmer. The IE-75000-R contains emulation board IE-75000-R-EM. The board is connected to the IE-75000-R.			
	IE-75001-R	The IE-75001-R is an in-circuit emulator used to debug hardware and software when developing an application system using the 75X series and 75XL series. Use this emulator together with optional emulation board IE-75300-R-EM and emulation probe EP-75008CU-R or EP-75008GB-R to develop application systems of the μPD750108 subseries. For efficient debugging, connect the emulator to the host machine and a PROM programmer.			
	IE-75300-R-EM	The IE-75300-R-EM is an emulation board used to evaluate an application system using the μPD750108 subseries. Use this board together with the IE-75000-R or IE-75001-R.			
	EP-75008CU-R	The EP-75008CU-R is an emulation probe for the μPD750108CU. Connect this emulation probe to the IE-75000-R or IE-75001-R, and the IE-75300-R-EM.			
	EP-75008GB-R	The EP-75008GB-R is an emulation probe for the μPD750108GB. Connect this emulation probe to the IE-75000-R or IE-75001-R, and the IE-75300-R-EM.			
	EV-9200G-44	A 44-pin conversion socket, the EV-9200G-44, supplied with this probe facilitates the connection of the probe to the target system.			
Software	IE control program	This program enables the host machine to control the IE-75000-R or IE-75001-R through the RS-232-C and Centronics interface.			
		Host machine	OS	Distribution media	Part number
		PC-9800 series	MS-DOS Ver. 3.30 to Ver. 6.2[Note 2]	3.5-inch 2HD	μS5A13IE75X
				5.25-inch 2HD	μS5A10IE75X
		IBM PC/AT and compatibles	See "**OS for IBM PC**."	3.5-inch 2HC	μS7B13IE75X
				5.25-inch 2HC	μS7B10IE75X

Notes 1. Maintenance service only

2. These software products cannot use the task swap function, which is available in MS DOS Ver. 5.00 or later.

Remarks 1. Operation of the IE control program is guaranteed only on the above host machines and OSs.

2. The μPD750104, μPD750106, μPD750108, and μPD75P0116 are collectively called the μPD750108 subseries.

OS for IBM PC

The following IBM PC OSs are supported.

OS	Version
PC DOS™	Ver. 5.02 to Ver. 6.3 J6.1/V**Note** to J6.3/V**Note**
MS-DOS	Ver. 5.0 to Ver. 6.22 5.0/V**Note** to 6.2/V**Note**
IBM DOS™	J5.02/V**Note**

Note Only English version is supported.

Caution These software products cannot use the task swap function, which is available in MS-DOS Ver. 5.0 or later.

APPENDIX C RELATED DOCUMENTS

Some documents are preliminary editions, but they are not so specified in the tables below.

Documents related to devices

Document name	Document number	
	Japanese	English
μPD750104, 750106, 750108, 750104(A), 750106(A), 750108(A) Data Sheet	U12301J	U12301E (This manual)
μPD75P0116 Data Sheet	U12603J	U12603E
μPD750108 User's Manual	U11330J	U11330E
μPD750008, 750108 Instruction List	U11456J	-
75XL Series Selection Guide	U10453J	U10453E

Documents related to development tools

Document name			Document number	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846	EEU-1416
	IE-75300-R-EM User's Manual		U11354J	U11354E
	EP-75008CU-R User's Manual		EEU-699	EEU-1317
	EP-75008GB-R User's Manual		EEU-698	EEU-1305
	PG-1500 User's Manual		U11940J	EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 Controller User's Manual	PC-9800 series (MS-DOS) base	EEU-704	EEU-1291
		IBM PC series (PC DOS) base	EEU-5008	U10540E

Other related documents

Document name	Document number	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grade on NEC Semiconductor Devices	C11531J	C11531E
Reliability and Quality Control of NEC Semiconductor Devices	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	-
Semiconductor Device Quality Guarantee Guide	C11893J	MEI-1202
Microcontroller-Related Products Guide - by third parties	U11416J	-

Caution The above related documents are subject to change without notice. Be sure to use the latest edition when you design your system.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

[GLOBAL SUPPORT]
http://www.necel.com/en/support/support.html

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