DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

Phase-out/Discontinued

μPD98408

6-PORT 25M ATM PHY LSI

The μPD98408 is an ATM physical layer LSI IC that complies with ATM25 (25.6 Mbps) and which supports TC sublayer and PMD sublayer functions. Interfacing with the ATM layer and AAL layer LSI is implemented at UTOPIA Level 2.

Detailed descriptions of its functions, etc., are given in the following user's manual. Be sure to read it for design purposes.

μPD98408 User's Manual: S11409E

FEATURES

- Provides a 25.6-Mbps ATM PHY (PMD & TC) function for six circuits
- Conforms to the ATM Forum PHY interface specifications (af-phy-0040.000 November 1995).
- UTOPIA Level 2 V1.0 (af-phy-0039.000 June 1995: max. 8 bits/40 MHz) interface
- Three-cell built-in transmit/receive FIFOs for each circuit
- PMD sublayer functions:
  - (a) Built-in clock recovery.
  - (b) Built-in equalizer.
- TC sublayer functions:
  - (a) NRZI encoder/decoder.
  - (b) Command byte insertion/detection.
  - (c) 4B/5B encoder/decoder.
  - (d) Cell scrambler/descrambler.
  - (e) HEC generation/verification.
- CPU interface: Intel or Motorola can be selected.
- Supports STP and UTP (Categories 3, 4, 5).
- Loopback function: Loopback in the PMD and ATM layers.
- Operation And Maintenance (OAM) functions: Input failure detection, HEC error detection and 4B/5B code error detection.
- Test function: Supports JTAG.
- Power supply voltage: 3.3 V ± 5 %.

ORDERING INFORMATION

Part Number	Package
μPD98408GD-LML	208-pin plastic QFP (fine pitch) (28 × 28)

Remark This document indicates active low pins in the format of "xxx_B" (_B after the pin name).

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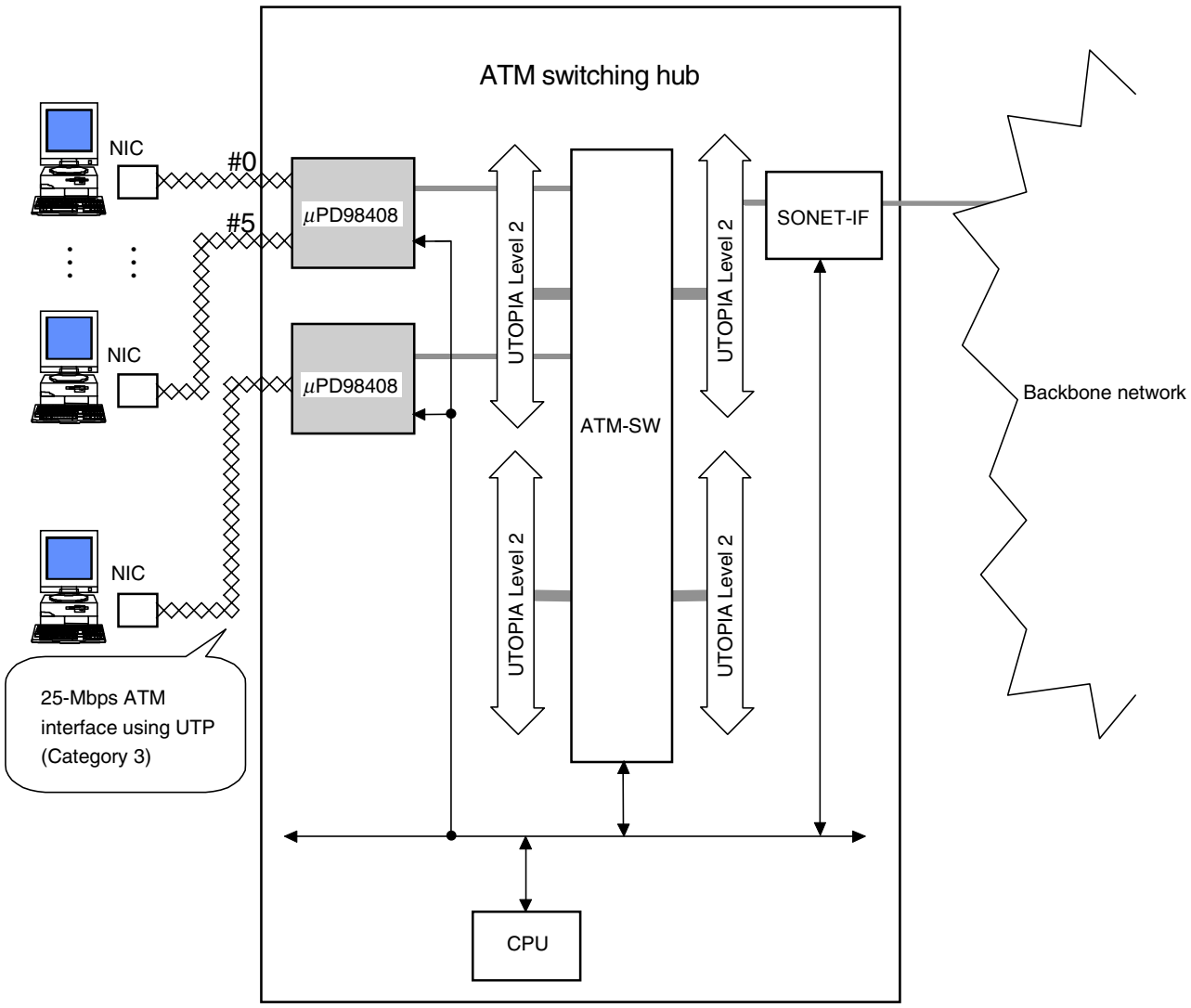
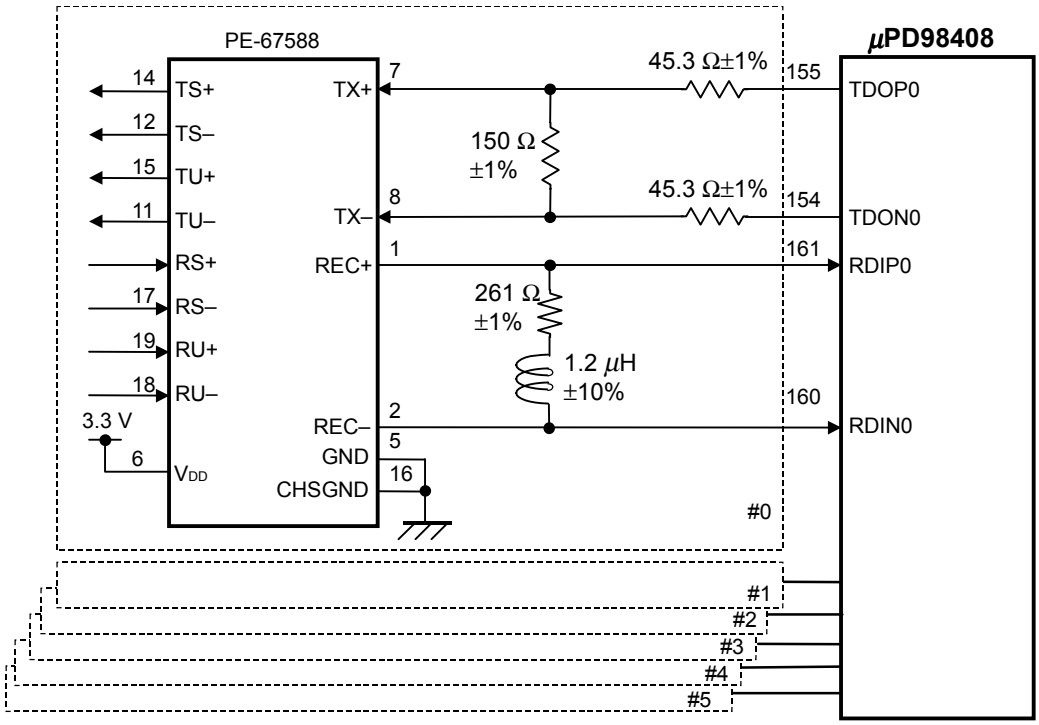
The mark ★ shows major revised points.

SYSTEM CONFIGURATION EXAMPLE (APPLICATION)

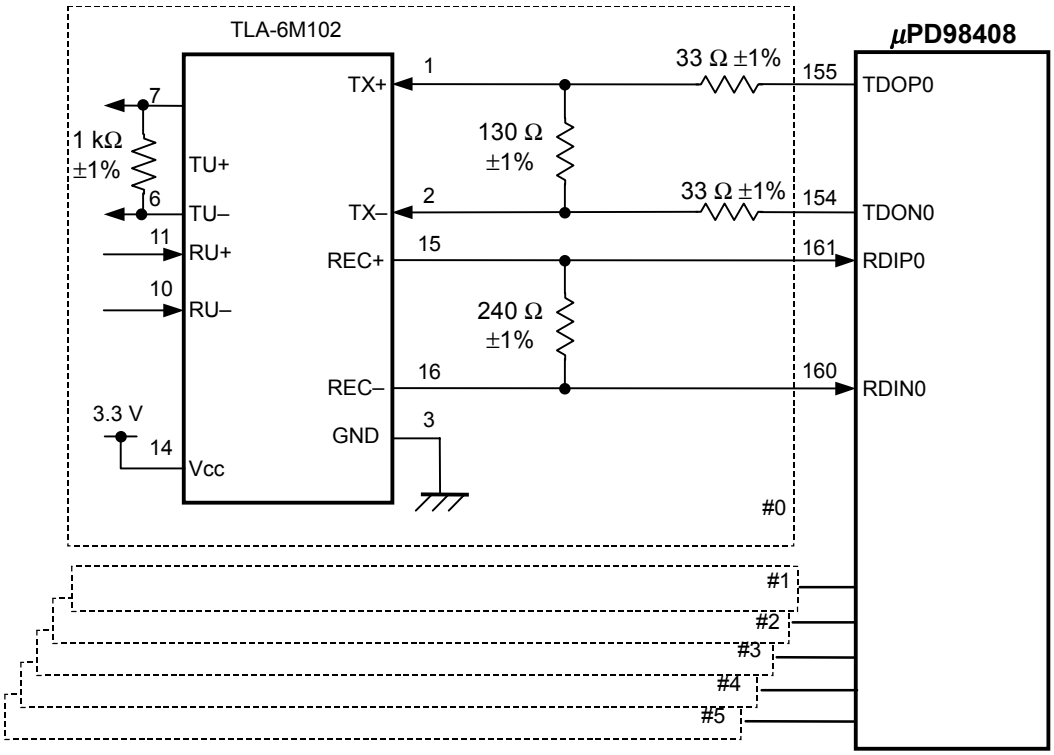


★ SYSTEM CONFIGURATION EXAMPLE (CONNECTION WITH MAGNETICS)

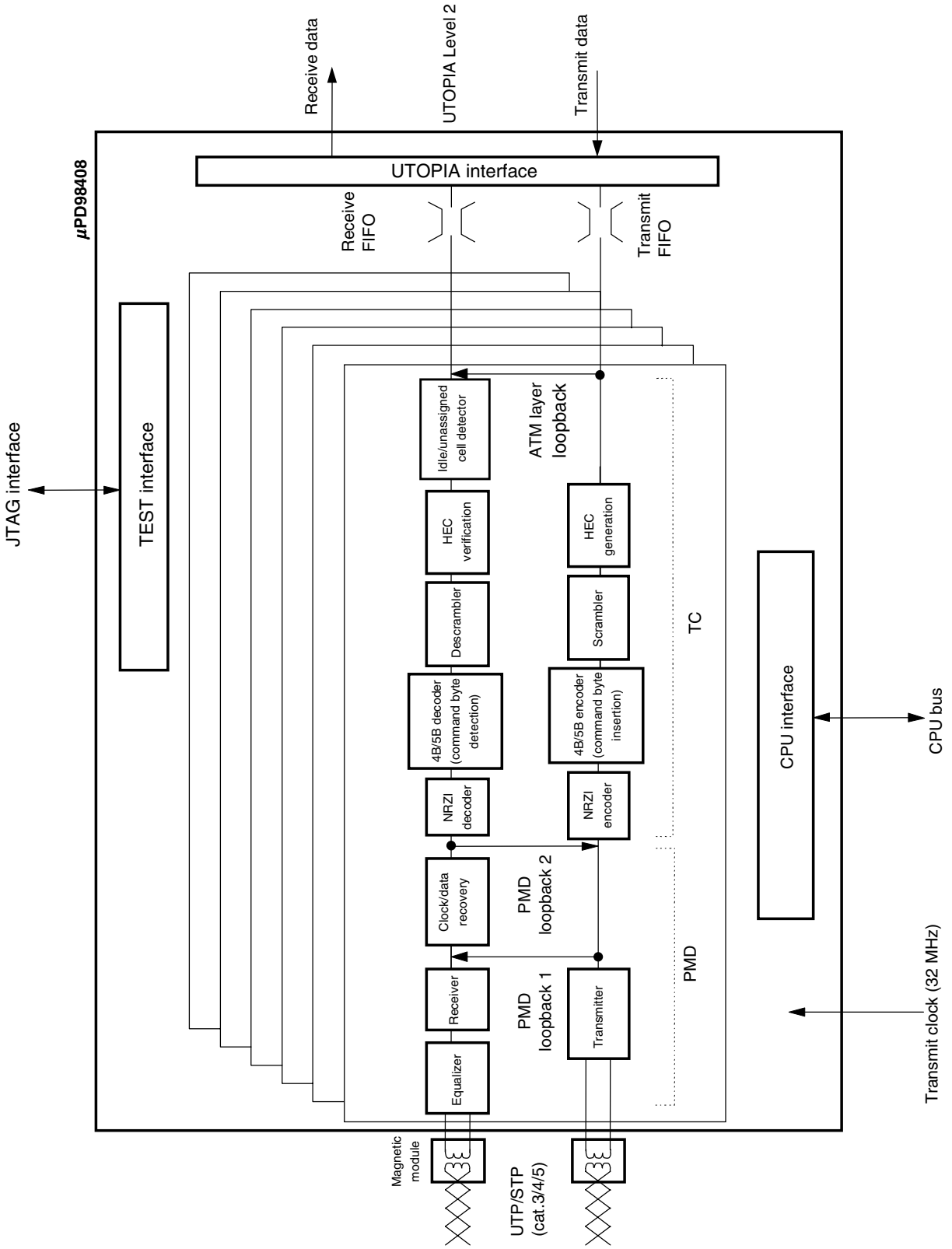
THE EXAMPLE of CONNECTION WITH PE-67588 (Pulse Inc.) MAGNETICS



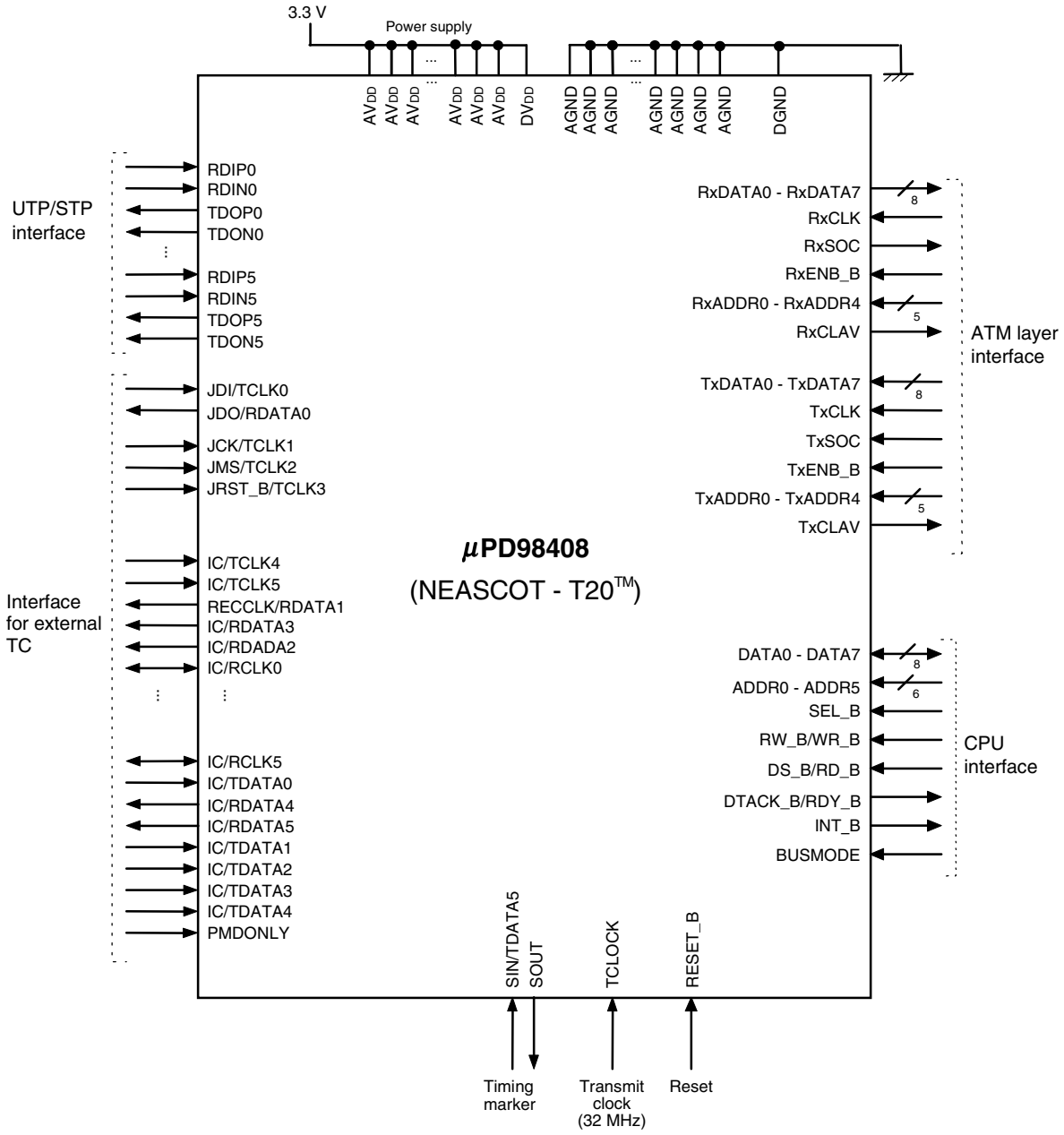
THE EXAMPLE of CONNECTION WITH TLA-6M102 (TDK™ Co.) MAGNETICS



BLOCK DIAGRAM



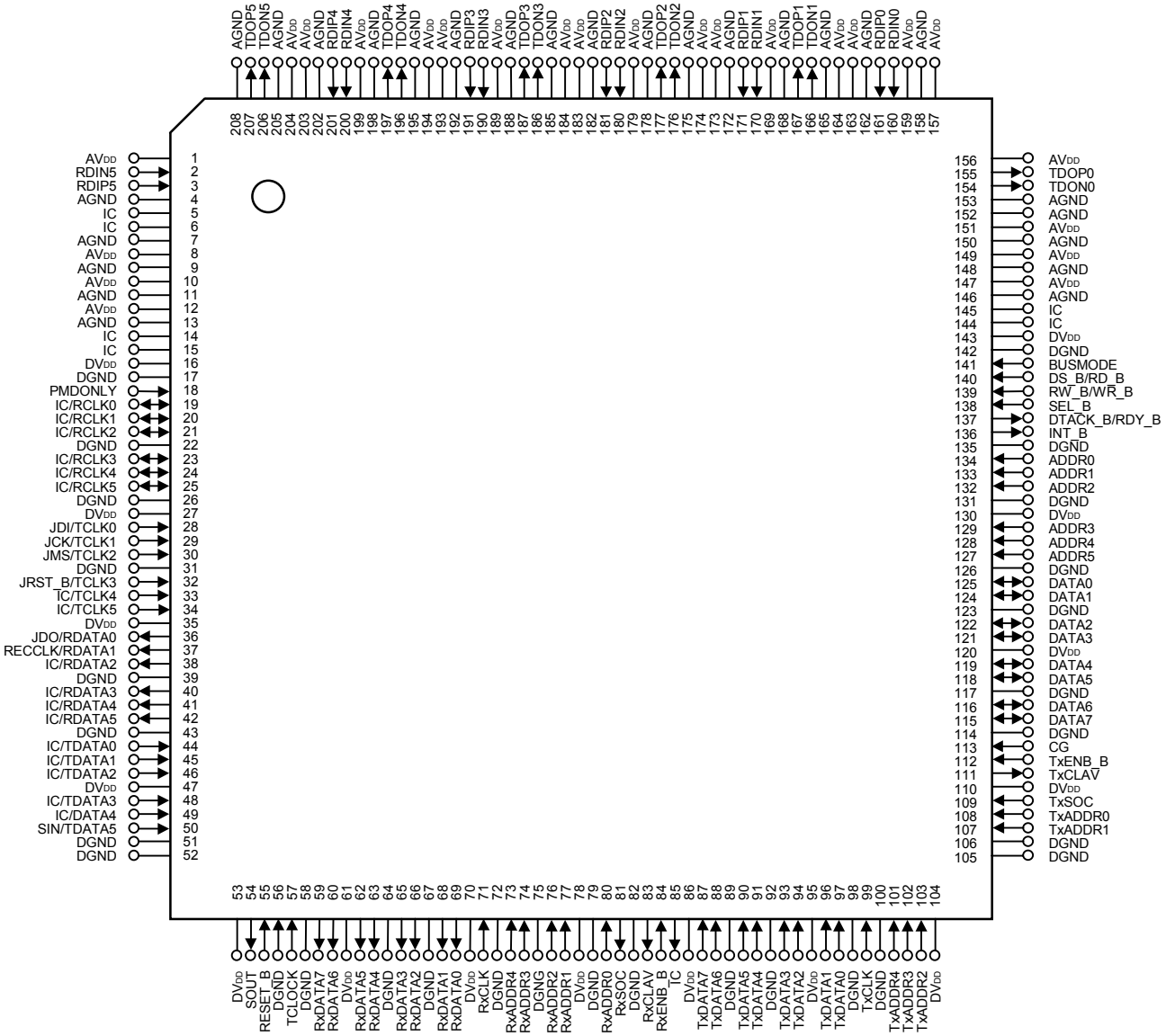
PIN LAYOUT


3.3 V
Power supply
AVDD AVDD AVDD AVDD AVDD AVDD DVDD
AGND AGND AGND AGND AGND AGND AGND DGND
UTP/STP interface
RDIP0
RDIN0
TDOP0
TDON0
RDIP5
RDIN5
TDOP5
TDON5
JDI/TCLK0
JDO/RDATA0
JCK/TCLK1
JMS/TCLK2
JRST_B/TCLK3
Interface for external TC
IC/TCLK4
IC/TCLK5
RECCLK/RDATA1
IC/RDATA3
IC/RDADA2
IC/RCLK0
IC/RCLK5
IC/TDATA0
IC/RDATA4
IC/RDATA5
IC/TDATA1
IC/TDATA2
IC/TDATA3
IC/TDATA4
PMDONLY
μPD98408
(NEASCOT - T20TM)
RxDATA0 - RxDATA7
RxCLK
RxSOC
RxENB_B
RxADDR0 - RxADDR4
RxCLAV
TxDATA0 - TxDATA7
TxCLK
TxSOC
TxENB_B
TxADDR0 - TxADDR4
TxCLAV
ATM layer interface
DATA0 - DATA7
ADDR0 - ADDR5
SEL_B
RW_B/WR_B
DS_B/RD_B
DTACK_B/RDY_B
INT_B
BUSMODE
CPU interface
SIN/TDATA5
SOUT
TCLOCK
RESET_B
Timing marker
Transmit clock (32 MHz)
Reset

PIN CONFIGURATION (TOP VIEW)

- 208-pin plastic QFP (fine pitch) (28 × 28)

μPD98408GD-LML



PIN NAMES

ADDR0-ADDR5	: Address	RxADDR0-RxADDR4	: Receive address
AGND	: Analog ground	RxCLAV	: Receive cell available
AV_{DD}	: Analog supply voltage	RxCLK	: Receive data clock
BUSMODE	: Bus mode	RxDATA0-RxDATA7	: Receive data
CG	: Connect GND	RxENB_B	: Receive enable
DATA0-DATA7	: Data	RxSOC	: Receive start address of ATM cell
DGND	: Digital ground	SEL_B	: Selector
DS_B/RD_B	: Data strove/read	SIN/TDATA5	: Signal in/transmit data
DTACK_B/RDY_B	: Data acknowledge/ready	SOUT	: Signal out
DV_{DD}	: Digital supply voltage	TCLOCK	: Transmit clock
IC	: Internal connect	TDON0-TDON5	: Transmit data output negative
IC/RCLK0-IC/RCLK5	: Internal connect/receive clock	TDOP0-TDOP5	: Transmit data output positive
IC/RDATA2-IC/RDATA5	: Internal connect/receive data	TxADDR0-TxADDR4	: Transmit address
IC/TCLK4, IC/TCLK5	: Internal connect/transmit clock	TxCLAV	: Transmit cell available
IC/TDATA0-IC/TDATA4	: Internal connect/transmit data	TxCLK	: Transmit data clock
INT_B	: Interrupt	TxDATA0-TxDATA7	: Transmit data
JCK/TCLK1	: JTAG test clock/transmit clock	TxENB_B	: Transmit enable
JDI/TCLK0	: JTAG test data input/transmit clock	TxSOC	: Transmit start address of ATM cell
JDO/RDATA0	: JTAG test data output/recieve data		
JMS/TCLK2	: JTAG test mode select/transmit clock		
JRST_B/TCLK3	: JTAG test reset/transmit clock		
PMDONLY	: PMD only		
RDIN0-RDIN5	: Receive data input negative		
RDIP0-RDIP5	: Receive data input positive		
RECCLK/RDATA1	: Recovery clock/receive data		
RESET_B	: Reset		
RW_B/WR_B	: Read write/write		

CONTENTS

1. PIN FUNCTIONS

1.1 Power Supply

Pin Name	Pin No.	I/O	Active Level	Function
AV_{DD}	1, 8, 10, 12, 147, 149, 151, 156, 157,159, 163, 164, 169,173, 174, 179, 183,184, 189, 193, 194,199, 203, 204	–	–	+3.3-V power supply pins for analog circuits.
DV_{DD}	16, 27, 35, 47, 53, 61, 70, 78, 86, 95, 104, 110, 120, 130, 143	–	–	+3.3-V power supply pins for digital circuits.
AGND	4, 7, 9, 11, 13, 146, 148, 150, 152,153, 158, 162, 165,168, 172, 175, 178,182, 185, 188, 192,195, 198, 202, 205, 208	–	–	Analog circuit grounding pins.
DGND	17, 22, 26, 31, 39, 43, 51, 52, 56, 58, 64, 67, 72, 75, 79, 82, 89, 92, 98, 100, 105, 106, 114, 117, 123, 126, 131, 135, 142	–		Digital circuit grounding pins.

Caution On the PC board layout, AGND and DGND should be connected to the same, wide plane.
On the PC board layout, AV_{DD} and DV_{DD} should be connected to the same, wide plane.
For details, refer to the User's Manual (S11409E).

1.2 UTP/STP Interface

Pin Name	Pin No.	I/O	Active Level	Function
RDIP0	161	I	–	Receive data inputs from circuit #0 (analog balanced signal inputs).
RDIN0	160	I	–	
TDOP0	155	O	–	Transmit data outputs to circuit #0 (analog balanced signal outputs).
TDON0	154	O	–	
RDIP1	171	I	–	Receive data inputs from circuit #1 (analog balanced signal inputs).
RDIN1	170	I	–	
TDOP1	167	O	–	Transmit data outputs to circuit #1 (analog balanced signal outputs).
TDON1	166	O	–	
RDIP2	181	I	–	Receive data inputs from circuit #2 (analog balanced signal inputs).
RDIN2	180	I	–	
TDOP2	177	O	–	Transmit data outputs to circuit #2 (analog balanced signal outputs).
TDON2	176	O	–	
RDIP3	191	I	–	Receive data inputs from circuit #3 (analog balanced signal inputs).
RDIN3	190	I	–	
TDOP3	187	O	–	Transmit data outputs to circuit #3 (analog balanced signal outputs).
TDON3	186	O	–	
RDIP4	201	I	–	Receive data inputs from circuit #4 (analog balanced signal inputs).
RDIN4	200	I	–	
TDOP4	197	O	–	Transmit data outputs to circuit #4 (analog balanced signal outputs).
TDON4	196	O	–	
RDIP5	3	I	–	Receive data inputs from circuit #5 (analog balanced signal inputs).
RDIN5	2	I	–	
TDOP5	207	O	–	Transmit data outputs to circuit #5 (analog balanced signal outputs).
TDON5	206	O	–	

1.3 UTOPIA Interface

Pin Name	Pin No.	I/O	Active Level	Function
RxDATA0-RxDATA7	69, 68, 66, 65, 63, 62, 60, 59	O Tristate	–	8-bit data bus used for receive data output to the ATM layer device. Data is output in sync with the positive-going edge of RxCLK.
RxCLK	71	I	–	Input pin of the clock for receive data transfer to the ATM layer device.(Max. 40 MHz)
RxSOC	81	O Tristate	H	Receive cell start address signal output, which outputs the signal for informing the ATM layer device of the start byte position of the receive cell. The start byte position is that position where RxSOC = 1.
RxENB_B	84	I	L	RxDATA0-RxDATA7 and RxSOC output enable signal input. When 0 is input, outputs RxDATA0-RxDATA7 and RxSOC are enabled.
RxADDR0-RxADDR4	80, 77, 76, 74, 73	I	–	Input pins for the signal indicating the address of the μPD98408.
RxCLAV	83	O Tristate	H	Cell receive available signal output. Becomes 1 when the μPD98408 has an output cell.
TxDATA0-TxDATA7	97, 96, 94, 93, 91, 90, 88, 87	I	–	8-bit data bus used for transmit data input to the ATM layer device. Data is input in sync with the positive-going edge of TxCLK.
TxCLK	99	I	–	Input pin of the clock for the transmit data transfer to the ATM layer device. (Max. 40 MHz)
TxSOC	109	I	H	Transmit cell start address signal input, which inputs the signal indicating the start byte position of the transmit cell input from the ATM layer device. The start byte position is that position where TxSOC = 1.
TxENB_B	112	I	L	Transmit enable signal input, which inputs a signal indicating that the ATM layer device is outputting valid transmit data at TxDATA0-TxDATA7. 0 for enable and 1 for disable.
TxADDR0-TxADDR4	108, 107, 103, 102, 101	I	–	Input pins of the signal indicating the address of the μPD98408 which transmits data
TxCLAV	111	O Tristate	H	Cell transmit available signal output. Goes to 1 when the μPD98408 is ready to receive a cell.

1.4 CPU Interface

Pin Name	Pin No.	I/O	Active Level	Function
BUSMODE	141	I	–	Selects the CPU interface operation mode. 0: <DS_B, RW_B, DTACK_B> style (Motorola compatible) 1: <RD_B, WR_B, RDY_B> style (Intel compatible)
DATA0-DATA7	125, 124, 122, 121, 119, 118, 116, 115	I/O	–	Used to transfer data between the CPU and an internal register (8-bit). The MSB is DATA7.
ADDR0-ADDR5	134, 133, 132, 129, 128, 127	I	–	Used to set the address of an internal register (6-bit).
SEL_ B	138	I	L	Register access enable signal. 0 for enable.
DS_B/RD_B	140	I	L/L	• When BUSMODE = 0, becomes the data strobe signal (DS_B) of the Motorola-compatible interface. In read cycle: DS_B = 0 for read data enable. In write cycle: DS_B = 0 for write data strobe. • When BUSMODE = 1, becomes the read instruction signal of the Intel-compatible interface. RD_B = 0 for read instruction.
RW_B/WR_B	139	I	L/L	• When BUSMODE = 0, becomes the read/write control signal (RW_B) of the Motorola-compatible interface. 0: Write cycle 1: Read cycle • When BUSMODE = 1, becomes the write instruction signal of the Intel-compatible interface. WR_B = 0 for write instruction.
DTACK_B/RDY_B	137	O	L/L	• When BUSMODE = 0, becomes the data acknowledge signal (DTACK_B) of the Motorola-compatible interface. This signal indicates the completion of data transmission over the data bus. DTACK_B is set to 0 upon the completion of data transmission. • When BUSMODE = 1, becomes the ready signal (RDY_B) of the Intel-compatible interface. This signal indicates the completion of data transmission over the data bus. RDY_B is set to 0 upon the completion of data transmission.
INT_B	136	O	L	Notifies the CPU of the occurrence of an interrupt factor.

1.5 Other Pins

(1/3)

Pin Name	Pin No.	I/O	Active Level	Function
JDI/TCLK0	28	I	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (JDI): JTAG boundary scan data input pin. • When PMDONLY = 1 (TCLK0): Input pin for transmit clock for the PMD transmitter (Circuit 0).
JDO/ RDATA0	36	O	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (JDO): JTAG boundary scan data output pin. • When PMDONLY = 1 (RDATA0): Output pin for data received from the PMD receiver (Circuit 0).
JCK/TCLK1	29	I	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (JCK): JTAG boundary scan clock input pin. • When PMDONLY = 1 (TCLK1): Input pin for transmit clock for the PMD transmitter (Circuit 1).
JMS/TCLK2	30	I	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (JMS): JTAG boundary scan mode select signal input pin. • When PMDONLY = 1 (TCLK2): Input pin for transmit clock for the PMD transmitter (Circuit 2).
JRST_B/ TCLK3	32	I	L/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (JRST_B): JTAG boundary scan reset signal input pin. • When PMDONLY = 1 (TCLK3): Input pin for transmit clock for the PMD transmitter (Circuit 3).

★ **Remark** About the treatment of JTAG boundary scan pins for normal operation

A pulse input to the RESET_B pin does not reset the JTAG logic.

If the JTAG logic has not been reset, the μPD98408 may not operate normally. Either of the following two methods can be used to reset the JTAG logic. If the JRST_B pin is not connected to a ground, be sure to reset the JTAG logic, using either method, after the power is switched on.

- Resetting the JTAG logic without using the JRST_B pin
  Use the JMS and JCK pins to reset the JTAG logic and keep it reset (with the JRST_B pin pulled up).
  Fix the JMS pin at 1 (pulled up), and input five or more clock cycles to the JCK pin.

- Using the JRST_B pin to reset the JTAG logic
  If a low pulse is input to the JRST_B pin, and the JMS and JRST_B pins are pulled up and kept at a high level, the JTAG logic is kept reset, so it does not affect normal operations. As for the JDI and JCK pins, keep the input level pulled down or up.

(2/3)

Pin Name	Pin No.	I/O	Active Level	Function
IC/TCLK4	33	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TCLK4): Input pin for transmit clock for the PMD transmitter (Circuit 4).
IC/TCLK5	34	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TCLK5): Input pin for transmit clock for the PMD transmitter (Circuit 5).
RECCLK/ RDATA1	37	O	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (RECCLK): Output pin for the recovery clock on the receive data. The recovery clock of circuit 0 is output. • When PMDONLY = 1 (RDATA1): Output pin for data received from the PMD receiver (Circuit 1).
IC/RDATA3	40	O	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (RDATA3): Output pin for data received from the PMD receiver (Circuit 3).
IC/RDATA2	38	O	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (RDATA2): Output pin for data received from the PMD receiver (Circuit 2).
IC/ RCLK0- RCLK5	19, 20, 21, 23, 24, 25	O/I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to these pins. • When PMDONLY = 1 (RCLK0-RCLK5): Output pins for the clock received from the PMD receiver (Circuits 0 to 5).
IC/TDATA0	44	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TDATA0): Input pin for transmit data for the PMD transmitter (Circuit 0).
IC/RDATA4	41	O	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (RDATA4): Output pin for the data received from the PMD receiver (Circuit 4).

(3/3)

Pin Name	Pin No.	I/O	Active Level	Function
IC/RDATA5	42	O	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (RDATA5): Output pin for the data received from the PMD receiver (Circuit 5).
IC/TDATA1	45	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TDATA1): Input pin for transmit data for the PMD transmitter (Circuit 1).
IC/TDATA2	46	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TDATA2): Input pin for transmit data for the PMD transmitter (Circuit 2).
IC/TDATA3	48	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TDATA3): Input pin for transmit data for the PMD transmitter (Circuit 3).
IC/TDATA4	49	I (with pull-down resistor)	–/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (IC): No signal should be connected to this pin. • When PMDONLY = 1 (TDATA4): Input pin for transmit data for the PMD transmitter (Circuit 4).
SIN/TDATA5	50	I (with pull-down resistor)	H/–	Two pin functions can be selected according to the level of the PMDONLY pin. • When PMDONLY = 0 (SIN): X_8 command transmit timing signal input pin. • When PMDONLY = 1 (TDATA5): Input pin for transmit data for the PMD transmitter (Circuit 5).
SOUT	54	O	H	X_8 command receive timing signal output pin.
PMDONLY	18	I (with pull-down resistor)	–	Specifies the mode of the μPD98408: whether it is operated as PMD + TC or as PMD only. 0: Operation as PMD + TC. 1: Operation as PMD only.
TCLOCK	57	I	–	Transmit clock (32 MHz) input pin
RESET_B	55	I	L	Input pin for the reset signal for the entire μPD98408.
IC	5, 6, 14, 15, 85, 144, 145	–	–	No signal should be connected to these pins.
CG	113	I	–	Should be connected to GND for normal use.

1.6 Handling Unused Pins

Pin Name	I/O	Recommended Connection When Not in Use
RDIP0-RDIP5	I	Pull up with a resistor (1 kΩ).
RDIN0-RDIN5	I	Pull up with a resistor (1 kΩ).
TDOP0-TDOP5	O	Open.
TDON0-TDON5	O	Open.
JDI/TCLK0	I	Pull up with a resistor.
JDO/RDATA0	O	Open.
JCK/TCLK1	I	Pull up with a resistor.
JMS/TCLK2	I	Pull up with a resistor.
JRST_B/TCLK3	I	Pull up with a resistor.
IC/TCLK4	I (with pull-down resistor)	Open.
IC/TCLK5	I (with pull-down resistor)	Open.
RECCLK/RDATA1	O	Open.
IC/RDATA3	O	Open.
IC/RDATA2	O	Open.
IC/RCLK0-IC/RCLK5	I/O (with pull-down resistor)	Open.
IC/TDATA0	I (with pull-down resistor)	Open.
IC/RDATA4	O	Open.
IC/RDATA5	O	Open.
IC/TDATA1	I (with pull-down resistor)	Open.
IC/TDATA2	I (with pull-down resistor)	Open.
IC/TDATA3	I (with pull-down resistor)	Open.
IC/TDATA4	I (with pull-down resistor)	Open.
SIN/TDATA5	I (with pull-down resistor)	Open.
SOUT	O	Open.
PMDONLY	I (with pull-down resistor)	Open.

1.7 Pin States at Reset

Pin Name	I/O	Pin States at Reset
TDOP0-TDOP5	O	Not defined
TDON0-TDON5	O	Not defined
RxDATA0-RxDATA7	Tristate O	Hi-Z
RxSOC	Tristate O	Hi-Z
RxCLAV	Tristate O	Hi-Z
TxCLAV	Tristate O	Hi-Z
DATA0-DATA7	I/O	Hi-Z
DTACK_B/RDY_B	O	High level
INT_B	O	High level
JDO/RDATA0	O	Not defined
RECCLK/RDATA1	O	Not defined
SOUT	O	Low level

2. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I		–0.5 to +6.6	V
Output voltage	V_O		–0.5 to +6.6	V
Output current	I_{O1}	**Note 1**	10	mA
	I_{O2}	**Note 2**	30	mA
Storage temperature	T_{stg}		–65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Notes 1. Applies to pins JDO/RDATA0, RECCLK/RDATA1, IC/RDATA2, IC/RDATA3, IC/RDATA4, IC/RDATA5, SOUT, and IC/RCLK0-IC/RCLK5.

2. Applies to pins RxDATA0-RxDATA7, RxSOC, RxCLAV, TxCLAV, INT_B, DTACK_B/RDY_B, and DATA0-DATA7.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		3.135	3.3	3.465	V
High-level input voltage	V_{IH}		2.0	–	5.5	V
Low-level input voltage	V_{IL}		0	–	0.8	V
Operating ambient temperature	T_A		–40	–	+85	°C

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3.3 V ± 5 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_L	$V_I = V_{DD}$ or GND	–	–	2	μA
High-level output current	I_{OH1}	V_{OH} = 2.4 V **Note 1**	–3.0	–	–	mA
	I_{OH2}	V_{OH} = 2.4 V **Note 2**	–8.0	–	–	mA
Low-level output current	I_{OL1}	V_{OL} = 0.4 V **Note 1**	3.0	–	–	mA
	I_{OL2}	V_{OL} = 0.4 V **Note 2**	9.0	–	–	mA
High-level output voltage	V_{OH1}	I_{OH} = 0 mA **Note 3**	V_{DD} – 0.4	–	–	V
	V_{OH2}	I_{OH} = 0 mA When **Note 3** is not applied	V_{DD} – 0.2	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 0 mA	–	–	0.1	V
★ Supply current	I_{DD}	In operation **Note 4**	–	330	460	mA

Notes 1. Applies to pins JDO/RDATA0, RECCLK/RDATA1, IC/RDATA2, IC/RDATA3, IC/RDATA4, IC/RDATA5, SOUT, and IC/RCLK0-IC/RCLK5.

2. Applies to pins RxDATA0-RxDATA7, RxSOC, RxCLAV, TxCLAV, INT_B, DTACK_B/RDY_B, and DATA0-DATA7.

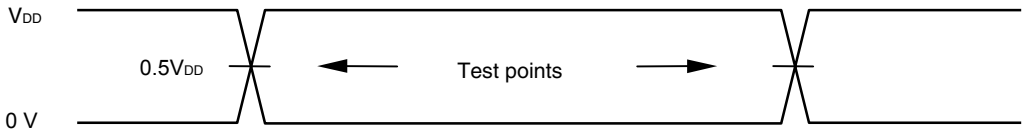
3. Applies to pins IC/RCLK0-IC/RCLK5 only when 1 is input to the PMDONLY pin (only PMD operates).

★ 4. Power consumption when resistors and magnetic module components are connected to the UTP interface pins (TDOPn/TDONn, RDIPn/RDINn) (refer to **SYSTEM CONFIGURATION EXAMPLE (CONNECTION WITH MAGNETICS)**).

CAPACITANCE

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	Frequency = 1 MHz	–	10	20	pF
Output capacitance	C_O	Frequency = 1 MHz	–	10	20	pF
I/O capacitance	C_{IO}	Frequency = 1 MHz	–	10	20	pF

AC Test I/O Waveform

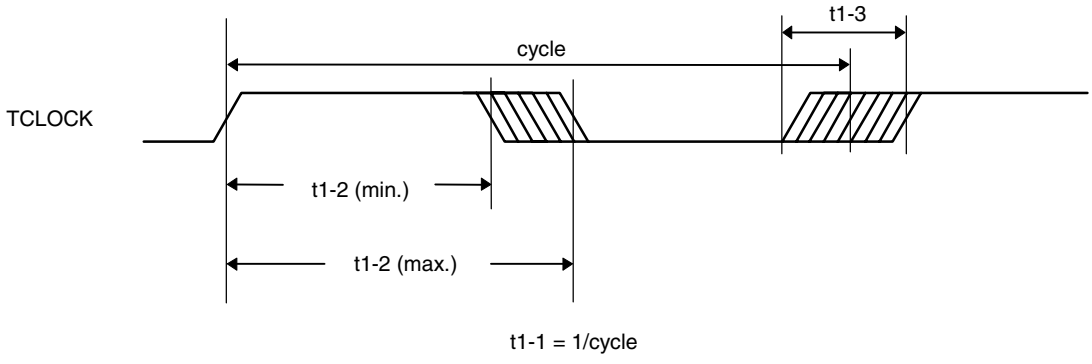


AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3.3 V ± 5 %)

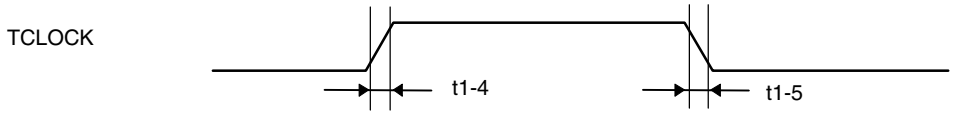
TCLOCK

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCLOCK frequency	t1-1		–	32	–	MHz
TCLOCK duty	t1-2		40	–	60	%
TCLOCK frequency accuracy	t1-3		–	–	100	ppm
TCLOCK rise time	t1-4	Measurement of 10 to 90 % transition time	–	–	5	ns
TCLOCK fall time	t1-5	Measurement of 10 to 90 % transition time	–	–	5	ns

TCLOCK Input



t1-1 = 1/cycle

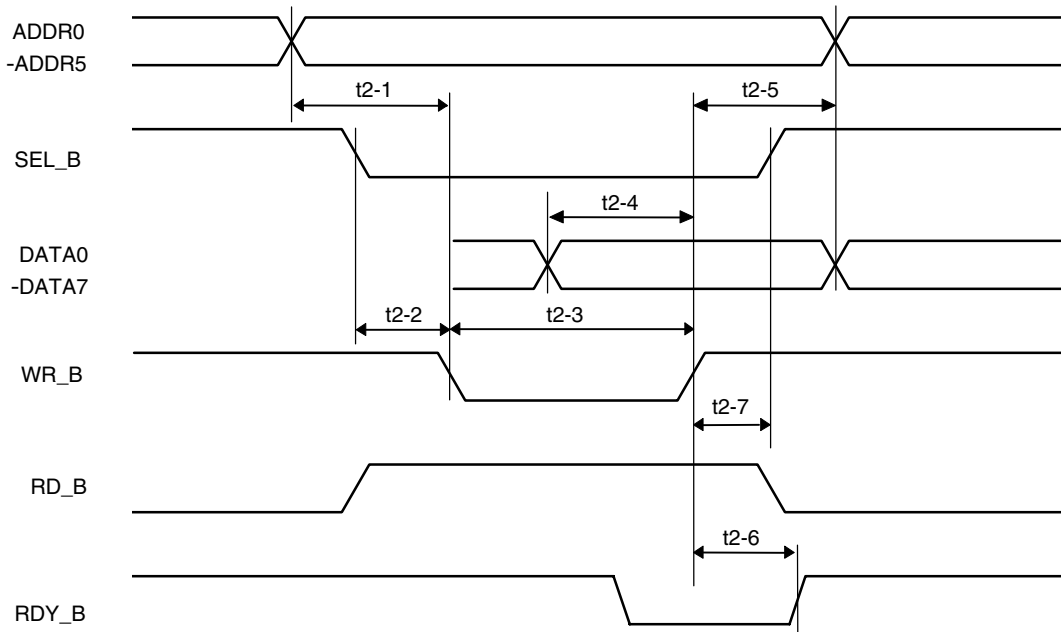


CPU INTERFACE

(1) Write operation (when BUSMODE = 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to WR_B↓)	t2-1		10	–	–	ns
SEL_B setup time (referred to WR_B↓)	t2-2		5	–	–	ns
WR_B pulse width	t2-3		50	–	–	ns
DATA setup time (referred to WR_B↑)	t2-4		16	–	–	ns
ADDR/DATA hold time (referred to WR_B↑)	t2-5		4	–	–	ns
RDY_B disable time (referred to WR_B↑)	t2-6		–	–	10	ns
SEL_B hold time (referred to WR_B↑)	t2-7		0	–	–	ns

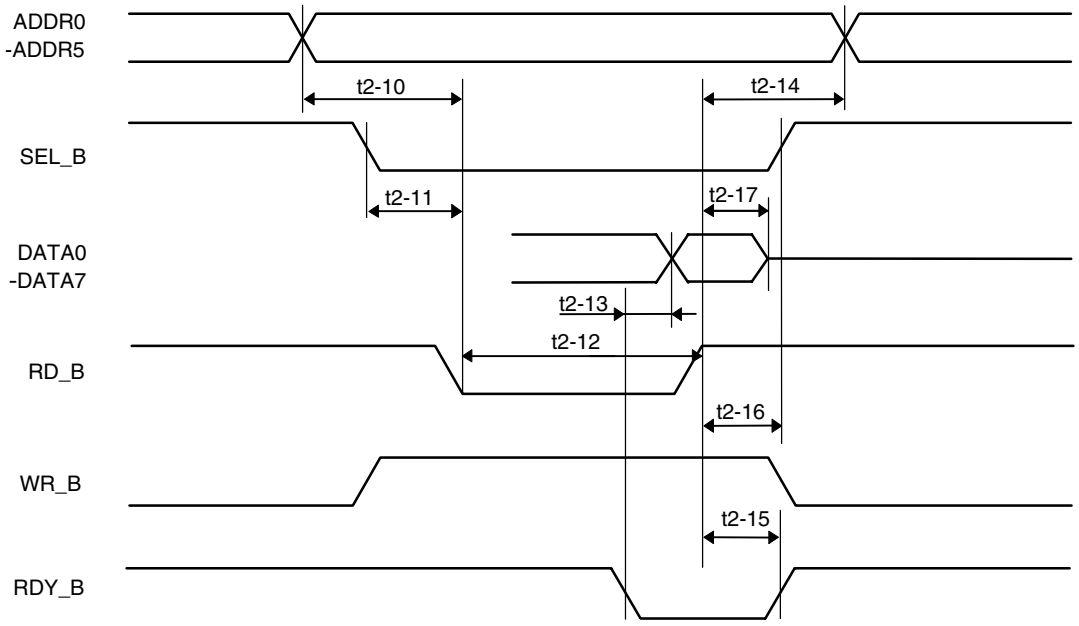
CPU Interface Write Operation (BUSMODE = 1)



(2) Read operation (when BUSMODE = 1)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to RD_B↓)	t2-10		10	–	–	ns
SEL_B setup time (referred to RD_B↓)	t2-11		5	–	–	ns
RD_B pulse width	t2-12		50	–	–	ns
DATA fixed time (referred to RDY_B↓)	t2-13		–	–	10	ns
ADDR hold time (referred to RD_B↑)	t2-14		4	–	–	ns
RDY_B disable time (referred to RD_B↑)	t2-15		–	–	10	ns
SEL_B hold time (referred to RD_B↑)	t2-16		0	–	–	ns
DATA invalid/tristate time (referred to RD_B↑)	t2-17		0	–	–	ns

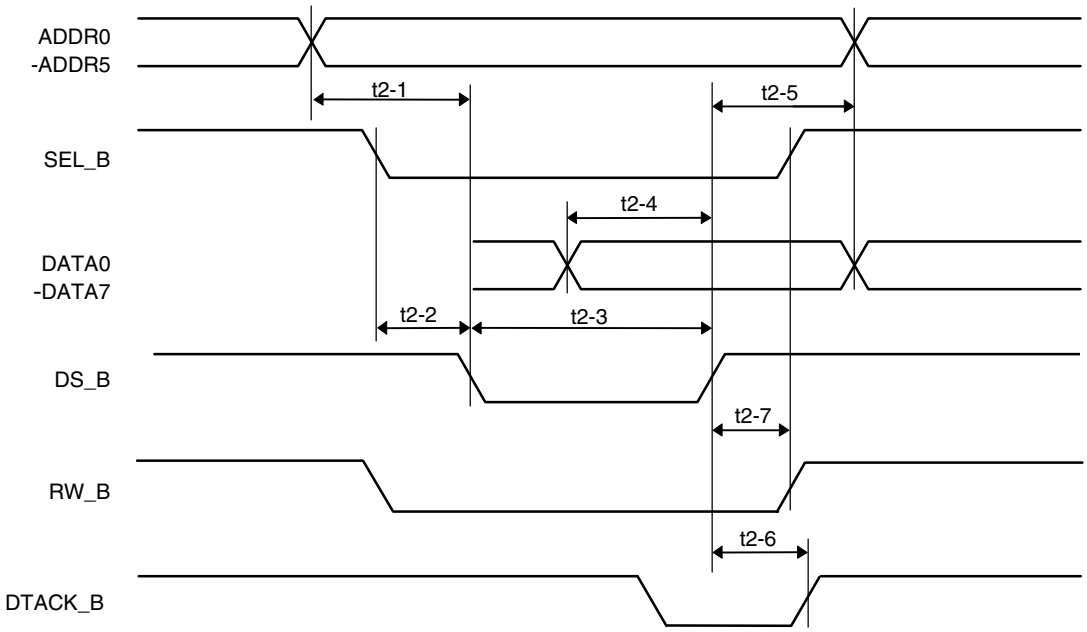
CPU Interface Read Operation (BUSMODE = 1)



(3) Write operation (when BUSMODE = 0)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to DS_B↓)	t2-1		10	–	–	ns
SEL_B or RW_B setup time (referred to DS_B↓)	t2-2		5	–	–	ns
DS_B pulse width	t2-3		50	–	–	ns
DATA setup time (referred to DS_B↑)	t2-4		15	–	–	ns
ADDR/DATA hold time (referred to DS_B↑)	t2-5		4	–	–	ns
DTACK_B disable time (referred to DS_B↑)	t2-6		–	–	10	ns
SEL_B or RW_B hold time (referred to DS_B↑)	t2-7		0	–	–	ns

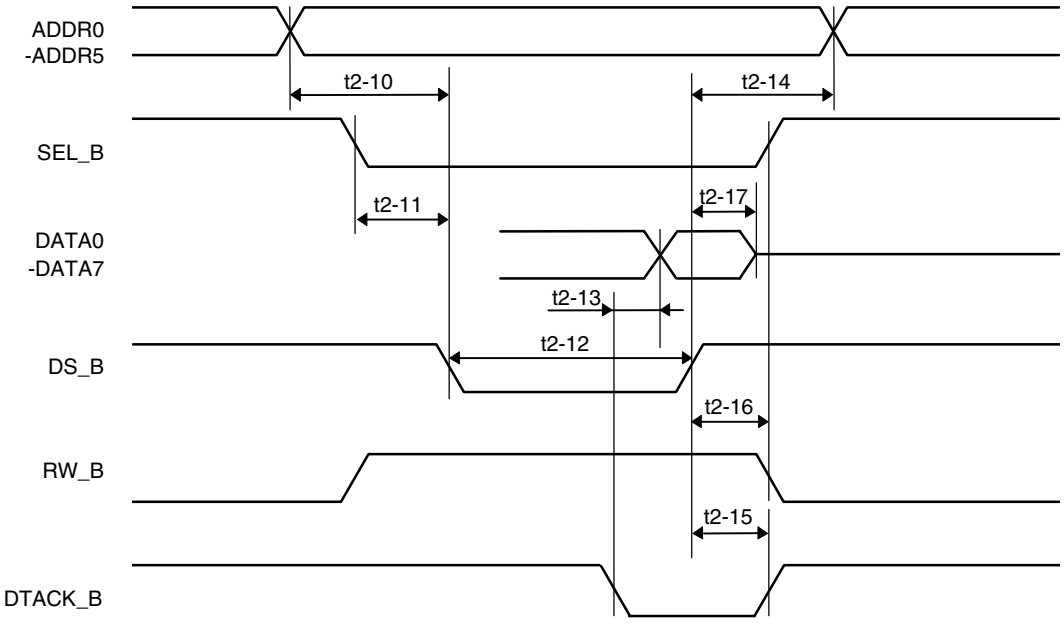
CPU Interface Write Operation (BUSMODE = 0)



(4) Read operation (when BUSMODE = 0)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADDR setup time (referred to DS_B↓)	t2-10		10	–	–	ns
SEL_B or RW_B setup time (referred to DS_B↓)	t2-11		5	–	–	ns
DS_B pulse width	t2-12		50	–	–	ns
DATA fixed time (referred to DTACK_B↓)	t2-13		–	–	10	ns
ADDR hold time (referred to DS_B↑)	t2-14		4	–	–	ns
DTACK_B disable time (referred to DS_B↑)	t2-15		–	–	10	ns
SEL_B or RW_B hold time (referred to DS_B↑)	t2-16		0	–	–	ns
DATA invalid/tristate time (referred to DS_B↑)	t2-17		0	–	–	ns

CPU Interface Read Operation (BUSMODE = 0)



UTOPIA INTERFACE

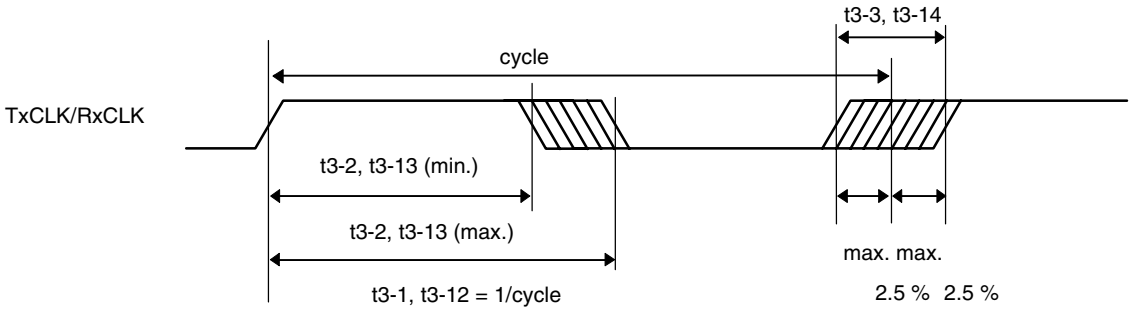
(1) Transmission

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TxCLK frequency	t3-1		0	–	40	MHz
TxCLK duty cycle	t3-2		40	–	60	%
TxCLK jitter (peak to peak)	t3-3		–	–	5	%
TxCLK rise time	t3-4	Measurement of 10 to 90 % transition time	–	–	3	ns
TxCLK fall time	t3-5	Measurement of 10 to 90 % transition time	–	–	3	ns
TxDATA[7:0], TxSOC, TxENB_B, or TxADDR[4:0] setup time	t3-6		8	–	–	ns
TxDATA[7:0], TxSOC, TxENB_B, or TxADDR[4:0] hold time	t3-7		1	–	–	ns
TxCLAV low-impedance delay time (referred to TxCLK↑)	t3-8		8	–	–	ns
TxCLAV high-impedance delay time (referred to TxCLK↑)	t3-9		0	–	–	ns
TxCLAV low-impedance delay time (referred to TxCLK↑)	t3-10		1	–	–	ns
TxCLAV high-impedance delay time (referred to TxCLK↑)	t3-11		1	–	–	ns

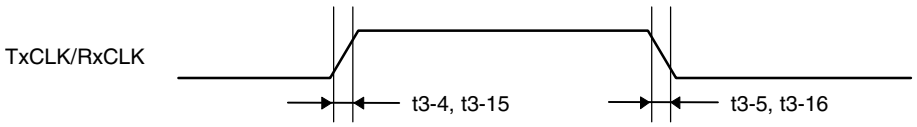
(2) Reception

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RxCLK frequency	t3-12		0	–	40	MHz
RxCLK duty cycle	t3-13		40	–	60	%
RxCLK jitter (peak to peak)	t3-14		–	–	5	%
RxCLK rise time	t3-15	Measurement of 10 to 90 % transition time	–	–	3	ns
RxCLK fall time	t3-16	Measurement of 10 to 90 % transition time	–	–	3	ns
RxENB_B or RxADDR[4:0] setup time	t3-17		8	–	–	ns
RxENB_B or RxADDR[4:0] hold time	t3-18		1	–	–	ns
RxDATA[7:0], RxSOC, or RxCLAV low-impedance delay time (referred to RxCLK↑)	t3-19		8	–	–	ns
RxDATA[7:0], RxSOC, or RxCLAV high-impedance delay time (referred to RxCLK↑)	t3-20		0	–	–	ns
RxDATA[7:0], RxSOC, or RxCLAV low-impedance delay time (referred to RxCLK↑)	t3-21		1	–	–	ns
RxDATA[7:0], RxSOC, or RxCLAV high-impedance delay time (referred to RxCLK↑)	t3-22		1	–	–	ns

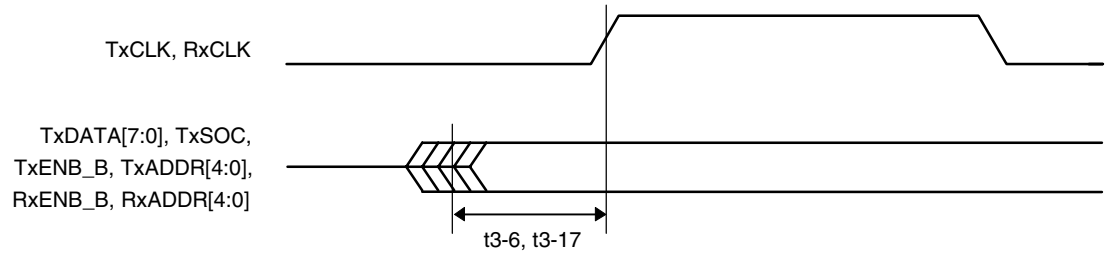
TxCLK or RxCLK Timing - 1



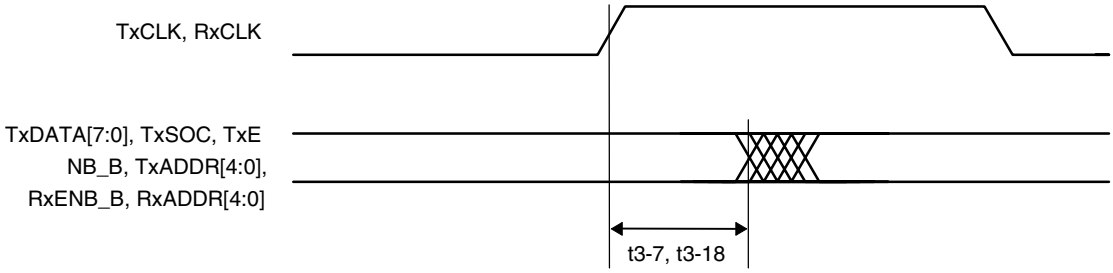
TxCLK or RxCLK Timing - 2



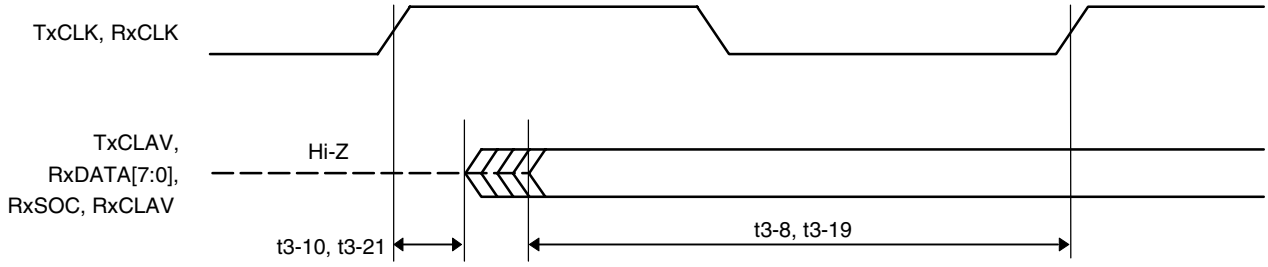
Input Signal Setup Timing



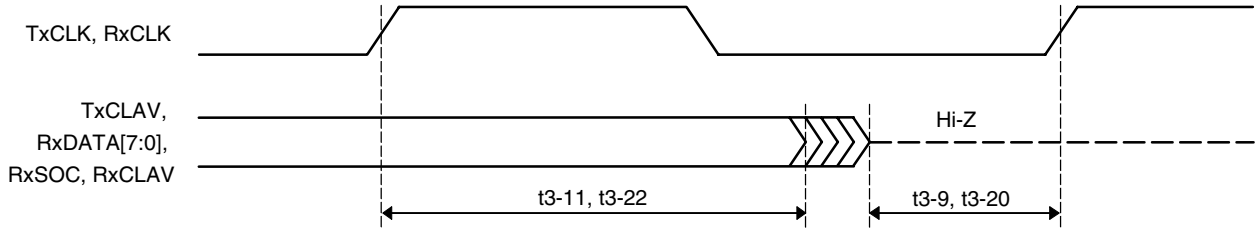
Input Signal Hold Timing



Output Delay Time - 1



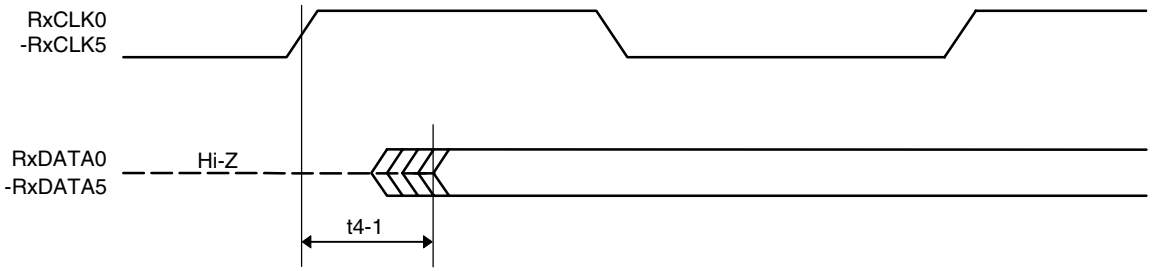
Output Delay Time - 2



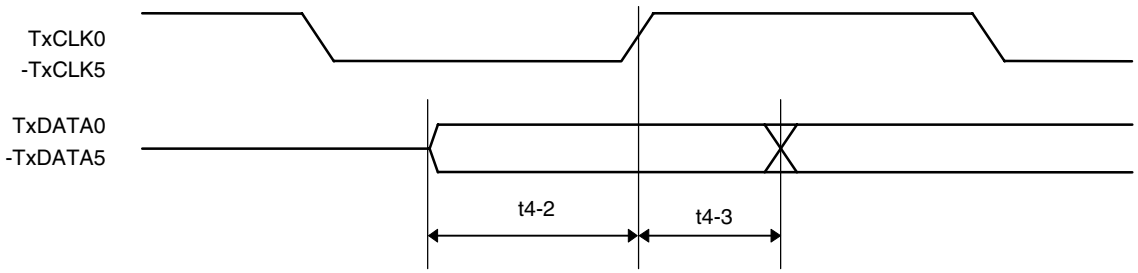
PMDONLY MODE

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RxDATA delay time (referred to RxCLK↑)	t4-1		0.5	–	15.0	ns
TxDATA setup time (referred to TxCLK↑)	t4-2		8.0	–	–	ns
TxDATA hold time (referred to TxCLK↑)	t4-3		0.5	–	–	ns

Reception Data Output Delay Time



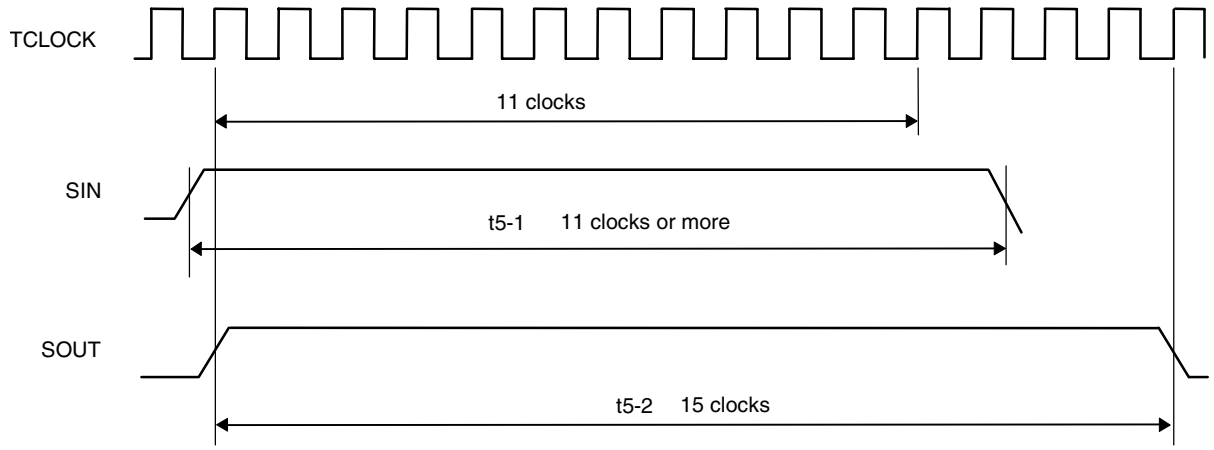
Transmission Data Setup/Hold Time



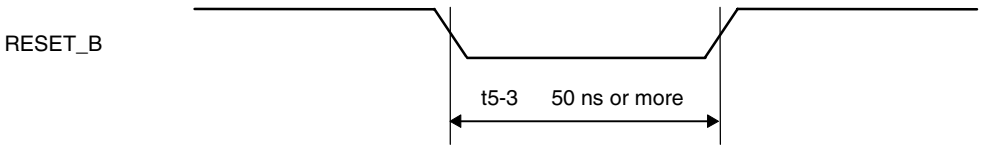
OTHERS

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIN pulse width	t5-1		11	–	–	TCLOCK clock
SOUT pulse width	t5-2		–	15	–	TCLOCK clock
RESET_B pulse width	t5-3		50	–	–	ns

SIN and SOUT Timings

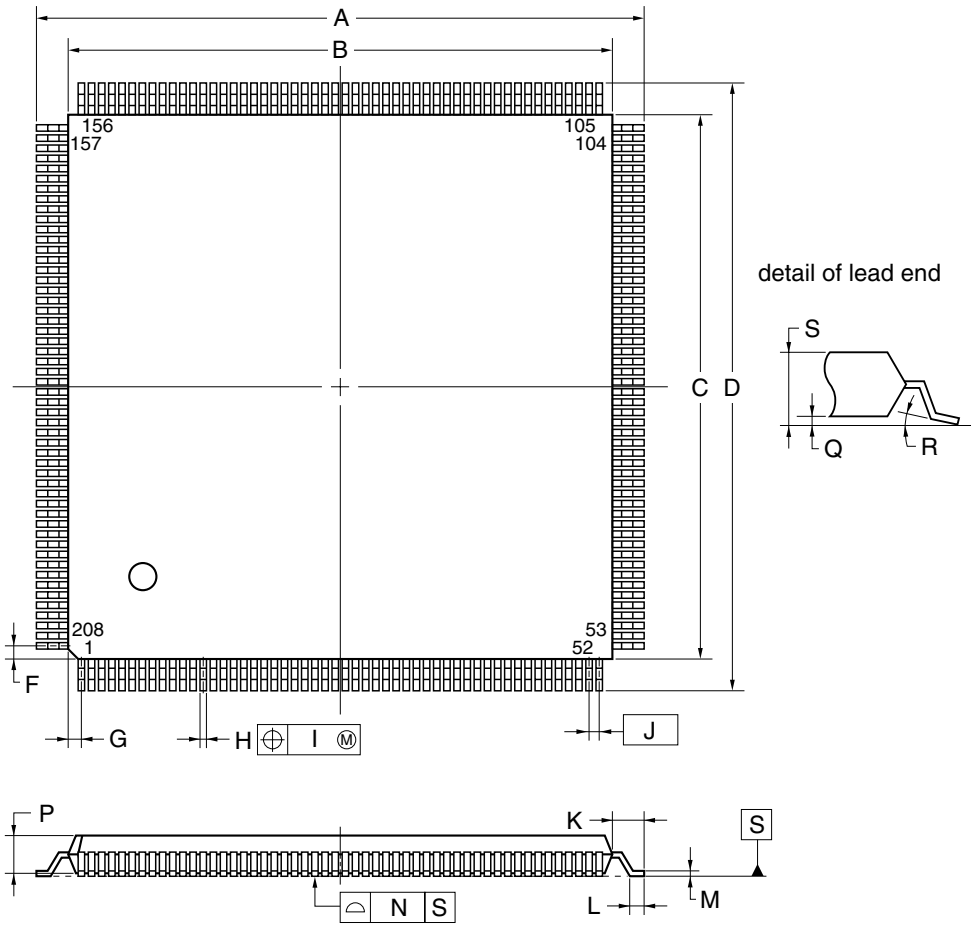


RESET_B Timing



★ 3. PACKAGE DRAWING

208-PIN PLASTIC QFP (FINE PITCH) (28x28)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	30.6±0.2
B	28.0±0.2
C	28.0±0.2
D	30.6±0.2
F	1.25
G	1.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.3±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	3.2±0.1
Q	0.4±0.1
R	5°±5°
S	3.8 MAX.

P208GD-50-LML,MML,SML,WML-7

4. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD98408.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Surface-Mount Type

- μPD98408GD-LML: 208-pin plastic QFP (fine pitch) (28 × 28)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (36 hours of pre-baking is required at 125 °C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	IR35-367-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days[Note] (36 hours of pre-baking is required at 125 °C afterward) <Caution> Non-heat-resistant trays, such as magazine and taping trays, cannot be baked before unpacking.	VP15-367-2
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	–

Note Maximum number of days during which the product can be stored at a temperature of 25 °C and a relative humidity of 65 % or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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