88SB2211

PCI Express-to-PCI Bridge

Datasheet

Doc. No. MV-S104870-U0, Rev. B
February 27, 2008, Preliminary

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.xx

For more information, visit our website at: www.marvell.com

88SB2211

PCI Express-to-PCI Bridge

Datasheet

Product Overview

The Marvell® 88SB2211 X1 PCI Express to 32-bit PCI bridge connects legacy PCI parallel bus devices to the new, advanced serial PCI Express interface. The 88SB2211 is a PCI Express-to-PCI forward and reverse bridge. It is fully compliant with the PCI-SIG PCI Express-to-PCI Bridge Specification.

Features

- **Marvell 88SB2211 X1 PCI Express to 32-bit PCI Bridge**
  - PCI Express-to-PCI/PCI-X Bridge Specification 1.0 compliant
  - Forward transparent bridge
  - Single PCI Express 1.0a X1 port
  - Single 32-bit PCI2.3 33 MHz port
  - Single TWSI port
  - Eight General Purpose I/O pins
  - Single 3.3V power supply
  - 64-bit addressing support
  - VGA and ISA addressing support for legacy operation
  - Adjustable read prefetch algorithm
  - Access to all internal registers from the PCI Express port (in Forward Bridge mode only)
  - IEEE Standard 1149.1 JTAG Interface
- **PCI Express Interface**
  - PCI Express Base Specifications, Revision 1.0a compliant
  - Integrated PCI Express PHY based on proven Marvell SERDES technology
  - X1 link width, at 2.5 GHz signaling
  - 100-MHz differential PCI Express reference clock generation, saving an external oscillator
  - Link CRC
  - Lane polarity reversal support
  - 128-byte Maximum Payload Size (MPS)
  - Single Virtual Channel (VC-0)
  - Advanced error reporting capability
  - Up to four master non-posted requests outstanding
  - Up to four target non-posted requests outstanding
  - Interrupt emulation message support
  - Error message support
- **PCI Interface**
  - PCI Local Bus Specifications, Revision 2.3 compliant
  - 32-bit, 33 MHz operation
  - 3.3V, 5V tolerant
  - Internal arbiter support for five external masters
  - PCI clock source for up to five external agents
  - Fast Back-to-Back capable
  - Up to four active target delayed reads
- **Power Management**
  - Advanced Configuration Power Interface Specifications (ACPI) compliant
  - Supports all device power management states: D0, D1, D2, D3Hot, and D3Cold
  - Supports D3Cold wake-up events upstream forwarding (PMEn/WAKEn)
- **Two Wire Serial Interface (TWSI) Port**
  - Optional EEPROM initialization
  - Internal register access
- **Forward Bridge Applications**
  - ATCA PCI Express based platforms
  - PCI extension for server, desktop, and mobile motherboards
  - ExpressCard and MiniCard applications
  - Split chassis platforms
  - PCI Express docking stations
- **Reverse Bridge Applications**
  - PICMG based platforms
  - PCI Express extensions for PCI platforms
  - PC-Card (PCMCIA) and Mini-PCI applications
- **LQFP128, 14 x 20 mm package, 0.5 mm pitch**

Table of Contents

List of Tables

List of Figures

Preface

About This Document

This datasheet provides the hardware specifications for the 88SB2211 PCI Express-to-PCI Bridge, including detailed pin information, configuration settings, electrical characteristics, and physical specifications. It also provides detailed definitions of the registers implemented in the device.

In this document the 88SB2211 is often referred to as the “device”.

Related Documents

- *88SB2211 Hardware Design Guidelines*, Document number MV-S300975-00[1].
- *PCI Local Bus Specification*, Revision 2.3
- *PCI Express Base Specification*, Revision 1.0a
- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0

1. Contact your local Marvell® sales representative for information about receiving this document.

Document Conventions

The following conventions are followed in this document:

Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Gb: gigabit GB: gigabyte Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Overview

The Marvell® 88SB2211 is a PCI Express-to-PCI bridge that connects legacy PCI parallel bus devices to the new advanced serial PCI Express interface. The 88SB2211 can also operate as a reverse bridge (PCI-to-PCI Express), enabling connection of PCI Express devices to the legacy PCI bus.

The 88SB2211 device is fully compliant with the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0, and supports a transparent forward or reverse bridging scheme. It is a single function bridge with a single PCI Express virtual channel (VC-0). It also supports the standard PCI-to-PCI bridge programming model.

The PCI Express port is fully compliant with the *PCI Express Base Specification*, Revision 1.0a. It supports an X1 link operation, allowing simultaneous 250 MBps throughput in the upstream and downstream directions. The PCI Express port contains an integrated PCI Express PHY, based on proven Marvell SERDES technology. For both downstream and upstream traffic, the 88SB2211 supports up to four outstanding non-posted requests. It supports a Maximum Payload Size (MPS) of 128 bytes, Advanced Error Reporting (AER) capability, lane polarity inversion for easy board routing, and advanced PCI Express Power Management (PM) features.

The PCI port is 32 bits wide and operates at 33 MHz. It is fully compliant with *PCI Local Bus Specification*, Revision 2.3. The 88SB2211 provides an internal arbiter and buffered clock outputs for up to five subordinate PCI devices. It supports 64-bit addressing, VGA and ISA addressing for legacy operation, and a tunable prefetch algorithm, which is useful for system throughput optimization.

Power management (PM) features include all conventional PCI D-states (software controlled), and PCI Express active state link PM mechanisms (hardware controlled). PME and Wake protocols are also supported, enabling the host system to further reduce power consumption.

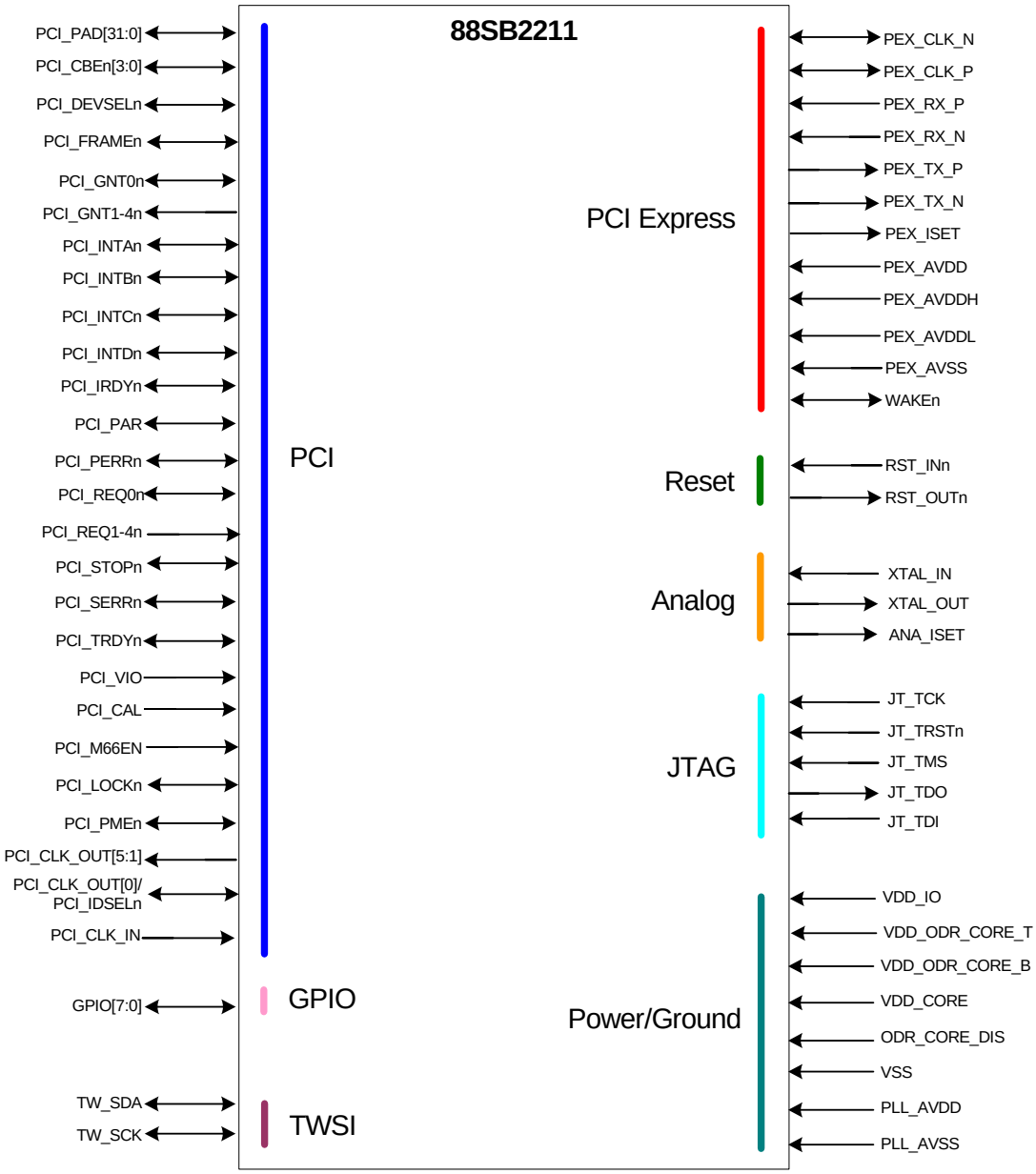
The 88SB2211 also contains a single TWSI port for optional initialization, a single IEEE Standard 1149.1 JTAG port for testability, and eight General Purpose I/O pins (GPIOs) for further system customization.

The 88SB2211 can operate from a single 3.3V power rail, to reduce system cost. This is achieved by various On Die Regulators (ODRs) embedded in the device. To further optimize the power consumption, the ODRs can be bypassed.

2 Pin Information

The 88SB2211 is available in a 128-pin, LQFP package. Figure 1 is the pin logic diagram for the device.

Figure 1: 88SB2211 Interface Pin Logic Diagram



2.1 Summary List of Functional Pins

Table 1 indicates the conventions used to identify I/O or O type pins and their pad type.

Table 1: Pin Assignment Table Conventions

Abbreviation	Description
I	Input
O	Output
I/O	Input/Output
t/s	Tri-State pin
s/t/s	Sustained Tri-State pin The pin is driven to its inactive value for one cycle before float. A pull-up is required to sustain the inactive value.
o/d	Open Drain pin The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
CML	Current Mode Logic
Analog	Analog Supply/Signal
Power	VDD Power Supply
GND	Ground Supply
PCI	• PCI pad 3.3V according to the PCI standard • 5V tolerant
HCSL	High-speed Current Steering Logic
Calib	I/O Calibration Pin

Table 2 lists the pin count for each interface in the LQFP package.

Table 2: Functional Pin List Summary

Interface	Prefix	Count LQFP Package
PCI Express	PEX_	12
PCI	PCI_	70
Reset	RST_	2
TWSI	TW_	2
JTAG	JT_	5
GPIO	GPIO	8
VDD_IO	-	16
VDD_CORE	-	2

Table 2: Functional Pin List Summary (Continued)

Interface	Prefix	Count LQFP Package
VDD_ODR_CORE_T	-	1
VDD_ODR_CORE_B	-	1
ODR_CORE_DIS	-	1
PLL_AVDD	-	1
PLL_AVSS	-	1
Analog	-	3
Ground (VSS)	-	3
NC (Not Connected)	-	0
Total		128

2.2 PCI Express Interface Pin Assignments

Table 3: PCI Express Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
PEX_CLK_P PEX_CLK_N	I/O	HSCL	PCI Express Reference Clock Differential pair of PCI Express 100 MHz reference clock. The PCI Express clock direction is determined according to the reset strapping (see Clock Mode Select in Table 12, Reset Configuration, on page 23).
PEX_RX_P PEX_RX_N	I	CML	PCI Express Receive Lane Differential pair of PCI Express receive data.
PEX_TX_P PEX_TX_N	O	CML	PCI Express Transmit Lane Differential pair of PCI Express transmit data.
PEX_ISET	O	Analog	PCI Express Current Reference Connect to an external 6.04+/-1% kΩ resistor.
PEX_AVDD	I	Power	Connect this pin to a decoupling capacitor. **NOTE:** When ODR is bypassed (see GPIO[3] in Table 12, Reset Configuration, on page 23), this pin is the PCI Express PHY 2.5V analog power supply.
PEX_AVDDH	I	Power	PCI Express PHY Filtered Power Supply (3.3V)
PEX_AVDDL	I	Power	Connect this pin to a decoupling capacitor. **NOTE:** When ODR is bypassed (see GPIO[2] in Table 12, Reset Configuration, on page 23), this pin is the PCI Express PHY 1.5V analog power supply.
PEX_AVSS	I	Ground	PCI Express PHY Ground
WAKEn	o/d I/O	PCI	PCI Express Wake (WAKE#) When working in Forward Bridge mode, this signal is an output. When working in Reverse Bridge mode, this signal is an input.

2.3 PCI 32-bit Interface Pin Assignments

Table 4: PCI 32-bit Bus Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
PCI_VIO	I	PCI	PCI Voltage I/O Clamping reference voltage for PCI (3.3V or 5V).
PCI_M66EN	I	PCI	PCI 66 MHz Enable The 88SB2211 does not support 66 MHz PCI. Therefore, pull this pin down to 0.
PCI_PAD[31:0]	t/s I/O	PCI	PCI Address/Data 32-bit PCI multiplexed address/data bus. Driven by the transaction master during the address phase and the write data phase. Driven by the target device during the read data phase.
PCI_CBEn[3:0]	t/s I/O	PCI	PCI Command/Byte Enable A multiplexed command/byte-enable bus, driven by the transaction master. Contains the command during the address phase, and the byte-enable during data phase.
PCI_PAR	t/s I/O	PCI	PCI Parity Even parity is calculated for PCI_PAD[31:0] and PCI_CBEn[3:0]. Driven by the transaction master for the address phase and the write data phase. This pin is driven by the target for the read data phase.
PCI_FRAMEn	s/t/s I/O	PCI	PCI Frame Asserted by the transaction master to indicate the beginning of a transaction. The master de-asserts PCI_FRAMEn to indicate that the next data phase is the final data phase transaction.
PCI_DEVSELn	s/t/s I/O	PCI	PCI Device Select Asserted by the target of the current access. As a master, the target device is expected to assert PCI_DEVSELn within five bus cycles. Otherwise, it aborts the cycle. As a target, PCI_DEVSELn is asserted at a medium speed; two cycles after the assertion of PCI_FRAMEn.
PCI_IRDYn	s/t/s I/O	PCI	PCI Initiator Ready Asserted by the transaction master to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI_TRDYn and PCI_IRDYn are asserted.
PCI_TRDYn	s/t/s I/O	PCI	PCI Target Ready Asserted by the target to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI_TRDYn and PCI_IRDYn are asserted.
PCI_STOPn	s/t/s I/O	PCI	PCI Stop Asserted by target to indicate transaction termination. Used by a target device to generate a Retry, Disconnect, or Target Abort termination signal.

Table 4: PCI 32-bit Bus Interface Pin Assignments (Continued)

Pin Name	I/O / Pin Type		Description
PCI_REQ0n PCI_REQ1n PCI_REQ2n PCI_REQ3n PCI_REQ4n	I/O I I I I	PCI	PCI Bus Request When the internal PCI Arbiter is used, these pins are used as the request inputs from the external agents. When an external arbiter is used, PCI_REQ0n is used as the REQn output of the bridge.
PCI_GNT0n PCI_GNT1n PCI_GNT2n PCI_GNT3n PCI_GNT4n	t/s I/O t/s O t/s O t/s O t/s O	PCI	PCI Bus Grant When the internal PCI Arbiter is used, these pins are used as the grant outputs for the external agents. When an external arbiter is used, PCI_GNT0n is used as the GNTn input of the bridge.
PCI_PERRn	s/t/s I/O	PCI	PCI Parity Error Asserted when a data parity error is detected. Asserted by a target device in response to bad address or write data parity, or by the master device in response to bad read data parity.
PCI_SERRn	o/d I/O	PCI	PCI System Error Asserted when a system error is detected.
PCI_LOCKn	I/O	PCI	PCI Lock
PCI_PMEn	o/d I/O	PCI	PCI Power Management Event
PCI_CLK_OUT[0] PCI_IDSELn	O I	PCI	PCI Clock Output/PCI IDSEL **NOTE:** In Reverse Bridge mode, PCI_CLK_OUT[0] acts as the device PCI_IDSELn pin (input).
PCI_CLK_OUT[5:1]	O	PCI	PCI Clock Output
PCI_CLK_IN	I	PCI	PCI Clock Input
PCI_INTAn	o/d I/O	PCI	PCI Interrupt Request A
PCI_INTBn	o/d I/O	PCI	PCI Interrupt Request B
PCI_INTCn	o/d I/O	PCI	PCI Interrupt Request C
PCI_INTDn	o/d I/O	PCI	PCI Interrupt Request D
PCI_CAL	I	Calib	PCI Pads Calibration Input (Refer to the *88SB2211 Hardware Design Guidelines* for a description of the pin connectivity).

2.4 Reset Pin Assignments

Table 5: Reset Pin Assignments

Pin Name	I/O / Pin Type		Description
RST_INn	I	PCI	Reset In • When working in Forward Bridge mode, this is the PCI Express reset input signal (PERST#). • When working in Reverse Bridge mode, this is the PCI reset input signal (PRST#).
RST_OUTn	O	PCI	Reset Out • When working in Forward Bridge mode, this is the PCI reset output signal. • When working in Reverse Bridge mode, this is the PCI Express reset output signal.

2.5 TWSI Interface Pin Assignments

Table 6: TWSI Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
TW_SDA	o/d I/O	PCI	TWSI Port Serial Data Address or write data driven by the TWSI master or read response data driven by the TWSI slave. **NOTE:** The 88SB2211 slave address is 7'h2F (7'b0101111). Since this pin contains and internal pull-up, it can be left unconnected when not used. If used, it requires an external pull-up.
TW_SCL	o/d I/O	PCI	TWSI Port Serial Clock Serves as output when acting as a TWSI master. Serves as input when acting as a TWSI slave. **NOTE:** Since this pin contains and internal pull-up, it can be left unconnected when not used. If used, it requires an external pull-up.

2.6 JTAG Interface Pin Assignments

Table 7: JTAG Pin Assignments

Pin Name	I/O / Pin Type		Description
JT_TCK	I	PCI	JTAG Clock Clock input for the JTAG controller. **NOTE:** This pin is internally pulled down to 0.
JT_TRSTn	I	PCI	JTAG Reset When asserted, resets the JTAG controller. **NOTE:** This pin is internally pulled down to 0.[1]
JT_TMS	I	PCI	Core JTAG Mode Select Controls the Core JTAG controller state. Sampled with the rising edge of JT_TCK. **NOTE:** This pin is internally pulled up to 1.
JT_TDO	O	PCI	JTAG Data Out Driven on the falling edge of JT_TCK.
JT_TDI	I	PCI	JTAG Data In JTAG serial data input. Sampled with the JT_TCK rising edge. **NOTE:** This pin is internally pulled up to 1.

1. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP can be reset by driving the JT_TMS signal HIGH for five JT_TCK cycles.

2.7 GPIO Interface Pin Assignments

Table 8: GPIO Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
GPIO[7:0]	t/s I/O	PCI	General Purpose Pin Various functions

2.8 Analog Interface Pin Assignments

Table 9: Analog Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
XTAL_IN	I	Analog	Crystal Input/Reference Clock Input 25 MHz. When using a crystal, this pin is used as the XTAL_IN input. **NOTE:** When not using crystal, this pin must be pulled down to 0.
XTAL_OUT	O	Analog	Crystal Output **NOTE:** Leave unconnected if a crystal is not used.
ANA_ISET	O	Analog	Current Reference Connect to an external 6.04 kΩ resistor.

2.9 Power/Ground Pin Assignments

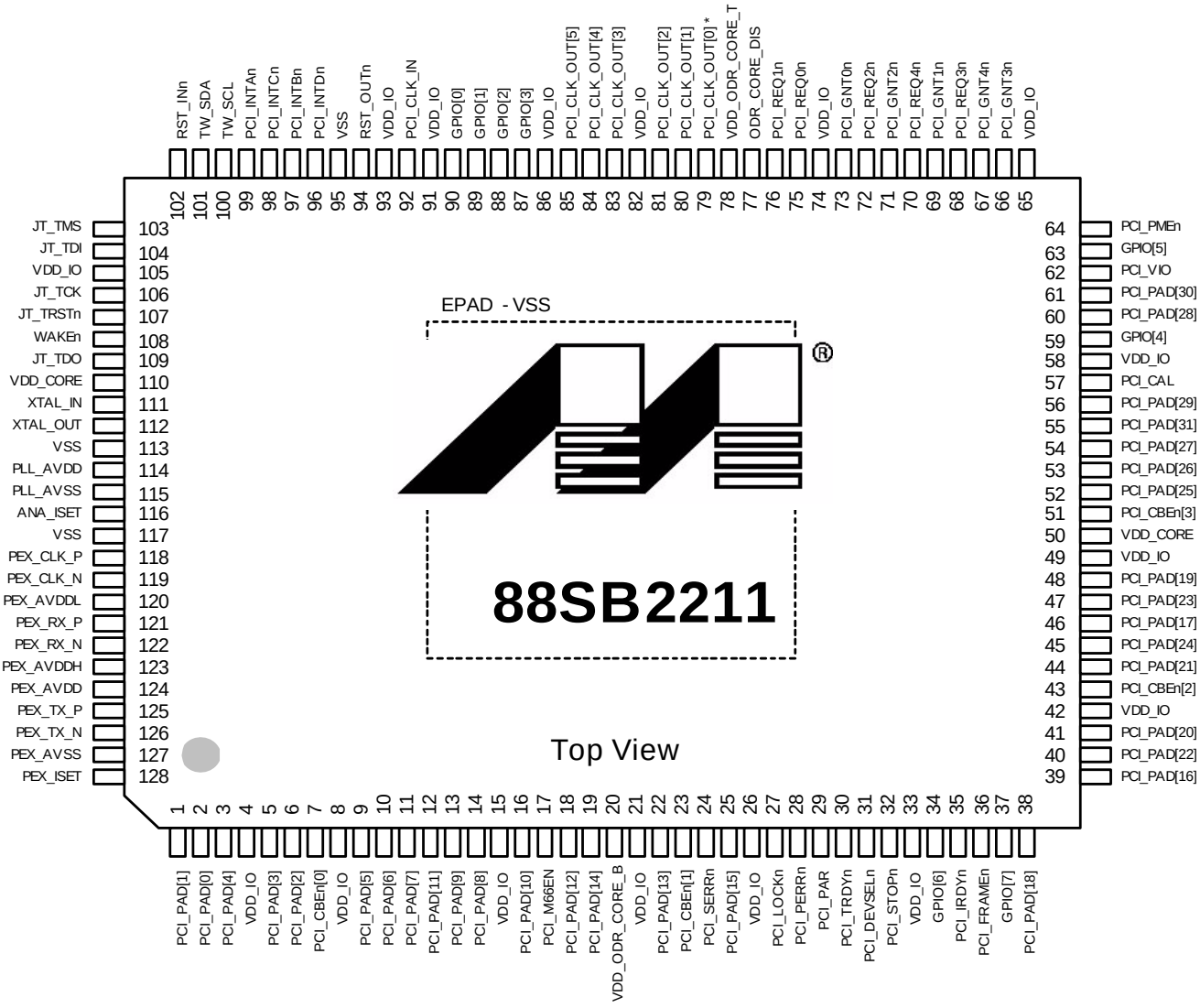
Table 10: Power/Ground Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
VDD_IO	I/O	Power	3.3V power supply for all interfaces, excluding PCI Express interface.
VDD_ODR_ CORE_T	I	Power	3.3V filtered power supply for the core voltage (1.2V) ODR.
VDD_ODR_ CORE_B	I	Power	3.3V filtered power supply for the core voltage (1.2V) ODR.
VDD_CORE	I	Power	Connect these pins to decoupling capacitors (0.1 µF). **NOTE:** When ODR is bypassed (ODR_CORE_DIS = 1), these pins are the VDD_CORE 1.2V power supply.
ODR_CORE_DIS	I	Analog	Core Voltage On-Die-Regulator Control • VSS—Core On-Die-Regulator Enabled (default) • 3.3V—Core On-Die-Regulator Disabled (Bypassed)
VSS	I	GND	Ground
PLL_AVDD	I	Power	PLL 3.3V Filtered Power
PLL_AVSS	I	GND	PLL Ground

3 88SB2211 Pinout

This section provides the pin map and pinout table for the 88SB2211—128 LQFP.
See 2 "Pin Information" on page 11 for a detailed description of the pin signals.

Figure 2: 128 LQFP Pinout (Top View)



* In Reverse Bridge mode, pin 79 acts as the device PCI_IDSELn pin (input).

Table 11: 128 LQFP Pinout Pin List by Pin Number

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	PCI_PAD[1]	44	PCI_PAD[21]	87	GPIO[3]
2	PCI_PAD[0]	45	PCI_PAD[24]	88	GPIO[2]
3	PCI_PAD[4]	46	PCI_PAD[17]	89	GPIO[1]
4	VDD_IO	47	PCI_PAD[23]	90	GPIO[0]
5	PCI_PAD[3]	48	PCI_PAD[19]	91	VDD_IO
6	PCI_PAD[2]	49	VDD_IO	92	PCI_CLK_IN
7	PCI_CBEn[0]	50	VDD_CORE	93	VDD_IO
8	VDD_IO	51	PCI_CBEn[3]	94	RST_OUTn
9	PCI_PAD[5]	52	PCI_PAD[25]	95	VSS
10	PCI_PAD[6]	53	PCI_PAD[26]	96	PCI_INTDn
11	PCI_PAD[7]	54	PCI_PAD[27]	97	PCI_INTBn
12	PCI_PAD[11]	55	PCI_PAD[31]	98	PCI_INTCn
13	PCI_PAD[9]	56	PCI_PAD[29]	99	PCI_INTAn
14	PCI_PAD[8]	57	PCI_CAL	100	TW_SCL
15	VDD_IO	58	VDD_IO	101	TW_SDA
16	PCI_PAD[10]	59	GPIO[4]	102	RST_INn
17	PCI_M66EN	60	PCI_PAD[28]	103	JT_TMS
18	PCI_PAD[12]	61	PCI_PAD[30]	104	JT_TDI
19	PCI_PAD[14]	62	PCI_VIO	105	VDD_IO
20	VDD_ODR_CORE_B	63	GPIO[5]	106	JT_TCK
21	VDD_IO	64	PCI_PMEn	107	JT_TRSTn
22	PCI_PAD[13]	65	VDD_IO	108	WAKEn
23	PCI_CBEn[1]	66	PCI_GNT3n	109	JT_TDO
24	PCI_SERRn	67	PCI_GNT4n	110	VDD_CORE
25	PCI_PAD[15]	68	PCI_REQ3n	111	XTAL_IN
26	VDD_IO	69	PCI_GNT1n	112	XTAL_OUT
27	PCI_LOCKn	70	PCI_REQ4n	113	VSS
28	PCI_PERRn	71	PCI_GNT2n	114	PLL_AVDD
29	PCI_PAR	72	PCI_REQ2n	115	PLL_AVSS
30	PCI_TRDYn	73	PCI_GNT0n	116	ANA_ISET
31	PCI_DEVSELn	74	VDD_IO	117	VSS
32	PCI_STOPn	75	PCI_REQ0n	118	PEX_CLK_P
33	VDD_IO	76	PCI_REQ1n	119	PEX_CLK_N
34	GPIO[6]	77	ODR_CORE_DIS	120	PEX_AVDDL
35	PCI_IRDYn	78	VDD_ODR_CORE_T	121	PEX_RX_P
36	PCI_FRAMEn	79	PCI_CLK_OUT[0] *	122	PEX_RX_N
37	GPIO[7]	80	PCI_CLK_OUT[1]	123	PEX_AVDDH
38	PCI_PAD[18]	81	PCI_CLK_OUT[2]	124	PEX_AVDD
39	PCI_PAD[16]	82	VDD_IO	125	PEX_TX_P
40	PCI_PAD[22]	83	PCI_CLK_OUT[3]	126	PEX_TX_N
41	PCI_PAD[20]	84	PCI_CLK_OUT[4]	127	PEX_AVSS
42	VDD_IO	85	PCI_CLK_OUT[5]	128	PEX_ISET
43	PCI_CBEn[2]	86	VDD_IO		

* In Reverse Bridge mode, pin 79 acts as the device PCI_IDSELn pin (input).

4 Reset Configuration

4.1 Pins Sample Configuration

Unless specifically noted, all reset sampled pins are sampled upon de-assertion of RST_INn.

Table 12 describes the reset pins configuration.

Table 12: Reset Configuration

Pin	Configuration Function
PCI_M66EN	PCI 66 MHz Enable
	0 = Disabled 1 = Enabled Sampled upon de-assertion of PCI_PRSTn. **NOTE:** Since the 88SB2211 does not support PCI 66 MHz, this pin must be pulled down to 0.
PCI_REQn[0]	PCI Slot 0 Enable
	Enables both PCI_CLK_OUT[0] output and PCI_REQn[0] input. When disabled, the clock output is forced to zero, and the request input is internally masked. 0 = Disabled 1 = Enabled **NOTE:** Internally pulled up to 1. When working with an external arbiter, PCI_CLK_OUT[0] is enabled by default, since this signal functions as PCI_REQ output and the PCI specification requires a pull up on this signal. Shutting down PCI_CLK_OUT[0] is only supported via the Table 52, Forward Bridge PCI Clock Output Control Register, on page 81 or Table 101, Reverse Bridge PCI Clock Output Control Register, on page 124 access.
PCI_REQn[1]	PCI Slot 1 Enable
	Enables both PCI_CLK_OUT[1] output and PCI_REQn[1] input. When disabled, the clock output is forced to zero, and the request input is internally masked. 0 = Disabled 1 = Enabled **NOTE:** Internally pulled up to 1. When working with the internal arbiter providing REQ/GNT coupled to slot 1, this signal must be pulled up, according to the PCI specification. in this case, shutting down PCI_CLK_OUT[1] is only supported via the Table 52, Forward Bridge PCI Clock Output Control Register, on page 81 or Table 101, Reverse Bridge PCI Clock Output Control Register, on page 124 access.

Table 12: Reset Configuration (Continued)

Pin	Configuration Function
PCI_REQn[2]	PCI Slot 2 Enable
	Enables both PCI_CLK_OUT[2] output and PCI_REQn[2] input. When disabled, the clock output is forced to zero, and the request input is masked internally. 0 = Disabled 1 = Enabled **NOTE:** Internally pulled up to 1. When working with the internal arbiter providing REQ/GNT coupled to slot 2, this signal must be pulled up according to the PCI specification. Shutting down PCI_CLK_OUT[2] in this case is only supported via Table 52, Forward Bridge PCI Clock Output Control Register, on page 81 or Table 101, Reverse Bridge PCI Clock Output Control Register, on page 124 access.
PCI_REQn[3]	PCI Slot 3 Enable
	Enables both PCI_CLK_OUT[3] output and PCI_REQn[3] input. When disabled, the clock output is forced to zero, and the request input is internally masked. 0 = Disabled 1 = Enabled **NOTE:** Internally pulled up to 1. When working with the internal arbiter providing REQ/GNT coupled to slot 3, this signal must be pulled up according to the PCI specification. In this case, shutting down PCI_CLK_OUT[3] is only supported via Table 52, Forward Bridge PCI Clock Output Control Register, on page 81 or Table 101, Reverse Bridge PCI Clock Output Control Register, on page 124 access.
PCI_REQn[4]	PCI Slot 4 Enable
	Enables both PCI_CLK_OUT[4] output and PCI_REQn[4] input. When disabled, the clock output is forced to 0, and the request input is masked internally. 0 = Disabled 1 = Enabled **NOTE:** Internally pulled up to 1. When working with the internal arbiter providing REQ/GNT coupled to slot 4, this signal must be pulled up, according to the PCI specification. In this case, shutting down PCI_CLK_OUT[4] is only supported via Table 52, Forward Bridge PCI Clock Output Control Register, on page 81 or Table 101, Reverse Bridge PCI Clock Output Control Register, on page 124 access.
GPIO[0]	Serial ROM Initialization
	0 = Disabled 1 = Enabled **NOTE:** Internally pulled down to 0.

Table 12: Reset Configuration (Continued)

Pin	Configuration Function
GPIO[1]	PCI Express Reference Clock Source Select
	0 = 100 MHz differential reference clock 1 = 125 MHz single-ended reference clock **NOTE:** Internally pulled down to 0. Refer to Clock Mode Select reset configuration for additional information on the reference clock options.
GPIO[2]	1.5V On Die Regulator Disable
	0 = 1.5V ODR Enabled. 1 = 1.5V ODR Disabled. 1.5V fed directly from the board. **NOTE:** Internally pulled down to 0.
GPIO[3]	2.5V On Die Regulator Disable
	0 = 2.5V ODR Enabled. 1 = 2.5V ODR Disabled. 2.5V fed directly from the board. **NOTE:** Internally pulled down to 0.
PCI_GNTn[1]	Internal PCI Arbiter Enable
	0 = Disabled 1 = Enabled **NOTE:** Internally pulled up to 1.
PCI_GNTn[3:2]	Clock Mode Select
	0 = XTAL Clock Source mode Reference clock to the PLL is XTAL_IN (25 MHz). PEX_CLK_N and PEX_CLK_P are inputs. 1 = XTAL Clock Source mode (PCI Express Clock Internal Generation) Reference clock to the PLL is XTAL_IN (25 MHz). PEX_CLK_N and PEX_CLK_P are outputs. **NOTE:** When working in this mode, only PCI agents 0, 1, and 2 are supported in the device internal arbiter. 2 = PCI Clock Source mode Reference clock to the PLL is PCI_CLK_IN (applicable only when the PCI clock period is exactly 30 ns). PEX_CLK_N and PEX_CLK_P are outputs. 3 = PCI Express Clock Source mode Reference clock to the PLL are PEX_CLK_N and PEX_CLK_P. (inputs) See the *88SB2211 Hardware Design Guidelines* for additional information about the clock modes. **NOTE:** PCI_GNTn[3] and PCI_GNTn[2] are internally pulled up to 1.
PCI_GNTn[4]	Bridge Mode Select
	0 = Reverse Bridge mode—The host is on PCI side. 1 = Forward Bridge mode—The host is on PCI Express side. **NOTE:** Internally pulled up to 1.

Note

PCI_CLK_OUT[5] is automatically disabled when all five PCI_CLK_OUT[4:0] pins are disabled.

5 Electrical Specifications (Preliminary)

The numbers specified in this section are PRELIMINARY and SUBJECT TO CHANGE.

5.1 Absolute Maximum Ratings

Table 13: Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD_CORE	-0.5	1.5	V	Core voltage
VDD_ODR_CORE_B	-0.5	4.0	V	Input voltage for: Core ODR
VDD_ODR_CORE_T	-0.5	4.0	V	Input voltage for: Core ODR
ODR_CORE_DIS	-0.5	4.0	V	Core ODR disable signal
PLL_AVDD	-0.5	4.0	V	Analog supply for the internal PLL
VDD_IO[1]	-0.5	4.0	V	I/O voltage for: PCI, TWSI and JTAG interfaces
PCI_VIO[1]	-0.5	6.0	V	I/O voltage for: PCI interface
PEX_AVDDH	-0.5	4.0	V	High voltage for: PCI Express interface
PEX_AVDD	-0.5	3.0	V	Analog voltage for: PCI Express interface when bypassing 2.5V ODR
PEX_AVDDL	-0.5	1.8	V	Analog voltage for: PCI Express interface when bypassing 1.5V ODR
TC	-40	125	° C	Case temperature
TSTG	-40	125	° C	Storage temperature

1. Input voltage must not exceed the respective interface supply voltage more than 0.7 V.

Caution

- Exposure to conditions at or beyond the maximum rating may damage the device.
- Operation beyond the recommended operating conditions (Table 14) is neither recommended nor guaranteed.

Note

Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell® Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

5.2 Recommended Operating Conditions

Table 14: Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
VDD_CORE	1.1	1.2	1.3	V	Core voltage when bypassing the 3.3V Core ODR
VDD_ODR_CORE_B	3	3.3	3.6	V	Input voltage for: Core ODR
VDD_ODR_CORE_T	3	3.3	3.6	V	Input voltage for: Core ODR
PLL_AVDD	3	3.3	3.6	V	Analog supply for the internal PLL
VDD_IO	3	3.3	3.6	V	I/O voltage for: PCI, TWSI, and JTAG interfaces
PCI_VIO	4.75	5	5.25	V	I/O voltage for: PCI interface
	3	3.3	3.6	V	
PEX_AVDDH	3	3.3	3.6	V	High voltage for: PCI Express interface
PEX_AVDD	2.375	2.5	2.625	V	Analog voltage for: PCI Express interface when bypassing 2.5V ODR
PEX_AVDDL	1.425	1.5	1.575	V	Analog voltage for: PCI Express interface when bypassing 1.5V ODR
TJ	0		125	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

5.3 Power Dissipation

Table 15: Power Dissipation

Interface	Symbol	Test Conditions	Typ	Max	Units
Power Dissipation (Utilizing all ODRs)	Pd		700	820	mW
Power Dissipation (ODRs)	Pd		630		mW
Power Dissipation (No ODRs utilization)	Pd		500		mW

Note: Typ power is the maximal power measured at typical conditions.

5.4 Current Consumption

Table 16: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
PCI (33 MHz 32-bit) Interface	I_{PCI}	25 pf load	100	mA
PCI Express interface (with ODR disabled)	I_{PEX_AVDDH}	AVDDH @ 3.3V	0	mA
	I_{PEX_AVDD}	AVDD @ 2.5V	20	mA
	I_{PEX_AVDDL}	AVDDL @ 1.5V	40	mA
PCI Express interface (with ODR enabled)	I_{PEX_AVDDH}	AVDDH @ 3.3V	65	mA
	I_{PEX_AVDD}	AVDD @ 2.5V	0	mA
	I_{PEX_AVDDL}	AVDDL @ 1.5V	0	mA
Core VDD_CORE, VDD_ODR_CORE_B, or VDD_ODR_CORE_T	I_{VDD_CORE}		80	mA

Notes:

1. Current in mA is calculated using maximum recommended VDDIO specification for each power rail.
2. All output clocks toggling at their specified rate.
3. Maximum drawn current from the power supply.
4. When the Core ODR is not bypassed, the core current is drawn from both VDD_ODR_CORE_B and VDD_ODR_CORE_T.

5.5 DC Electrical Specifications

5.5.1 PCI, JTAG, and GPIO 3.3V Interfaces DC Electrical Specifications

The values in Table 17 also apply to the ODR_CORE_DIS signal.

Table 17: PCI, JTAG, and GPIO 3.3V Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.5*VDDIO		VIO+0.5	V	-
Output low level	VOL	IOL = 1.5 mA	-		0.1*VDDIO	V	-
Output high level	VOH	IOH = -0.5 mA	0.9*VDDIO		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

5.5.2 Two-Wire Serial Interface (TWSI) 3.3V DC Electrical Specifications

Table 18: TWSI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

5.6 AC Electrical Specifications

See 5.7 "Differential Interface Electrical Characteristics" on page 41 for differential interface specifications.

5.6.1 Reference Clock AC Timing Specifications

Table 19: Reference Clock AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
XTAL_IN Reference Clock					
Frequency	F_{XTAL_IN}	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	DC_{XTAL_IN}	40	60	%	
Slew rate	SR_{XTAL_IN}	0.7		V/ns	1
Pk-Pk jitter	JR_{XTAL_IN}		200	ps	

Note:

1. Slew rate is measured from 20% to 80% of the reference clock signal.

5.6.2 PCI Interface AC Timing

5.6.2.1 PCI Interface AC Timing Table

Table 20: PCI Interface AC Timing Table

Description	Symbol	PCI 33 MHz @ 3.3V Min	PCI 33 MHz @ 3.3V Max	Units	Notes
Clock cycle time	Tcyc	30.0	-	ns	1
Clock high time	Thigh	11.0	-	ns	-
Clock low time	Tlow	11.0	-	ns	-
Clock slew rate	-	1.0	4.0	V/ns	2
Clock rising edge to signal valid delay for bused signals	Tval	2.0	11.0	ns	3, 4
Clock rising edge to signal valid delay for point to point signals	Tval(ptp)	2.0	12.0	ns	3, 4
Input setup time to Clock rising edge for bused signals	Tsu	7.0	-	ns	4, 6, 8
Input setup time to Clock rising edge for point to point signals	Tsu(ptp)	10, 12	-	ns	4, 5, 6
Input hold time from Clock rising edge	Th	0.0	-	ns	6
Reset active time	Trst	1.0	-	ms	7
Output rise slew rate	tr	1.0	4.0	V/ns	9
Output fall slew rate	tf	1.0	4.0	V/ns	9

Notes:

1. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in the PCI Interface Clock waveform.
3. See the timing measurment conditions in the Output Timing Measurement Conditions figure.
4. Point-to-point signals applies to REQn and GNTn only. All other signals are bused.
5. GNTn has a setup of 10 ns; REQn has a setup of 12 ns.
6. See the timing measurement conditions in the Input Timing Measurement Conditions figure.
7. RSTn is asserted and deasserted asynchronously with respect to Clock.
8. Setup time applies only when the device is not driving the pin.
   Devices cannot drive and receive signals at the same time.
9. The test load is specified in the Tval (Min) Test Load figure.

5.6.2.2 PCI Interface Test Circuit

Figure 3: Tval (Max) Rising Edge Test Load

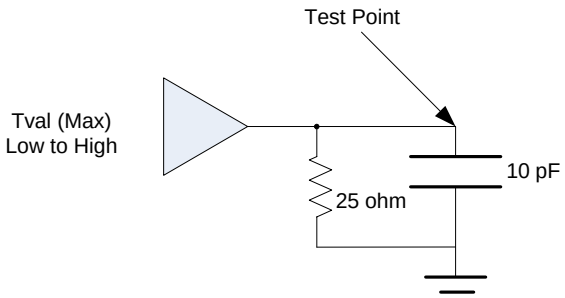


Figure 4: Tval (Max) Falling Edge Test Load

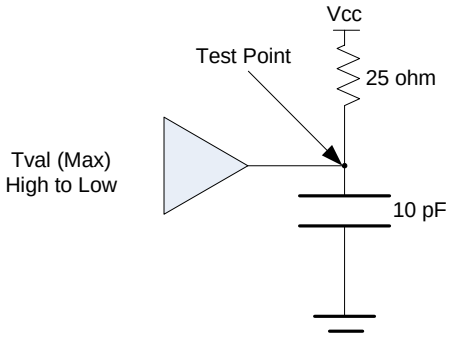
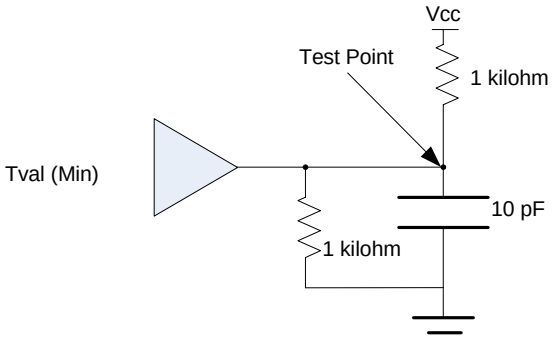


Figure 5: Tval (Min) Test Load & Output Slew Rate Test Load



5.6.2.3 PCI Interface Measurement Condition Parameters

Table 21: PCI Interface Measurement Condition Parameters

Symbol	PCI	Units	Notes
Vth	0.6 Vcc	V	-
Vtl	0.2 Vcc	V	-
Vtest	0.4 Vcc	V	-
Vtrise	0.285 Vcc	V	1
Vtfall	0.615 Vcc	V	1
Output rise slew rate	0.3 Vcc to 0.6 Vcc	V	-
Output fall slew rate	0.6 Vcc to 0.3 Vcc	V	-
Input signal slew rate	1.5	V/ns	-

Notes:

1. Vtrise and Vtfall are reference voltages for timing definitions only.

5.6.2.4 PCI Interface AC Timing Measurement Waveforms

Figure 6: PCI Interface Clock Waveform

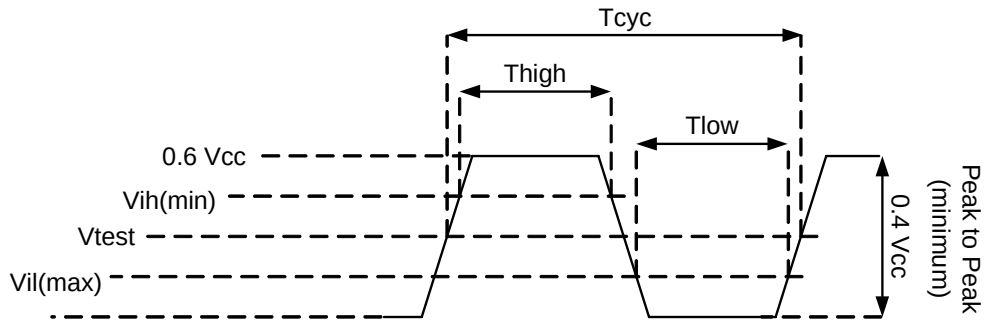


Figure 7: PCI Interface Output Timing Measurement Conditions

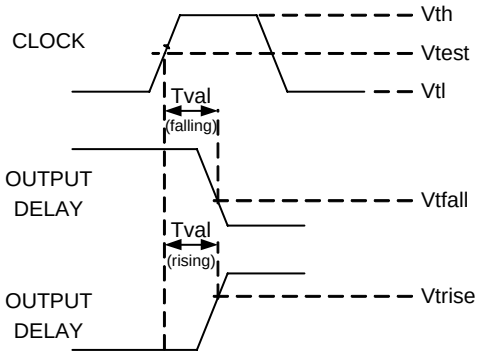
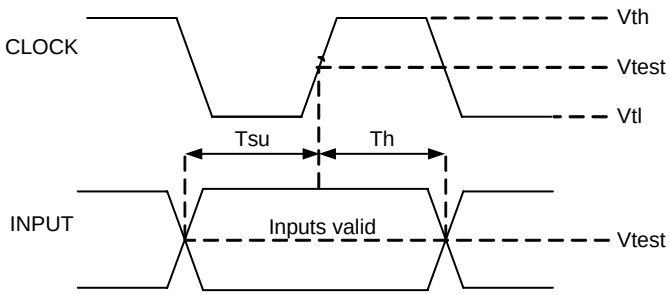


Figure 8: PCI Interface Input Timing Measurement Conditions



5.6.3 Two-Wire Serial Interface (TWSI) AC Timing

5.6.3.1 TWSI AC Timing Table

Table 22: TWSI AC Timing Table

Description	Symbol	100 kHz		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

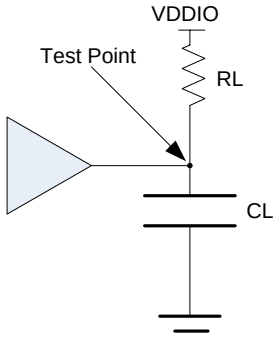
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

5.6.3.2 TWSI Test Circuit

Figure 9: TWSI Test Circuit



5.6.3.3 TWSI AC Timing Diagrams

Figure 10: TWSI Output Delay AC Timing Diagram

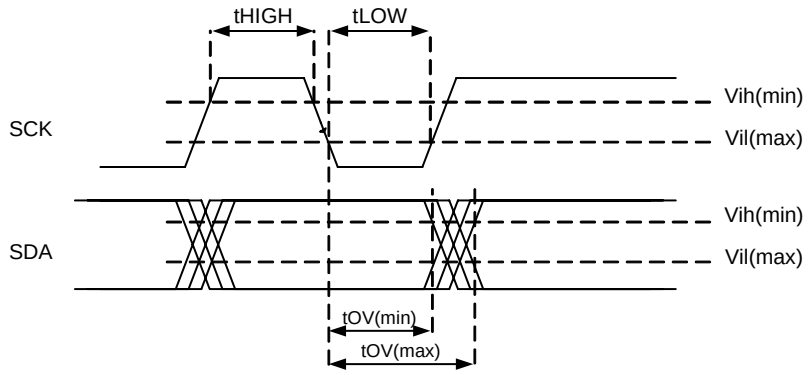
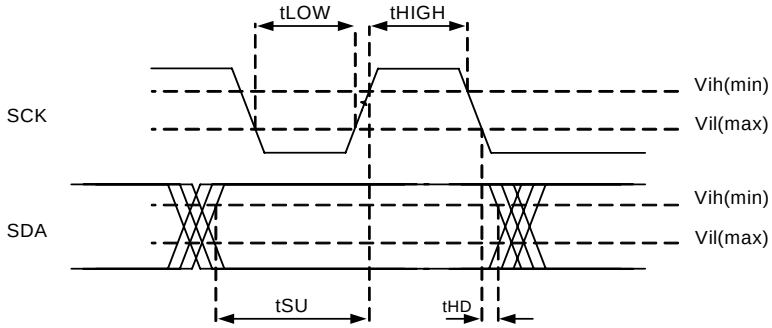


Figure 11: TWSI Input AC Timing Diagram



5.6.4 JTAG Interface AC Timing

5.6.4.1 JTAG Interface AC Timing Table

Table 23: JTAG Interface 5 MHz AC Timing Table

Description	Symbol	5 MHz		Units	Notes
		Min	Max		
JTClk frequency	fCK	5.0		MHz	-
JTClk minimum pulse width	Tpw	0.40	0.60	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.50	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	10.0	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	75.0	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	20.0	ns	1

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

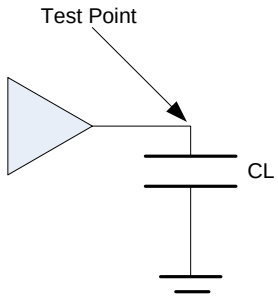
General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 20 pF.

2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.

5.6.4.2 JTAG Interface Test Circuit

Figure 12: JTAG Interface Test Circuit



5.6.4.3 JTAG Interface AC Timing Diagrams

Figure 13: JTAG Interface Output Delay AC Timing Diagram

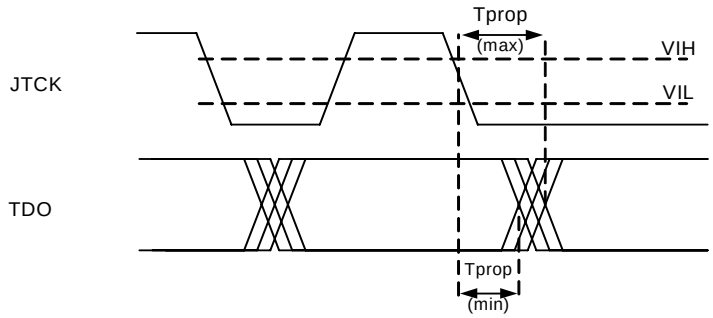
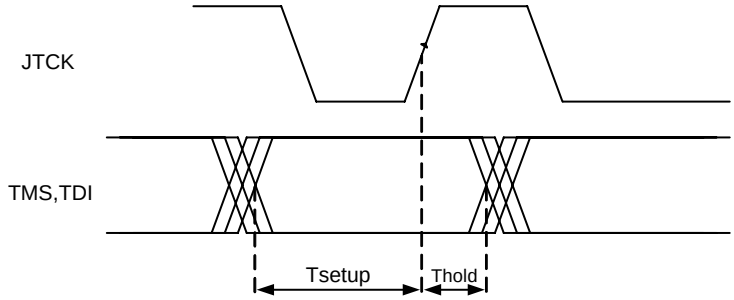


Figure 14: JTAG Interface Input AC Timing Diagram



5.7 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the PCI Express interface.

5.7.1 Differential Interface Reference Clock Characteristics

Table 24: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Input Clock frequency	fCK	100.0		MHz	-
Input Clock duty cycle	DCrefclk	0.45	0.55	tCK	-
Input Clock rise/fall time	TRrefclk	175.0	700.0	pS	1, 3
Input Clock rise/fall time variation	dlTRrefclk	-	125.0	pS	1, 3
Input high voltage	VIHrefclk	660.0	850.0	mV	1
Input low voltage	VILrefclk	-150.0	50.0	mV	1
Absolute crossing point voltage	Vcross	250.0	550.0	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140.0	mV	1
Absolute maximum input voltage (overshoot)	Vmax	-	1.15	V	1
Absolute minimum input voltage (undershoot)	Vmin	-	-0.3	V	1
Absolute differential clock period	Tperabs	9.872	-	nS	2
Differential clock cycle-to-cycle jitter	Tccjit	-	125.0	pS	-

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 1.0a, April 2003, section 2.6.3 for more information.

1. Defined on a single ended signal.
2. Including jitter and spread spectrum.
3. Defined from 0.175V to 0.525V.

PCI Express Interface Spread Spectrum Requirements

Table 25: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	0.0	33.0	kHz	-
Fspread	-0.5	0.0	%	-

5.7.2 PCI Express Interface Electrical Characteristics

5.7.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 26: PCI Express Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400.0		ps	-
Baud rate tolerance	Bppm	-300.0	300.0	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.7	-	UI	-
Differential return loss	TRLdiff	12.0	-	dB	1
Common mode return loss	TRLcm	6.0	-	dB	1
DC differential TX impedance	ZTXdiff	80.0	120.0	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	15.0	-	dB	1
Common mode return loss	RRLcm	6.0	-	dB	1
DC differential RX impedance	ZRXdiff	80.0	120.0	Ohm	-
DC common input impedance	ZRXcm	40.0	60.0	Ohm	-

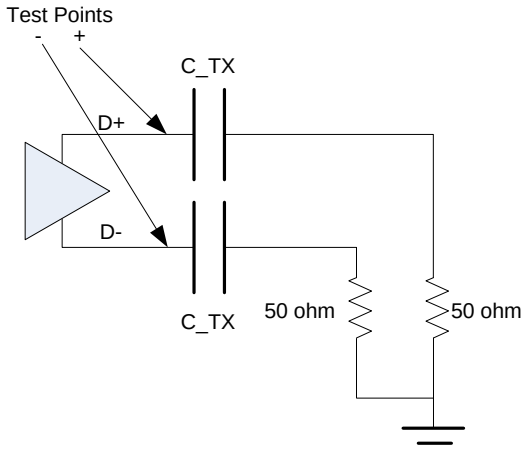
Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.0a, April, 2003.

1. Defined from 50 MHz to 1.25 GHz.
2. Does not account for SSC dictated variations.

5.7.2.2 PCI Express Interface Test Circuit

Figure 15: PCI Express Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

6 Thermal Data

This section provides the package thermal data for the 88SB2211. This data is derived from simulations that were run according to the JEDEC standard.

The thermal parameters are preliminary and subject to change.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products. Before designing a system it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products,* Document Number MV-S300281-00[1]
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Document Number MV-S700019-00[1]

Table 27 shows the LQFP package thermal data for the 88SB2211. The simulation was done according to the JEDEC standard.

Table 27: 128 LQFP Package Thermal Data

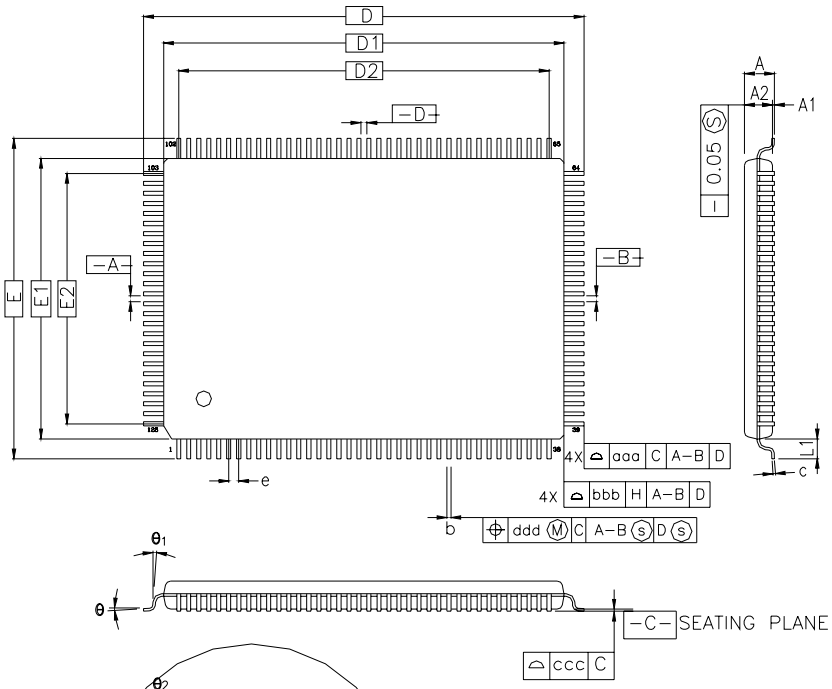
Parameter	Definition	Airflow Value		
		0 m/s	1 m/s	2 m/s
θ_{JA}	Thermal resistance: junction to ambient	55.2	49.4	47.7
ψ_{Jt}	Thermal characterization parameter: junction to case center	5.9	6.5	6.9
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	26.3		
Ψ_{JB}	Thermal characterization parameter: junction to the bottom of the package.	43.5	42.1	41.3
θ_{JB}	Thermal resistance: junction to the bottom of the package (not air-flow dependent)	44.5		

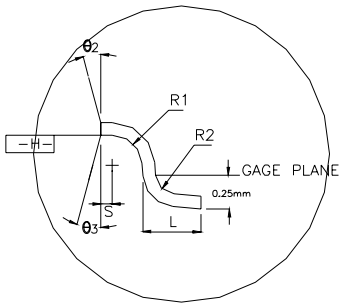
1. Contact your local Marvell® sales representative for information about receiving this document.

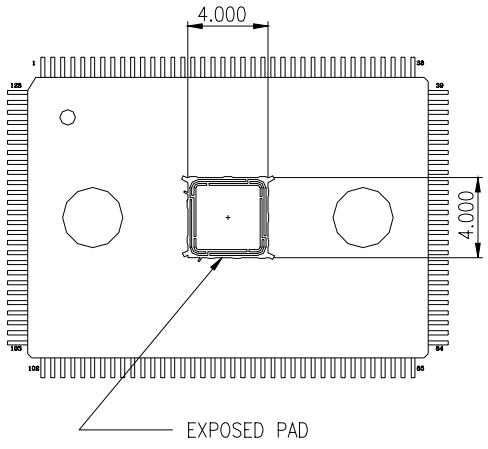
7 Package Mechanical Information

This section provides the package mechanical information for the 88SB2211 128-pin LQFP package.

Figure 16: 128-Pin LQFP Package Diagram







COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

8 Part Order Numbering/Package Marking

8.1 Part Order Numbering

Figure 17 shows the part order numbering scheme for the 88SB2211. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 17: Sample Part Number

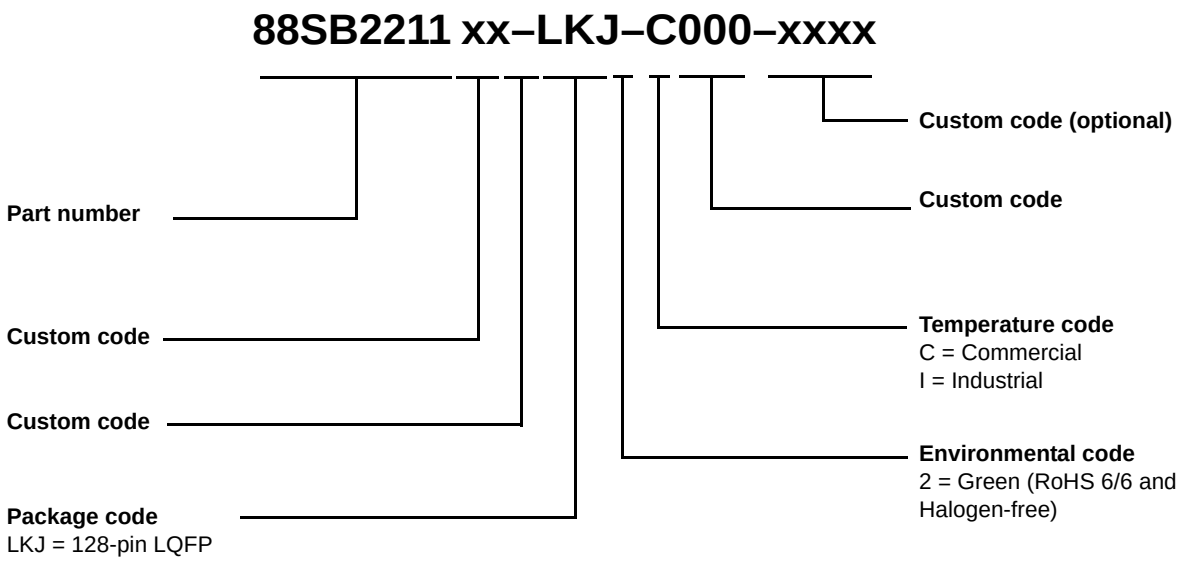


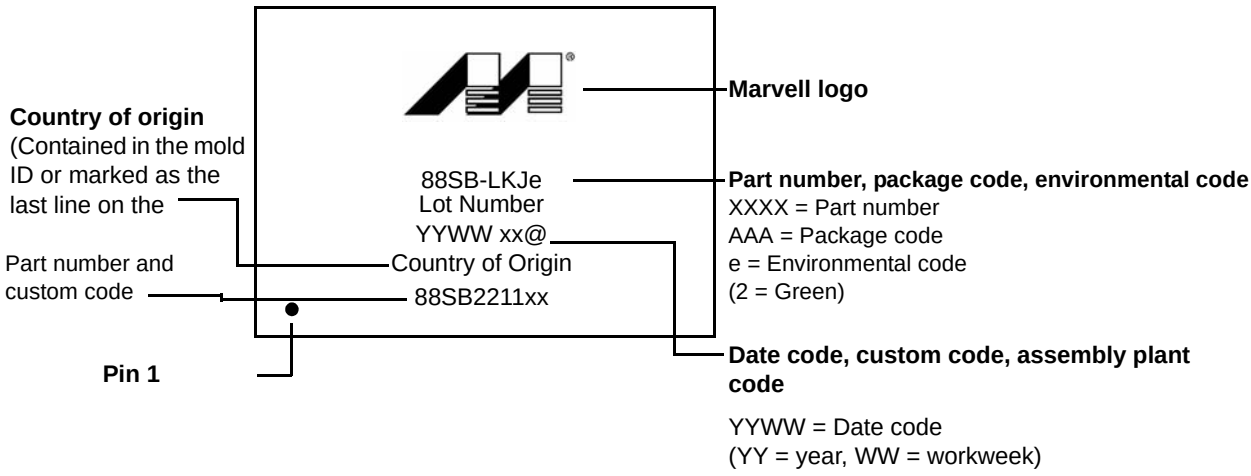
Table 28: 88SB2211 Part Order Options

Package Type	Part Order Number
128-pin LQFP	88SB2211xx-LKJ2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package)

8.2 Package Marking

Figure is an example of the package marking and pin 1 location for the 88SB2211 LQFP package.

LQFP Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

88SB2211

Register Set

THIS PAGE INTENTIONALLY LEFT BLANK

List of Registers

A 88SB2211 Register Set

A.1 Registers Overview

This section details the 88SB2211 registers.

A.2 Register Description

All registers are 32-bits wide [31:0]. The 88SB2211 registers use the PCI Byte Ordering (Little Endian) in which the Most Significant Byte (MSB) of a multi-byte expression is located in the highest address. The bits within a given byte are always ordered so that Bit [7] is the Most Significant Bit (MSb) and Bit [0] is the Least Significant Bit (LSb).

The 88SB2211 can operate in either Forward Bridge or Reverse Bridge mode. A full register set for each of these modes appear in:

- Section A.3, Forward Bridge Mode Configuration Registers, on page 57
- Section A.4, Reverse Bridge Mode Configuration Registers, on page 98

A.2.1 Register Field Type xxx Codes

The 88SB2211 registers are made up of up to 32-bit fields, where each field is associated with one or more bits. Each of these register fields have a unique programming functionality and their operation is defined by the field's type. The following list describes the function of each type:

Table 29: Standard Register Field Type Codes

Type	Description
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains cleared until a read operation is performed through the management interface or a reset occurs.
Retain	The register value is retained after software reset is executed.
RO	Read Only. Writing to this type of field may cause unpredictable results.
ROC	Read Only Clear. After read, register field is cleared to zero.
RSVD	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RW	Read and Write.
RW0C	Read-only status, Write-0 to clear status register. Register bits indicate status when read, a set bit indicates a status event may be cleared by writing a 0. Writing a 1 to RW0C bits have no effect.
RW1C	Read-only status, Write-1 to clear status register. Register bits indicate status when read, a set bit indicates a status event may be cleared by writing a 1. Writing a 0 to RW1C bits have no effect.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is cleared to zero when the function is complete.

Table 29: Standard Register Field Type Codes (Continued)

Type	Description
Special	Used in special cases where the register type functionality does not conform to any of the standard types listed in this table. Refer to the Description Column of the register table for a full definition of the field/register type and functionality.
Update	Value written to the register field does not take effect until a software reset is executed. The value can still be read after it is written.
WO	Write Only. A write to the register field will trigger an internal function and a read will return an undefined value.
X	These bits do not exist.

A.3 Forward Bridge Mode Configuration Registers

The following table provides a summarized list of all of the Forward Bridge Mode Configuration registers, including the register names, their type, offset, and a reference to the corresponding table and page for a detailed description of each register and its fields.

Table 30: Register Map Table for the Forward Bridge Mode Configuration Registers

Register Name	Offset	Table and Page
Forward Bridge Mode Configuration Header		
Device and Vendor ID Register	0x00000	Table 31, p. 58
Forward Bridge Command and Status Register	0x00004	Table 32, p. 59
Class Code and Revision ID Register	0x00008	Table 33, p. 62
Forward Bridge BIST Header Type and Cache Line Size Register	0x0000C	Table 34, p. 62
Forward Bridge PCI Express Secondary Latency Timer and Subordinate Secondary and Primary Bus Numbers Register	0x00018	Table 35, p. 63
Forward Bridge PCI Express Secondary Status I/O Limit and I/O Base Register	0x0001C	Table 36, p. 63
Memory Limit and Memory Base Register	0x00020	Table 37, p. 65
Prefetchable Memory Limit and Prefetchable Memory Base Register	0x00024	Table 38, p. 66
Prefetchable Base Upper 32 Bits Register	0x00028	Table 39, p. 67
Prefetchable Limit Upper 32 Bits Register	0x0002C	Table 40, p. 67
I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits	0x00030	Table 41, p. 67
Capabilities Pointer Register	0x00034	Table 42, p. 68
Forward Bridge Control Interrupt Pin and Interrupt Line Register	0x0003C	Table 43, p. 68
Power Management Capability Header Register	0x00040	Table 44, p. 71
Forward Bridge Power Management Control and Status Register	0x00044	Table 45, p. 72
Forward Bridge PCI Express Capability Register	0x00048	Table 46, p. 73
Forward Bridge PCI Express Device Capabilities Register	0x0004C	Table 47, p. 74
Forward Bridge PCI Express Device Control Status Register	0x00050	Table 48, p. 75
Forward Bridge PCI Express Link Control Status Register	0x00058	Table 49, p. 78
Forward Bridge Mode Device Specific		
Forward Bridge PCI Internal Arbiter Control Register	0x00070	Table 50, p. 79
GPIO Control Register	0x00074	Table 51, p. 80
Forward Bridge PCI Clock Output Control Register	0x00078	Table 52, p. 81
Forward Bridge Prefetch and CRS Control Register	0x00080	Table 53, p. 82
Marvell Diagnostic PCI Express PHY Indirect Access Register	0x000F4	Table 54, p. 85
Marvell Diagnostic Indirect Address Register	0x000F8	Table 55, p. 85
Marvell Diagnostic Indirect Data Register	0x000FC	Table 56, p. 86

Table 30: Register Map Table for the Forward Bridge Mode Configuration Registers (Continued)

Register Name	Offset	Table and Page
Forward Bridge Mode Extended Configuration Space		
PCI Express Advanced Error Report Header Register	0x00100	Table 57, p. 86
PCI Express Uncorrectable Error Status Register	0x00104	Table 58, p. 86
PCI Express Uncorrectable Error Mask Register	0x00108	Table 59, p. 87
PCI Express Uncorrectable Error Severity Register	0x0010C	Table 60, p. 89
PCI Express Correctable Error Status Register	0x00110	Table 61, p. 90
PCI Express Correctable Error Mask Register	0x00114	Table 62, p. 90
PCI Express Advanced Error Capability and Control Register	0x00118	Table 63, p. 91
PCI Express Header Log First DWORD Register	0x0011C	Table 64, p. 92
PCI Express Header Log Second DWORD Register	0x00120	Table 65, p. 92
PCI Express Header Log Third DWORD Register	0x00124	Table 66, p. 92
PCI Express Header Log Fourth DWORD Register	0x00128	Table 67, p. 92
PCI Uncorrectable Error Status Register	0x0012C	Table 68, p. 92
Forward Bridge PCI Uncorrectable Error Mask Register	0x00130	Table 69, p. 94
PCI Uncorrectable Error Severity Register	0x00134	Table 70, p. 95
PCI Error Capability and Control Register	0x00138	Table 71, p. 96
PCI Header Log First DWORD Register	0x0013C	Table 72, p. 96
PCI Header Log Second DWORD Register	0x00140	Table 73, p. 97
PCI Header Log Third DWORD Register	0x00144	Table 74, p. 97
PCI Header Log Fourth DWORD Register	0x00148	Table 75, p. 97

A.3.1 Forward Bridge Mode Configuration Header

Table 31: Device and Vendor ID Register
Offset: 0x00000

Bit	Field	Type/InitVal	Description
15:0	VenID	RO 0x11AB	Vendor ID This field identifies Marvell as the vendor of the device.
31:16	DevID	RO 0x2211	Device ID

Table 32: Forward Bridge Command and Status Register
Offset: 0x00004

Bit	Field	Type/InitVal	Description
0	IOEn	RW 0x0	I/O Space Enable. Controls the 88SB2211response as a target to I/O transactions on the primary interface that address a device that resides behind the bridge. **NOTE:** Software should ensure that outstanding transactions involving the bridge are completed prior to disabling this bit. 0 = Disable: Respond to all I/O requests on the primary interface with an Unsupported Request Completion. Forward all I/O transactions from the secondary interface to the primary interface. 1 = Enable: forwarding of I/O requests to the secondary interface.
1	MemEn	RW 0x0	Memory Space Enable Controls the 88SB2211 response as a target to memory accesses on the primary interface that addresses a device that resides behind the bridge in both the non-prefetchable and prefetchable memory ranges. **NOTE:** Software should ensure that outstanding transactions involving the bridge are completed prior to disabling this bit. 0 = Disable: Respond to all Memory Requests on the primary interface as Unsupported Request Received. Forward all memory requests from the secondary interface to the primary interface. 1 = Enable: forwarding of memory transactions to the secondary interface.
2	MasEn	RW 0x0	Master Enable Controls the ability of the 88SB2211 to issue memory and I/O read/write requests on the primary interface. Disabling this bit prevents the bridge from issuing any memory or I/O read/write requests on the primary interface. **NOTE:** Message Signaled Interrupt (MSI)/Enhanced Message Signaled Interrupt (MSI-X) transactions are in-band Memory Writes; disabling the Bus Master Enable bit disables MSI/MSI-X transactions as well. When this bit is zero, the 88SB2211 disables response as a target to all memory or I/O transactions on the secondary interface (they cannot be forwarded to the primary interface). This bit does not affect the issuing of completions on the primary interface or the forwarding of completions. **NOTE:** Software should ensure that outstanding transactions involving the bridge are completed prior to disabling this bit. 0 = Disable: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on secondary interface. 1 = Enable: the bridge to operate as a master on the primary interface for memory and I/O transactions forwarded from the secondary interface.
3	Reserved_3	RO 0x0	Special Cycle Enable Does not apply to PCI Express devices.

Table 32: Forward Bridge Command and Status Register (Continued)
Offset: 0x00004

Bit	Field	Type/InitVal	Description
4	Reserved_4	RSVD 0x0	Memory Write and Invalidate The 88SB2211 does not support forwarding of Memory Write Requests from the PCI Express interface as Memory Write and Invalidate transactions on the PCI interface.
5	Reserved_5	RSVD 0x0	VGA Palette Snoop does not apply to PCI Express bridges.
6	PErrRes	RW 0x0	Parity Error Response This bit controls the 88SB2211's setting of the <MasDataPerr> status bit[24] in this register in response to a received poisoned data error as a requester (master) on the PCI Express. **NOTE:** The setting of this bit does not affect the DetectedPErr status bit. 0 = Disabled: MasDataPerr assertion is disabled. 1 = Enabled: MasDataPerr assertion is enabled.
7	Reserved_7	RSVD 0x0	Reserved
8	SErrEn	RW 0x0	PCI_SERRn Enable This bit enables reporting of Non-Fatal and Fatal errors to the Root Complex. Upon detection of either Non-Fatal or Fatal error by the 88SB2211, this bit controls the assertion of SSysErr status bit[30] in this register and the generation of a corresponding ERR_FATAL or ERR_NONFATAL error message. In addition, upon PCI_SERRn assertion detected on the PCI interface, this bit controls the generation of a corresponding ERR_FATAL or ERR_NONFATAL error message. **NOTE:** PCI Express uncorrectable error messages are reported if enabled either through this bit or through bits <NFErrRepEn> or <FErrRepEn> in the PCI Express Device Control Status. 0 = Disable: reporting of Non-Fatal and Fatal errors. 1 = Enable: reporting of Non-Fatal and Fatal errors.
9	PrFbtbEn	RO 0x0	Primary Fast Back-to-Back Transactions Enable Does not apply to PCI Express devices. 0 = Disable: generation of fast back-to-back transactions on the primary interface. 1 = Enable: generation of fast back-to-back transactions on the primary interface.
10	Reserved_10	RO 0x0	Interrupt Disable The 88SB2211 has no internal interrupt resources, and therefore, this bit has no effect. 0 = Enabled: Interrupt messages enabled. 1 = Disabled: Interrupt messages disabled.
18:11	Reserved_18_11	RSVD 0x0	Reserved

Table 32: Forward Bridge Command and Status Register (Continued)
Offset: 0x00004

Bit	Field	Type/InitVal	Description
19	Reserved_19	RSVD 0x0	Interrupt Status The 88SB2211 has no internal interrupt resources, and therefore, this bit has no effect. This bit is hardwired to 0. 0 = No_interrupt: asserted. 1 = Interrupt: asserted.
20	CapList	RO 0x1	Capability List Support This bit indicates that the 88SB2211 configuration header includes capability list.
21	66MHzCap	RO 0x0	Primary 66 MHz Capable Does not apply to PCI Express devices.
22	Reserved_22	RSVD 0x0	Reserved
23	FbtbCap	RO 0x0	Primary Fast Back-to-Back Transactions Capable Does not apply to PCI Express devices.
24	MasDataPerr	RW1C 0x0	Master Data Parity Error Reports detection of uncorrectable data errors by the 88SB2211. This bit is set when <PErrRes> bit[6] of this register is set and either of the following occur: - The 88SB2211 receives a poisoned completion on the PCI Express interface. - The 88SB2211 transmits a poisoned write request on the PCI Express interface.
26:25	DevSelTim	RO 0x0	Primary PCI_DEVSELn Timing Does not apply to PCI Express.
27	STarAbort	RW1C 0x0	Signaled Target Abort This bit is set when the 88SB2211 generates a completion with Completer Abort Completion Status in response to a request received on the PCI Express interface.
28	RTAbort	RW1C 0x0	Received Target Abort This bit is set when the 88SB2211, as a requester (master), receives a completion with the status Completer Abort.
29	RMAbort	RW1C 0x0	Received Master Abort This bit is set when the 88SB2211 receives a completion with Unsupported Request Completion Status on the PCI Express interface.

Table 32: Forward Bridge Command and Status Register (Continued)
Offset: 0x00004

Bit	Field	Type/InitVal	Description
30	SSysErr	RW1C 0x0	Signaled System Error This bit is set when the 88SB2211 sends an ERR_FATAL or ERR_NONFATAL message. This bit is not set if the <SErrEn> field in this register is de-asserted.
31	DetParErr	RW1C 0x0	Detected Parity Error This bit is set when the 88SB2211 receives a poisoned TLP on the PCI Express interface. **NOTE:** The bit is set regardless of the state of the <PErrRes> bit in this register.

Table 33: Class Code and Revision ID Register
Offset: 0x00008

Bit	Field	Type/InitVal	Description
7:0	RevID	RO 0x1	88SB2211 Revision Number
15:8	ProgIF	RO 0x0	Register Level Programming Interface
23:16	SubClass	RO 0x04	88SB2211 Sub class -- PCI-to-PCI bridge
31:24	BaseClass	RO 0x06	88SB2211 Base Class -- Bridge device

Table 34: Forward Bridge BIST Header Type and Cache Line Size Register
Offset: 0x0000C

Bit	Field	Type/InitVal	Description
7:0	CacheLine	RW 0x00	88SB2211 Cache Line Size This field specifies the system cache line size in units of Dwords. The value in this register is used by the 88SB2211 for the following purposes: 1. To determine the PCI interface command type when forwarding memory read transactions from the PCI Express interface. 2. To determine the read transactions prefetch size of the PCI when acting as target. 8 = 32 Bytes prefetch 16 = 64 Bytes prefetch 32 = 128 Bytes prefetch

Table 34: Forward Bridge BIST Header Type and Cache Line Size Register (Continued)
Offset: 0x0000C

Bit	Field	Type/InitVal	Description
15:8	Reserved_15_8	RSVD 0x0	Primary Latency Timer Does not apply to PCI Express. Those bits are hardwired to 0.
23:16	HeadType	RO 0x01	88SB2211 Configuration Header Type Type 1 single-function configuration header.
31:24	BIST	RO 0x00	Built-In Self Test (BIST) The 88SB2211 does not support BIST.

Table 35: Forward Bridge PCI Express Secondary Latency Timer and Subordinate Secondary and Primary Bus Numbers Register
Offset: 0x00018

Bit	Field	Type/InitVal	Description
7:0	PriBusNm	RW 0x0	Primary Bus Number **NOTE:** This field is not captured from type 0 configuration write accesses.
15:8	SecBusNm	RW 0x0	Secondary Bus Number Used for type 1 configuration access handling.
23:16	SubBusNm	RW 0x0	Subordinate Bus Number Used for type 1 configuration access handling.
31:24	SecLatTimer	RW 0x0	PCI Latency Timer Specifies (in PCI Clock units) the value of the Latency Timer value of the 88SB2211. Used by PCI master when acting as a requester.

Table 36: Forward Bridge PCI Express Secondary Status I/O Limit and I/O Base Register
Offset: 0x0001C

Bit	Field	Type/InitVal	Description
3:0	IOBaseType	RO 0x1	I/O Base Type Indicates that the 88SB2211 supports 32-bit I/O addressing.

Table 36: Forward Bridge PCI Express Secondary Status I/O Limit and I/O Base Register (Continued)
Offset: 0x0001C

Bit	Field	Type/InitVal	Description
7:4	IOBase	RW 0x0	I/O Base Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits.
11:8	IOLimitType	RO 0x1	I/O Limit Type Indicates that the 88SB2211 supports 32-bit I/O addressing.
15:12	IOLimit	RW 0x0	I/O Limit Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits. **NOTE:** If there are no I/O addresses on the secondary side of the bridge, this field can be programmed to a smaller value than the <IOBase> field. In that case, the bridge does not forward any I/O transactions from the primary interface to the secondary, and does forward all I/O transactions from the secondary interface to the primary interface. **NOTE:**
20:16	Reserved_20_16	RSVD 0x0	Reserved
21	66MHzCap	RO 0x1	66 MHz Capable
22	Reserved_22	RSVD 0x0	Reserved
23	FbtbCap	RO 0x1	Fast back-to-back capable. Indicates that the 88SB2211 bridge is able of responding to fast back-to-back transactions on the secondary bus.
24	DataPar	RW1C 0x0	Master Data Parity Error This bit is used to report the detection of an uncorrectable data error by the bridge. This bit is set if the bridge is the bus master of the transaction on the secondary interface, the <SecPerrResEn> bit in the Forward Bridge Control Interrupt Pin and Interrupt Line Register is set, and either of the following two conditions occur: - The bridge asserts PCI_PERRn on a read transaction. - The bridge detects PCI_PERRn asserted on a write transaction. If the <SecPerrResEn> bit is set to zero, this bit is not be set when an error is detected.
26:25	DevSelTim	RO 0x1	PCI_DEVSELn Timing Indicates the 88SB2211 device's PCI_DEVSELn timing as Medium.

Table 36: Forward Bridge PCI Express Secondary Status I/O Limit and I/O Base Register (Continued)
Offset: 0x0001C

Bit	Field	Type/InitVal	Description
27	STarAbort	RW1C 0x0	Signaled Target Abort This bit reports the signaling of a Target-Abort termination by the bridge when it responds as the target of a transaction on its secondary interface.
28	RTAbort	RW1C 0x0	Received Target Abort This bit reports the detection of a Target-Abort termination by the bridge when it is the master of a transaction on its secondary interface.
29	RMAbort	RW1C 0x0	Received Master Abort. This bit reports the detection of a Master-Abort termination by the bridge when it is the master of a transaction on its secondary interface.
30	RSysErr	RW1C 0x0	Received System Error This bit reports the detection of an PCI_SERRn assertion on the secondary interface of the bridge.
31	DetParErr	RW1C 0x0	Detected Parity Error This bit reports the detection of an uncorrectable address, attribute, or data error by the bridge on its secondary interface. This bit must be set when any of the following three conditions are true: - The bridge detects an uncorrectable address or attribute error as a potential target. - The bridge detects an uncorrectable data error when it is the target of a write transaction. - The bridge detects an uncorrectable data error when it is the master of a read transaction (immediate read data). The bit is set irrespective of the state of the <SecPerrResEn> bit in the Forward Bridge Control Interrupt Pin and Interrupt Line Register.

Table 37: Memory Limit and Memory Base Register
Offset: 0x00020

Bit	Field	Type/InitVal	Description
3:0	Reserved	RO 0x0	This bit is hardwired to 0.
15:4	MemBase	RW 0x0	Memory base Defines the bottom address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h
19:16	Reserved	RO 0x00	This bit is hardwired to 0.

Table 37: Memory Limit and Memory Base Register (Continued)
Offset: 0x00020

Bit	Field	Type/InitVal	Description
31:20	MemLimit	RW 0x0	Memory limit Defines the top address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. **NOTE:** If there are no memory-mapped I/O addresses on the secondary side of the bridge, the <MemLimit> field must be programmed to a smaller value than the <MemBase> field. If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus. **NOTE:**

Table 38: Prefetchable Memory Limit and Prefetchable Memory Base Register
Offset: 0x00024

Bit	Field	Type/InitVal	Description
3:0	PerBaseType	RO 0x1	Prefetchable Memory Base Type Indicates that the 88SB2211 supports 64-bit Prefetchable Memory addressing.
15:4	PreBase	RW 0x0	Prefetchable Memory Base Defines the bottom address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base address upper 32-bit register specifies the bit [63:32] of the 64-bit prefetchable memory address.
19:16	PreLimitType	RO 0x1	Prefetchable Memory Limit Defines the top address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable-limit upper 32-bit register specifies the bit [63:32] of the 64-bit prefetchable memory address. **NOTE:** If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus. **NOTE:**

Table 38: Prefetchable Memory Limit and Prefetchable Memory Base Register (Continued)
Offset: 0x00024

Bit	Field	Type/InitVal	Description
31:20	PreLimit	RW 0x0	Prefetchable Memory Limit Defines the top address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. **NOTE:** If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus. **NOTE:**

Table 39: Prefetchable Base Upper 32 Bits Register
Offset: 0x00028

Bit	Field	Type/InitVal	Description
31:0	PreBaseUp	RW 0x0	Prefetchable Memory-base Upper 32 Bits Defines the upper 32 bits of the bottom address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other.

Table 40: Prefetchable Limit Upper 32 Bits Register
Offset: 0x0002C

Bit	Field	Type/InitVal	Description
31:0	PreLimitUp	RW 0x0	Prefetchable Memory-limit Upper 32 Bits. Defines the upper-limit of the 64-bit prefetchable memory address range that determines when to forward memory transactions from one interface to the other.

Table 41: I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits
Offset: 0x00030

Bit	Field	Type/InitVal	Description
15:0	IOBaseUp	RW 0x0	I/O Base Upper 16 Bits Defines the upper 16 bits of the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other.
31:16	IOLimitUp	RW 0x0	I/O Limit Upper 16 Bits Defines the upper-limit address of the 32-bit I/O memory address range that determines when to forward I/O transactions from one interface to the other.

Table 42: Capabilities Pointer Register
Offset: 0x00034

Bit	Field	Type/InitVal	Description
7:0	CapPtr	RO 0x40	Capability List Pointer The current value in this field points to the PCI Power Management capability set in Power Management Capability Header at offset 0x40.
31:8	Reserved	RSVD 0x0	Reserved

Table 43: Forward Bridge Control Interrupt Pin and Interrupt Line Register
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
7:0	IntLine	RW 0x0	Provides interrupt line routing information.
15:8	IntPin	RO 0x0	Indicates that the 88SB2211 does not implement a virtual interrupt pin.
16	SecPerrResEn	RW 0x0	Secondary Parity Error Response Enable Controls the response of the bridge to uncorrectable address, attribute, and data errors on the secondary interface. If this bit is set, the bridge takes its normal action when an uncorrectable address, attribute, or data error is detected. If this bit is cleared, the bridge ignores any uncorrectable address, attribute, and data errors that it detects and continue normal operation. The bridge generates parity even if parity error reporting is disabled. Also, the bridge forwards poisoned data from conventional PCI to PCI Express as an uncorrectable conventional PCI data error, regardless of the setting of this bit. 0 = Ignore: uncorrectable address, attribute, and data errors on the secondary interface. 1 = Enable: uncorrectable address, attribute, and data error detection and reporting on the secondary interface.
17	SecSerrEn	RW 0x0	Secondary PCI_SERRn Enable Controls the forwarding of secondary interface PCI_SERRn assertions to the primary interface. The bridge transmits an ERR_FATAL or ERR_NONFATAL message, according to the severity level, on the primary interface when all of the following are true: - PCI_SERRn is asserted on the secondary interface. - This bit is set or Advanced Error Reporting is supported and the PCI_SERRn Assertion Detected Mask bit is clear in the Secondary Uncorrectable Error Mask register. - The PCI_SERRn Enable bit is set in the Command register or the PCI Express-specific bits are set in the Device Control register of the PCI Express Capability Structure. 0 = Disable: the forwarding of PCI_SERRn from the secondary interface to ERR_FATAL and ERR_NONFATAL (PCI_SERRn might still be forwarded if the SERR Advanced Error mask bit is cleared). 1 = Enable: the forwarding of secondary PCI_SERRn to ERR_FATAL or ERR_NONFATAL.

Table 43: Forward Bridge Control Interrupt Pin and Interrupt Line Register (Continued)
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
18	IsaEn	RW 0x0	ISA Enable Controls the response of the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. 0 = Downstream: Forward downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers. 1 = Upstream: Forward upstream ISA I/O addresses in the address range defined by the I/O Base and I/O Limit registers that are in the first 64 KB of the PCI I/O address space (top 768 bytes of each 1-KB block).
19	VgaEn	RW 0x0	VGA Enable Controls the response of the bridge to VGA-compatible addresses. If this bit is set, the bridge forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to the primary interface): - Memory accesses in the range 000A 0000h to 000B FFFFh - I/O addresses in the first 64 KB of the I/O address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases). Address[15:10] may possess any value and is not used in the decoding. If the VGA Enable bit is set, forwarding of VGA addresses is independent of the value of the ISA Enable bit (located in the Bridge Control, Interrupt Pin and Interrupt Line), the I/O address range and memory address ranges defined by the I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits, the Memory Limit and Memory Base, and the Prefetchable Memory Limit and Prefetchable Memory Base of the bridge. The forwarding of VGA addresses is qualified by the <IOEn> and <MemEn> bits in the Command and Status. 0 = DoNotForward: VGA compatible memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges. 1 = Forward: VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the <IOEn> and <MemEn> bits are set) independent of the I/O and memory address ranges and independent of the <IsaEn> bit in this register.
20	Vga16BitDec	RW 0x0	VGA 16-bit Decode This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if the VGA Enable bit in this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. This read/write bit enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary whenever the VGA Enable bit is set to 1. 0 = 10-bit_address: Execute 10-bit address decodes on VGA I/O accesses. 1 = 16-bit_address: Execute 16-bit address decodes on VGA I/O accesses.

Table 43: Forward Bridge Control Interrupt Pin and Interrupt Line Register (Continued)
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
21	MAMode	RW 0x0	Master-Abort Mode Controls the behavior of a bridge when it receives a Master-Abort termination (e.g., an Unsupported Request on PCI Express) on either interface. 0 = DoNotReport: Master-Aborts. When a UR response is received from PCI Express for non-posted transactions, return FFFF FFFFh on reads and complete I/O writes normally. When a Master-Abort is received on the secondary interface for posted transactions initiated from the primary interface, no action is taken (i.e., all data is discarded). 1 = Report: UR Completions from PCI Express by signaling Target-Abort on the secondary interface. For posted transactions initiated from the primary interface and Master-Aborted on the secondary interface, the bridge returns an ERR_NONFATAL (by default) or ERR_FATAL transaction (provided the <SErrEn> bit is set in the Command and Status). The severity is selectable according to the Advanced Error Reporting Capability.
22	SecBusRst	RW 0x0	Secondary Bus Reset Forces the assertion of RST_OUTn on the secondary interface. The secondary RST_OUTn is asserted by the bridge whenever this bit is set. The primary bus interface and all configuration space registers are not affected by the setting of this bit. **NOTE:** RST_OUTn is asserted for as long as this bit is set, and software must observe proper PCI reset timing requirements. 0 = DoNotForce: Assertion of RST_OUTn is not forced. 1 = Force: Assertion of RST_OUTn is forced.
23	ScFbtbEn	RSVD 0x0	PCI Fast Back-to-Back Enable Controls ability of the bridge to generate fast back-to-back transactions to different devices on the PCI interface.
24	PrDT	RSVD 0x0	Primary Discard Timer Does not apply to PCI Express devices.
25	SecDT	RW 0x0	Secondary Discard Timer Controls the number of PCI clock cycles that the bridge waits for a master on the secondary interface to repeat a Delayed Transaction request. The counter starts once the Completion (PCI Express Completion associated with the Delayed Transaction Request) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the secondary bus). If the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and set the Discard Timer Status bit. 0 = 2^15_PCI: The Secondary Discard Timer counts 2^15 PCI clock cycles. 1 = 2^10_PCI: The Secondary Discard Timer counts 2^10 PCI clock cycles.

Table 43: Forward Bridge Control Interrupt Pin and Interrupt Line Register (Continued)
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
26	DTStt	RW1C 0x0	Discard Timer Status This bit is set to a 1 when the Secondary Discard Timer expires and a Delayed Completion is discarded from a queue in the bridge. 0 = No_discard: timer error 1 = Discard: timer error
27	DTSerrEn	RW 0x0	Discard Timer PCI_SERRn Enable This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the PCI Express interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge. The severity is selectable according to the Advanced Error Reporting Capability. 0 = DoNotGenerate: ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the Secondary Discard Timer. Note that an error message can still be sent if the Delayed Transaction Discard Timer Expired Mask bit in the Advanced Error Reporting Capability is clear. 1 = Generate: ERR_NONFATAL or ERR_FATAL on the primary interface if the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge.
31:28	Reserved	RSVD 0x0	Reserved

Table 44: Power Management Capability Header Register
Offset: 0x00040

Bit	Field	Type/InitVal	Description
7:0	CapID	RO 0x01	Capability ID Current value identifies the PCI Power Management capability.
15:8	NextPtr	RO 0x48	Next Item Pointer Current value points to PCI Express capability.
18:16	PMCVer	RO 0x2	PCI Power Management Capability Version
20:19	Reserved	RO 0x0	PME Clock Does not apply to PCI Express. This field is hardwired to 0.
21	DSI	RO 0x0	Device Specific Initialization The 88SB2211 does not requires device specific initialization.
24:22	AuxCur	RO 0x1	Auxiliary Current Requirements The 88SB2211 does not require current from VAUX in D3cold state.

Table 44: Power Management Capability Header Register (Continued)
Offset: 0x00040

Bit	Field	Type/InitVal	Description
25	D1Sup	RO 0x1	D1 Support The 88SB2211 supports D1 Power Management state.
26	D2Sup	RO 0x1	D2 Support The 88SB2211 supports D2 Power Management state.
31:27	PMESup	RO 0x1F	Power Management Event (PME) Support The 88SB2211 supports PME generation from D0, D1, D2, D3cold Power Management states.

Table 45: Forward Bridge Power Management Control and Status Register
Offset: 0x00044

Bit	Field	Type/InitVal	Description
1:0	PMState	RW 0x0	Power State This field controls the Power Management state of the 88SB2211. The device supports all Power Management states. **NOTE:** A transition from state D3 to state D0 causes an internal reset to occur. In states D1, D2 and D3hot, PCI Express memory and I/O accesses are disabled, as well as the interrupt emulation messages, and only configuration cycles are allowed. 0 = D0 1 = D1 2 = D2 3 = D3
7:2	Reserved_7_2	RSVD 0x0	Reserved
8	PME_en	RW 0x0	PME Enable Controls PM_PME Message Generation. **NOTE:** Power ON Sticky bit--not initialized by either fundamental or hot reset. 0 = Disabled 1 = Enabled
12:9	PMDataSel	RO 0x0	Data Select Data register is not implemented.
14:13	PMDataScale	RO 0x0	Data Scale Data register is not implemented.

Table 45: Forward Bridge Power Management Control and Status Register (Continued)
Offset: 0x00044

Bit	Field	Type/InitVal	Description
15	PME_Stat	RW1C 0x0	In forward mode the 88SB2211 does not generate Power Management events (PME). This field is hardwired to 0. **NOTE:** PME events are forwarded from the PCI port to the PCI Express port, but this is not reflected in this field as those events are not generated by the 88SB2211.
21:16	Reserved_21_16	RSVD 0x0	Reserved
22	B2B3Sup	RO 0x1	B2_B3 Support for D3hot When set, indicates that, when the bridge is programmed to D3hot, its secondary bus PCI clock is stopped and driven to 0 (B2). When cleared, indicates that, when the bridge is programmed to D3hot, its secondary bus has its power removed and its PCI clocks stopped (B3). This bit is only meaningful if the <BPCCEn> bit is set. **NOTE:** The 88SB2211 does not control the power of the PCI bus, and, therefore, is reporting B2 support. If the system supports PCI power removal upon D3, this field should be set to 0x0 via the TWSI serial initialization process. (This bit can be written from the TWSI port).
23	BPCCEn	RO 0x1	Bus Power/clock Control Enable When set, indicates that the bus power/clock control mechanism, as defined in section 4.7.1 of the PCI Power Management specification 1.1, is enabled. The Bstate and the secondary clocks are controlled accordingly. **NOTE:** To disable the Bus Power Clock Control, this field should be set to 0x0 via the TWSI serial initialization process. (This bit can be written from the TWSI port). **NOTE:** Shutting down the PCI Express clock out for Power management events by default is not enabled.
31:24	PMData	RO 0x0	Power Management Data Data register is not implemented.

Table 46: Forward Bridge PCI Express Capability Register
Offset: 0x00048

Bit	Field	Type/InitVal	Description
7:0	CapID	RO 0x10	Capability ID The current value of this field identifies the PCI Express capability.
15:8	NextPtr	RO 0x0	Next Item Pointer The current value of this field points to the end of the capability list (NULL).

Table 46: Forward Bridge PCI Express Capability Register (Continued)
Offset: 0x00048

Bit	Field	Type/InitVal	Description
19:16	CapVer	RO 0x1	Capability Version This field indicates the PCI Express Base spec 1.0a version of the PCI-Express capability.
23:20	DevType	RO 0x7	Device/Port Type PCI Express to PCI/PCI-X Bridge
24	SlotImp	RO 0x0	Slot Implemented
29:25	IntMsgNum	RO 0x0	Interrupt Message Number
31:30	Reserved	RSVD 0x0	Reserved

Table 47: Forward Bridge PCI Express Device Capabilities Register
Offset: 0x0004C

Bit	Field	Type/InitVal	Description
2:0	MaxPldSizeSup	RO 0x0	Maximum Payload Size Supported 128B MPS support. This bit is hardwired to 0.
4:3	PhntmFncSup	RO 0x0	Phantom Functions Support Phantom Functions are not supported. This bit is hardwired to 0.
5	ExtTagSup	RO 0x0	Extended Tag Field Support Extended tag is not supported. This bit is hardwired to 0.
11:6	Reserved_11_6	RSVD 0x0	Reserved
12	AttButPrs	RO 0x0	Attention Button Present The 88SB2211 does not support Attention Button. This bit is hardwired to 0.
13	AttIndPrs	RO 0x0	Attention Indicator Present The 88SB2211 does not support Attention Indicator This bit is hardwired to 0.

Table 47: Forward Bridge PCI Express Device Capabilities Register (Continued)
Offset: 0x0004C

Bit	Field	Type/InitVal	Description
14	PwrIndPrs	RO 0x0	Power Indicator Present The 88SB2211 does not support Attention Indicator. This bit is hardwired to 0.
15	Role-Based Error Reporting	RO 0x0	The 88SB2211 does not support Role Based Error Reporting.
17:16	Reserved_17_16	RSVD 0x0	Reserved
25:18	CapSPLVal	RO 0x0	Captured Slot Power Limit Value
27:26	CapSPLScl	RO 0x0	Captured Slot Power Limit Scale
31:28	Reserved_31_28	RSVD 0x0	Reserved

Table 48: Forward Bridge PCI Express Device Control Status Register
Offset: 0x00050

Bit	Field	Type/InitVal	Description
0	CorErrRepEn	RW 0x0	Correctable Error Reporting Enable Controls error message generation on behalf of errors on both the PCI Express and conventional PCI interfaces. 0 = Masked: ERR_COR error messages are masked. Status bit is not masked. 1 = Enabled: ERR_COR error messages enabled.
1	NFErrRepEn	RW 0x0	Non-Fatal Error Reporting Enable Controls error message generation on behalf of errors on both the PCI Express and conventional PCI interfaces. **NOTE:** ERR_NONFATAL error messages are still enabled when this field is 0, if the <SErrEn> bit in the Command and Status is set. 0 = Masked: ERR_NONFATAL error messages are masked. Status bit is not masked. 1 = Enabled: ERR_NONFATAL error messages enabled.
2	FErrRepEn	RW 0x0	Fatal Error Reporting Enable Controls error message generation on behalf of errors on both the PCI Express and conventional PCI interfaces. **NOTE:** ERR_FATAL error messages are still enabled when this field is 0, if the <SErrEn> bit in the Command and Status is set. 0 = Masked: ERR_FATAL error messages are masked. Status bit is still affected. 1 = Enabled: ERR_FATAL error messages enabled.

Table 48: Forward Bridge PCI Express Device Control Status Register (Continued)
Offset: 0x00050

Bit	Field	Type/InitVal	Description
3	URRepEn	RW 0x0	Unsupported Request (UR) Reporting Enable Controls error reporting on behalf of Unsupported Request errors detected on the PCI Express interface only. **NOTE:** UR related error messages are still enabled when URRepEn=0, if the <SErrEn> bit in the Command and Status is set. 0 = Masked: UR related error messages are masked. Status bit is not masked. 1 = Enabled: UR related error messages enabled.
4	EnRO	RO 0x0	Enable Relaxed Ordering The 88SB2211 never sets the Relaxed Ordering attribute in transactions it initiates as a requester. This bit is hardwired to 0.
7:5	MaxPldSz	RW 0x0	Maximum Payload Size The maximum payload size supported is 128B (refer to bit <MaxPldSizeSup> in the PCI Express Device Capabilities). 0 = 128B 1-7 Reserved
8	Reserved_8	RO 0x0	Extended Tag Field Enabled Not supported. This bit is hardwired to 0.
9	Reserved_9	RO 0x0	Phantom Function Enable Not supported. This bit is hardwired to 0.
10	AuxPwrEn	RW 0x0	Auxiliary (AUX) Power PM Enable Controls allocation of AUX power to the device. **NOTE:** Power On Reset Sticky bit is not initialized by either fundamental or hot reset. 0 = Disabled: Vaux is not allocated. 1 = Enabled: Vaux is allocated.
11	EnNS	RO 0x0	Enable No Snoop The 88SB2211 never sets the No Snoop attribute in transactions it initiates as a requester. This bit is hardwired to 0.
14:12	MaxRdRqSz	RW 0x2	Maximum Read Request Size This field limits the 88SB2211 maximum read request size as a requestor (master). 0 = 128B 1 = 256B 2 = 512B 3 = 1_KB 4 = 2_KB 5 = 4_KB

Table 48: Forward Bridge PCI Express Device Control Status Register (Continued)
Offset: 0x00050

Bit	Field	Type/InitVal	Description
15	BrCRSEn	RW 0x0	Bridge Configuration Retry Enable When set, this bit enables the 88SB2211 to return Configuration Request Retry Status (CRS) in response to a Configuration Request that targets a device below the bridge.
16	CorErrDet	RW1C 0x0	Correctable Error Detected This bit indicates the status of the correctable errors detected by the 88SB2211. It set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
17	NFErrDet	RW1C 0x0	Non-Fatal Error Detected This bit indicates the status of the Non-Fatal errors detected by the 88SB2211. It is set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
18	FErrDet	RW1C 0x0	Fatal Error Detected This bit indicates the status of the Fatal errors detected by the 88SB2211. It is set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
19	URDet	RW1C 0x0	Unsupported Request Detected This bit indicates that the 88SB2211 receives an unsupported request. It is set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
20	AuxPwrDet	RO 0x0	AUX Power Detected Indicates that the 88SB2211 detected AUX power.
21	TransPend	RO 0x0	Transactions Pending The 88SB2211 does not issue non-posted requests on its own behalf. This bit is hardwired to 0.
31:22	Reserved_31_22	RSVD 0x0	Reserved

Table 49: Forward Bridge PCI Express Link Control Status Register
Offset: 0x00058

Bit	Field	Type/InitVal	Description
1:0	aspm_cnt	RW 0x0	Active State Link PM Control This field controls the level of active state PM supported on the link. 0 = Disabled 1 = L0s_entry_supported 2 = Reserved 3 = L0s_L1_entry_supported
2	Reserved_2	RSVD 0x0	Reserved
3	RCB	RO 0x0	Read Completion Boundary Not applicable to the 88SB2211. This bit is hardwired to 0.
4	Reserved_4	RO 0x0	RESERVED
5	Reserved_5	RO 0x0	RESERVED
6	CmnClkCfg	RW 0x0	Common Clock Configuration When set by software, this bit indicates that both devices on the link use a distributed common reference clock.
7	ExtdSnc	RW 0x0	Extended Sync When set, this bit forces extended transmission of 4096 FTS ordered sets followed by a single skip ordered set in exit from L0s and extra (1024) TS1 at exit from L1. **NOTE:** This bit is used for test and measurement only. **NOTE:**
15:8	Reserved_15_8	RSVD 0x0	Reserved
19:16	LnkSpd	RO 0x1	Link Speed The only link speed available is 2.5 Gbps. 0 = Reserved 1 = 2.5 Gbps 2-15 = Reserved The value of this field is undefined when the link is not up.
25:20	NegLnkWdth	RO 0x0	Negotiated Link Width The only link width available is x1. 0 = Reserved 1 = x1 2-63 = Reserved The value of this field is undefined when the link is not up.
26	Reserved_26	RO 0x0	Reserved

Table 49: Forward Bridge PCI Express Link Control Status Register (Continued)
Offset: 0x00058

Bit	Field	Type/InitVal	Description
27	LnkTrn	RO 0x0	Link Training This bit indicates that link training is in progress. This bit is cleared once link training is complete.
28	SltClkCfg	RO 0x1	Slot Clock Configuration . 0 = IndependentClock: The 88SB2211 uses an independent clock, irrespective of the presence of a reference clock on the connector. 1 = ReferenceClock: The 88SB2211 uses the reference clock that the platform provides.
31:29	Reserved_31_29	RSVD 0x0	Reserved

A.3.2 Forward Bridge Mode Device Specific

Table 50: Forward Bridge PCI Internal Arbiter Control Register
Offset: 0x00070

Bit	Field	Type/InitVal	Description
0	InternalArbEN	RO SAR	Enable Internal Arbiter Operation **NOTE:** Initial value is strapped on reset, from PCI_GNT1n signal. 0 = Disable 1 = Enable
1	BrokenDetEn	RW 0x0	Broken Master Detection Enable If set to 1, broken master detection is enabled. A master is said to be broken if it fails to respond to grant assertion within a timeout specified in <BrokenValue> field. 0 = Disabled: Broken Master Detection Disabled 1 = Enabled: Broken Master Detection Enabled
5:2	BrokenValue	RW 0xF	Broken Master Detection Value The value sets the maximum number of PCI clock cycles that the arbiter waits for a PCI master to respond to its grant assertion. If a PCI master fails to assert PCI_FRAMEn within this time, the PCI arbiter aborts the transaction and performs a new arbitration cycle. 0-3 = Reserved. Do not use. 4 = Allows 2 PCI clock cycles for a broken master detection. 5 = Allows 3 PCI clock cycles for a broken master detection. ... 16 = Allows 13 PCI clock cycles for a broken master detection. **NOTE:** The set value must be greater than 3.

Table 50: Forward Bridge PCI Internal Arbiter Control Register (Continued)
Offset: 0x00070

Bit	Field	Type/InitVal	Description
6	BrokenDet	RW1C 0x0	Broken Master Detected Reports if a broken master was detected. This bit is set upon Broken Master Detection. It remains asserted until cleared by writing 1. 0 = Detected: Broken Master was detected. 1 = Not Detected: Broken Master was not detected.
7	Reserved_7	RSVD 0x0	Reserved
14:8	ParkingDis	RW 0x0	Parking Disable **NOTE:** The arbiter parks on the last master granted unless disabled through the ParkingDis bit. When ParkingDis is all 1s, the PCI arbiter parks on the internal PCI master. ParkingDis[0] corresponds to the internal PCI master. ParkingDis[x] corresponds to external agent x (REQn or GNTn signals). 0 = Enabled: Parking on the associated PCI master is enabled. 1 = Disabled: Parking on the associated PCI master is disabled.
15	RESERVED_15	RW 0x1	Reserved
16	RESERVED_16	RW 0x1	Reserved
31:17	Reserved_31_17	RSVD 0x0	Reserved

Table 51: GPIO Control Register
Offset: 0x00074

Bit	Field	Type/InitVal	Description
7:0	GPIOOutEn	RW 0x0	General Purpose I/O Output Enable Controls the direction of the GPIO signal. By default all GPIO pins are inputs. **NOTE:** GPIOOutEn[N] controls GPIO[N] pin, N=0..7 0 = Input 1 = Output
15:8	GPIODataOut	RW 0x0	General Purpose I/O Data Out Controls the data driven on the GPIO pins, when configured as an output by the <GPIOOutEn> field. **NOTE:** GPIODataOut[N] controls GPIO[N] pin, N=0..7
23:16	GPIODataIn	RO 0x0	General Purpose I/O Data In Reads the current state of the GPIO pin. Valid only when GPIO pin is configured as an input by the <GPIOOutEn> field. **NOTE:** GPIODataIn[N] reads GPIO[N] pin, N=0..7

Table 51: GPIO Control Register (Continued)
Offset: 0x00074

Bit	Field	Type/InitVal	Description
31:24	Reserved	RSVD 0x0	Reserved

Table 52: Forward Bridge PCI Clock Output Control Register
Offset: 0x00078

Bit	Field	Type/InitVal	Description
0	ClockOutDis0	RW SAR	PCI Clock Out 0 Disable Controls the activation of PCI_CLK_OUT[0]. When set, PCI_CLK_OUT[0] is driven to 0. The initial value of this field is sampled at reset from PCI_REQn[0] pin. Refer to the Reset Strapping in Section "Reset Configuration". 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
1	ClockOutDis1	RW SAR	PCI Clock Out 1 Disable Controls the activation of PCI_CLK_OUT[1]. When set, PCI_CLK_OUT[1] is driven to 0. The initial value of this field is sampled at reset from PCI_REQn[1] pin. Refer to the Reset Strapping in Section "Reset Configuration". 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
2	ClockOutDis2	RW SAR	PCI Clock Out 2 Disable Controls the activation of PCI_CLK_OUT[2]. When set, PCI_CLK_OUT[2] is driven to 0. The initial value of this field is sampled at reset from PCI_REQn[2] pin. Refer to Reset Strapping in Section "Reset Configuration". 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
3	ClockOutDis3	RW SAR	PCI Clock Out 3 Disable Controls the activation of PCI_CLK_OUT[3]. When set, PCI_CLK_OUT[3] is driven to 0. The initial value of this field is sampled at reset from PCI_REQn[3] pin. Refer to Reset Strapping in Section "Reset Configuration". 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
4	ClockOutDis4	RW SAR	PCI Clock Out 4 Disable Controls the activation of PCI_CLK_OUT[4]. When set, PCI_CLK_OUT[4] is driven to 0. The initial value of this field is sampled at reset from PCI_REQn[4] pin. Refer to Reset Strapping in Section "Reset Configuration". 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled

Table 52: Forward Bridge PCI Clock Output Control Register (Continued)
Offset: 0x00078

Bit	Field	Type/InitVal	Description
5	ClockOutDis5	RW SAR	PCI Clock Out 5 Disable Controls the activation of PCI_CLK_OUT[5] When set, PCI_CLK_OUT[5] is driven to 0. The initial value of this field is sampled at reset from PCI_REQn[4:0] pins. If all are strapped low, PCI_CLK_OUT[5] is disabled. Refer to Reset Strapping in Section "Reset Configuration". 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
31:6	Reserved	RSVD 0x0	Reserved

Table 53: Forward Bridge Prefetch and CRS Control Register
Offset: 0x00080

Bit	Field	Type/InitVal	Description
1:0	MrmPrftchMd	RW 0x3	Read Multiple Prefetch Mode 0 = Prefetch_disabled 1 = Prefetch_enabled 2 = Reserved 3 = Aggressive_Prefetch_enabled
2	MrmAggrInitWM	RW 0x1	Memory Read Multiple Aggressive Prefetch Initial Read Water Mark Controls the number of 128-bytes buffers to be pre-fetched initially. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = Two: The 88SB2211 pre-fetches two 128-bytes buffers initially. 1 = Three: The 88SB2211 pre-fetches three 128-bytes buffers initially.
5:3	MrmAggrNextWM	RW 0x0	Memory Read Multiple Aggressive Prefetch Next Read Watermark Controls the criteria for issuing the next prefetch read request on the PCI Express interface. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One data cycle: Fetch next buffer after one data cycle is driven on the bus. 1 = Two data cycles: Fetch next buffer after two data cycles are driven on the bus. 2 = Three data cycles: Fetch next buffer after three data cycles are driven on the bus. 3 = Four data cycles: Fetch next buffer after four data cycles are driven on the bus. 4 = Five data cycles: Fetch next buffer after five data cycles are driven on the bus. 5 = Six data cycles: Fetch next buffer after six data cycles are driven on the bus. 6 = Seven data cycles: Fetch next buffer after seven data cycles are driven on the bus. 7 = Eight data cycles: Fetch next buffer after eight data cycles are driven on the bus.

Table 53: Forward Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
6	MrmAggrResWM	RW 0x0	Memory Read Multiple Aggressive Prefetch Response Watermark Controls the criteria for responding to the delayed read on the PCI bus. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One: The 88SB2211 drives read data on the bus as soon as it has one 128-byte read buffer. 1 = Two: The 88SB2211 drives read data on the bus as soon as it has two 128-byte read buffers.
7	Reserved_7	RO 0x1	Reserved
9:8	MrlPrftchMd	RW 0x1	Memory Read Line Prefetch Mode 0 = Prefetch_disabled 1 = Prefetch_enabled 2 = Reserved 3 = Aggressive_Prefetch_enabled
10	MrlAggrInitWM	RW 0x0	Memory Read Line Aggressive Prefetch Initial Read Watermark Controls the number of 128-bytes buffers to be pre-fetched initially. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = Two: The 88SB2211 pre-fetches two 128-bytes buffers initially. 1 = Three: The 88SB2211 pre-fetches three 128-bytes buffers initially.
13:11	MrlAggrNextWM	RW 0x0	Memory Read Line Aggressive Prefetch Next Read Watermark Controls the criteria for issuing the next prefetch read request on the PCI Express interface. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One data cycle: Fetch next buffer after one data cycle is driven on the bus. 1 = Two data cycles: Fetch next buffer after two data cycles are driven on the bus. 2 = Three data cycles: Fetch next buffer after three data cycles are driven on the bus. 3 = Four data cycles: Fetch next buffer after four data cycles are driven on the bus. 4 = Five data cycles: Fetch next buffer after five data cycles are driven on the bus. 5 = Six data cycles: Fetch next buffer after six data cycles are driven on the bus. 6 = Seven data cycles: Fetch next buffer after seven data cycles are driven on the bus. 7 = Eight data cycles: Fetch next buffer after eight data cycles are driven on the bus.

Table 53: Forward Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
14	MrlAggrResWM	RW 0x0	Memory Read Multiple Aggressive Prefetch Response Watermark Controls the criteria for responding to the delayed read on the PCI bus. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One: The 88SB2211 drives read data on the bus as soon as it has one 128-byte read buffer. 1 = Two: The 88SB2211 drives read data on the bus as soon as it has two 128-byte read buffers.
15	Reserved_15	RW 0x0	Reserved
17:16	MrPrftchMd	RW 0x0	Memory Read Prefetch Mode 0 = Prefetch_disabled 1 = Prefetch_enabled 2 = Reserved 3 = Aggressive_Prefetch_enabled
18	MrAggrInitWM	RW 0x0	Memory Read Aggressive Prefetch Initial Read Watermark Controls the number of 128-bytes buffers to be pre-fetched initially. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = Two: The 88SB2211 pre-fetches two 128-bytes buffers initially. 1 = Three: The 88SB2211 pre-fetches three 128-bytes buffers initially.
21:19	MrAggrNextWM	RW 0x0	Memory Read Aggressive Prefetch Next Read Watermark Controls the criteria for issuing the next prefetch read request on the PCI Express interface. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One data cycle: Fetch next buffer after one data cycle is driven on the bus. 1 = Two data cycles: Fetch next buffer after two data cycles are driven on the bus. 2 = Three data cycles: Fetch next buffer after three data cycles are driven on the bus. 3 = Four data cycles: Fetch next buffer after four data cycles are driven on the bus. 4 = Five data cycles: Fetch next buffer after five data cycles are driven on the bus. 5 = Six data cycles: Fetch next buffer after six data cycles are driven on the bus. 6 = Seven data cycles: Fetch next buffer after seven data cycles are driven on the bus. 7 = Eight data cycles: Fetch next buffer after eight data cycles are driven on the bus.

Table 53: Forward Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
22	MrAggrResWM	RW 0x0	Memory Read Aggressive Prefetch Response Watermark Controls the criteria for responding to the delayed read on the PCI bus. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One: The 88SB2211 drives read data on the bus as soon as it has one 128-byte read buffer. 1 = Two: The 88SB2211 drives read data on the bus as soon as it has two 128-byte read buffers.
23	Reserved_23	RW 0x0	Reserved
24	Reserved_24	RW 0x1	Reserved Always write 1.
25	Reserved_25	RW 0x1	Reserved Always write 1.
26	Reserved_26	RW 0x0	Reserved Always write 0.
27	Reserved_27	RW 0x0	Reserved Always write 0.
28	Reserved_28	RW 0x0	Reserved
29	Reserved_29	RW 0x0	Reserved
31:30	Reserved_31_30	RW 0x0	Reserved

Table 54: Marvell Diagnostic PCI Express PHY Indirect Access Register
Offset: 0x000F4

Bit	Field	Type/InitVal	Description
31:0	Reserved	RSVD 0x84CCE5	Reserved

Table 55: Marvell Diagnostic Indirect Address Register
Offset: 0x000F8

Bit	Field	Type/InitVal	Description
1:0	Reserved	RSVD 0x0	Reserved

Table 55: Marvell Diagnostic Indirect Address Register (Continued)
Offset: 0x000F8

Bit	Field	Type/InitVal	Description
13:2	Address	RW 0x0	Reserved **NOTE:** For Marvell usage only.
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 56: Marvell Diagnostic Indirect Data Register
Offset: 0x000FC

Bit	Field	Type/InitVal	Description
31:0	Data	RO 0x0	Reserved **NOTE:** For Marvell usage only.

A.3.3 Forward Bridge Mode Extended Configuration Space

Table 57: PCI Express Advanced Error Report Header Register
Offset: 0x00100

Bit	Field	Type/InitVal	Description
15:0	PECapID	RO 0x1	Extended Capability ID The current value of this field identifies the Advanced Error Reporting capability.
19:16	CapVer	RO 0x1	Capability Version
31:20	NextPtr	RO 0x0	Next Item Pointer This field indicates the last item in the extended capabilities linked list.

Table 58: PCI Express Uncorrectable Error Status Register
Offset: 0x00104

Bit	Field	Type/InitVal	Description
3:0	Reserved	RSVD 0x0	Reserved
4	DLPrtErr	RW1C 0x0	Data Link Protocol Error Status

Table 58: PCI Express Uncorrectable Error Status Register (Continued)
Offset: 0x00104

Bit	Field	Type/InitVal	Description
11:5	Reserved	RSVD 0x0	Reserved
12	RPsnTlpErr	RW1C 0x0	Poisoned TLP Status
13	FCPrtErr	RW1C 0x0	Flow Control Protocol Error Status Set upon DLLP update timeout (200s with no FC DLLP received).
14	CmpTOErr	RW1C 0x0	Completion Timeout Status
15	CAErr	RW1C 0x0	Completer Abort Status
16	UnexpCmpErr	RW1C 0x0	Unexpected Completion Status
17	Reserved	RSVD 0x0	Reserved
18	MalfTlpErr	RW1C 0x0	Malformed TLP Status
19	Reserved	RSVD 0x0	Reserved
20	URErr	RW1C 0x0	Unsupported Request Error Status
31:21	Reserved	RSVD 0x0	Reserved

Table 59: PCI Express Uncorrectable Error Mask Register
Offset: 0x00108

Bit	Field	Type/InitVal	Description
3:0	Reserved	RSVD 0x0	Reserved

Table 59: PCI Express Uncorrectable Error Mask Register (Continued)
Offset: 0x00108

Bit	Field	Type/InitVal	Description
4	DLPrtErrMsk	RW 0x0	Data Link Protocol Error Mask When an error is indicated in the PCI Express Uncorrectable Error Status and the corresponding bit is set: - The header is not logged in the Header Log Register - The First Error Pointer is not updated - An error message is not generated. The status bit is set regardless of the mask setting. 0 = Not_masked 1 = Masked
11:5	Reserved	RSVD 0x0	Reserved
12	RPsnTlpErrMsk	RW 0x0	Poisoned TLP Error Mask
13	FCPrtErrMsk	RW 0x0	Flow Control Protocol Error Mask
14	CmpTOErrMsk	RW 0x0	Completion Timeout Mask
15	CAErrMsk	RW 0x0	Completer Abort Mask
16	UnexpCmpErrMsk	RW 0x0	Unexpected Completion Mask
17	Reserved	RSVD 0x0	Reserved
18	MalfTlpErrMsk	RW 0x0	Malformed TLP Mask
19	Reserved	RSVD 0x0	Reserved
20	URErrMsk	RW 0x0	Unsupported Request Error Mask
31:21	Reserved	RSVD 0x0	Reserved

Table 60: PCI Express Uncorrectable Error Severity Register
Offset: 0x0010C

Bit	Field	Type/InitVal	Description
3:0	Reserved	RSVD 0x1	Reserved
4	DLPrtErrSev	RW 0x1	Data Link Protocol Error Severity Controls the severity indication of the Uncorrectable errors. Each bit controls the error type of the corresponding bit in the PCI Express Uncorrectable Error Status. 0 = Non-Fatal: Error type is Non-Fatal. 1 = Fatal: Error type is Fatal.
11:5	Reserved	RSVD 0x0	Reserved
12	RPsnTlpErrSev	RW 0x0	Poisoned TLP Error Severity
13	FCPrtErrSev	RW 0x1	Flow Control Protocol Error Severity
14	CmpTOErrSev	RW 0x0	Completion Timeout Severity
15	CAErSev	RW 0x0	Completer Abort Severity
16	UnexpCmpErrSev	RW 0x0	Unexpected Completion Severity
17	Reserved	RSVD 0x0	Reserved
18	MalfTlpErrSev	RW 0x1	Malformed TLP Severity
19	Reserved	RSVD 0x0	Reserved
20	URErrSev	RW 0x0	Unsupported Request Error Severity
31:21	Reserved	RSVD 0x0	Reserved

Table 61: PCI Express Correctable Error Status Register
Offset: 0x00110

Bit	Field	Type/InitVal	Description
0	RcvErr	RW1C 0x0	Receiver Error Status When set, this bit indicates that a Receiver error has occurred.
5:1	Reserved	RSVD 0x0	Reserved
6	BadTlpErr	RW1C 0x0	Bad TLP Status
7	BadDllpErr	RW1C 0x0	Bad DLLP Status
8	RplyRllovrErr	RW1C 0x0	Replay Number Rollover Status
11:9	Reserved	RSVD 0x0	Reserved
12	RplyTOErr	RW1C 0x0	Replay Timer Timeout status
31:13	Reserved	RSVD 0x0	Reserved

Table 62: PCI Express Correctable Error Mask Register
Offset: 0x00114

Bit	Field	Type/InitVal	Description
0	RcvMsk	RW 0x0	Receiver Error Mask If set, an error message is not generated upon occurrence of a Receiver error. 0 = Not_masked 1 = Masked
5:1	Reserved_5_1	RSVD 0x0	Reserved
6	BadTlpMsk	RW 0x0	Bad TLP Mask
7	BadDllpErrMsk	RW 0x0	Bad DLLP Mask
8	RplyRllovrMsk	RW 0x0	Replay Number Rollover Mask

Table 62: PCI Express Correctable Error Mask Register (Continued)
Offset: 0x00114

Bit	Field	Type/InitVal	Description
11:9	Reserved_11_9	RSVD 0x0	Reserved
12	RplyTOMsk	RW 0x0	Replay Timer Timeout Mask
13	AdvisoryNonFatalError	RO 0x0	Advisory Non-Fatal Error
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 63: PCI Express Advanced Error Capability and Control Register
Offset: 0x00118

Bit	Field	Type/InitVal	Description
4:0	FrstErrPtr	RO 0x0	First Error Pointer This field reports the bit position of the first error reported in the PCI Express Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself. 4 = FrstErrPtr_4: Data Link Protocol Error 12 = FrstErrPtr_12: Poisoned TLP Error 13 = FrstErrPtr_13: Flow Control Protocol Error 14 = FrstErrPtr_14: Completion Timeout Error 15 = FrstErrPtr_15: Completer Abort Status 16 = FrstErrPtr_16: Unexpected Completion Error 18 = FrstErrPtr_18: Malformed TLP Error 20 = FrstErrPtr_20: Unsupported Request Error
31:5	Reserved	RSVD 0x0	Reserved

Table 64: PCI Express Header Log First DWORD Register
Offset: 0x0011C

Bit	Field	Type/InitVal	Description
31:0	Hdrlog1DW	RO 0x0	Header Log First DWORD Logs the header of the first error reported in the PCI Express Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until the software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself.

Table 65: PCI Express Header Log Second DWORD Register
Offset: 0x00120

Bit	Field	Type/InitVal	Description
31:0	Hdrlog2DW	RO 0x0	Header Log Second DWORD

Table 66: PCI Express Header Log Third DWORD Register
Offset: 0x00124

Bit	Field	Type/InitVal	Description
31:0	Hdrlog3DW	RO 0x0	Header Log Third DWORD

Table 67: PCI Express Header Log Fourth DWORD Register
Offset: 0x00128

Bit	Field	Type/InitVal	Description
31:0	Hdrlog4DW	RO 0x0	Header Log Fourth DWORD

Table 68: PCI Uncorrectable Error Status Register
Offset: 0x0012C

Bit	Field	Type/InitVal	Description
0	Reserved_0	RSVD 0x0	Target-Abort on Split Completion Status Does not apply to conventional PCI.

Table 68: PCI Uncorrectable Error Status Register (Continued)
Offset: 0x0012C

Bit	Field	Type/InitVal	Description
1	Reserved_1	RSVD 0x0	Master-Abort on Split Completion Status Does not apply to conventional PCI.
2	RcvTA	RW1C 0x0	Received Target-Abort Status
3	RcvMA	RW1C 0x0	Received Master-Abort Status
6:4	Reserved_6_4	RSVD 0x0	Reserved
7	UCDataErr	RW1C 0x0	Uncorrectable Data Error Status
8	Reserved_8	RSVD 0x0	Uncorrectable Attribute Error Status Does not apply to conventional PCI.
9	UCAddrErr	RW1C 0x0	Uncorrectable Address Error Status
10	DTExp	RW1C 0x0	Delayed Transaction Discard Timer Expired Status No header log.
11	PerrDetected	RW1C 0x0	PCI_PERRn Assertion Detected
12	SerrDetected	RW1C 0x0	PCI_SERRn Assertion Detected No header log.
13	InternalBrErr	RW1C 0x0	Internal Bridge Error Status No header log.
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 69: Forward Bridge PCI Uncorrectable Error Mask Register
Offset: 0x00130

Bit	Field	Type/InitVal	Description
0	Reserved_1_0	RSVD 0x0	Reserved
1	Reserved_1	RW 0x0	Reserved
2	RcvTAMsk	RW 0x0	Received Target-Abort Mask Status bit is set regardless of the mask setting. 0 = Not_masked 1 = Masked
3	RcvMAMsk	RW 0x1	Received Master-Abort Mask
4	Reserved_4	RSVD 0x0	Reserved
6:5	Reserved_6_5	RW 0x1	Reserved
7	UCDataErrMsk	RW 0x1	Uncorrectable Data Error Mask
8	UCAttrErrMsk	RW 0x1	Uncorrectable Attribute Error Mask
9	UCAddrErrMsk	RW 0x1	Uncorrectable Address Error Mask SAR upon EP/RC mode.
10	DTExp	RW 0x1	Delayed Transaction Discard Timer Expired Mask Header in not Logged. SAR upon EP/RC mode.
11	PerrDetectedMsk	RW 0x0	PCI_PERRn Assertion Detected Mask
12	SerrDetectedMsk	RW 0x1	PCI_SERRn Assertion Detected Mask Header in not logged.
13	InternalBrErrMsk	RW 0x0	Internal Bridge Error Mask No header log.

Table 69: Forward Bridge PCI Uncorrectable Error Mask Register (Continued)
Offset: 0x00130

Bit	Field	Type/InitVal	Description
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 70: PCI Uncorrectable Error Severity Register
Offset: 0x00134

Bit	Field	Type/InitVal	Description
0	Reserved_1_0	RSVD 0x0	Reserved
1	Reserved_1	RW 0x0	Reserved
2	RcvTASev	RW 0x0	Received Target-Abort Severity Controls the severity indication of the PCI Express Secondary Uncorrectable errors. Each bit controls the error type of the corresponding bit in the PCI Express Secondary Uncorrectable Error Status. 0 = Non-Fatal: Error type is Non-Fatal. 1 = Fatal: Error type is Fatal.
3	RcvMASev	RW 0x0	Received Master-Abort Severity
4	Reserved_4	RSVD 0x0	Reserved
6:5	Reserved_6_5	RW 0x2	Reserved
7	UCDataErrSev	RW 0x0	Uncorrectable Data Error Severity
8	UCAttrErrSev	RW 0x1	Uncorrectable Attribute Error Severity
9	UCAddrErrSev	RW 0x1	Uncorrectable Address Error Severity
10	DTExpSev	RW 0x0	Delayed Transaction Discard Timer Expired Severity
11	PerrDetectedSev	RW 0x0	PCI_PERRn Assertion Severity

Table 70: PCI Uncorrectable Error Severity Register (Continued)
Offset: 0x00134

Bit	Field	Type/InitVal	Description
12	SerrDetectedSev	RW 0x1	PCI_SERRn Assertion Severity
13	InternalBrErrSev	RW 0x0	Internal Bridge Error Severity
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 71: PCI Error Capability and Control Register
Offset: 0x00138

Bit	Field	Type/InitVal	Description
4:0	SecUCFrstErrPtr	RO 0x0	PCI Uncorrectable First Error Pointer This field reports the bit position of the first error reported in the PCI Express Secondary Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself. **NOTE:** The bits in this field are sticky bits--they are not initialized or modified by reset.
31:5	Reserved	RSVD 0x0	Reserved

Table 72: PCI Header Log First DWORD Register
Offset: 0x0013C

Bit	Field	Type/InitVal	Description
31:0	SHL_TransAttr	RO 0x0	PCI Header Log First DWORD Logs the header of the first error reported in the PCI Express Secondary Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself. Transaction Attribute The value transferred on AD[31:0] during the attribute phase. This field is not relevant to conventional PCI. This field is hardwired to 0.

Table 73: PCI Header Log Second DWORD Register
Offset: 0x00140

Bit	Field	Type/InitVal	Description
3:0	SHL_TransAttr	RO 0x0	Transaction Attribute The value transferred on PCI_CBE[3:0]n during the attribute phase. This field is not relevant to conventional PCI. This field is hardwired to 0.
7:4	SHL_TransCmdLow	RO 0x0	Transaction Command Lower The 4-bit value transferred on PCI_CBE[3:0]n during the first address phase.
11:8	SHL_TransCmdUp	RO 0x0	Transaction Command Upper The 4-bit value transferred on PCI_CBE[3:0]n during the second address phase of a DAC transaction.
31:12	Reserved	RSVD 0x0	Reserved

Table 74: PCI Header Log Third DWORD Register
Offset: 0x00144

Bit	Field	Type/InitVal	Description
31:0	SHL_AddrLow	RO 0x0	Transaction Address Low. The 32-bit value transferred on AD[31:0] during the first address phase.

Table 75: PCI Header Log Fourth DWORD Register
Offset: 0x00148

Bit	Field	Type/InitVal	Description
31:0	SHL_AddrHigh	RO 0x0	Transaction Address High. The 32-bit value transferred on AD[31:0] during the second address phase. In the case of a 32-bit address, this field is set to zero.

A.4 Reverse Bridge Mode Configuration Registers

The following table provides a summarized list of all of the Reverse Bridge Mode Configuration registers, including the register names, their type, offset, and a reference to the corresponding table and page for a detailed description of each register and its fields.

Table 76: Register Map Table for the Reverse Bridge Mode Configuration Registers

Register Name	Offset	Table and Page
Reverse Bridge Mode Configuration Header		
Device and Vendor ID Register	0x00000	Table 77, p. 99
Reverse Bridge Command and Status Register	0x00004	Table 78, p. 100
Class Code and Revision ID Register	0x00008	Table 79, p. 103
Reverse Bridge BIST Header Type and Cache Line Size Register	0x0000C	Table 80, p. 104
Reverse Bridge PCI Express Secondary Latency Timer and Subordinate Secondary and Primary Bus Numbers Register	0x00018	Table 81, p. 104
Reverse Bridge PCI Express Secondary Status I/O Limit and I/O Base Register	0x0001C	Table 82, p. 105
Memory Limit and Memory Base Register	0x00020	Table 83, p. 106
Prefetchable Memory Limit and Prefetchable Memory Base Register	0x00024	Table 84, p. 107
Prefetchable Base Upper 32 Bits Register	0x00028	Table 85, p. 108
Prefetchable Limit Upper 32 Bits Register	0x0002C	Table 86, p. 108
I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits	0x00030	Table 87, p. 108
Capabilities Pointer Register	0x00034	Table 88, p. 109
Reverse Bridge Control Interrupt Pin and Interrupt Line Register	0x0003C	Table 89, p. 109
Power Management Capability Header Register	0x00040	Table 90, p. 112
Reverse Bridge Power Management Control and Status Register	0x00044	Table 91, p. 113
Reverse Bridge PCI Express Capability Register	0x00048	Table 92, p. 114
Reverse Bridge PCI Express Device Capabilities Register	0x0004C	Table 93, p. 115
Reverse Bridge PCI Express Device Control Status Register	0x00050	Table 94, p. 116
Reverse Bridge PCI Express Link Control Status Register	0x00058	Table 95, p. 118
Reverse Bridge PCI Express Slot Capabilities Register	0x0005C	Table 96, p. 119
Reverse Bridge PCI Express Slot Control Status Register	0x00060	Table 97, p. 121
Reverse Bridge PCI Express Root Control Capabilities Register	0x00064	Table 98, p. 122
Reverse Bridge PCI Express Root Status Register	0x00068	Table 99, p. 123
Reverse Bridge Mode Device Specific		
GPIO Control Register	0x00074	Table 100, p. 124
Reverse Bridge PCI Clock Output Control Register	0x00078	Table 101, p. 124
Reverse Bridge Prefetch and CRS Control Register	0x00080	Table 102, p. 125
Marvell Diagnostic PCI Express PHY Indirect Access Register	0x000F4	Table 103, p. 129

Table 76: Register Map Table for the Reverse Bridge Mode Configuration Registers (Continued)

Register Name	Offset	Table and Page
Marvell Diagnostic Indirect Address Register	0x000F8	Table 104, p. 129
Marvell Diagnostic Indirect Data Register	0x000FC	Table 105, p. 129
Reverse Bridge Mode Extended Configuration Space		
PCI Express Advanced Error Report Header Register	0x00100	Table 106, p. 130
PCI Express Uncorrectable Error Status Register	0x00104	Table 107, p. 130
PCI Express Uncorrectable Error Mask Register	0x00108	Table 108, p. 131
PCI Express Uncorrectable Error Severity Register	0x0010C	Table 109, p. 132
PCI Express Correctable Error Status Register	0x00110	Table 110, p. 133
PCI Express Correctable Error Mask Register	0x00114	Table 111, p. 134
PCI Express Advanced Error Capability and Control Register	0x00118	Table 112, p. 135
PCI Express Header Log First DWORD Register	0x0011C	Table 113, p. 135
PCI Express Header Log Second DWORD Register	0x00120	Table 114, p. 135
PCI Express Header Log Third DWORD Register	0x00124	Table 115, p. 136
PCI Express Header Log Fourth DWORD Register	0x00128	Table 116, p. 136
PCI Uncorrectable Error Status Register	0x0012C	Table 117, p. 136
Reverse Bridge PCI Uncorrectable Error Mask Register	0x00130	Table 118, p. 137
PCI Uncorrectable Error Severity Register	0x00134	Table 119, p. 138
PCI Error Capability and Control Register	0x00138	Table 120, p. 139
PCI Header Log First DWORD Register	0x0013C	Table 121, p. 140
PCI Header Log Second DWORD Register	0x00140	Table 122, p. 140
PCI Header Log Third DWORD Register	0x00144	Table 123, p. 141
PCI Header Log Fourth DWORD Register	0x00148	Table 124, p. 141

A.4.1 Reverse Bridge Mode Configuration Header

Table 77: Device and Vendor ID Register
Offset: 0x00000

Bit	Field	Type/InitVal	Description
15:0	VenID	RO 0x11AB	Vendor ID This field identifies Marvell as the vendor of the device.
31:16	DevID	RO 0x2211	Device ID

Table 78: Reverse Bridge Command and Status Register
Offset: 0x00004

Bit	Field	Type/InitVal	Description
0	IOEn	RW 0x0	I/O Space Enable. Controls the 88SB2211 response as a target to I/O transactions on the primary interface that address a device that resides behind the bridge. **NOTE:** Software should ensure that outstanding transactions involving the bridge are completed prior to disabling this bit. 0 = Disable: Respond to all I/O requests on the primary interface with Master Abort. Forward all I/O transactions from the secondary interface to the primary interface. 1 = Enable: forwarding of I/O requests to the secondary interface.
1	MemEn	RW 0x0	Memory Space Enable Controls the 88SB2211 response as a target to memory accesses on the primary interface that addresses a device that resides behind the bridge in both the non-prefetchable and prefetchable memory ranges. **NOTE:** Software should ensure that outstanding transactions involving the bridge are completed prior to disabling this bit. 0 = Disable: Respond to all Memory Requests on the primary interface with Master Abort. Forward all memory requests from the secondary interface to the primary interface. 1 = Enable: forwarding of memory transactions to the secondary interface.
2	MasEn	RW 0x0	Master Enable Controls the ability of the 88SB2211 to issue memory and I/O read/write requests on the primary interface. Disabling this bit prevents the bridge from issuing any memory or I/O read/write requests on the primary interface. When this bit is zero, 88SB2211 disables response as a target to all memory or I/O transactions on the secondary interface (they cannot be forwarded to the primary interface). This bit does not affect the issuing of completions on the primary interface or the forwarding of completions. **NOTE:** Software should ensure that outstanding transactions involving the bridge are completed prior to disabling this bit. 0 = Disable: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on secondary interface. 1 = Enable: the bridge to operate as a master on the primary interface for memory and I/O transactions forwarded from the secondary interface.
3	Reserved_3	RSVD 0x0	Reserved
4	Reserved_4	RSVD 0x0	Reserved
5	Reserved_5	RSVD 0x0	VGA Palette Snoop Does not apply to PCI Express bridges.

Table 78: Reverse Bridge Command and Status Register (Continued)
Offset: 0x00004

Bit	Field	Type/InitVal	Description
6	PErrRes	RW 0x0	Parity Error Response Enable Controls the response of the bridge to uncorrectable address, attribute, and data errors on the PCI interface. If this bit is set, the bridge takes its normal action when an uncorrectable address, attribute, or data error is detected. If this bit is cleared, the bridge ignores any uncorrectable address, attribute, and data errors that it detects and continue normal operation. The bridge generates parity even if parity error reporting is disabled. Also, the bridge forwards poisoned data from conventional PCI to PCI Express as an uncorrectable conventional PCI data error, regardless of the setting of this bit. 0 = Ignore: uncorrectable address, attribute, and data errors on the secondary interface 1 = Enable: uncorrectable address, attribute, and data error detection and reporting on the secondary interface
7	Reserved_7	RSVD 0x0	Reserved
8	SErrEn	RW 0x0	PCI_SERRn Enable This bit enables the assertion of PCI_SERRn on the PCI interface of the 88SB2211. PCI_SERRn is asserted when any of the following three conditions are true: -Reception of Fatal, Non-Fatal, or Correctable error messages on the PCI Express interface masked by see the Reverse Bridge PCI Express Root Control Capabilities register, bits [2:0] (a dedicated Mask bit for each error message type) - The 88SB2211 detects uncorrectable data in a special cycle transaction on the PCI interface. - The 88SB2211 detects an uncorrectable data error when it is the PCI master of a read transaction, and the read was not poisoned TLP on the PCI Express interface. 0 = Disable: PCI_SERRn assertion on PCI interface is disabled. 1 = Enable: PCI_SERRn assertion on PCI interface is enabled.
9	PrFbtbEn	RW 0x0	Fast Back-to-Back Enable Controls generation of fast back-to-back transactions on the PCI bus. 0 = Disable: generation of fast back-to-back transactions on the PCI interface is disabled. 1 = Enable: generation of fast back-to-back transactions on the PCI interface is enabled.
10	Reserved_10	RSVD 0x0	Interrupt Disable The 88SB2211 has no internal interrupt resources, and therefore, this bit has no effect.
18:11	Reserved_18_11	RSVD 0x0	Reserved

Table 78: Reverse Bridge Command and Status Register (Continued)
Offset: 0x00004

Bit	Field	Type/InitVal	Description
19	Reserved_19	RSVD 0x0	Interrupt Status The 88SB2211 has no internal interrupt resources, and therefore, this bit has no effect.
20	CapList	RO 0x1	Capability List Support This bit indicates that the 88SB2211 configuration header includes capability list.
21	66MHzCap	RO 0x1	66 MHz Capable
22	Reserved_22	RSVD 0x0	Reserved
23	FbtbCap	RO 0x1	PCI fast back-to-back capable. Indicates that the 88SB2211 bridge is able of responding to fast back-to-back transactions on the PCI bus.
24	MasDataPerr	RW1C 0x0	Master Data Parity Error This bit is used to report the detection of an uncorrectable data error by the bridge. This bit is set if the bridge is the bus master of the transaction on the PCI interface, the <PErrRes> bit in the Control register is set, and either of the following two conditions occur: - The bridge asserts PCI_PERRn on a read transaction. - The bridge detects PCI_PERRn asserted on a write transaction. If the <PErrRes> bit is set to zero, this bit is not set when an error is detected.
26:25	DevSelTim	RO 0x1	PCI_DEVSELn Timing Indicates the 88SB2211 device's PCI_DEVSELn timing as Medium. This bit is hardwired to 1.
27	STarAbort	RW1C 0x0	Signaled Target Abort This bit reports the signaling of a Target-Abort termination by the 88SB2211 when it responds as the target of a transaction on its PCI interface.
28	RTAbort	RW1C 0x0	Received Target Abort This bit reports the detection of a Target-Abort termination by the 88SB2211 when it is the master of a transaction on its PCI interface.
29	RMAbort	RW1C 0x0	Received Master Abort. This bit reports the detection of a Master-Abort termination by the 88SB2211 when it is the master of a transaction on its PCI interface.

Table 78: Reverse Bridge Command and Status Register (Continued)
Offset: 0x00004

Bit	Field	Type/InitVal	Description
30	SSysErr	RW1C 0x0	Signalled System Error This bit reports the assertion of PCI_SERRn on the PCI interface of the 88SB2211. This bit is not set if the <SErrEn> field in this register is de-asserted. 0 = Not asserted: PCI_SERRn was not asserted on PCI interface. 1 = Asserted: PCI_SERRn was asserted on PCI interface.
31	DetParErr	RW1C 0x0	Detected Parity Error This bit reports the detection of an uncorrectable address, attribute, or data error by the 88SB2211 on its PCI interface. This bit must be set when any of the following three conditions are true: - The 88SB2211 detects an uncorrectable address error as a potential target. -The 88SB2211 detects an uncorrectable data error when it is the target of a write transaction. - The 88SB2211 detects an uncorrectable data error when it is the PCI master of a read transaction **NOTE:** The bit is set regardless of the state of the <PErrRes> bit in this register. 0 = Not_detected: Uncorrectable address, attribute, or data error not detected on PCI interface 1 = Detected: Uncorrectable address, attribute, or data error detected on PCI interface

Table 79: Class Code and Revision ID Register
Offset: 0x00008

Bit	Field	Type/InitVal	Description
7:0	RevID	RO 0x1	88SB2211 Revision Number
15:8	ProgIF	RO 0x0	Register Level Programming Interface
23:16	SubClass	RO 0x04	88SB2211 Sub class -- PCI-to-PCI bridge
31:24	BaseClass	RO 0x06	88SB2211 Base Class -- Bridge device

Table 80: Reverse Bridge BIST Header Type and Cache Line Size Register
Offset: 0x0000C

Bit	Field	Type/InitVal	Description
7:0	CacheLine	RW 0x00	88SB2211 Cache Line Size This field specifies the system cache line size in units of Dwords. The value in this register is used by the 88SB2211 for the following purposes: 1. To determine the PCI interface command type when forwarding memory read transactions from the PCI Express interface. 2. To determine the read transactions prefetch size of the PCI when acting as target. 8 = 32 Bytes prefetch 16 = 64 Bytes prefetch 32 = 128 Bytes prefetch
15:8	PrLatTimer	RW 0x0	PCI Latency Timer Specifies (in PCI Clock units) the value of the Latency Timer value of the 88SB2211. Used by PCI master when acting as a requester.
23:16	HeadType	RO 0x01	88SB2211 Configuration Header Type Type 1 single-function configuration header.
31:24	BIST	RO 0x00	Built-In Self Test (BIST) The 88SB2211 does not support BIST.

Table 81: Reverse Bridge PCI Express Secondary Latency Timer and Subordinate Secondary and Primary Bus Numbers Register
Offset: 0x00018

Bit	Field	Type/InitVal	Description
7:0	PrimBusNm	RW 0x0	Primary Bus Number
15:8	SecBusNm	RW 0x0	Secondary Bus Number Used for type 1 configuration access handling.
23:16	SubBusNm	RW 0x0	Subordinate Bus Number Used for type 1 configuration access handling.
31:24	Reserved_31_24	RSVD 0x0	Secondary latency Timer Does not apply to PCI Express.

Table 82: Reverse Bridge PCI Express Secondary Status I/O Limit and I/O Base Register
Offset: 0x0001C

Bit	Field	Type/InitVal	Description
3:0	IOBaseType	RO 0x1	I/O Base Type Indicates that the 88SB2211 supports 32-bit I/O addressing.
7:4	IOBase	RW 0x0	I/O Base Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits.
11:8	IOLimitType	RO 0x1	I/O Limit Type Indicates that the 88SB2211 supports 32-bit I/O addressing.
15:12	IOLimit	RW 0x0	I/O Limit Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. The upper 4 bits are writable and correspond to address bits [15:12]. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits. **NOTE:** If there are no I/O addresses on the secondary side of the bridge, this field can be programmed to a smaller value than the <IOBase> field. In that case, the bridge does not forward any I/O transactions from the primary interface to the secondary, and does forward all I/O transactions from the secondary interface to the primary interface. **NOTE:**
20:16	Reserved_20_16	RSVD 0x0	Reserved
21	66MHzCap	RSVD 0x0	Secondary 66 MHz Capable Does not apply to PCI Express devices.
22	Reserved_22	RSVD 0x0	Reserved
23	FbtbCap	RSVD 0x0	Secondary Fast Back-to-Back Transactions Capable Does not apply to PCI Express devices.
24	DataPar	RW1C 0x0	Master Data Parity Error Reports detection of uncorrectable data errors by the 88SB2211. This bit is set when <SecPerrResEn> bit[16] of Reverse Bridge Control Interrupt Pin and Interrupt Line Register is set and either of the following occur: - The 88SB2211 receives a poisoned completion on the PCI Express interface. - The 88SB2211 transmits a poisoned write request on the PCI Express interface.

Table 82: Reverse Bridge PCI Express Secondary Status I/O Limit and I/O Base Register (Continued)
Offset: 0x0001C

Bit	Field	Type/InitVal	Description
26:25	DevSelTim	RSVD 0x0	Secondary PCI_DEVSELn Timing Does not apply to PCI Express.
27	STarAbort	RW1C 0x0	Signaled Target Abort This bit is set when the 88SB2211 generates a completion with Completer Abort Completion Status in response to a request received on the PCI Express interface.
28	RTAbort	RW1C 0x0	Received Target Abort This bit is set when the 88SB2211, as a requester (master), receives a completion with the status Completer Abort.
29	RMAbort	RW1C 0x0	Received Master Abort This bit is set when the 88SB2211 receives a completion with Unsupported Request Completion Status on the PCI Express interface.
30	RSysErr	RW1C 0x0	Received System Error This bit is set when the 88SB2211 receives an ERR_FATAL or ERR_NONFATAL message. This bit is not set if the <SErrEn> field of Command and Status register is not set.
31	DetParErr	RW1C 0x0	Detected Parity Error This bit is set when the 88SB2211 receives a poisoned TLP on the PCI Express interface. **NOTE:** The bit is set regardless of the state of the <PErrRes> bit in this register.

Table 83: Memory Limit and Memory Base Register
Offset: 0x00020

Bit	Field	Type/InitVal	Description
3:0	Reserved	RO 0x0	This bit is hardwired to 0.
15:4	MemBase	RW 0x0	Memory base Defines the bottom address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h

Table 83: Memory Limit and Memory Base Register (Continued)
Offset: 0x00020

Bit	Field	Type/InitVal	Description
19:16	Reserved	RO 0x00	This bit is hardwired to 0.
31:20	MemLimit	RW 0x0	Memory limit Defines the top address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. **NOTE:** If there are no memory-mapped I/O addresses on the secondary side of the bridge, the <MemLimit> field must be programmed to a smaller value than the <MemBase> field. If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus. **NOTE:**

Table 84: Prefetchable Memory Limit and Prefetchable Memory Base Register
Offset: 0x00024

Bit	Field	Type/InitVal	Description
3:0	PerBaseType	RO 0x1	Prefetchable Memory Base Type Indicates that the 88SB2211 supports 64-bit Prefetchable Memory addressing.
15:4	PreBase	RW 0x0	Prefetchable Memory Base Defines the bottom address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base address upper 32-bit register specifies the bit [63:32] of the 64-bit prefetchable memory address.
19:16	PreLimitType	RO 0x1	Prefetchable Memory Limit Defines the top address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable-limit upper 32-bit register specifies the bit [63:32] of the 64-bit prefetchable memory address. **NOTE:** If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus. **NOTE:**

Table 84: Prefetchable Memory Limit and Prefetchable Memory Base Register (Continued)
Offset: 0x00024

Bit	Field	Type/InitVal	Description
31:20	PreLimit	RW 0x0	Prefetchable Memory Limit Defines the top address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. **NOTE:** If there is no prefetchable memory, and there is no memory-mapped I/O on the secondary side of the bridge, then the bridge does not forward any memory transactions from the primary bus to the secondary, and does forward all memory transactions from the secondary bus to the primary bus. **NOTE:**

Table 85: Prefetchable Base Upper 32 Bits Register
Offset: 0x00028

Bit	Field	Type/InitVal	Description
31:0	PreBaseUp	RW 0x0	Prefetchable Memory-base Upper 32 Bits Defines the upper 32 bits of the bottom address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other.

Table 86: Prefetchable Limit Upper 32 Bits Register
Offset: 0x0002C

Bit	Field	Type/InitVal	Description
31:0	PreLimitUp	RW 0x0	Prefetchable Memory-limit Upper 32 Bits. Defines the upper-limit of the 64-bit prefetchable memory address range that determines when to forward memory transactions from one interface to the other.

Table 87: I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits
Offset: 0x00030

Bit	Field	Type/InitVal	Description
15:0	IOBaseUp	RW 0x0	I/O Base Upper 16 Bits Defines the upper 16 bits of the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other.
31:16	IOLimitUp	RW 0x0	I/O Limit Upper 16 Bits Defines the upper-limit address of the 32-bit I/O memory address range that determines when to forward I/O transactions from one interface to the other.

Table 88: Capabilities Pointer Register
Offset: 0x00034

Bit	Field	Type/InitVal	Description
7:0	CapPtr	RO 0x40	Capability List Pointer The current value in this field points to the PCI Power Management capability set in Power Management Capability Header at offset 0x40.
31:8	Reserved	RSVD 0x0	Reserved

Table 89: Reverse Bridge Control Interrupt Pin and Interrupt Line Register
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
7:0	IntLine	RW 0x0	Provides interrupt line routing information.
15:8	IntPin	RO 0x0	Indicates that the 88SB2211 does not implement a virtual interrupt pin.
16	SecPerrResEn	RW 0x0	Secondary Parity Error Response Enable This bit controls the 88SB2211's setting of the <DataPar> secondary status bit[24] in response to a received poisoned data error as a requester (master) on the PCI Express port. **NOTE:** The setting of this bit does not affect the <DetParErr> secondary status bit.
17	SecSerrEn	RW 0x0	Secondary PCI_SERRn Enable Controls the forwarding of secondary interface reception of ERR_FATAL or ERR_NONFATAL messages to PCI_SERRn assertions on the PCI interface. The bridge asserts PCI_SERRn on the PCI bus only if the <SErrEn> is set in the Command register. 0 = Disable: the forwarding of secondary interface reception of ERR_FATAL or ERR_NONFATAL messages to PCI_SERRn assertions on the PCI interface. 1 = Enable: the forwarding of secondary interface reception of ERR_FATAL or ERR_NONFATAL messages to PCI_SERRn assertions on the PCI interface.

Table 89: Reverse Bridge Control Interrupt Pin and Interrupt Line Register (Continued)
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
18	IsaEn	RW 0x0	ISA Enable Controls the response of the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. 0 = Downstream: Forward downstream all I/O addresses in the address range defined by the I/O Base and I/O Limit registers. 1 = Upstream: Forward upstream ISA I/O addresses in the address range defined by the I/O Base and I/O Limit registers that are in the first 64 KB of the PCI I/O address space (top 768 bytes of each 1-KB block).
19	VgaEn	RW 0x0	VGA Enable Controls the response of the bridge to VGA-compatible addresses. If this bit is set, the bridge forwards the following accesses on the primary interface to the secondary interface (and, conversely, blocks the forwarding of these addresses from the secondary to the primary interface): - Memory accesses in the range 000A 0000h to 000B FFFFh - I/O addresses in the first 64 KB of the I/O address space (Address[31:16] for PCI Express are 0000h) and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases). Address[15:10] may possess any value and is not used in the decoding. If the VGA Enable bit is set, forwarding of VGA addresses is independent of the value of the ISA Enable bit (located in the Bridge Control, Interrupt Pin and Interrupt Line), the I/O address range and memory address ranges defined by the I/O Limit Upper 16 Bits Register and I/O Base Upper 16 Bits, the Memory Limit and Memory Base, and the Prefetchable Memory Limit and Prefetchable Memory Base of the bridge. The forwarding of VGA addresses is qualified by the <IOEn> and <MemEn> bits in the Command and Status. 0 = DoNotForward: VGA compatible memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges. 1 = Forward: VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the <IOEn> and <MemEn> bits are set) independent of the I/O and memory address ranges and independent of the <IsaEn> bit in this register.
20	Vga16BitDec	RW 0x0	VGA 16-bit Decode This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if the VGA Enable bit in this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. This read/write bit enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from primary to secondary whenever the VGA Enable bit is set to 1. 0 = 10-bit_address: Execute 10-bit address decodes on VGA I/O accesses. 1 = 16-bit_address: Execute 16-bit address decodes on VGA I/O accesses.

Table 89: Reverse Bridge Control Interrupt Pin and Interrupt Line Register (Continued)
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
21	MAMode	RW 0x0	Master-Abort Mode Controls the behavior of a bridge when it receives a Master-Abort termination (e.g., an Unsupported Request on PCI Express) on either interface. 0 = DoNotReport: Master-Aborts. When a UR response is received from PCI Express for non-posted transactions, return FFFF FFFFh on reads and complete I/O writes normally. When a Master-Abort is received on the PCI interface for posted transactions initiated from the PCI Express interface, no action is taken (i.e., all data is discarded). When a Master-Abort is received on the PCI interface for non-posted transactions initiated from the PCI Express interface, the 88SB2211 completes it as an unsupported request. 1 = Report: UR Completions from PCI Express by signaling Target-Abort on the PCI interface. For posted transactions initiated from the PCI Express interface and Master-Aborted on the PCI interface, the bridge asserts PCI_SERRn (provided the <SErrEn> bit is set in the Command and Status). When a Master-Abort is received on the PCI interface for non-posted transactions initiated from the PCI Express interface, the 88SB2211 completes it as an unsupported request.
22	SecBusRst	RW 0x0	Secondary Bus Reset Forces the assertion of RST_OUT or the transmission of Hot reset on the PCI Express interface to the End Point. -If the PCI Express link state is L2/L3 RST_OUT is asserted to the Endpoint. -In all other cases hot reset is sent to the Endpoint. 0 = DoNotForce: Assertion of RST_OUTn is not forced. 1 = Force: Assertion of RST_OUTn is forced.
23	ScFbtbEn	RSVD 0x0	Secondary Fast-Back-To-Back Enable Does not apply to PCI Express devices.
24	PrDT	RW 0x0	Primary Discard Timer Controls the number of PCI clock cycles that the bridge waits for a master on the PCI interface to repeat a Delayed Transaction request. The counter starts once the Completion (PCI Express Completion associated with the Delayed Transaction Request) has reached the head of the upstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the primary bus). If the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and set the Discard Timer Status bit. 0 = 2^15_PCI: The Primary Discard Timer counts 2^15 PCI clock cycles. 1 = 2^10_PCI: The Primary Discard Timer counts 2^10 PCI clock cycles.
25	SecDT	RSVD 0x0	Secondary Discard Timer Does not apply to PCI Express devices.

Table 89: Reverse Bridge Control Interrupt Pin and Interrupt Line Register (Continued)
Offset: 0x0003C

Bit	Field	Type/InitVal	Description
26	DTStt	RW1C 0x0	Discard Timer Status This bit is set to a 1 when the PCI Discard Timer expires and a Delayed Completion is discarded from a queue in the bridge. 0 = No_discard: timer error 1 = Discard: timer error
27	DTSerrEn	RW 0x0	Discard Timer PCI_SERRn Enable This bit enables the bridge to generate PCI_SERRn assertion on PCI interface when the PCI Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge. 0 = DoNotAssert: PCI_SERRn on the PCI interface as a result of the expiration of the PCI Discard Timer. 1 = Assert: PCI_SERRn on the PCI interface if the PCI Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge.
31:28	Reserved	RSVD 0x0	Reserved

Table 90: Power Management Capability Header Register
Offset: 0x00040

Bit	Field	Type/InitVal	Description
7:0	CapID	RO 0x01	Capability ID Current value identifies the PCI Power Management capability.
15:8	NextPtr	RO 0x48	Next Item Pointer Current value points to PCI Express capability.
18:16	PMCVer	RO 0x2	PCI Power Management Capability Version
20:19	Reserved	RO 0x0	PME Clock Does not apply to PCI Express. This field is hardwired to 0.
21	DSI	RO 0x0	Device Specific Initialization The 88SB2211 does not requires device specific initialization.
24:22	AuxCur	RO 0x1	Auxiliary Current Requirements The 88SB2211 does not require current from VAUX in D3cold state.
25	D1Sup	RO 0x1	D1 Support The 88SB2211 supports D1 Power Management state.

Table 90: Power Management Capability Header Register (Continued)
Offset: 0x00040

Bit	Field	Type/InitVal	Description
26	D2Sup	RO 0x1	D2 Support The 88SB2211 supports D2 Power Management state.
31:27	PMESup	RO 0x1F	Power Management Event (PME) Support The 88SB2211 supports PME generation from D0, D1, D2, D3cold Power Management states.

Table 91: Reverse Bridge Power Management Control and Status Register
Offset: 0x00044

Bit	Field	Type/InitVal	Description
1:0	PMState	RW 0x0	Power State This field controls the Power Management state of the 88SB2211. The device supports all Power Management states. When writing D3, the read value from this field is the previous value, only after the PCI Express link is in L2/L3 state does the read value move to D3 state. **NOTE:** A transition from state D3 to state D0 causes an internal reset. In states D1, D2 and D3hot, PCI memory and I/O accesses are disabled, as well as the interrupt emulation messages, and only configuration cycles are allowed. 0 = D0 1 = D1 2 = D2 3 = D3
7:2	Reserved_7_2	RSVD 0x0	Reserved
8	PME_en	RW 0x0	PME Enable Controls PM_PME Message Generation. **NOTE:** Power ON Sticky bit--not initialized by either fundamental or hot reset. 0 = Disabled 1 = Enabled
12:9	PMDataSel	RO 0x0	Data Select Data register is not implemented.
14:13	PMDataScale	RO 0x0	Data Scale Data register is not implemented.

Table 91: Reverse Bridge Power Management Control and Status Register (Continued)
Offset: 0x00044

Bit	Field	Type/InitVal	Description
15	PME_Stat	RW1C 0x0	This bit is set whenever PCI_PMEn is asserted on PCI bus. These are the scenarios which will lead to PCI_PMEn assertion: 1. PCI Express PME Message is received. 2. PCI Express WAKEn signal is asserted. This bit can be set only if <PME_en> is set. **NOTE:** Power On Sticky bit--not initialized by either fundamental or hot reset.
21:16	Reserved_21_16	RSVD 0x0	Reserved
22	B2B3Sup	RO 0x1	B2_B3 Support for D3hot Shutting down, the PCI Express clock is not supported for D2 and D3hot by default. When cleared, indicates that, when the 88SB2211 is programmed to D3hot, its secondary bus has its power removed, and its PCI Express clocks are stopped (B3). This bit is only meaningful if the <BPCCEn> bit is set.
23	BPCCEn	RO 0x1	Bus Power/clock Control Enable When set, indicates that the bus power/clock control mechanism, as defined in section 4.7.1 of the PCI Power Management specification 1.1, is enabled. The Bstate and the secondary clocks are controlled accordingly. **NOTE:** To disable the Bus Power Clock Control, this field should be set to 0x0 via the TWSI serial initialization process. (This bit can be written from the TWSI port). **NOTE:** Shutting down the PCI Express clock out for Power management events by default is not enabled.
31:24	PMData	RO 0x0	Power Management Data Data register is not implemented.

Table 92: Reverse Bridge PCI Express Capability Register
Offset: 0x00048

Bit	Field	Type/InitVal	Description
7:0	CapID	RO 0x10	Capability ID The current value of this field identifies the PCI Express capability.
15:8	NextPtr	RO 0x0	Next Item Pointer The current value of this field points to the end of the capability list (NULL).

Table 92: Reverse Bridge PCI Express Capability Register (Continued)
Offset: 0x00048

Bit	Field	Type/InitVal	Description
19:16	CapVer	RO 0x1	Capability Version This field indicates the PCI Express Base spec 1.0a version of the PCI-Express capability.
23:20	DevType	RO 0x8	Device/Port Type PCI/PCI-X to PCI Express Bridge
24	SlotImp	RO 0x1	Slot Implemented
29:25	IntMsgNum	RO 0x0	Interrupt Message Number This bit is hardwired to 0.
31:30	Reserved	RSVD 0x0	Reserved

Table 93: Reverse Bridge PCI Express Device Capabilities Register
Offset: 0x0004C

Bit	Field	Type/InitVal	Description
2:0	MaxPldSizeSup	RO 0x0	Maximum Payload Size Supported 128B MPS support. This bit is hardwired to 0.
4:3	PhntmFncSup	RO 0x0	Phantom Functions Support Phantom Functions are not supported. This bit is hardwired to 0.
5	ExtTagSup	RO 0x0	Extended Tag Field Support Extended tag is not supported. This bit is hardwired to 0.
11:6	Reserved_11_6	RSVD 0x0	Reserved
12	AttButPrs	RO 0x0	Attention Button Present The 88SB2211 does not support Attention Button. This bit is hardwired to 0.
13	AttIndPrs	RO 0x0	Attention Indicator Present The 88SB2211 does not support Attention Indicator This bit is hardwired to 0.

Table 93: Reverse Bridge PCI Express Device Capabilities Register (Continued)
Offset: 0x0004C

Bit	Field	Type/InitVal	Description
14	PwrIndPrs	RO 0x0	Power Indicator Present The 88SB2211 does not support Attention Indicator. This bit is hardwired to 0.
15	Role-Based Error Reporting	RO 0x0	The 88SB2211 does not support Role Based Error Reporting.
31:16	Reserved_31_16	RSVD 0x0	Reserved

Table 94: Reverse Bridge PCI Express Device Control Status Register
Offset: 0x00050

Bit	Field	Type/InitVal	Description
2:0	reserved_2_0	RW 0x0	RESERVED
3	URRepEn	RW 0x0	Unsupported Request (UR) Reporting Enable Controls error reporting on behalf of Unsupported Request errors detected on the PCI Express interface only. **NOTE:** UR related PCI_SERRn assertion is still enabled when URRepEn=0, if the <SErrEn> bit in the Command and Status is set. 0 = Masked: UR related error messages are masked. Status bit is not masked. 1 = Enabled: UR related error messages enabled.
4	EnRO	RO 0x0	Enable Relaxed Ordering The 88SB2211 never sets the Relaxed Ordering attribute in transactions it initiates as a requester. This bit is hardwired to 0.
7:5	MaxPldSz	RW 0x0	Maximum Payload Size The maximum payload size supported is 128B (refer to bit <MaxPldSizeSup> in the PCI Express Device Capabilities). 0 = 128B 1-7 = Reserved
8	Reserved_8	RO 0x0	Extended Tag Field Enabled Not supported. This bit is hardwired to 0.
9	Reserved_9	RO 0x0	Phantom Function Enable Not supported. This bit is hardwired to 0.

Table 94: Reverse Bridge PCI Express Device Control Status Register (Continued)
Offset: 0x00050

Bit	Field	Type/InitVal	Description
10	AuxPwrEn	RW 0x0	Auxiliary (AUX) Power PM Enable Controls allocation of AUX power to the device. **NOTE:** Power On Reset Sticky bit is not initialized by either fundamental or hot reset. 0 = Disabled: Vaux is not allocated. 1 = Enabled: Vaux is allocated.
11	EnNS	RO 0x0	Enable No Snoop The 88SB2211 never sets the No Snoop attribute in transactions it initiates as a requester. This bit is hardwired to 0.
14:12	MaxRdRqSz	RW 0x2	Maximum Read Request Size This field limits the 88SB2211 maximum read request size as a requestor (master). 0 = 128B 1 = 256B 2 = 512B 3 = 1_KB 4 = 2_KB 5 = 4_KB
15	BrCRSEn	RW 0x0	Bridge Configuration Retry Enable When the 88SB2211 is configured to root-complex, this bit is not relevant.
16	CorErrDet	RW1C 0x0	Correctable Error Detected This bit indicates the status of the correctable errors detected by the 88SB2211. It set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
17	NFErrDet	RW1C 0x0	Non-Fatal Error Detected This bit indicates the status of the Non-Fatal errors detected by the 88SB2211. It is set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
18	FErrDet	RW1C 0x0	Fatal Error Detected This bit indicates the status of the Fatal errors detected by the 88SB2211. It is set for the corresponding errors on both the PCI Express and conventional PCI interfaces.
19	URDet	RW1C 0x0	Unsupported Request Detected This bit indicates that the 88SB2211 receives an unsupported request. It is set for the corresponding errors on both the PCI Express and conventional PCI interfaces.

Table 94: Reverse Bridge PCI Express Device Control Status Register (Continued)
Offset: 0x00050

Bit	Field	Type/InitVal	Description
20	AuxPwrDet	RO 0x0	AUX Power Detected Indicates that the 88SB2211 detected AUX power.
21	TransPend	RO 0x0	Transactions Pending The 88SB2211 does not issue non-posted requests on its own behalf. This bit is hardwired to 0.
31:22	Reserved_31_22	RSVD 0x0	Reserved

Table 95: Reverse Bridge PCI Express Link Control Status Register
Offset: 0x00058

Bit	Field	Type/InitVal	Description
1:0	aspm_cnt	RW 0x0	Active State Link PM Control This field controls the level of active state PM supported on the link. 0 = Disabled 1 = L0s_entry_supported 2 = Reserved 3 = L0s_L1_entry_supported
2	Reserved_2	RSVD 0x0	Reserved
3	RCB	RO 0x0	Read Completion Boundary Not applicable to the 88SB2211. This bit is hardwired to 0.
4	LnkDis	RW 0x0	Link Disable Activation procedure: 1. Set this bit to trigger link disable. 2. Poll <DLDown> de-assertion (PCI Express Status Register, bit 0) ensure the link is disabled. 3. Clear the bit to exit to detect and enable the link again.
5	RetrnLnk	RW 0x0	Retrain Link This bit forces the device to initiate link retraining. Always returns 0 when read.
6	CmnClkCfg	RW 0x0	Common Clock Configuration When set by software, this bit indicates that both devices on the link use a distributed common reference clock.

Table 95: Reverse Bridge PCI Express Link Control Status Register (Continued)
Offset: 0x00058

Bit	Field	Type/InitVal	Description
7	ExtdSnc	RW 0x0	Extended Sync When set, this bit forces extended transmission of 4096 FTS ordered sets followed by a single skip ordered set in exit from L0s and extra (1024) TS1 at exit from L1. **NOTE:** This bit is used for test and measurement only. **NOTE:**
15:8	Reserved_15_8	RSVD 0x0	Reserved
19:16	LnkSpd	RO 0x1	Link Speed The only link speed available is 2.5 Gbps. 0 = Reserved 1 = 2.5 Gbps 2-15 = Reserved The value of this field is undefined when the link is not up.
25:20	NegLnkWdth	RO 0x0	Negotiated Link Width The only link width available is x1. 0 = Reserved 1 = x1 2-63 = Reserved The value of this field is undefined when the link is not up.
26	Reserved_26	RO 0x0	Reserved
27	LnkTrn	RO 0x0	Link Training This bit indicates that link training is in progress. This bit is cleared once link training is complete.
28	SltClkCfg	RO 0x1	Slot Clock Configuration . 0 = IndependentClock: The 88SB2211 uses an independent clock, irrespective of the presence of a reference clock on the connector. 1 = ReferenceClock: The 88SB2211 uses the reference clock that the platform provides.
31:29	Reserved_31_29	RSVD 0x0	Reserved

Table 96: Reverse Bridge PCI Express Slot Capabilities Register
Offset: 0x0005C

Bit	Field	Type/InitVal	Description
0	Attention Button Present	RO 0x0	RESERVED - Not Supported

Table 96: Reverse Bridge PCI Express Slot Capabilities Register (Continued)
Offset: 0x0005C

Bit	Field	Type/InitVal	Description
1	Power Controller Present	RO 0x0	RESERVED - Not Supported
2	MRL Sensor Present	RO 0x0	RESERVED - Not Supported
3	Attention Indicator Present	RO 0x0	RESERVED - Not Supported
4	Power Indicator Present	RO 0x0	RESERVED - Not Supported
5	Hot-Plug Surprise	RO 0x0	RESERVED - Not Supported
6	Hot-Plug Capable	RO 0x0	RESERVED - Not Supported
14:7	Slot Power Limit Value	RW 0x19	In combination with the Slot PowerLimit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field except when the Slot Power Limit Scale field equals 00b (1.0x) and Slot Power Limit Value exceeds 239, the following alternative encodings are used: 240 = 250 W Slot Power Limit 241 = 275 W Slot Power Limit 242 = 300 W Slot Power Limit 243-255 = Reserved Writes to this register also cause the 88SB2211 to send the Set_Slot_Power_Limit Message.
16:15	Slot Power Limit Scale	RW 0x0	Slot Power Limit Scale Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the 88SB2211 to send the Set_Slot_Power_Limit Message. 0 = 00: 1.0x 1 = 01: 0.1x 2 = 10: 0.01x 3 = 11: 0.001x
17	Electromechanical Interlock Present	RO 0x0	RESERVED - Not Supported
18	No Command Completed Support	RO 0x0	RESERVED - Not Supported
31:19	Physical Slot Number	RO 0x0	RESERVED - Not Supported

Table 97: Reverse Bridge PCI Express Slot Control Status Register
Offset: 0x00060

Bit	Field	Type/InitVal	Description
0	Attention Button Pressed Enable	RO 0x0	RESERVED - Not Supported
1	Power Fault Detected Enable	RO 0x0	RESERVED - Not Supported
2	MRL Sensor Changed Enable	RO 0x0	RESERVED - Not Supported
3	Presence Detect Changed Enable	RO 0x0	RESERVED - Not Supported
4	Command Completed Interrupt Enable	RO 0x0	RESERVED - Not Supported
5	Hot-Plug Interrupt Enable	RO 0x0	RESERVED - Not Supported
7:6	Attention Indicator Control	RO 0x0	RESERVED - Not Supported
9:8	Power Indicator Control	RO 0x0	RESERVED - Not Supported
10	Power Controller Control	RO 0x0	RESERVED - Not Supported
11	Electromechanical Interlock Control	RO 0x0	RESERVED - Not Supported
12	Data Link Layer State Changed Enable	RO 0x0	RESERVED - Not Supported
15:13	RESERVED	RSVD 0x0	RESERVED
16	Attention Button Pressed	RO 0x0	RESERVED - Not Supported
17	Power Fault Detected	RO 0x0	RESERVED - Not Supported

Table 97: Reverse Bridge PCI Express Slot Control Status Register (Continued)
Offset: 0x00060

Bit	Field	Type/InitVal	Description
18	MRL Sensor Changed	RO 0x0	RESERVED - Not Supported
19	Presence Detect Changed	RO 0x0	RESERVED - Not Supported
20	Command Completed	RO 0x0	RESERVED - Not Supported
21	MRL Sensor State	RO 0x0	RESERVED - Not Supported
22	Presence Detect State	RO 0x1	RESERVED - Not Supported
23	Electromechanical Interlock Status	RO 0x0	RESERVED - Not Supported
24	Data Link Layer State Changed	RO 0x0	RESERVED - Not Supported
31:25	RESERVED_31_25	RSVD 0x0	RESERVED

Table 98: Reverse Bridge PCI Express Root Control Capabilities Register
Offset: 0x00064

Bit	Field	Type/InitVal	Description
0	System Error on Correctable Error Enable	RW 0x0	If Set, this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system PCI_SERRn assertion on the PCI bus. **NOTE:** PCI_SERRn is asserted on PCI bus only if both SErrEn bit of Command register and SecSerrEn of Bridge Control register are enabled. **NOTE:**
1	System Error on Non-Fatal Error Enable	RW 0x1	If set, this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system PCI_SERRn assertion on the PCI bus. **NOTE:** PCI_SERRn is asserted on the PCI bus only if both <SErrEn> bit of the Command register and the <SecSerrEn> bit of the of Bridge Control register are enabled. **NOTE:**

Table 98: Reverse Bridge PCI Express Root Control Capabilities Register (Continued)
Offset: 0x00064

Bit	Field	Type/InitVal	Description
2	System Error on Fatal Error Enable	RW 0x1	If Set, this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself. The mechanism for signaling a System Error to the system PCI_SERRn assertion on the PCI bus. **NOTE:** PCI_SERRn is asserted on PCI bus only if both <SErrEn> bit of Command register and SecSerrEn of Bridge Control register are enabled. **NOTE:**
3	PME Interrupt Enable	RW 0x0	When Set, this bit enables <PME Status> interrupt generation upon receipt of a PME Message as reflected in the PME Status bit, in Reverse Bridge Mode Configuration register.
4	CRS Software Visibility Enable	RO 0x0	RESERVED - not supported.
15:5	RESERVED_15_5	RSVD 0x0	RESERVED
16	CRS Software Visibility	RO 0x0	RESERVED - not supported.
31:17	RESERVED_31_17	RSVD 0x0	RESERVED

Table 99: Reverse Bridge PCI Express Root Status Register
Offset: 0x00068

Bit	Field	Type/InitVal	Description
15:0	PME Requester ID	RO 0x0	This field indicates the PCI Requester ID of the last PM_PME Requester. This field is only valid when the PME Status is Set.
16	PME Status	RW1C 0x0	This bit indicates that PM_PME message was sent by the PME Requester indicated in the PME Requester ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1b.
17	PME Pending	RO 0x0	This bit indicates that one more PME is pending.
18	Pme_To_Ack_Rcv	RW1C 0x0	Set if PME_TO_ACK message was received.
31:19	RESERVED_31_19	RSVD 0x0	RESERVED

A.4.2 Reverse Bridge Mode Device Specific

Table 100: GPIO Control Register
Offset: 0x00074

Bit	Field	Type/InitVal	Description
7:0	GPIOOutEn	RW 0x0	General Purpose I/O Output Enable Controls the direction of the GPIO signal. By default all GPIO pins are inputs. **NOTE:** GPIOOutEn[N] controls GPIO[N] pin, N=0..7 0 = Input 1 = Output
15:8	GPIODataOut	RW 0x0	General Purpose I/O Data Out Controls the data driven on the GPIO pins, when configured as an output by the <GPIOOutEn> field. **NOTE:** GPIODataOut[N] controls GPIO[N] pin, N=0..7
23:16	GPIODataIn	RO 0x0	General Purpose I/O Data In Reads the current state of the GPIO pin. Valid only when GPIO pin is configured as an input by the <GPIOOutEn> field. **NOTE:** GPIODataIn[N] reads GPIO[N] pin, N=0..7
31:24	Reserved	RSVD 0x0	Reserved

Table 101: Reverse Bridge PCI Clock Output Control Register
Offset: 0x00078

Bit	Field	Type/InitVal	Description
0	ClockOutDis0	RW SAR	PCI Clock Out 0 Disable Controls the activation of PCI_CLK_OUT[0]. When set, PCI_CLK_OUT[0] is driven to 0. 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
1	ClockOutDis1	RW 0x1	PCI Clock Out 1 Disable Controls the activation of PCI_CLK_OUT[1]. When set, PCI_CLK_OUT[1] is driven to 0. 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
2	ClockOutDis2	RW 0x1	PCI Clock Out 2 Disable Controls the activation of PCI_CLK_OUT[2]. When set, PCI_CLK_OUT[2] is driven to 0. 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled

Table 101: Reverse Bridge PCI Clock Output Control Register (Continued)
Offset: 0x00078

Bit	Field	Type/InitVal	Description
3	ClockOutDis3	RW 0x1	PCI Clock Out 3 Disable Controls the activation of PCI_CLK_OUT[3]. When set, PCI_CLK_OUT[3] is driven to 0. 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
4	ClockOutDis4	RW 0x1	PCI Clock Out 4 Disable Controls the activation of PCI_CLK_OUT[4]. When set, PCI_CLK_OUT[4] is driven to 0. 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
5	ClockOutDis5	RW 0x1	PCI Clock Out 5 Disable Controls the activation of PCI_CLK_OUT[5] When set, PCI_CLK_OUT[5] is driven to 0. 0 = Enabled: PCI clock enabled 1 = Disabled: PCI clock disabled
31:6	Reserved	RSVD 0x0	Reserved

Table 102: Reverse Bridge Prefetch and CRS Control Register
Offset: 0x00080

Bit	Field	Type/InitVal	Description
1:0	MrmPrftchMd	RW 0x3	Read Multiple Prefetch Mode 0 = Prefetch_disabled 1 = Prefetch_enabled 2 = Reserved 3 = Aggressive_Prefetch_enabled
2	MrmAggrInitWM	RW 0x1	Memory Read Multiple Aggressive Prefetch Initial Read Water Mark Controls the number of 128-bytes buffers to be pre-fetched initially. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = Two: The 88SB2211 pre-fetches two 128-bytes buffers initially. 1 = Three: The 88SB2211 pre-fetches three 128-bytes buffers initially.

Table 102: Reverse Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
5:3	MrmAggrNextWM	RW 0x0	Memory Read Multiple Aggressive Prefetch Next Read Watermark Controls the criteria for issuing the next prefetch read request on the PCI Express interface. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One data cycle: Fetch next buffer after one data cycle is driven on the bus. 1 = Two data cycles: Fetch next buffer after two data cycles are driven on the bus. 2 = Three data cycles: Fetch next buffer after three data cycles are driven on the bus. 3 = Four data cycles: Fetch next buffer after four data cycles are driven on the bus. 4 = Five data cycles: Fetch next buffer after five data cycles are driven on the bus. 5 = Six data cycles: Fetch next buffer after six data cycles are driven on the bus. 6 = Seven data cycles: Fetch next buffer after seven data cycles are driven on the bus. 7 = Eight data cycles: Fetch next buffer after eight data cycles are driven on the bus.
6	MrmAggrResWM	RW 0x0	Memory Read Multiple Aggressive Prefetch Response Watermark Controls the criteria for responding to the delayed read on the PCI bus. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One: The 88SB2211 drives read data on the bus as soon as it has one 128-byte read buffer. 1 = Two: The 88SB2211 drives read data on the bus as soon as it has two 128-byte read buffers.
7	Reserved_7	RW 0x0	Reserved
9:8	MrlPrftchMd	RW 0x1	Memory Read Line Prefetch Mode 0 = Prefetch_disabled 1 = Prefetch_enabled 2 = Reserved 3 = Aggressive_Prefetch_enabled
10	MrlAggrInitWM	RW 0x0	Memory Read Line Aggressive Prefetch Initial Read Watermark Controls the number of 128-bytes buffers to be pre-fetched initially. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = Two: The 88SB2211 pre-fetches two 128-bytes buffers initially. 1 = Three: The 88SB2211 pre-fetches three 128-bytes buffers initially.

Table 102: Reverse Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
13:11	MrlAggrNextWM	RW 0x0	Memory Read Line Aggressive Prefetch Next Read Watermark Controls the criteria for issuing the next prefetch read request on the PCI Express interface. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One data cycle: Fetch next buffer after one data cycle is driven on the bus. 1 = Two data cycles: Fetch next buffer after two data cycles are driven on the bus. 2 = Three data cycles: Fetch next buffer after three data cycles are driven on the bus. 3 = Four data cycles: Fetch next buffer after four data cycles are driven on the bus. 4 = Five data cycles: Fetch next buffer after five data cycles are driven on the bus. 5 = Six data cycles: Fetch next buffer after six data cycles are driven on the bus. 6 = Seven data cycles: Fetch next buffer after seven data cycles are driven on the bus. 7 = Eight data cycles: Fetch next buffer after eight data cycles are driven on the bus.
14	MrlAggrResWM	RW 0x0	Memory Read Multiple Aggressive Prefetch Response Watermark Controls the criteria for responding to the delayed read on the PCI bus. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One: The 88SB2211 drives read data on the bus as soon as it has one 128-byte read buffer. 1 = Two: The 88SB2211 drives read data on the bus as soon as it has two 128-byte read buffers.
15	Reserved_15	RW 0x0	Reserved
17:16	MrPrftchMd	RW 0x0	Memory Read Prefetch Mode 0 = Prefetch_disabled 1 = Prefetch_enabled 2 = Reserved 3 = Aggressive_Prefetch_enabled
18	MrAggrInitWM	RW 0x0	Memory Read Aggressive Prefetch Initial Read Watermark Controls the number of 128-bytes buffers to be pre-fetched initially. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = Two: The 88SB2211 pre-fetches two 128-bytes buffers initially. 1 = Three: The 88SB2211 pre-fetches three 128-bytes buffers initially.

Table 102: Reverse Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
21:19	MrAggrNextWM	RW 0x0	Memory Read Aggressive Prefetch Next Read Watermark Controls the criteria for issuing the next prefetch read request on the PCI Express interface. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One data cycle: Fetch next buffer after one data cycle is driven on the bus. 1 = Two data cycles: Fetch next buffer after two data cycles are driven on the bus. 2 = Three data cycles: Fetch next buffer after three data cycles are driven on the bus. 3 = Four data cycles: Fetch next buffer after four data cycles are driven on the bus. 4 = Five data cycles: Fetch next buffer after five data cycles are driven on the bus. 5 = Six data cycles: Fetch next buffer after six data cycles are driven on the bus. 6 = Seven data cycles: Fetch next buffer after seven data cycles are driven on the bus. 7 = Eight data cycles: Fetch next buffer after eight data cycles are driven on the bus.
22	MrAggrResWM	RW 0x0	Memory Read Aggressive Prefetch Response Watermark Controls the criteria for responding to the delayed read on the PCI bus. **NOTE:** Relevant only if Aggressive Prefetch is enabled by the <MrmPrftchMd> bit. 0 = One: The 88SB2211 drives read data on the bus as soon as it has one 128-byte read buffer. 1 = Two: The 88SB2211 drives read data on the bus as soon as it has two 128-byte read buffers.
23	Reserved_23	RW 0x0	Reserved
24	Reserved_24	RW 0x1	Reserved Always write 1.
25	Reserved_25	RW 0x1	Reserved Always write 1.
26	Reserved_26	RW 0x0	Reserved Always write 0.
27	Reserved_27	RW 0x0	Reserved Always write 0.
28	Reserved_28	RW 0x0	Reserved
29	Reserved_29	RW 0x0	Reserved

Table 102: Reverse Bridge Prefetch and CRS Control Register (Continued)
Offset: 0x00080

Bit	Field	Type/InitVal	Description
31:30	CrsCtrl	RW 0x0	Determines the 88SB2211 response when a PCI-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry Status. 0 = CrsRtry: Retry configuration transactions on PCI bus on every received CRS. 1 = CrsTa: Target-Abort configuration transactions on PCI bus on every received CRS. 2 = Crs1Sec: Retry configuration transactions on PCI bus from first received CRS. Target-Abort configuration transactions on PCI bus 1 second after first received CRS. 3 = Crs8Sec: Retry configuration transactions on PCI bus from first received CRS. Target-Abort configuration transactions on PCI bus 8 seconds after first received CRS.

Table 103: Marvell Diagnostic PCI Express PHY Indirect Access Register
Offset: 0x000F4

Bit	Field	Type/InitVal	Description
31:0	Reserved	RSVD 0x84CCE5	Reserved

Table 104: Marvell Diagnostic Indirect Address Register
Offset: 0x000F8

Bit	Field	Type/InitVal	Description
1:0	Reserved	RSVD 0x0	Reserved
13:2	Address	RW 0x0	Reserved **NOTE:** For Marvell usage only.
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 105: Marvell Diagnostic Indirect Data Register
Offset: 0x000FC

Bit	Field	Type/InitVal	Description
31:0	Data	RO 0x0	Reserved **NOTE:** For Marvell usage only.

A.4.3 Reverse Bridge Mode Extended Configuration Space

Table 106: PCI Express Advanced Error Report Header Register
Offset: 0x00100

Bit	Field	Type/InitVal	Description
15:0	PECapID	RO 0x1	Extended Capability ID The current value of this field identifies the Advanced Error Reporting capability.
19:16	CapVer	RO 0x1	Capability Version
31:20	NextPtr	RO 0x0	Next Item Pointer This field indicates the last item in the extended capabilities linked list.

Table 107: PCI Express Uncorrectable Error Status Register
Offset: 0x00104

Bit	Field	Type/InitVal	Description
3:0	Reserved	RSVD 0x0	Reserved
4	DLPrtErr	RW1C 0x0	Data Link Protocol Error Status
11:5	Reserved	RSVD 0x0	Reserved
12	RPsnTlpErr	RW1C 0x0	Poisoned TLP Status
13	FCPrtErr	RW1C 0x0	Flow Control Protocol Error Status Set upon DLLP update timeout (200s with no FC DLLP received).
14	CmpTOErr	RW1C 0x0	Completion Timeout Status
15	CAErr	RW1C 0x0	Completer Abort Status
16	UnexpCmpErr	RW1C 0x0	Unexpected Completion Status
17	Reserved	RSVD 0x0	Reserved

Table 107: PCI Express Uncorrectable Error Status Register (Continued)
Offset: 0x00104

Bit	Field	Type/InitVal	Description
18	MalfTlpErr	RW1C 0x0	Malformed TLP Status
19	Reserved	RSVD 0x0	Reserved
20	URErr	RW1C 0x0	Unsupported Request Error Status
31:21	Reserved	RSVD 0x0	Reserved

Table 108: PCI Express Uncorrectable Error Mask Register
Offset: 0x00108

Bit	Field	Type/InitVal	Description
3:0	Reserved	RSVD 0x0	Reserved
4	DLPrtErrMsk	RW 0x0	Data Link Protocol Error Mask When an error is indicated in the PCI Express Uncorrectable Error Status and the corresponding bit is set: - The header is not logged in the Header Log Register - The First Error Pointer is not updated - An error message is not generated. The status bit is set regardless of the mask setting. 0 = Not_masked 1 = Masked
11:5	Reserved	RSVD 0x0	Reserved
12	RPsnTlpErrMsk	RW 0x0	Poisoned TLP Error Mask
13	FCPrtErrMsk	RW 0x0	Flow Control Protocol Error Mask
14	CmpTOErrMsk	RW 0x0	Completion Timeout Mask
15	CAErrMsk	RW 0x0	Completer Abort Mask
16	UnexpCmpErrMsk	RW 0x0	Unexpected Completion Mask

Table 108: PCI Express Uncorrectable Error Mask Register (Continued)
Offset: 0x00108

Bit	Field	Type/InitVal	Description
17	Reserved	RSVD 0x0	Reserved
18	MalfTlpErrMsk	RW 0x0	Malformed TLP Mask
19	Reserved	RSVD 0x0	Reserved
20	URErrMsk	RW 0x0	Unsupported Request Error Mask
31:21	Reserved	RSVD 0x0	Reserved

Table 109: PCI Express Uncorrectable Error Severity Register
Offset: 0x0010C

Bit	Field	Type/InitVal	Description
3:0	Reserved	RSVD 0x1	Reserved
4	DLPrtErrSev	RW 0x1	Data Link Protocol Error Severity Controls the severity indication of the Uncorrectable errors. Each bit controls the error type of the corresponding bit in the PCI Express Uncorrectable Error Status. 0 = Non-Fatal: Error type is Non-Fatal. 1 = Fatal: Error type is Fatal.
11:5	Reserved	RSVD 0x0	Reserved
12	RPsnTlpErrSev	RW 0x0	Poisoned TLP Error Severity
13	FCPrtErrSev	RW 0x1	Flow Control Protocol Error Severity
14	CmpTOErrSev	RW 0x0	Completion Timeout Severity
15	CAErSev	RW 0x0	Completer Abort Severity

Table 109: PCI Express Uncorrectable Error Severity Register (Continued)
Offset: 0x0010C

Bit	Field	Type/InitVal	Description
16	UnexpCmpErrSev	RW 0x0	Unexpected Completion Severity
17	Reserved	RSVD 0x0	Reserved
18	MalfTlpErrSev	RW 0x1	Malformed TLP Severity
19	Reserved	RSVD 0x0	Reserved
20	URErrSev	RW 0x0	Unsupported Request Error Severity
31:21	Reserved	RSVD 0x0	Reserved

Table 110: PCI Express Correctable Error Status Register
Offset: 0x00110

Bit	Field	Type/InitVal	Description
0	RcvErr	RW1C 0x0	Receiver Error Status When set, this bit indicates that a Receiver error has occurred.
5:1	Reserved	RSVD 0x0	Reserved
6	BadTlpErr	RW1C 0x0	Bad TLP Status
7	BadDllpErr	RW1C 0x0	Bad DLLP Status
8	RplyRllovrErr	RW1C 0x0	Replay Number Rollover Status
11:9	Reserved	RSVD 0x0	Reserved
12	RplyTOErr	RW1C 0x0	Replay Timer Timeout status
31:13	Reserved	RSVD 0x0	Reserved

Table 111: PCI Express Correctable Error Mask Register
Offset: 0x00114

Bit	Field	Type/InitVal	Description
0	RcvMsk	RW 0x0	Receiver Error Mask If set, an error message is not generated upon occurrence of a Receiver error. 0 = Not_masked 1 = Masked
5:1	Reserved_5_1	RSVD 0x0	Reserved
6	BadTlpMsk	RW 0x0	Bad TLP Mask
7	BadDllpErrMsk	RW 0x0	Bad DLLP Mask
8	RplyRllovrMsk	RW 0x0	Replay Number Rollover Mask
11:9	Reserved_11_9	RSVD 0x0	Reserved
12	RplyTOMsk	RW 0x0	Replay Timer Timeout Mask
13	AdvisoryNonFatalError	RO 0x0	Advisory Non-Fatal Error
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 112: PCI Express Advanced Error Capability and Control Register
Offset: 0x00118

Bit	Field	Type/InitVal	Description
4:0	FrstErrPtr	RO 0x0	First Error Pointer This field reports the bit position of the first error reported in the PCI Express Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself. 4 = FrstErrPtr_4: Data Link Protocol Error 12 = FrstErrPtr_12: Poisoned TLP Error 13 = FrstErrPtr_13: Flow Control Protocol Error 14 = FrstErrPtr_14: Completion Timeout Error 15 = FrstErrPtr_15: Completer Abort Status 16 = FrstErrPtr_16: Unexpected Completion Error 18 = FrstErrPtr_18: Malformed TLP Error 20 = FrstErrPtr_20: Unsupported Request Error
31:5	Reserved	RSVD 0x0	Reserved

Table 113: PCI Express Header Log First DWORD Register
Offset: 0x0011C

Bit	Field	Type/InitVal	Description
31:0	Hdrlog1DW	RO 0x0	Header Log First DWORD Logs the header of the first error reported in the PCI Express Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until the software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself.

Table 114: PCI Express Header Log Second DWORD Register
Offset: 0x00120

Bit	Field	Type/InitVal	Description
31:0	Hdrlog2DW	RO 0x0	Header Log Second DWORD

Table 115: PCI Express Header Log Third DWORD Register
Offset: 0x00124

Bit	Field	Type/InitVal	Description
31:0	Hdrlog3DW	RO 0x0	Header Log Third DWORD

Table 116: PCI Express Header Log Fourth DWORD Register
Offset: 0x00128

Bit	Field	Type/InitVal	Description
31:0	Hdrlog4DW	RO 0x0	Header Log Fourth DWORD

Table 117: PCI Uncorrectable Error Status Register
Offset: 0x0012C

Bit	Field	Type/InitVal	Description
0	Reserved_0	RSVD 0x0	Target-Abort on Split Completion Status Does not apply to conventional PCI.
1	Reserved_1	RSVD 0x0	Master-Abort on Split Completion Status Does not apply to conventional PCI.
2	RcvTA	RW1C 0x0	Received Target-Abort Status
3	RcvMA	RW1C 0x0	Received Master-Abort Status
6:4	Reserved_6_4	RSVD 0x0	Reserved
7	UCDataErr	RW1C 0x0	Uncorrectable Data Error Status
8	Reserved_8	RSVD 0x0	Uncorrectable Attribute Error Status Does not apply to conventional PCI.
9	UCAddrErr	RW1C 0x0	Uncorrectable Address Error Status

Table 117: PCI Uncorrectable Error Status Register (Continued)
Offset: 0x0012C

Bit	Field	Type/InitVal	Description
10	DTExp	RW1C 0x0	Delayed Transaction Discard Timer Expired Status No header log.
11	PerrDetected	RW1C 0x0	PCI_PERRn Assertion Detected
12	SerrDetected	RW1C 0x0	PCI_SERRn Assertion Detected No header log.
13	InternalBrErr	RW1C 0x0	Internal Bridge Error Status No header log.
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 118: Reverse Bridge PCI Uncorrectable Error Mask Register
Offset: 0x00130

Bit	Field	Type/InitVal	Description
0	Reserved_1_0	RSVD 0x0	Reserved
1	Reserved_1	RW 0x0	Reserved
2	RcvTAMsk	RW 0x0	Received Target-Abort Mask Status bit is set regardless of the mask setting. 0 = Not_masked 1 = Masked
3	RcvMAMsk	RW 0x1	Received Master-Abort Mask
4	Reserved_4	RSVD 0x0	Reserved
6:5	Reserved_6_5	RW 0x1	Reserved
7	UCDataErrMsk	RW 0x1	Uncorrectable Data Error Mask

Table 118: Reverse Bridge PCI Uncorrectable Error Mask Register (Continued)
Offset: 0x00130

Bit	Field	Type/InitVal	Description
8	UCAttrErrMsk	RW 0x1	Uncorrectable Attribute Error Mask
9	UCAddrErrMsk	RW 0x0	Uncorrectable Address Error Mask SAR upon EP/RC mode.
10	DTExp	RW 0x0	Delayed Transaction Discard Timer Expired Mask Header in not Logged. SAR upon EP/RC mode.
11	PerrDetectedMsk	RW 0x0	PCI_PERRn Assertion Detected Mask
12	SerrDetectedMsk	RW 0x1	PCI_SERRn Assertion Detected Mask Header in not logged.
13	InternalBrErrMsk	RW 0x0	Internal Bridge Error Mask No header log.
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 119: PCI Uncorrectable Error Severity Register
Offset: 0x00134

Bit	Field	Type/InitVal	Description
0	Reserved_1_0	RSVD 0x0	Reserved
1	Reserved_1	RW 0x0	Reserved
2	RcvTASev	RW 0x0	Received Target-Abort Severity Controls the severity indication of the PCI Express Secondary Uncorrectable errors. Each bit controls the error type of the corresponding bit in the PCI Express Secondary Uncorrectable Error Status. 0 = Non-Fatal: Error type is Non-Fatal. 1 = Fatal: Error type is Fatal.
3	RcvMASev	RW 0x0	Received Master-Abort Severity

Table 119: PCI Uncorrectable Error Severity Register (Continued)
Offset: 0x00134

Bit	Field	Type/InitVal	Description
4	Reserved_4	RSVD 0x0	Reserved
6:5	Reserved_6_5	RW 0x2	Reserved
7	UCDataErrSev	RW 0x0	Uncorrectable Data Error Severity
8	UCAttrErrSev	RW 0x1	Uncorrectable Attribute Error Severity
9	UCAddrErrSev	RW 0x1	Uncorrectable Address Error Severity
10	DTExpSev	RW 0x0	Delayed Transaction Discard Timer Expired Severity
11	PerrDetectedSev	RW 0x0	PCI_PERRn Assertion Severity
12	SerrDetectedSev	RW 0x1	PCI_SERRn Assertion Severity
13	InternalBrErrSev	RW 0x0	Internal Bridge Error Severity
31:14	Reserved_31_14	RSVD 0x0	Reserved

Table 120: PCI Error Capability and Control Register
Offset: 0x00138

Bit	Field	Type/InitVal	Description
4:0	SecUCFrstErrPtr	RO 0x0	PCI Uncorrectable First Error Pointer This field reports the bit position of the first error reported in the PCI Express Secondary Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself. **NOTE:** The bits in this field are sticky bits--they are not initialized or modified by reset.

Table 120: PCI Error Capability and Control Register (Continued)
Offset: 0x00138

Bit	Field	Type/InitVal	Description
31:5	Reserved	RSVD 0x0	Reserved

Table 121: PCI Header Log First DWORD Register
Offset: 0x0013C

Bit	Field	Type/InitVal	Description
31:0	SHL_TransAttr	RO 0x0	PCI Header Log First DWORD Logs the header of the first error reported in the PCI Express Secondary Uncorrectable Error Status. This field locks upon receipt of the first uncorrectable error that is not masked. It remains locked until software clears it by writing 1 to the corresponding status bit. Upon receipt of the next uncorrectable error that is not masked, the field locks again until cleared as described above. This lock and clear process continues to repeat itself. Transaction Attribute The value transferred on AD[31:0] during the attribute phase. This field is not relevant to conventional PCI. This field is hardwired to 0.

Table 122: PCI Header Log Second DWORD Register
Offset: 0x00140

Bit	Field	Type/InitVal	Description
3:0	SHL_TransAttr	RO 0x0	Transaction Attribute The value transferred on PCI_CBE[3:0]n during the attribute phase. This field is not relevant to conventional PCI. This field is hardwired to 0.
7:4	SHL_TransCmdLow	RO 0x0	Transaction Command Lower The 4-bit value transferred on PCI_CBE[3:0]n during the first address phase.
11:8	SHL_TransCmdUp	RO 0x0	Transaction Command Upper The 4-bit value transferred on PCI_CBE[3:0]n during the second address phase of a DAC transaction.
31:12	Reserved	RSVD 0x0	Reserved

Table 123: PCI Header Log Third DWORD Register
Offset: 0x00144

Bit	Field	Type/InitVal	Description
31:0	SHL_AddrLow	RO 0x0	Transaction Address Low. The 32-bit value transferred on AD[31:0] during the first address phase.

Table 124: PCI Header Log Fourth DWORD Register
Offset: 0x00148

Bit	Field	Type/InitVal	Description
31:0	SHL_AddrHigh	RO 0x0	Transaction Address High. The 32-bit value transferred on AD[31:0] during the second address phase. In the case of a 32-bit address, this field is set to zero.

B Revision History

Table 125: Revision History

Document Type	Revision	Date
Initial release	A	November 14, 2007
Release	B	February 27, 2008
1. This document is now unrestricted. 2. Figure 1, 88SB2211 Interface Pin Logic Diagram, on page 11 changed PCI_CLK_OUT[0]/PCI_IDSELn from input to bi-directional. 3. Updated Table 15, Power Dissipation, on page 29.		

This page is intentionally left blank.

Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.752.9028

www.marvell.com

Marvell. Moving Forward Faster