Signetics

8X305
Microcontroller

Product Specification

Military
Customer Specific Products

FEATURES

- **Fetch, Decode, and Execute a 16-bit instruction in a minimum of 200ns (one machine cycle)**
- **Bit-oriented instruction set (addressable single- or multiple-bit subfields)**
- **Separate buses for instruction, instruction Address and 3-State I/O**
- **Thirteen 8-bit general-purpose working registers**
- **Source/destination architecture**
- **Bipolar low-power Schottky technology/TTL inputs and outputs**
- **On-chip oscillator and timing generation**
- **Single +5V supply**
- **Multiple package options**

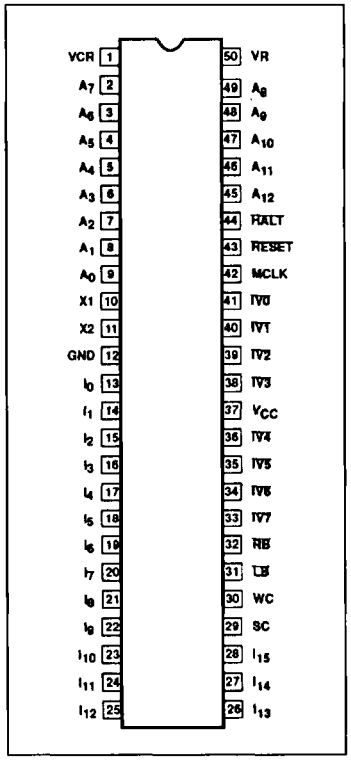
PRODUCT DESCRIPTION

The Signetics 8X305 Microcontroller is a high-speed bipolar micro-processor implemented with low-power Schottky technology. In a single chip, the 8X305 combines speed, flexibility, and a bit-oriented instruction set. These features and other basic characteristics of the chip combine to provide cost-effective solutions for a broad range of applications. The 8X305 is particularly useful in systems that require high-sped bit manipulations — sophisticated controllers, data communications, very fast interface control, and other applications of a similar nature.

The 8X305 can fetch, decode, and execute a 16-bit instruction word in a minimum of 200ns. Within one instruction cycle, the 8-bit data-processing path can be programmed to rotate, mask, shift, and/or merge single or multiple bit subfields and, in addition, perform an ALU operation; in the same instruction, an external data field can be input, processed, and output to a specified destination — likewise, single or multiple bit data fields can be fetched, processed, operated on by the ALU, and moved to a different location — all in a timeframe of 200ns. To interface with I/O and program memory, the 8X305 uses a 13-bit instruction address bus, a 16-bit instruction bus, an 8-bit bidirectional multiplexed I/O data/address bus and a 5-bit I/O control bus.

A wide selection of I/O devices, interface chips, and special-purpose parts are available for systems use. In most applications, the more powerful 8X305 is functionally interchangeable with its predecessor — the 8X300.

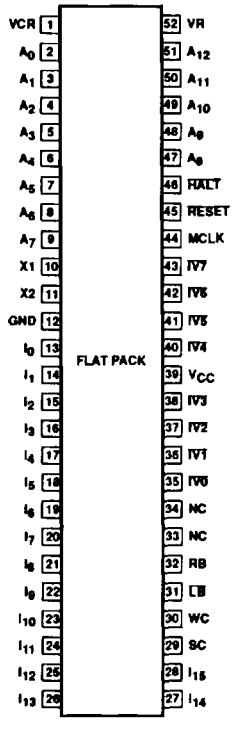
PIN CONFIGURATION

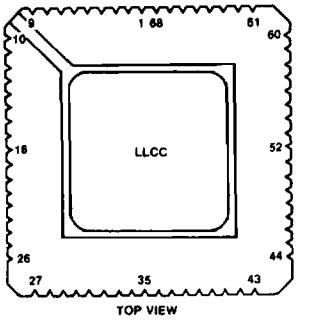


ORDERING INFORMATION

PACKAGES	CLOCK FREQUENCY	ORDER CODE
50–Pin DIP 0.9in	10MHz	8X305–10/BXA
68–Pin LLCC	10MHz	8X305–10/BUA
52–Pin FLAT PACK	10MHz	8X305–10/BYA
50–Pin DIP 0.9in	8MHz	8X305/BXA
68–Pin LLCC	8MHz	8X305/BUA
52–Pin FLAT PACK	8MHz	8X305/BYA

PIN CONFIGURATIONS





CD09390S

PIN DESCRIPTION

FLATPACK PIN NO.	LLCC PIN NO.	DIP PIN NO.	IDENTIFIER	FUNCTION
1	1, 68	1	VCR	Regulated voltage input from series-pass transistor (2N5320 or equivalent).
2–9, 47–51	4–11, 62–66	2–9, 45–49	$A_0 - A_{12}$	Program Address Lines: These active-high outputs permit direct addressing of up to 8192 words of program storage; A_{12} is Least Significant Bit.
10–11	12, 13	10, 11	X1, X2	Timing generator connections for a capacitor, a series resonant crystal, or an external clock source with complementary outputs.
12	2,3, 14–16	12	GND	Ground.
13–28	17–23, 28–36	13–28	$I_0 - I_{15}$	Instruction Lines: These active-high input lines receive 16-bit instructions from program storage; I_{15} is Least Significant Bit.
29	37	29	SC	Select Command: When high (binary 1), an address is being output on pins $\overline{IV0}$ through $\overline{IV7}$.
30	38	30	WC	Write Command: When high (binary 1), data is being output on pins $\overline{IV0}$ through $\overline{IV7}$.
31	39	31	$\overline{LB}$	Left Bank Control: When low (binary 0), devices connected to the Left Bank are accessed. (Note: Typically the $\overline{LB}$ signal is tied to the $\overline{ME}$ input pin of I/O peripherals.)

FLATPACK PIN NO.	LLCC PIN NO.	DIP PIN NO.	IDENTIFIER	FUNCTION
32	45	32	$\overline{RB}$	Right Bank Control: When low (binary 0), devices connected to the Right Bank are accessed. (Note: Typically, the $\overline{RB}$ signal is tied to the $\overline{ME}$ input pin of I/O peripherals.)
35–38, 40–43	46–49, 55–58	33–36, 38–41	$\overline{IV0} - \overline{IV7}$	Interface Vector (Input/Output Bus) — these bidirectional active-low 3-State lines communicate data and/or addresses to I/O devices and memory locations. A low voltage level equals a binary "1"; $\overline{IV7}$ is Least Significant Bit.
39	50–52	37	V_{CC}	+5V power supply.
44	59	42	MCLK	Master Clock: This active-high output signal is used for clocking I/O devices and/or synchronization of external logic.
45	60	43	$\overline{RESET}$	When $\overline{RESET}$ input is low (binary 0), the 8X305 is initialized — sets Program Counter/Address Register to zero and inhibits MCLK. For the period of time $\overline{RESET}$ is low, the Left Bank/Right Bank ($\overline{LB}/\overline{RB}$) signals are forced high asynchronously.
46	61	44	$\overline{HALT}$	When $\overline{HALT}$ input is low (binary 0), internal operation of the 8X305 stops at the start of next instruction; MCLK is not inhibited nor is any internal register affected; however, both the Left Bank/Right Bank ($\overline{LB}/\overline{RB}$) signals are synchronously driven high during the first quarter of the instruction cycle time and remain high during the time HALT is low.
52	67	50	VR	Internally-generated reference output voltage for external series-pass regulator transistor.
33, 34	24–27, 40–44, 53, 54	–	No Connect	

NOTE: Multiple V_{CC}, GND, and V_{CR} pins must be externally connected.

ELECTRICAL PERFORMANCE CHARACTERISTICS AND TEST REQUIREMENTS

For Absolute Maximum Ratings, Recommended Operating Conditions, and Electrical Test Requirements, refer to Military Drawing 85502.
For Detail Application Notes, contact Signetics Military Marketing at (408) 991-2722.