Signetics

8X371

8-Bit Latched Bidirectional I/O Port

Product Specification

Military
Customer Specific Products

FEATURES

- **Two bidirectional 8-bit busses**
- **Independent bus operation (user-bus priority for data entry)**
- **User data input synchronous with respect to MCLK**
- **3-State TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305**
- **Single +5V supply**
- **0.4", 24-pin DIP**

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the $\overline{UIC}$ and $\overline{UOC}$ inputs. Data input to the UD bus is synchronous with MCLK, that is, with $\overline{UIC}$ Low, information is written into the data latches only when MCLK is High. Output drivers on the UD bus are enabled when $\overline{UOC}$ is Low and $\overline{UIC}$ is High.

PRODUCT DESCRIPTION

The 8X371 I/O Port is a bidirectional device designed for use as an interface element in systems that use TTL-compatible busses. Typically, the 8X371 is used with the 8X305 Microcontroller and its associated Interface Vector ($\overline{IV}$) bus; however, it can also be used with an equivalent microprocessor. As shown in the logic diagram of Figure 1, the 8X371 consists of eight identical data latches — bits 0 through 7. The latches are accessed from either of two 8-bit busses — the Microcontroller ($\overline{IV}$ bus) and the user data (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time; in such situations, the user bus always has priority. A Master Enable ($\overline{ME}$) input is available for additional control over the $\overline{IV}$ bus. The data latches are transparent, in that, while either bus is enabled for input, all input-data transitions are propagated to the other bus, if enabled for output.

Table 1. Input/Output Control Of UD Bus

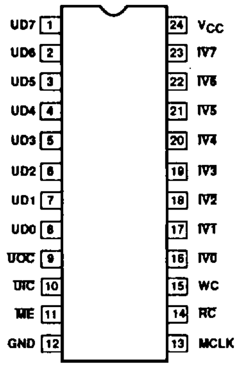
$\overline{UIC}$	$\overline{UOC}$	MCLK	FUNCTION OF UD BUS
H	L	X	Output data
L	X	H	Input data
L	X	L	Inactive
H	H	X	Inactive

NOTE:
X = don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin DIP	8X371/BXA

PIN CONFIGURATION



PIN NO.	IDENTIFIER	FUNCTION
1–8	UD7–UD0	3-State, bidirectional User Data (UD) bus; UD0 and corresponds to $\overline{IV0}$.
9	$\overline{UOC}$	User Output Control – active low input to enable data output to UD0 – UD7.
10	$\overline{UIC}$	User Input Control – active low input to enable data input from UD0 – UD7.
11	$\overline{ME}$	Master Enable – active low input to enable the $\overline{IV}$ bus for data input, or data output; UD–bus operations are unaffected.
12	GND	Ground.
13	MCLK	Master Clock – active high input (from Microcontroller used to strobe data into data latches from the $\overline{IV}$ and UD buses.
14	$\overline{RC}$	Read Control – active low input to enable data output to $\overline{IV0}$ – $\overline{IV7}$.
15	WC	Write Command – active high input (from Micontroller) to enable the writing of data into the data latches from the $\overline{IV}$ bus (provided $\overline{UIC}$ is not low).
16–23	$\overline{IV0}$–$\overline{IV7}$	Interface Vector (Input/Output Bus) – 3-State, bidirectional, Microcontroller data bus; $\overline{IV0}$ corresponds to UD0.
24	V_{CC}	+5V power supply.

8-Bit Latched Bidirectional I/O Port

8X371

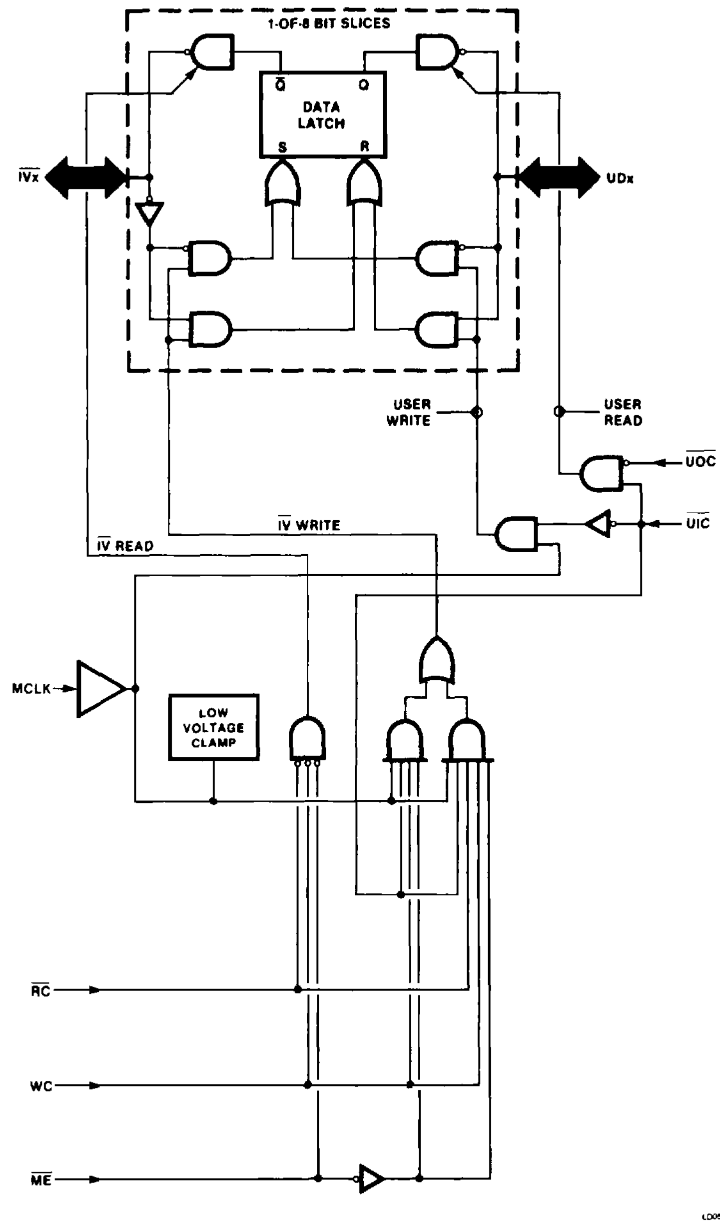


Figure 1. Logic Diagram for 8X371 I/O Port

$\overline{IV}$ Bus Control

Input/output control of the $\overline{IV}$ bus is shown in Table 2; this bus is controlled by $\overline{RC}$, WC, $\overline{ME}$, and MCLK. The $\overline{IV}$ bus is enabled for output (Microcontroller read operation) when $\overline{ME}$, $\overline{RC}$, and WC are all low. Data is written into the data latches from the $\overline{IV}$ bus when $\overline{ME}$ is low and both WC and MCLK are high. To avoid data-input conflicts, inputs from the $\overline{IV}$ bus are inhibited when $\overline{UIC}$ is low; under all other conditions, the $\overline{IV}$ and UD busses operate independently. The Microcontroller Left Bank ($\overline{LB}$) and Right Bank ($\overline{RB}$) outputs can control the $\overline{ME}$ inputs for two banks of I/O devices, thus acting as a ninth address bit. If more than one I/O Port (including the addressable parts — 8X372, 8X376, 8X382, etc.) are to be connected to the same bank ($\overline{LB}$ or $\overline{RB}$) of the Microcontroller, selection of each 8X371 must be accomplished with external logic to avoid bus conflicts.

Table 2. Input/Output Control Of $\overline{IV}$ Bus

$\overline{ME}$	$\overline{RC}$	WC	MCLK	$\overline{UIC}$	FUNCTION OF $\overline{IV}$ BUS
L	L	L	X	X	Output Data
L	X	H	H	H	Input Data
L	H	L	X	X	Inactive
L	X	H	X	L	Inactive
L	X	H	L	H	Inactive
H	X	X	X	X	Inactive

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: *A logic "1" in Microcontroller software corresponds to a high level on the UD bus even though the $\overline{IV}$ bus is inverted.*) The 8X382 wakes up in the unselected state with all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
T_{STG}	Storage temperature range	−65 to +150	°C

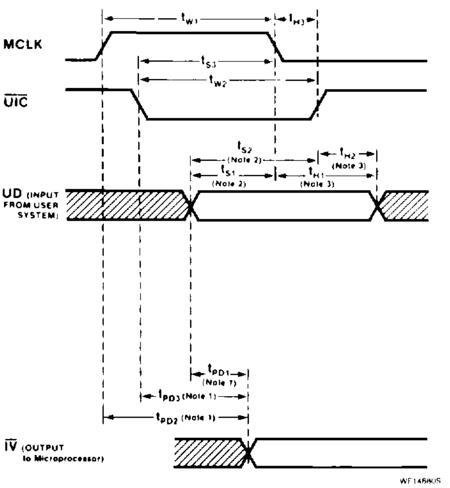
DC ELECTRICAL CHARACTERISTICS $4.75V \le V_{CC} \le 5.25V$, $-55°C \le T_C \le +125°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN; $I_I = -10mA$			−1.5	V
I_{IH}	High level input current[1]	V_{CC} = MAX; V_{IH} = 2.7V			100	µA
I_{IL}	Low level input current[1]	V_{CC} = MAX; V_{IL} = 0.5V			−550	µA
V_{OL}	Low level output voltage	V_{CC} = MIN; I_{OL} = 16mA			0.55	V
	$\overline{IV}$ bus ($\overline{IV0}$ – $\overline{IV7}$), User bus (UD4 – UD7)	V_{CC} = MIN; I_{OL} = 24mA			0.55	V
V_{OH}	High level output voltage	V_{CC} = MIN; I_{OH} = −3.2mA	2.4			V
I_{OS}	Short circuit output current[2]	V_{CC} = MAX	−20			mA
	$\overline{IV}$ bus ($\overline{IV0}$ – $\overline{IV7}$), UD bus (UD4 – UD7)	V_{CC} = MAX	−10			mA
I_{CC}	Supply current	V_{CC} = MAX; $\overline{ME}$ = $\overline{UOC}$ = V_{CC}			150	mA

AC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$

SYMBOL	PARAMETER	REFERENCES		TEST CONDITIONS	LIMITS		UNIT
		From	To		Min	Max	
Pulse Widths:							
T_{W1}	Clock high	$\uparrow$MCLK	$\downarrow$MCLK		30		ns
t_{W2}	User input control	$\downarrow\overline{UIC}$	$\uparrow\overline{UIC}$	MCLK = High	35		ns
Propagation Delays:							
t_{PD1}	UD propagation delay	UD	IV	MCLK = High $\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UCI}$ = Low		45	ns
t_{PD2}	UD clock delay	$\uparrow$MCLK	IV	UD = stable; $\overline{RC}$ = WC = $\overline{ME}$ = $\overline{UIC}$ = Low		55	ns
t_{PD3}	UD input delay	$\downarrow\overline{UIC}$	IV	UD = Stable; MCLK = High $\overline{RC}$ = WC = $\overline{ME}$ = Low		55	ns
t_{PD4}	IV data propagation delay	IV	UD	MCLK = WC = $\overline{UIC}$ = High; $\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low		45	ns
t_{PD5}	IV data clock delay	$\uparrow$MCLK	UD	WC = $\overline{UIC}$ = High; IV = Stable $\overline{ME}$ = $\overline{UOC}$ = $\overline{RC}$ = Low		55	ns
Output Enable Timing:							
t_{OE1}	UD output enable	$\downarrow$UOC	UD	$\overline{UIC}$ = High		45	ns
t_{OE2}	UD input recovery	$\uparrow\overline{UIC}$	UD	$\overline{UOC}$ = Low		45	ns
t_{OE3}	IV data master enable	$\downarrow\overline{ME}$	IV	WC = $\overline{RC}$ = Low		45	ns
t_{OE4}	IV data read enable	$\downarrow\overline{RC}$	IV	WC = $\overline{ME}$ = Low		45	ns
t_{OE5}	IV data write recovery	$\downarrow$WC	IV	$\overline{RC}$ = $\overline{ME}$ = Low		45	ns
Output Disable Timing:							
t_{OD1}	UD output disable	$\uparrow\overline{UOC}$	UD	$\overline{UIC}$ = High		40	ns
t_{OD2}	UD input override	$\downarrow\overline{UIC}$	UD	$\overline{UOC}$ = Low		45	ns
t_{OD3}[3]	IV data master disable	$\uparrow\overline{ME}$	IV	WC = $\overline{RC}$ = Low		40	ns
t_{OD4}[3]	IV data read disable	$\uparrow\overline{RC}$	IV	WC = $\overline{ME}$ = Low		40	ns
t_{OD5}[3]	IV data write override	$\uparrow$WC	IV	$\overline{RC}$ = $\overline{ME}$ = Low		40	ns
Setup Time:							
t_{S1}	UD clock setup time	UD	$\downarrow$MCLK	$\overline{UIC}$ = Low	15		ns
t_{S2}	UD setup time	UD	$\uparrow$UIC	MCLK = High	25		ns
t_{S3}	User input control setup time	$\downarrow\overline{UIC}$	$\downarrow$MCLK		25		ns
t_{S4}	IV data setup time	IV	$\downarrow$MCLK	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low	15		ns
t_{S5}[4]	IV master enable setup time	$\downarrow\overline{ME}$	$\downarrow$MLCK	WC = $\overline{UIC}$ = High	20		ns
t_{S6}	IV write control setup time	$\uparrow$WC	$\downarrow$MCLK	$\overline{ME}$ = Low; $\overline{UIC}$ = High	40		ns
Hold Times:							
t_{H1}	UD clock hold time	$\downarrow$MCLK	UD	$\overline{UIC}$ = Low	20		ns
t_{H2}	UD control hold time	$\uparrow\overline{UIC}$	UD	MCLK = High	10		ns
t_{H3}	User input control hold time	$\downarrow$MCLK	$\uparrow$UIC		0		ns
t_{H4}	IV data hold time	$\downarrow$MCLK	IV	WC = $\overline{UIC}$ = High; $\overline{ME}$ = Low — 25°C	5		ns
				Temp.	20		ns
t_{H5}[4]	IV master enable hold time	$\downarrow$MCLK	$\downarrow\overline{ME}$	WE = $\overline{UIC}$ = High	0		ns
t_{H6}	IV write control hold time	$\downarrow$MCLK	$\downarrow$WC	$\overline{ME}$ = Low; $\overline{UIC}$ = High	0		ns

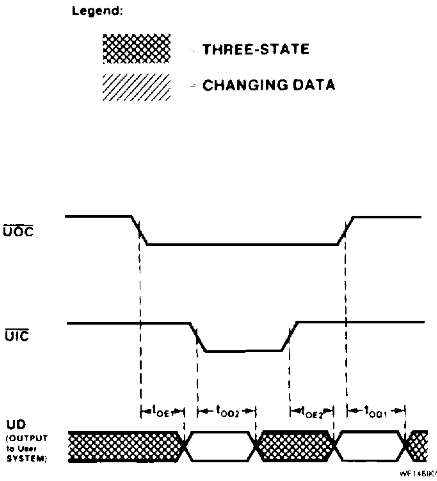
NOTES:
1. The input current includes the 3-State leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These parameters are measured with a capacitive loading of 50pF and represent the output driver turn-off time.
4. If $\overline{ME}$ is to be high (inactive), it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.



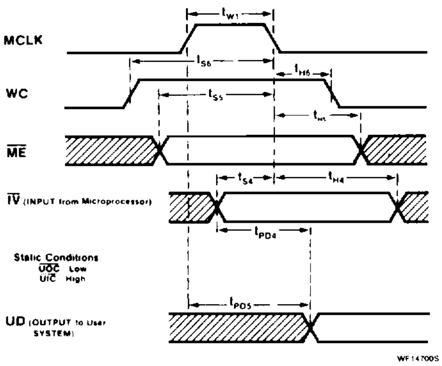
STATIC CONDITIONS:
SC = WC = $\overline{ME}$ = Low; $\overline{UOC}$ = High

NOTES:
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from t_{PD1}, t_{PD2}, and t_{PD3}.
2. The UD input must satisfy the setup-time requirements for both t_{S1} and t_{S2}.
3. Minimum hold-time required for the UD input is the earlier of the times specified by t_{H1} and t_{H2}.

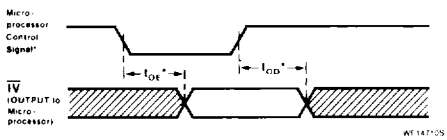
a. User Data Input Timing



b. User Data Output Timing



c. Microcontroller Write Cycle Timing



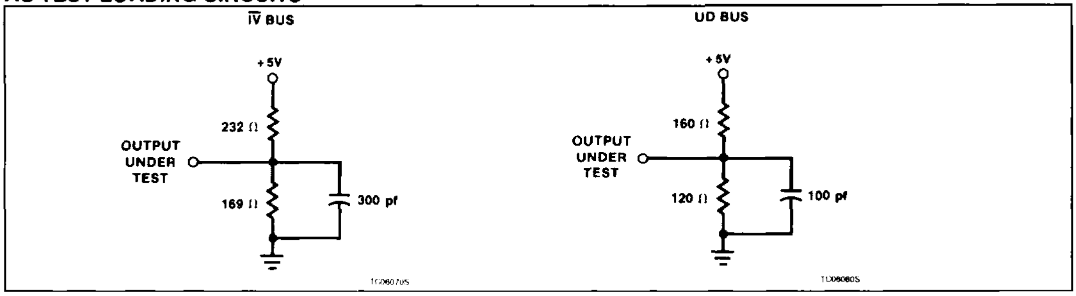
***PARAMETER KEY**

MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
$\overline{ME}$	t_{OE3} t_{OD3}	SC = WC = LOW
$\overline{RC}$	t_{OE4} t_{OD4}	SC = $\overline{ME}$ = LOW
SC	t_{OE5} t_{OD5}	$\overline{RC}$ = $\overline{ME}$ = LOW

d. Microcontroller Select Cycle Timing

Figure 2. Timing Diagrams

AC TEST LOADING CIRCUITS



APPLICATIONS

In some applications, performance of a Microcontroller system can be enhanced by using the 8X371 I/O Port instead of an addressable 8X372 port. Using a technique referred to as Extended Microcode or Fast IV Select, the address select cycles which normally precede a read or write operation when using an 8X372 can be eliminated by use of the 8X371.

This technique is often used in bit slice microprocessor designs and involves widening the program memory beyond the normal 16-bit requirement of the Microcontroller. the extra bits are used as enable signals for the 8X371 ports. Thus, the 8X371 is enabled during the instruction cycle in which it is required for input/output operations. Since the software overhead of separate address select cycles is eliminated, the overall system performance is improved.

As shown in the accompanying diagram, the program memory is extended by two bit positions (D_{16} and D_{17}), permitting any one of four 8X371 ports to be enabled during those instructions. Because of timing considerations, latches must be used to hold the Extended Microcode through the end of the instruction cycle. A decoder is used to obtain four enable signals from the two extra bits. The decoder outputs are ORed with the LB output of the 8X305; thus, all four I/O ports are placed on the Left Bank of the IV bus.

I/O PORT SELECTION USING EXTENDED MICROCODE