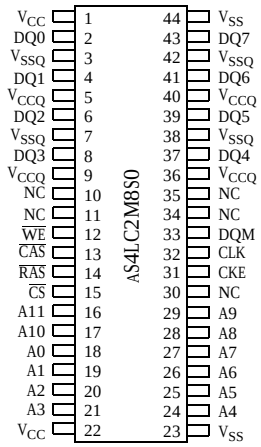
3.3V 2M×8/1M×16 CMOS synchronous DRAM

Features

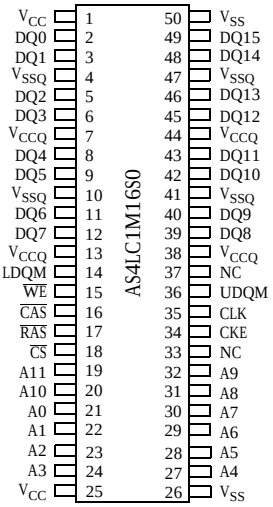
- Organization:
  1,048,576 words × 8 bits × 2 banks (2M×8)
  524,288 words × 16 bits × 2 banks (1M×16)
- All signals referenced to positive edge of clock
- Dual internal banks controlled by A11 (bank select)
- High speed
  - 125/100/83 MHz
  - 6/7/8.5 ns clock access time
- Low power consumption
  - Active: 576 mW max
  - Standby: 7.2 mW max, CMOS I/O
- 4096 refresh cycles, 64 ms refresh interval
- Auto refresh and self refresh
- Automatic and direct precharge
- Burst read, single write
- Can assert random column address in every cycle
- LVTTL compatible I/O
- 3.3V power supply
- JEDEC standard package, pinout and function
  - 400 mil, 44-pin TSOP II (2M×8)
  - 400 mil, 50-pin TSOP II (1M×16)
- Read/write data masking
- Programmable burst length (1/2/4/8/full page)
- Programmable burst sequence (sequential/interleaved)
- Programmable $\overline{CAS}$ latency (1/2/3)

Pin arrangement

TSOP II



TSOP II



Pin designation

Pin(s)	Description
DQM (2M×8) UDQM/LDQM (1M×16)	Output disable/write mask
A0 to A10	Address inputs
A11	Bank select
DQ0 to DQ7 (2M×8) DQ0 to DQ15 (1M×16)	Input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}, V_{CCQ}	Power (3.3V ± 0.3V)
V_{SS}, V_{SSQ}	Ground
CLK	Clock input
CKE	Clock enable

DRAM

Selection guide

	Symbol	AS4LC2M8S0-8	AS4LC2M8S0-10	AS4LC2M8S0-12	Unit
Bus frequency (CL = 3)	f_{max}	125	100	83.3	MHz
Maximum clock access time (CL = 3)	t_{AC}	6	7	8.5	ns
Minimum input setup time	t_S	2	2	3.0	ns
Minimum input hold time	t_H	1.0	1.0	1.0	ns
Row cycle time (CL=3, BL=1)	t_{RC}	72	80	90	ns
Maximum operating current	I_{CC1}	100	80	75	mA
Maximum CMOS standby current, self refresh	I_{CC6}	1	1	1	mA

Functional description

The AS4LC2M8S0 and AS4LC1M16S0 are high performance 16 megabit CMOS Synchronous Dynamic Random Access Memories (SDRAM) organized as 1,048,576 words × 8 bits × 2 banks and 524,288 words × 16 bits × 2 banks, respectively. Very high bandwidth is achieved using a pipelined architecture where all inputs and outputs are referenced to the rising edge of a common clock. Programmable burst mode can be used to read up to a full page of data (512 bytes for 2M×8 and 256 bytes for 1M×16) without selecting a new column address.

The two internal banks can be alternately accessed (read or write) at the maximum clock frequency for seamless interleaving operations. This provides a significant advantage over asynchronous EDO and fast page mode devices.

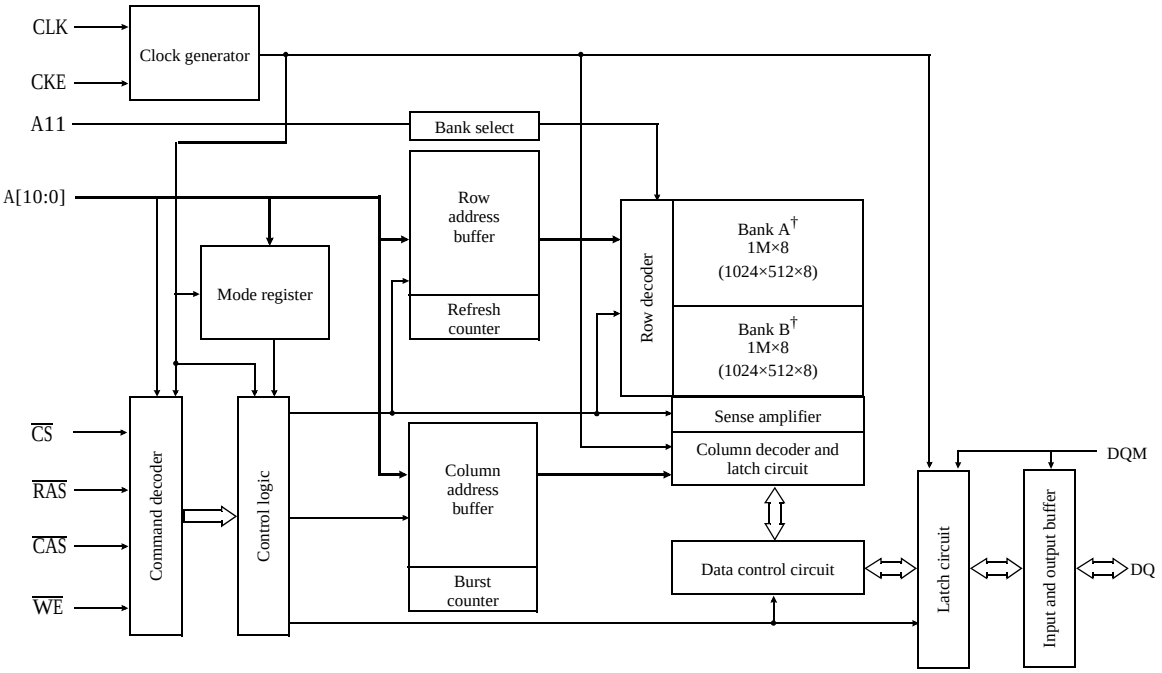
This SDRAM product also features a programmable mode register, allowing users to select read latency as well as burst length and type (sequential or interleaved). Lower latency improves first data access in terms of CLK cycles, while higher latency improves maximum frequency of operation. This feature enables flexible performance optimization for a variety of applications.

DRAM commands and functions are decoded from control inputs. Basic commands are as follows:

- Mode register set
- Select column, write
- Auto precharge with read/write
- De-activate bank
- Select column, read
- Self refresh
- Deactivate all banks
- Deselect, power down
- Select row, activate bank
- CBR refresh

Both devices are available in 400 mil plastic TSOP type 2 package. The AS4LC2M8S0 has 44 pins, and the AS4LC1M16S0 has 50 pins. Both devices operate with a power supply of 3.3V ± 0.3V. Multiple power and ground pins are provided for low switching noise and EMI. Inputs and outputs are LVTTL compatible.

Logic block diagram



† For AS4LC1M16S0, Banks A & B will read 1M×16 (1024×256×16).

Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit
Supply voltage	V_{CC},V_{CCQ}	3.0	3.3	3.6	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
	V_{IL}	–0.3†	–	0.8	V
Output voltage‡	V_{OH}	2.4	–	–	V
	V_{OL}	–	–	0.4	V
Ambient operating temperature	T_A	0		70	°C

†V_{IL} min = -1.5V for pulse widths less than 5 ns.

‡I_{OH} = -2mA, and I_{OL} = 2mA

Recommended operating conditions apply throughout this document unless otherwise specified.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Input voltage	V_{in},V_{out}	-1.0	+4.6	V
Power supply voltage	V_{CC},V_{CCQ}	-1.0	+4.6	V
Storage temperature (plastic)	T_{STG}	-55	+150	°C
Power dissipation	P_D	–	1	W
Short circuit output current	I_{out}	–	50	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC electrical characteristics

Parameter	Symbol	Test conditions		-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	Unit	Notes
Input leakage current	I_{IL}	0V ≤ V_{in} ≤ V_{CC}, Pins not under test = 0V		-5	+5	-5	+5	-5	+5	µA	
Output leakage current	I_{OL}	D_{OUT} disabled, 0V ≤ V_{out} ≤ V_{CCQ}		-5	+5	-5	+5	-5	+5	µA	
Operating current (one bank active)	I_{CC1}	t_{RC} ≥ min, IOL = 0mA, burst length = 1		–	100	–	80	–	75	mA	1
Precharge standby current (power down mode)	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = 15 ns		–	2.0	–	2.0	–	2.0	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CK} = ∞		–	2.0	–	2.0	–	2.0	mA	
Precharge standby current (non-power-down mode)	I_{CC2N}	CS ≥ V_{IH}(min), CKE ≥ V_{IH}(min), t_{CC} = 15 ns; input signals changed once during 30 ns		–	20	–	20	–	20	mA	
	I_{CC2NS}	CLK ≤ V_{IL}(max), CKE ≥ V_{IH}(min), t_{CK} = ∞; input signals stable		–	6	–	6	–	6	mA	
Active standby current (power down mode)	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = 15 ns		–	2	–	2	–	2	mA	
	I_{CC3PS}	CLK, CKE ≤ V_{IL}(max), t_{CK} = ∞		–	2	–	2	–	2	mA	
Active standby current (non power down mode, one bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CK} = 15 ns; input signals changed once during 30 ns		–	35	–	27	–	27	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≥ V_{IL}(max), t_{CK} = ∞; input signals stable		–	12	–	10	–	10	mA	
Operating current (burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst All banks activated t_{CCD} = t_{CCD}(min)	CL =3	–	130	–	120	–	110	mA	1,2
			CL =2	–	95	–	85	–	80		
			CL =1	–	70	–	60	–	55		
Refresh current	I_{CC5}	t_{RC} ≥ t_{RC}(min)		–	70	–	65	–	65	mA	3
Self refresh current	ICC6	CKE ≤ 0.2 V		–	2	–	2	–	2	mA	
				–	1	–	1	–	1	mA	4

CL = CAS latency

1 This parameter depends on output loading and cycle rates. Measured with outputs open, inputs only change one time during t_{CK} (min).

2 Assumed t_{CCD} (min)

3 Refresh period = 64ms.

4 Low power version

DRAM

AC parameters common to all waveforms

Symbol	Parameter	CAS latency	-8 Min	-8 Max	-10 Min	-10 Max	-12 Min	-12 Max	Unit	Notes
t_{RRD}	Row active to row active delay		16	–	20	–	24	–	ns	1
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time		20	–	26	–	30	–	ns	1
t_{RP}	Row precharge		20	–	26	–	30	–	ns	1
t_{RAS}	Row active		48	100,000	50	100,000	60	100,000	ns	1
t_{RC}	Row cycle time		72	–	80	–	90	–	ns	1
t_{CDL}	Last data in to new column address delay		1	–	1	–	1	–	CLK	2
t_{RDL}	Last data in to row precharge		1	–	1	–	1	–	CLK	2
t_{BDL}	Last data in to burst stop		1	–	1	–	1	–	CLK	2
t_{CCD}	Column address to column address delay		1	–	1	–	1	–	CLK	3
t_{CK}	CLK cycle time	3	8	1000	10	1000	12	1000	ns	4
		2	10	1000	14	1000	15	1000		4
		1	20	1000	28	1000	30	1000		4
t_{AC}	CLK to valid output delay	3	–	6	–	7	–	8.5	ns	4,5
		2	–	6	–	8.5	–	9.0		4,5
		1	–	16	–	23	–	25		4,5
t_{OH}	Output data hold time	3	3	–	3	–	3	–	ns	
		2	3	–	3	–	3	–		
		1	3	–	3	–	3	–		
t_{CH}	CLK high pulse width		3	–	3.5	–	4	–	ns	6
t_{CL}	CLK low pulse width		3	–	3.5	–	4	–	ns	6
t_{S}	Input setup time		2	–	2	–	3	–	ns	6
t_{H}	Input hold time		1	–	1	–	1	–	ns	6
t_{SLZ}	CLK to output in low Z	1	1	–	1	–	1	–	ns	5
t_{SHZ}	CLK to output in high Z	3	3	6	–	8	–	8	ns	
		2	3	7	–	11	–	11		
		1	3	15	–	18	–	18		

1 Minimum clock cycles = (Minimum time / clock cycle time) rounded up
2 Minimum delay required to complete write.
3 Column address change allowed every cycle.
4 Parameters dependent on CAS latency.
5 If clock rising time > 1ns, (tr/2-0.5)ns should be added to parameter.
6 If (tr and tf) > 1ns, [(tr+tf)/2-1]ns should be added to parameter.

Operating modes

Command			CKE_{n-1}	CKE_n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A11	A10	A9–A0	Note
Mode register set			H	X	L	L	L	L	X		Op code		1,2
Auto refresh			H	H	L	L	L	H	X		X		3
Self refresh	Entry		H	L	L	L	L	H	X		X		3
	Exit		L	H	L	H	H	H	X		X		3
					H	X	X	X	X		X		3
Bank activate			H	X	L	L	H	H	X	V	row address		
Read	Auto precharge disable		H	X	L	H	L	H	X	V	L	column address	4
	Auto precharge enable										H		4,5
Write	Auto precharge disable		H	X	L	H	L	L	X	V	L	column address	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X		X		6
Precharge	Selected bank		H	X	L	L	H	L	X	V	L	X	
	Both banks									X	H		
Clock suspend or active power down	Entry		H	L	H	X	X	X	X		X		
					L	V	V	V	X				
	Exit		L	H	X	X	X	X	X				
Precharge power down mode	Entry		H	L	H	X	X	X	X		X		
					L	H	H	H	X				
	Exit		L	H	H	X	X	X	X				
					L	V	V	V	X				
DQM			H	X	X	X	X	X	V	X	X	X	7
No operation command			H	X	H	X	X	X	X		X		
					L	H	H	H	X				

1 OP = operation code
A0~A11 see page 8

2 MRS can be issued only when both banks are precharged. A new command can be issued 2 clock cycles after MRS.

3 Auto refresh functions similarly to CBR DRAM refresh. However, precharge is automatic.
Auto/self refresh can only be issued after both banks are precharged.

4 A11: bank select address. If low during read, write, row active and precharge, bank A is selected.
If high during those states, bank B is selected. Both banks are selected and A11 is ignored if A10 is high during row precharge.

5 A new read/write command cannot be issued during a burst read/write with auto precharge.
It must be issued after the end of the burst. A new row active command can be issued after t_{RP} from the end of the burst.

6 Burst stop command valid at every burst length.

7 DQM sampled at positive edge of CLK. Data-in may be masked at every CLK (Write DQM latency is 0).
Data-out mask is active 2 CLK cycles after issuance. (Read DQM latency is 2).

Mode register fields

Register programmed with MRS

Address	A11~A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU†	WBL	TM		CAS latency			BT	burst length		

† RFU = 0 during MRS cycle.

Write burst length

A9	Length
0	Programmed burst length
1	Single burst

Burst type

A3	Type
0	Sequential
1	Interleaved

Test mode

A8	A7	Type
0	0	Mode register set
0	1	Reserved
1	0	Reserved
1	1	Reserved

CAS latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	Reserved

Burst length

A2	A1	A0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	X	X	Reserved†	Reserved

†Burst length = full page when A2~A0 = 1.

Burst sequence

(burst length = 4)

Initial address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Burst sequence

(burst length = 8)

Initial address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Pin descriptions

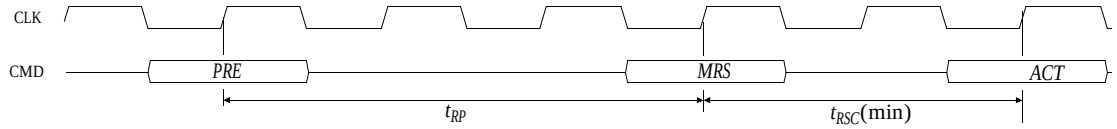
Pin	Name	Description
CLK	System clock	All operations synchronized to rising edge of CLK.
CKE	Clock enable	Controls CLK input. If CKE is high, the next CLK rising edge is valid. If CKE is low, the internal clock is suspended from the next clock cycle and the burst address and output states are frozen. If both banks are idle and CKE goes low, the SDRAM will enter power down mode from the next clock cycle. When in power down mode and CKE is low, no input commands will be acknowledged. To exit power down mode, raise CKE high before the rising edge of CLK.
$\overline{CS}$	Chip select	Enables or disables device operation by masking or enabling all inputs except CLK, CKE, DQM.
A0~A10	Address	Row and column addresses are multiplexed. Row address: A0~A10. Column address (2M×8): A0~A8. Column address (1Mx16): A0~A7.
A11	Bank select	Memory cell array is organized in 2 banks. A11 selects which internal bank will be active. A11 is latched during bank activate, read, write, mode register set, and precharge operations. Asserting A11 low selects Bank A; A11 high selects Bank B.
$\overline{RAS}$	Row address strobe	Enables row access and precharge operation. When $\overline{RAS}$ is low, row address is latched at the rising edge of CLK.
$\overline{CAS}$	Column address strobe	Enables column access. When $\overline{CAS}$ is low, column address is latched at the rising edge of CLK.
$\overline{WE}$	Write enable	Enables write operation and row precharge operation. When $\overline{WE}$ is low, input data is latched starting from $\overline{CAS}$.
DQM	Output disable/ write mask	Controls I/O buffers. When DQM is high, output buffers are disabled during a read operation and input data is masked during a write operation. DQM latency is 2 clocks for Read and 0 clocks for Write.
DQ0~DQ15	Data input/output	Data inputs/outputs are multiplexed.
V_{DD}/V_{SS}	Power supply/ground	Power and ground for core logic and input buffers.
V_{DDQ}/V_{SSQ}	Data output power/ground	Power and ground for data output buffers.

Device operation

Command	Pin settings	Description
Power up		The following sequence is recommended prior to normal operation. 1. Apply power, start clock, and assert CKE and DQM high. All other signals are NOP. 2. After power-up, pause for a minimum of 200µs. CKE/DQM = high; all others NOP. 3. Precharge both banks. 4. Perform Mode Register Set command to initialize mode register. 5. Perform a minimum of 8 auto refresh cycles to stabilize internal circuitry. (Steps 4 and 5 may be interchanged.)
Mode register set	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = low; A0~A11 = opcode	The mode register stores the user selected opcode for the SDRAM operating modes. The $\overline{CAS}$ latency, burst length, burst type, test mode and other vendor specific functions are selected/programmed during the Mode Register Set command cycle. The default setting of the mode register is not defined after power-up. Therefore, it is recommended that the power-up and mode register set cycle be executed prior to normal SDRAM operation. Refer to the Mode Register Set table and timing for details.
Device deselect and no operation	$\overline{CS}$ = high	The SDRAM performs a "no operation" (NOP) when $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ = high. Since the NOP performs no operation, it may be used as a wait state in performing normal SDRAM functions. The SDRAM is deselected when $\overline{CS}$ is high. $\overline{CS}$ high disables the command decoder such that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address inputs are ignored. Device deselection is also considered a NOP.
Bank activation	$\overline{CS}$ = $\overline{RAS}$ = low; $\overline{CAS}$ = $\overline{WE}$ = high; A0~A10 = row address; A11 = bank select	The SDRAM is configured with two internal banks. Use the Bank Activate command to select a row in one of the two idle banks. Initiate a read or write operation after t_{RCD}(min) from the time of bank activation.
Burst read	$\overline{CS}$ = $\overline{CAS}$ = A10 = low; $\overline{RAS}$ = $\overline{WE}$ = high; A11 = bank select, A0~A8 = column address; (A9 = don't care for 2M×8; A8,A9 = don't care for 1M×16)	Use the Burst Read command to access a consecutive burst of data from an active row in an active bank. Burst read can be initiated on any column address of an active row. The burst length, sequence and latency are determined by the mode register setting. The first output data appears after the $\overline{CAS}$ latency from the read command. The output goes into a high impedance state at the end of the burst (BL = 1,2,4,8) unless a new burst read is initiated to form a gapless output data stream. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write
Burst write	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ = A10 = low; $\overline{RAS}$ = high; A0~A9 = column address; (A9 = don't care for 2M×8; A8,A9 = don't care for 1M×16)	Use the Burst Write command to write data into the SDRAM on consecutive clock cycles to adjacent column addresses. The burst length and addressing mode is determined by the mode register opcode. Input the initial write address in the same clock cycle as the Burst Write command. Terminate the burst with a burst stop command, precharge command to the same bank or another burst read/write. DQM can also be used to mask the input data.
DQM operation		Use DQM to mask input and output data. It disables the output buffers in a read operation and masks input data in a write operation. The output data is invalid 2 clocks after DQM assertion (2 clock latency). Input data is masked on the same clock as DQM assertion (0 clock latency).
Burst stop	$\overline{CS}$ = $\overline{WE}$ = low; $\overline{RAS}$ = $\overline{CAS}$ = high	Use burst stop to terminate burst operation. This command may be used to terminate all legal burst lengths.

Command	Pin settings	Description
Bank precharge	$\overline{CS}$ = A10 = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = high; A11 = bank select; A0~A9 = don't care	The Bank Precharge command precharges the bank specified by A11. The precharged bank is switched from active to idle state and is ready to be activated again. Assert the precharge command after t_{RAS}(min) of the bank activate command in the specified bank. The precharge operation requires a time of t_{RP}(min) to complete.
Precharge all	$\overline{CS}$ = $\overline{RAS}$ = $\overline{WE}$ = low; $\overline{CAS}$ = A10 = high; A11 = bank select; A0~A9 = don't care	The Precharge All command precharges both banks simultaneously. Both banks are switched to the idle state on precharge completion.
Auto precharge	$\overline{CS}$ = $\overline{CAS}$ = $\overline{WE}$ (write) = low; $\overline{RAS}$ = $\overline{WE}$ (read) = A10 = high; A11 = bank select; A0~A9 = column address; (A9 = don't care for 2M×8; A8,A9 = don't care for 1M×16)	During auto precharge, the SDRAM adjusts internal timing to satisfy t_{RAS}(min) and t_{RP} for the programmed $\overline{CAS}$ latency and burst length. Couple the auto precharge with a burst read/write operation by asserting A10 to a high state at the same time the burst read/write commands are issued. At auto precharge completion, the specified bank is switched from active to idle state. Note that no new commands can be issued until the specified bank achieves the idle state
Clock suspend/ power down mode entry	CKE = low	When CKE is low, the internal clock is frozen or suspended from the next clock cycle and the state of the output and burst address are frozen. If both banks are idle and CKE goes low, the SDRAM enters power down mode at the next clock cycle. When in power down mode, no input commands are acknowledged as long as CKE remains low. To exit power down mode, raise CKE high before the rising edge of CLK.
Clock suspend/ power down mode exit	CKE = high	Resume internal clock operation by asserting CKE high before the rising edge of CLK. Subsequent commands can be issued one clock cycle after the end of the Exit command.
Auto refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = low; $\overline{WE}$ = $\overline{CKE}$ = high; A0~A11 = don't care	SDRAM storage cells must be refreshed every 64ms to maintain data integrity. Use the Auto Refresh command to accomplish the refreshing of all rows in both banks of the SDRAM. The row address is provided by an internal counter which increments automatically. Auto refresh can only be asserted when both banks are idle and the device is not in the power down mode. The time required to complete the auto refresh operation is t_{RC}(min). Use NOPs in the interim until the auto refresh operation is complete. This is the most common refresh mode. It is typically performed once every 15.6us or in a burst of 4096 auto refresh cycles every 64ms. Both banks will be in the idle state after this operation.
Self refresh	$\overline{CS}$ = $\overline{RAS}$ = $\overline{CAS}$ = CKE = low; $\overline{WE}$ = high; A0~A11 = don't care	Self refresh is another mode for refreshing SDRAM cells. In this mode, refresh address and timing are provided internally. Self refresh entry is allowed only when both banks are idle. The internal clock and all input buffers with the exception of CKE are disabled in this mode. Exit self refresh by restarting the external clock and then asserting CKE high. NOP's must follow for a time of t_{RC}(min) for the SDRAM to reach the idle state where normal operation is allowed. If burst auto refresh is used in normal operation, burst 4096 auto refresh cycles immediately after exiting self refresh.

Mode register set command waveform

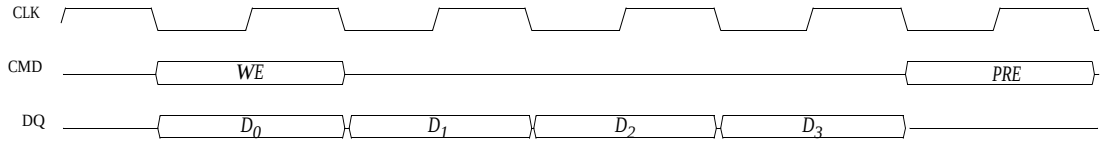


MRS can be issued only when both banks are idle.

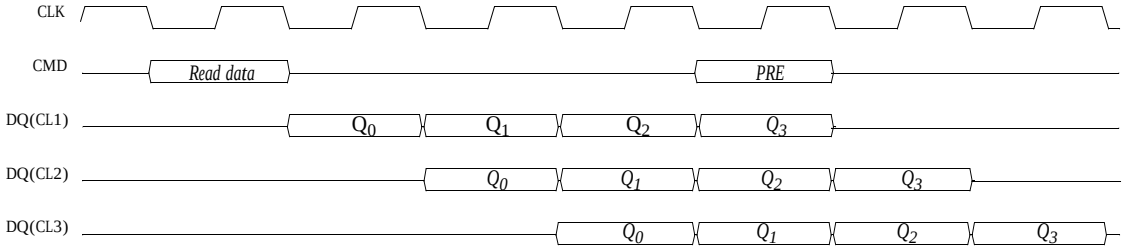
Precharge waveforms

Precharge can be asserted after t_{RAS} (min). The selected bank will enter the idle state after t_{RP}. The earliest assertion of the precharge command without losing any burst data is show below.

(normal write; BL = 4)



(normal read; BL = 4)

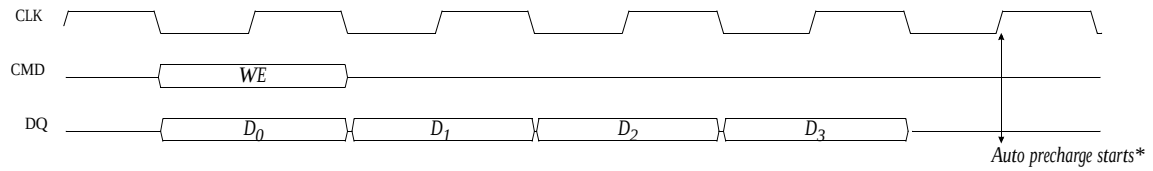


DRAM

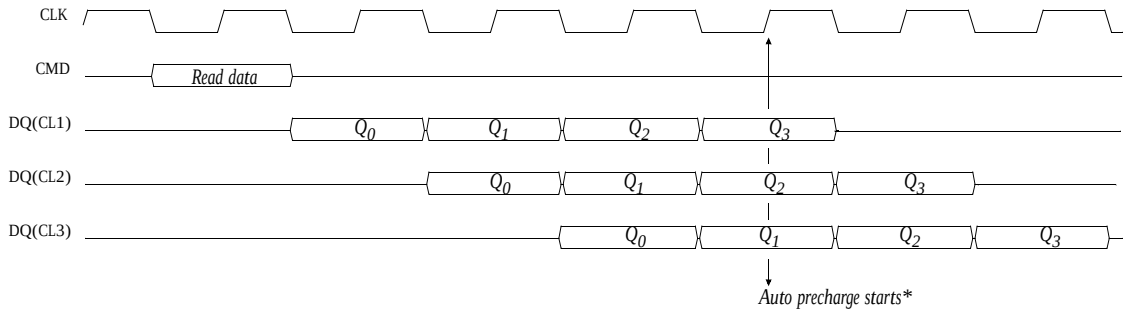
Auto precharge waveforms

A10 controls the selection of auto precharge during the read or write command cycle.

(write with auto precharge; BL = 4)



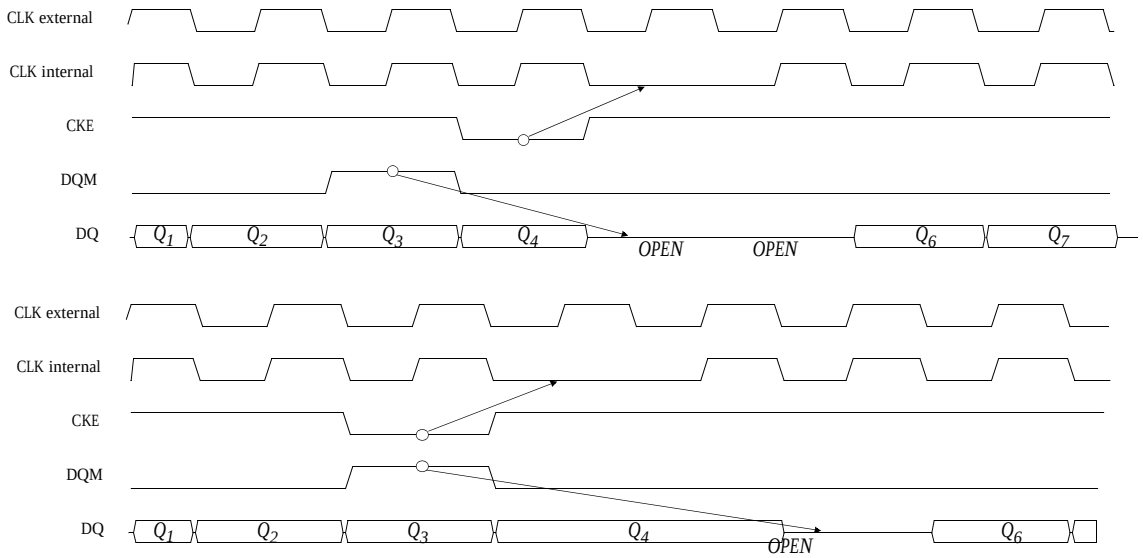
(read with auto precharge; BL = 4)



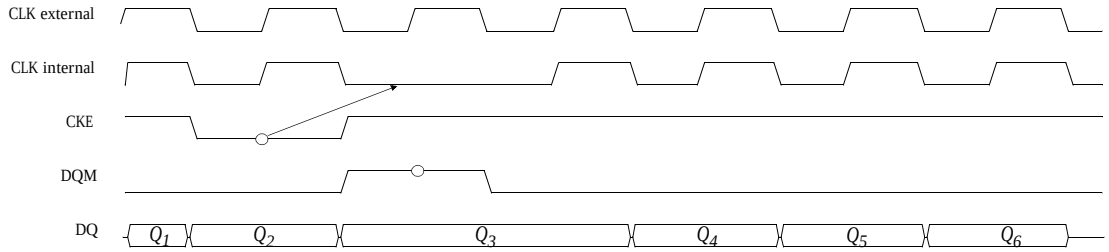
*The row active command of the precharge bank can be issued after t_{RP} from this point. The new read/write command of another activated bank can be issued from this point. At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

Clock suspension read waveforms

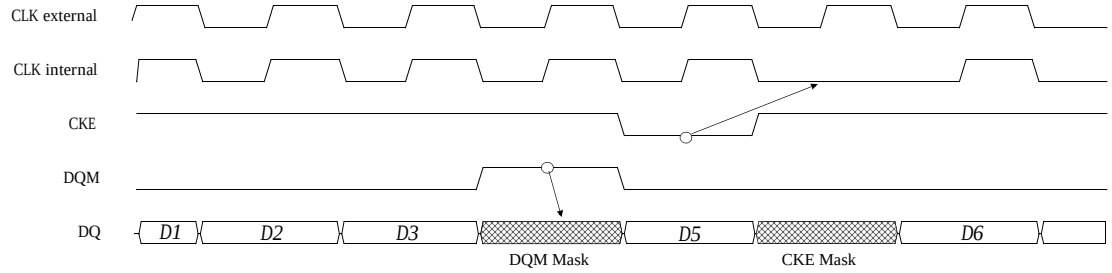
(BL = 8)

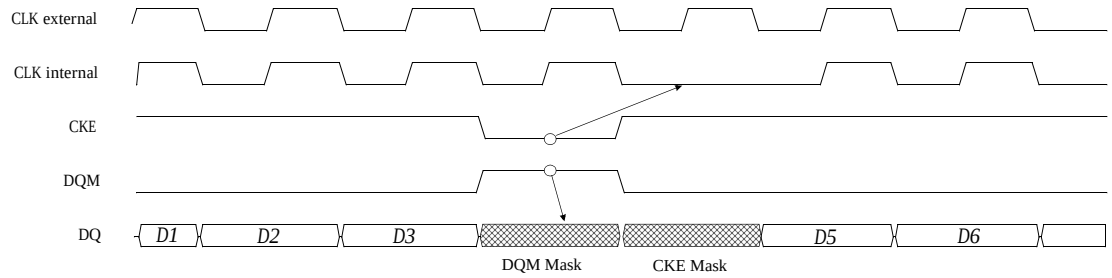


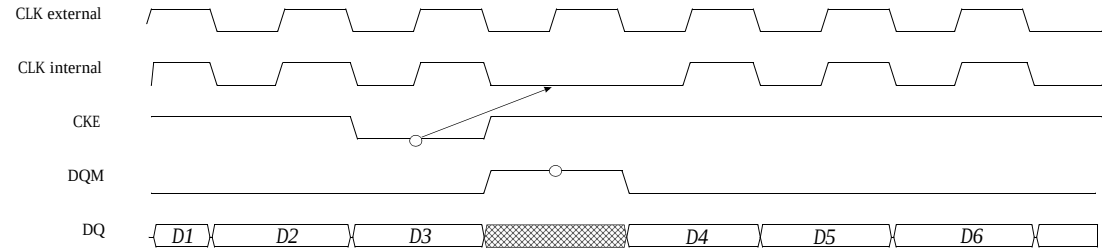
DRAM



Clock suspension write waveforms

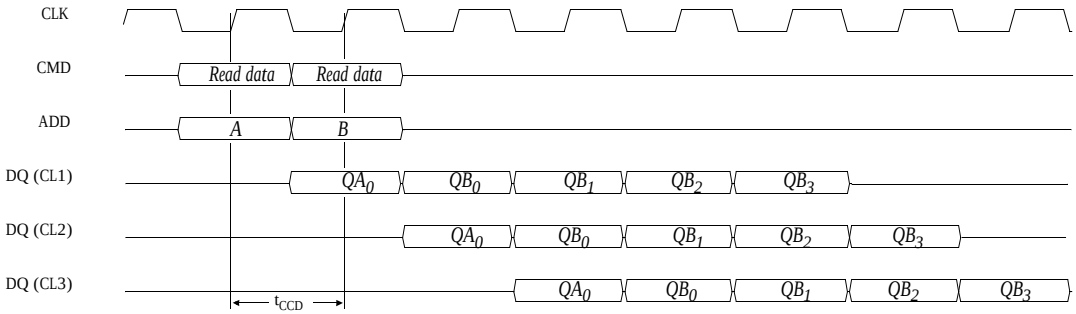






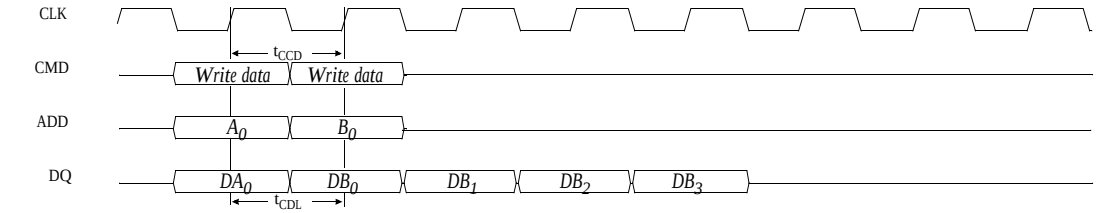
Read/write interrupt timing

read interrupted by read (BL = 4)



t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

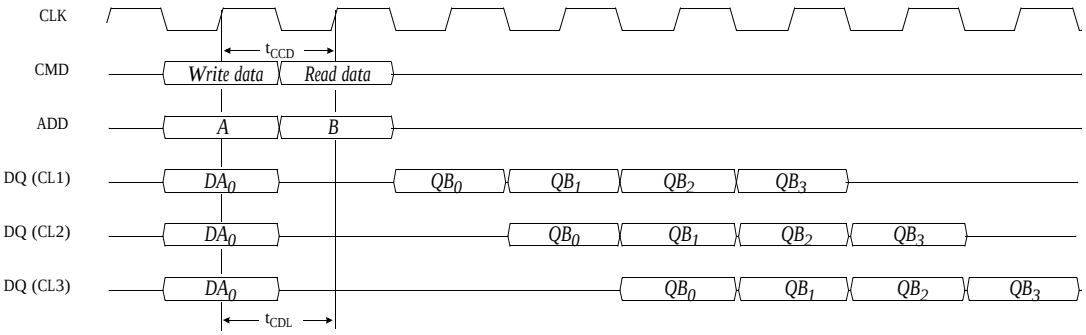
write interrupted by write (BL = 4)



t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

t_{CDL} = last address in to new column addres delay (= 1 CLK)

write interrupted by read (BL = 4)

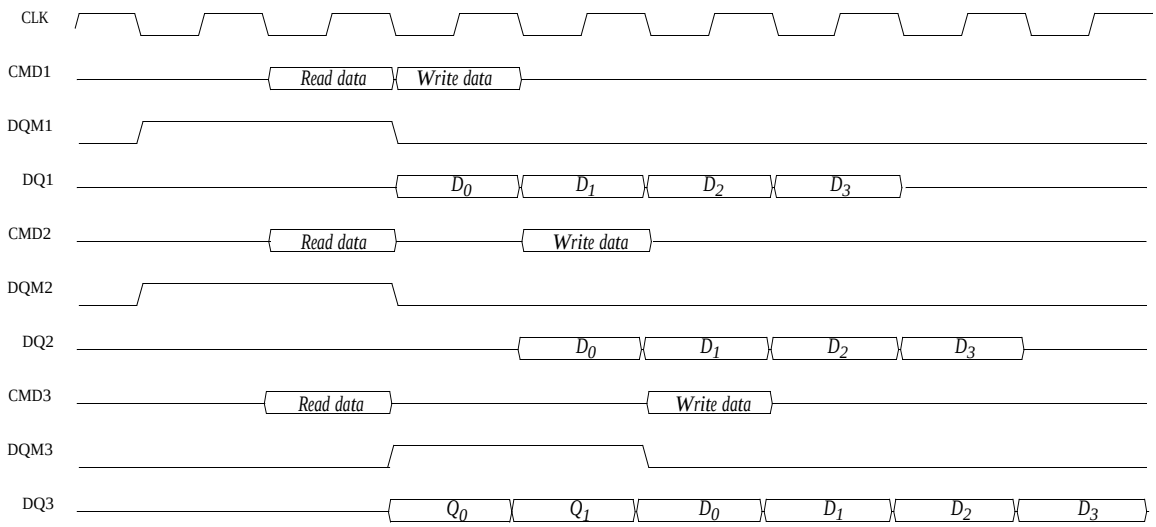


t_{CCD} = $\overline{CAS}$ to $\overline{CAS}$ delay (= 1 CLK)

t_{CDL} = last address in to new column addres delay (= 1 CLK)

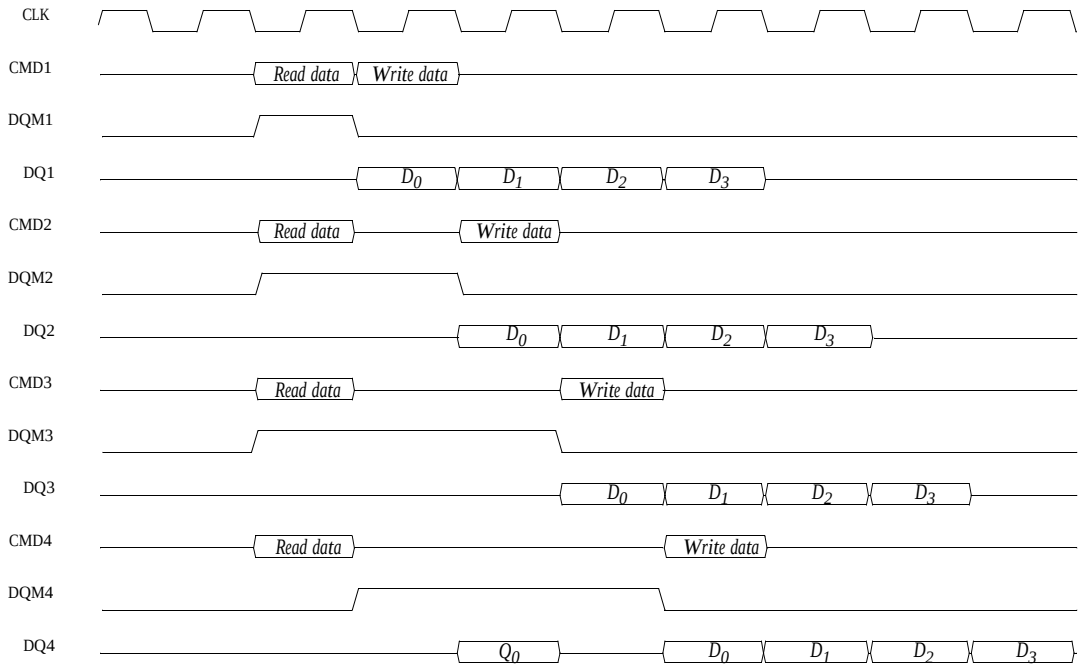
DRAM

read interrupted by write (CL = 1, BL = 4)



To prevent bus contention, maintain a gap between data in and data out.

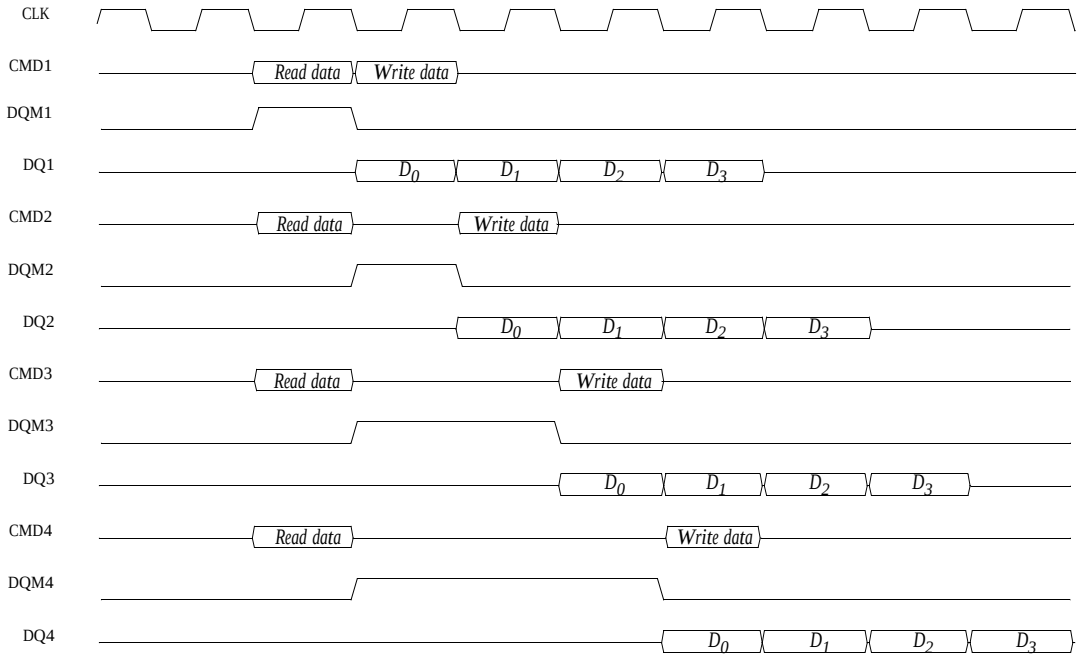
read interrupted by write (CL = 2, BL = 4)



To prevent bus contention, maintain a gap between data in and data out.

DRAM

read interrupted by write (CL = 3, BL = 4)



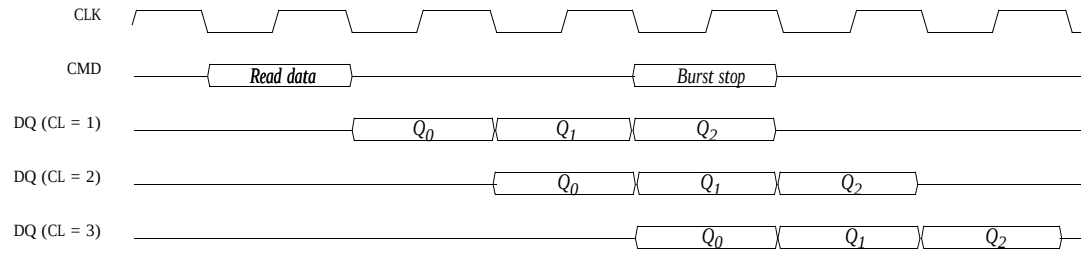
To prevent bus contention, maintain a gap between data in and data out.

Burst termination

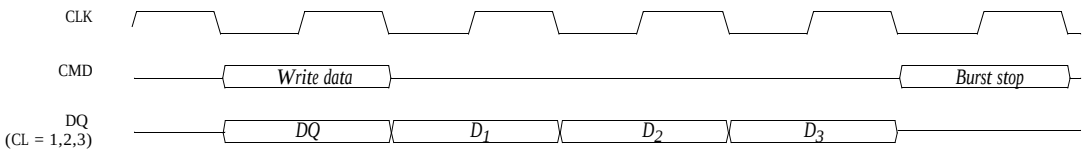
Burst operations may be terminated with a Read, Write, Burst Stop, or Precharge command. When Burst Stop is asserted during the read cycle, burst read data is terminated and the data bus goes to Hi-Z after $\overline{CAS}$ latency. When Burst Stop is asserted during the write cycle, burst write data is terminated and the databus goes to HI-Z simultaneously.

Burst stop command waveform

read cycle



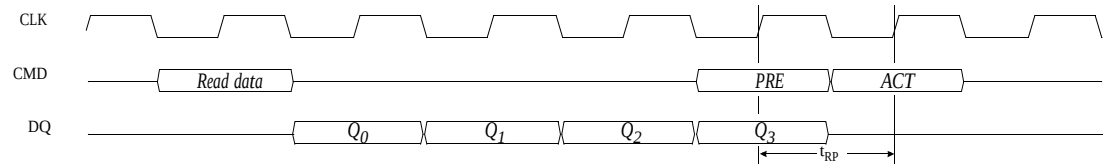
write cycle (BL = 8)



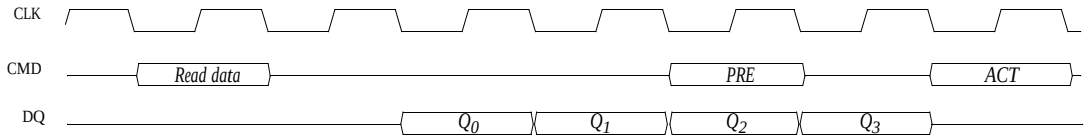
Precharge termination

A Precharge command terminates a burst read/write operation during the read cycle. The same bank can be activated after meeting t_{RP}

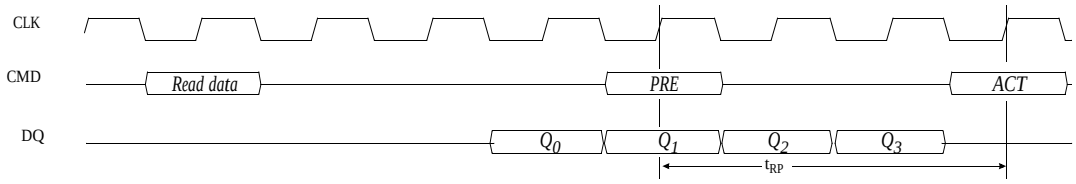
read cycle (CL = 1)



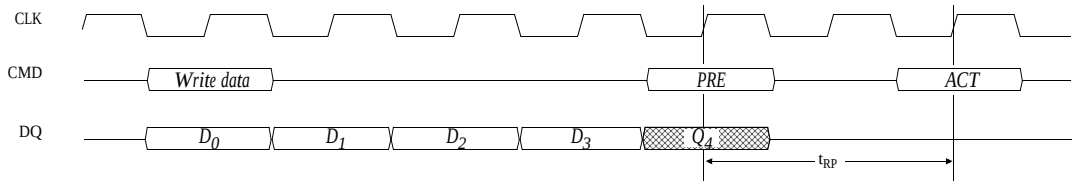
read cycle (CL = 2)



read cycle (CL = 3)

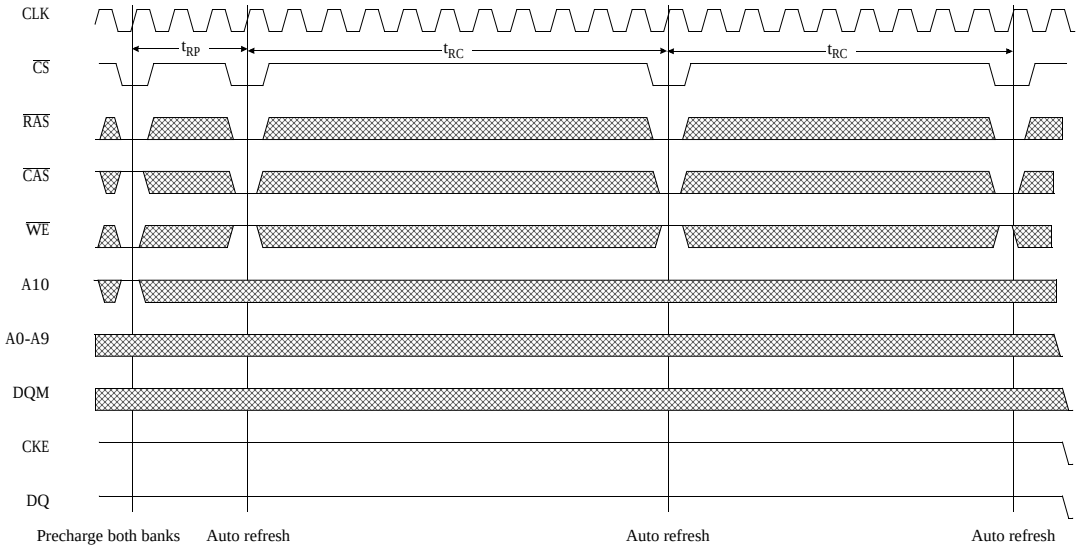


write cycle

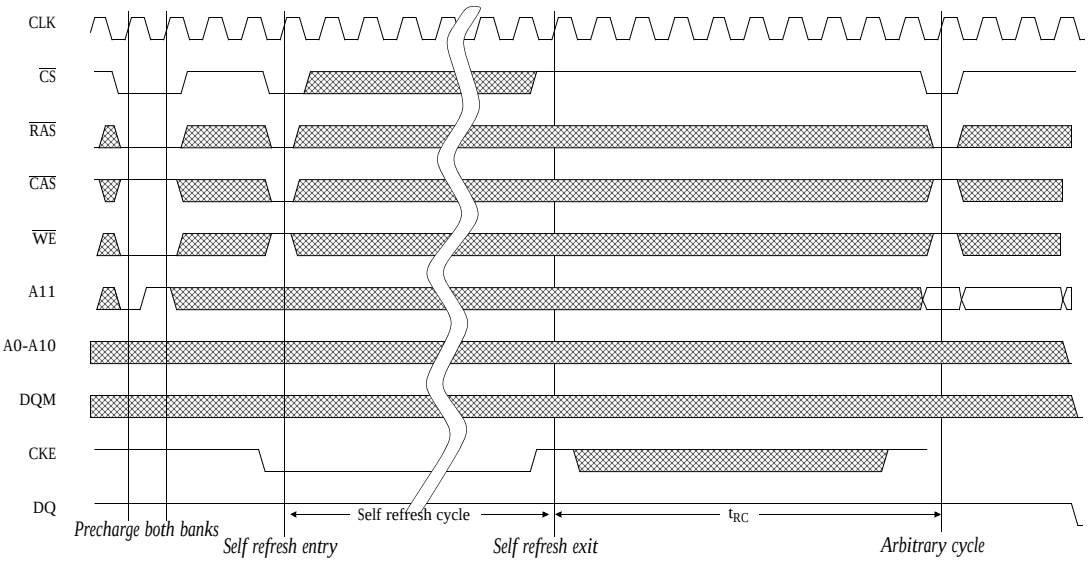


DRAM

Auto refresh waveform

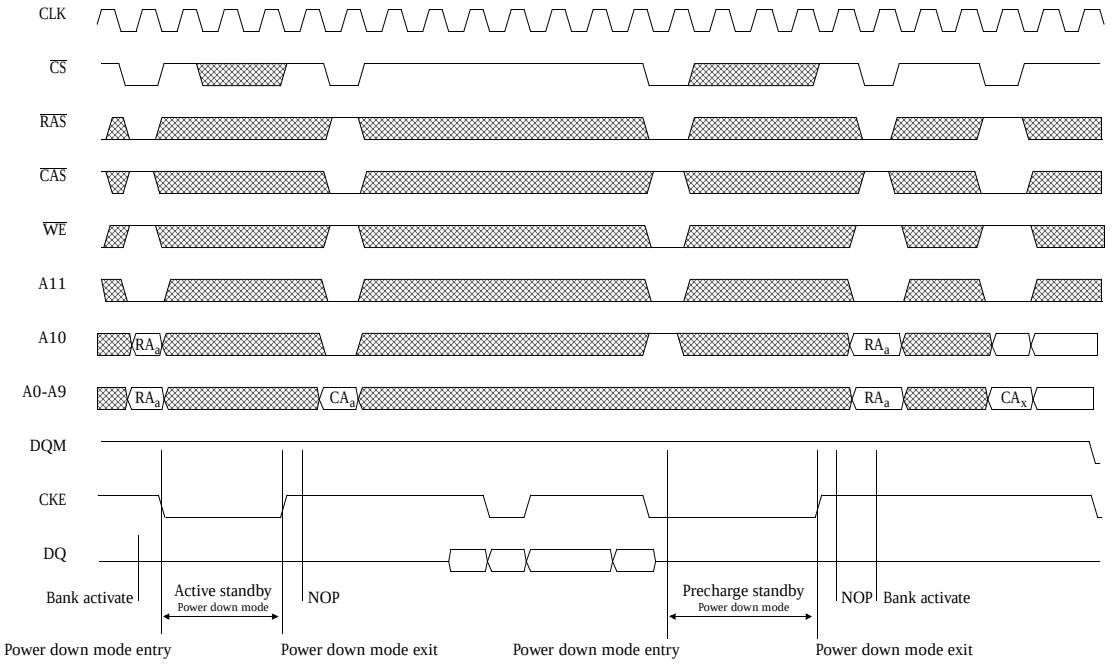


Self refresh waveform



Power down mode waveform

(CL = 3)



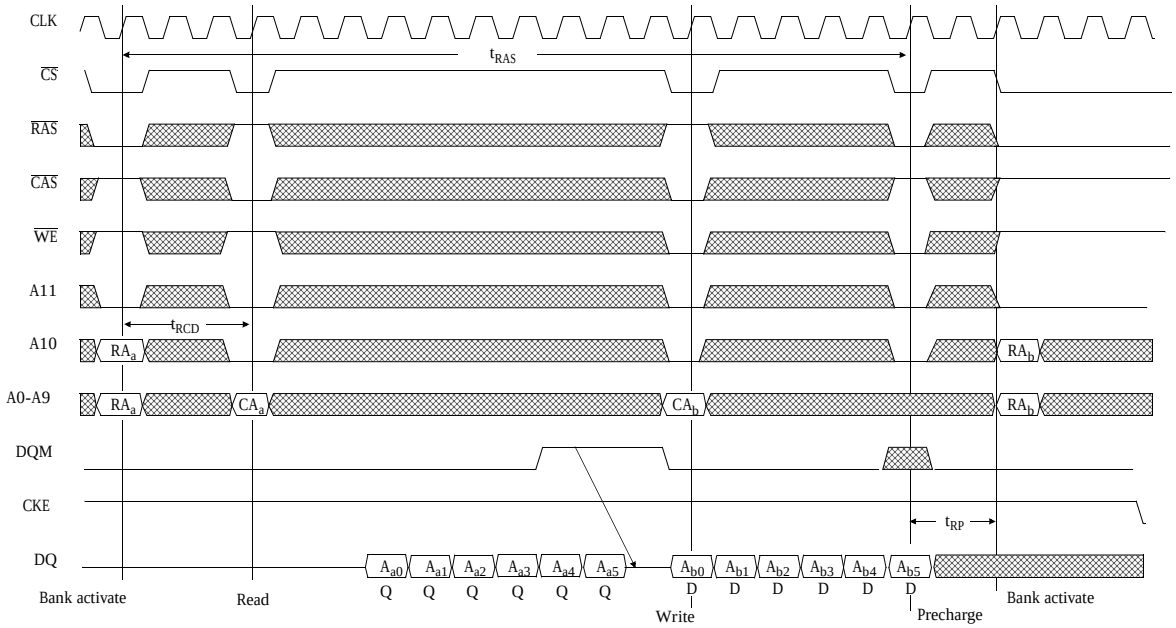
Enter power down mode by pulling CKE low.

All input/output buffers (except CKE buffer) are turned off in power down mode.

When CKE goes high, command input must be equal to no operation at next CLK rising edge.

Read/write waveform

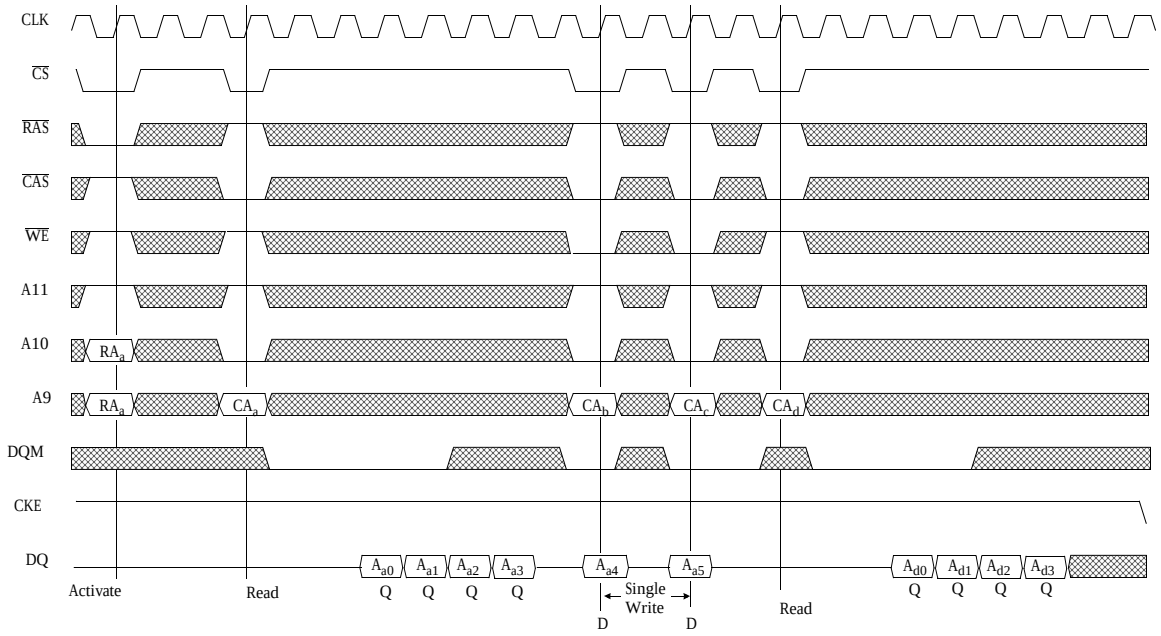
(BL = 8, CL = 3)



DRAM

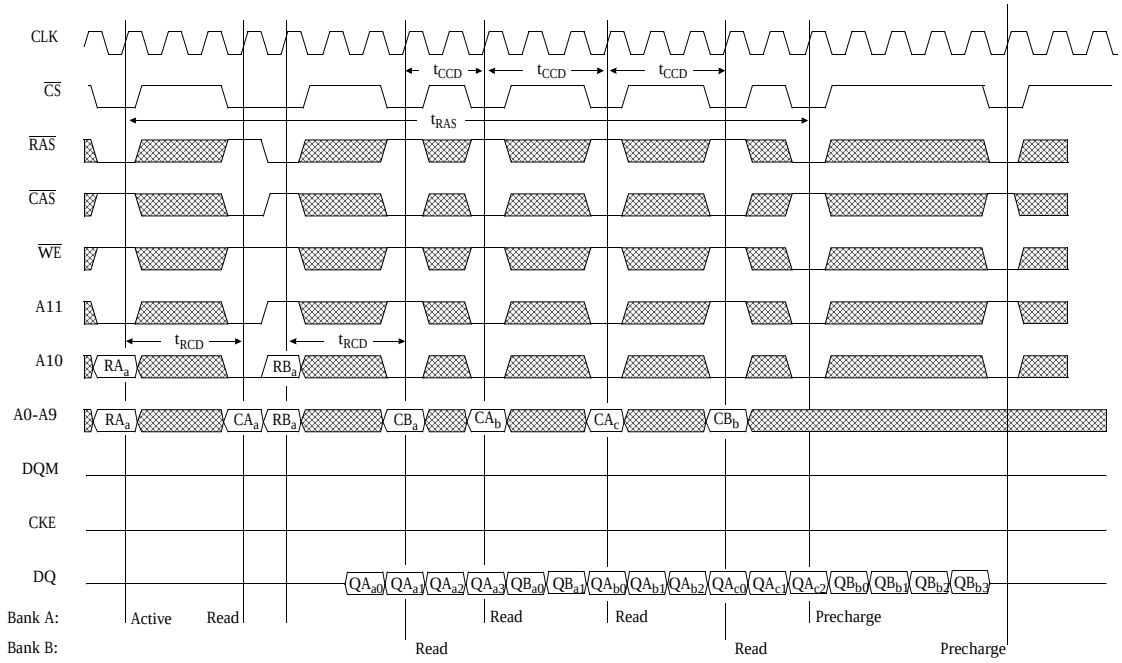
Burst read/single write waveform

(BL = 4, CL = 3)



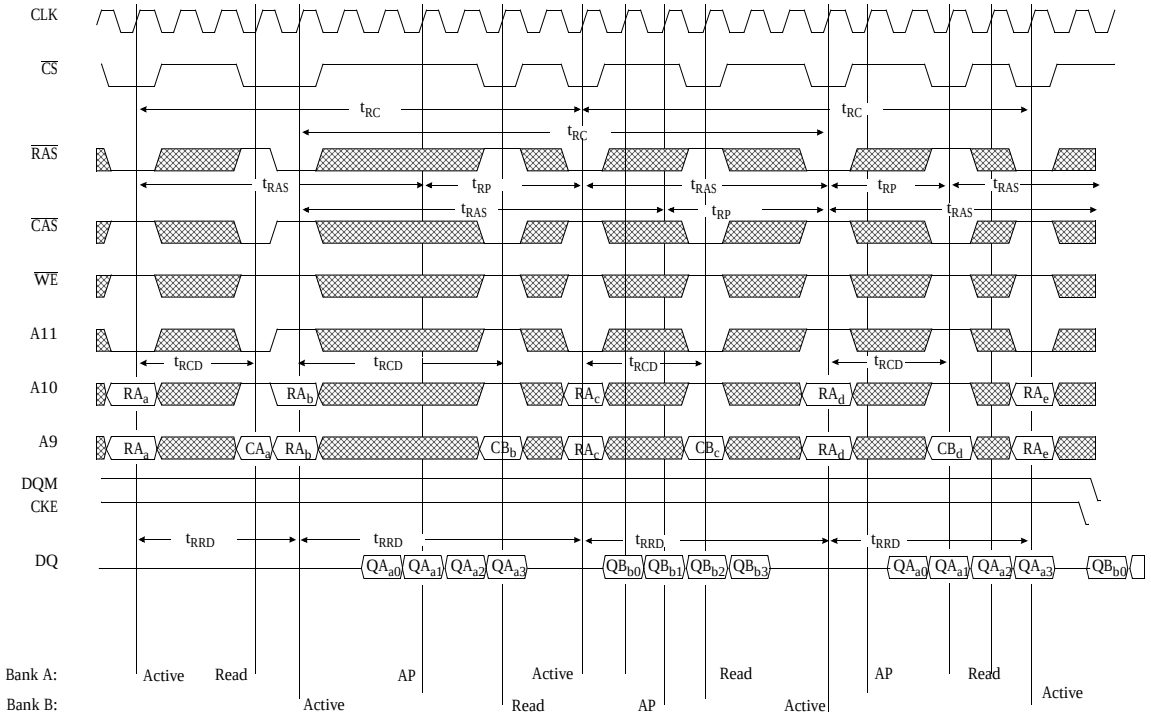
Interleaved bank read waveform

(BL = 4, CL = 3)



Interleaved bank read waveform

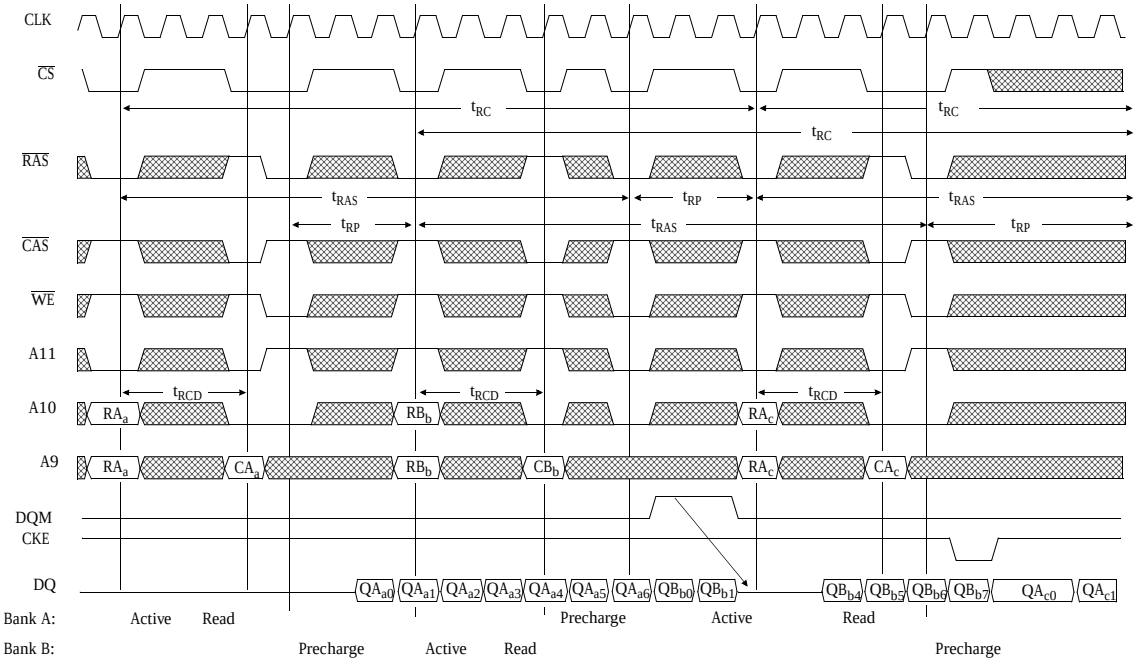
(BL = 4, CL = 3, Autoprecharge)



AP = internal precharge begins

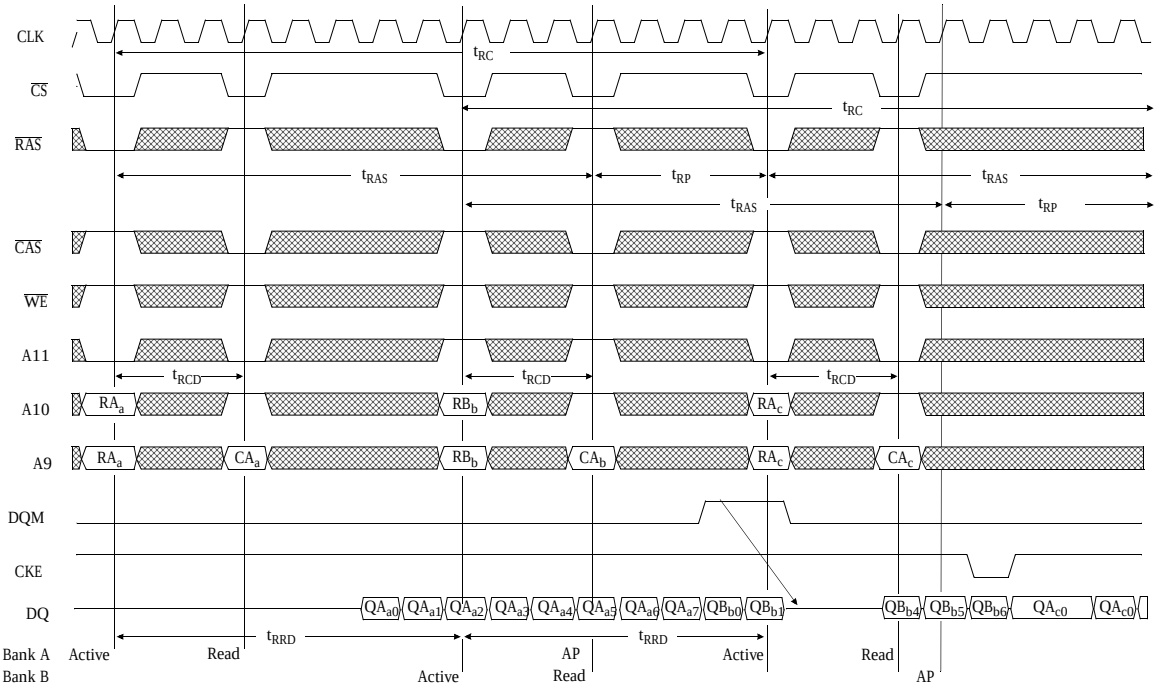
Interleaved bank read waveform

(BL = 8, CL = 3)



Interleaved bank read waveform

(BL = 8, CL = 3, Autoprecharge)

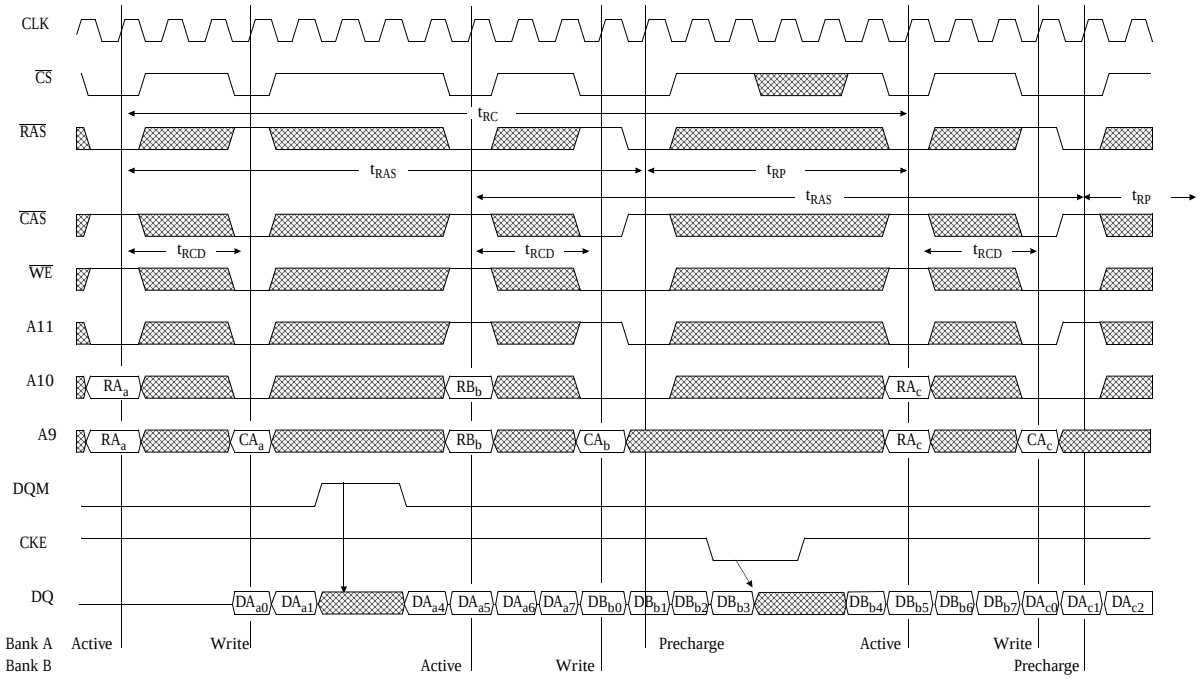


AP = internal precharge begins

DRAM

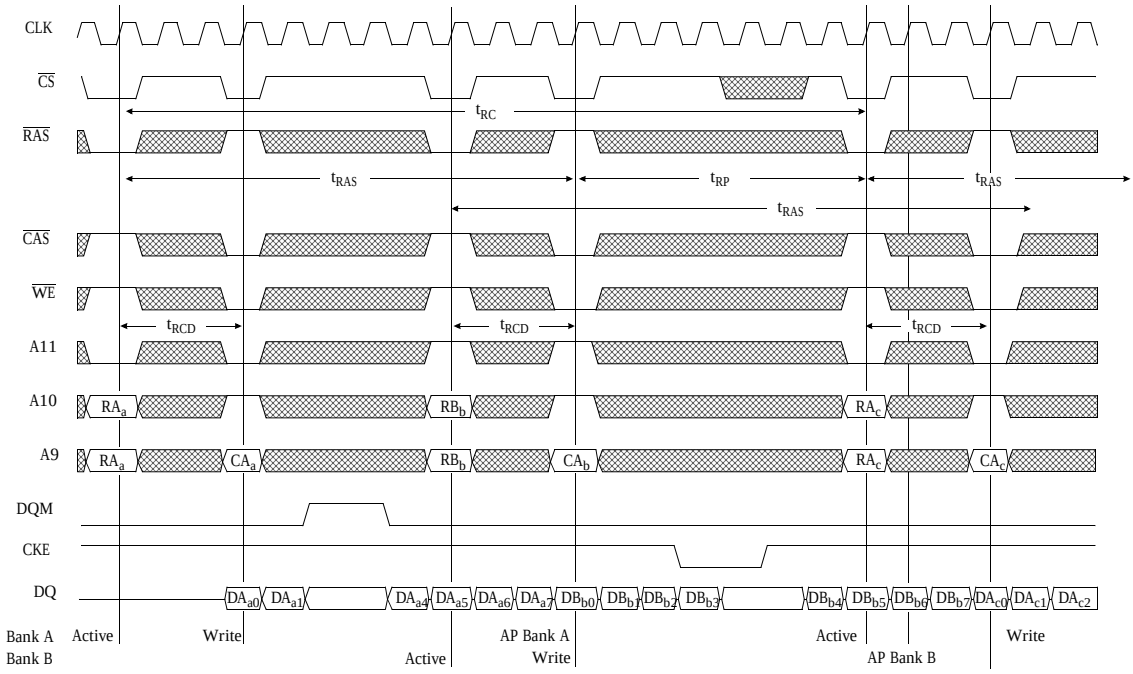
Interleaved bank write waveform

(BL = 8)



Interleaved bank write

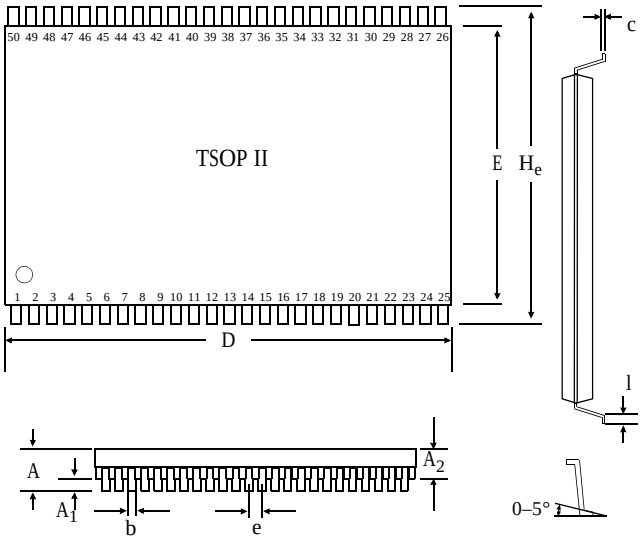
(BL = 8, Autoprecharge)



AP = internal precharge begins

DRAM

Package dimensions



	44-pin TSOP II		50-pin TSOP II	
	Min (mm)	Max (mm)	Min (mm)	Max (mm)
A	–	1.2		1.2
A_1	0.05	–	0.05	
A_2	0.95	1.05	0.95	1.05
b	0.30	0.45	0.30	0.45
c	0.127 (typical)		0.12	0.21
D	18.28	18.54	20.85	21.05
E	10.03	10.29	10.03	10.29
H_e	11.56	11.96	11.56	11.96
e	0.80 (typical)		0.80 (typical)	
l	0.40	0.60	0.40	0.60

DRAM

AC test conditions

- Input reference levels of V_{IH} = 2.4V and V_{IL} = 0.4V
- Output reference levels = 1.4V
- Input rise and fall times: 2 ns

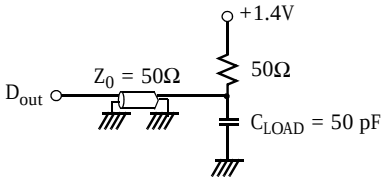


Figure A: Equivalent output load

Capacitance [15]

f = 1 MHz, T_a = 25°C, V_{CC} = 3.3V

Parameter	Symbol	Signals	Max	Unit
Input capacitance	C_{IN1}	A0 to A11	4	pF
	C_{IN2}	DQM, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CLK, CKE,	4	pF
I/O capacitance	$C_{I/O}$	DQ0 to DQ7 (2M×8) DQ0 to DQ15 (1M×16)	5	pF

Ordering information

Package \1/ frequency	8 ns	10 ns	12 ns
TSOP II, 400 mil, 44-pin	AS4LC2M8S0-8TC	AS4LC2M8S0-10TC	AS4LC2M8S0-12TC
TSOP II, 400 mil, 50-pin	AS4LC1M16S0-8TC	AS4LC1M16S0-10TC	AS4LC1M16S0-12TC

Part numbering system

AS4	LC	XXXS0	–XX	T	C
DRAM prefix	LC = 3.3V CMOS	Device number for synchronous DRAM	1/frequency	Package (device dependent): TSOP II 400 mil, 44 pin TSOP II 400 mil, 50 pin	Commercial temperature range, 0°C to 70 °C